THE DATASHEET OF

PGA2500IDB

SBOS289A − NOVEMBER 2003 − REVISED DECEMBER 2003

Digitally Controlled Microphone Preamplifier

FEATURES

- **Fully Differential Input-to-Output Architecture**
- **Digitally Controlled Gain Using Serial Port Interface:**
  - **Gain Range: 10dB through 65dB, 1dB per step**
  - **Unity (0dB) Gain Setting via Serial Port or Dedicated Control Pin**
- **Dynamic Performance:**
  - **Equivalent Input Noise with Z_S = 150Ω and Gain = 30dB: −128dBu**
  - **Total Harmonic Distortion plus Noise (THD+N) with Gain = 30dB: 0.0004%**
- **Zero Crossing Detection Minimizes Audible Artifacts when Gain Switching**
- **Integrated DC Servo Minimizes Output Offset Voltage**
- **Common-Mode Servo Improves CMRR**
- **Four-Wire Serial Control Port Interface:**
  - **Simple Interface to Microprocessor or DSP Serial Ports**
  - **Supports Daisy-Chaining of Multiple PGA2500 Devices**
- **Dedicated Input Pin for Selecting Unity Gain**
- **Overload Output Pin Provides Clipping Indication**
- **Four General-Purpose Digital Output Pins**
- **Requires ±5V Power Supplies**
- **Available in an SSOP-28 Package**

APPLICATIONS

- **Microphone Preamplifiers and Mixers**
- **Digital Mixers and Recorders**

DESCRIPTION

The PGA2500 is a digitally controlled, analog microphone preamplifier designed for use as a front end for high-performance audio analog-to-digital converters (ADCs). The PGA2500 features include low noise, wide dynamic range, and a differential signal path. An on-chip DC servo loop is employed to minimize DC offset, while a common-mode servo function may be used to enhance common-mode rejection.

The PGA2500 features a gain range of 10dB through 65dB (1dB/step), along with a unity gain setting. The wide gain range allows the PGA2500 to be used with a variety of microphones. Gain settings and internal functions are programmed using a 16-bit control word, which is loaded using a simple serial port interface. A serial data output pin provides support for daisy-chained connection of multiple PGA2500 devices. Four programmable digital outputs are provided for controlling the external switching of input pads, phantom power, high pass filters, and polarity reversal functions. The PGA2500 requires both +5V and −5V power supplies and is available in a small SSOP-28 package.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted(1)

	PGA2500	UNIT
Supply Voltage, VA+	+5.5	V
Supply Voltage, VA−	−5.5	V
Supply Voltage, VD−	−5.5	V
Voltage Difference, VA− to VD−	Less than 300	mV
Analog input voltage	(VA−) −0.3 to (VA+) +0.3	V
Digital input voltage	−0.3 to (VA+) + 0.3	V
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−60 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PGA2500	SSOP-28	DB	−40°C to +85°C	PGA2500I	PGA2500IDB	Rails, 48
					PGA2500IDBR	Tape and Reel, 1000

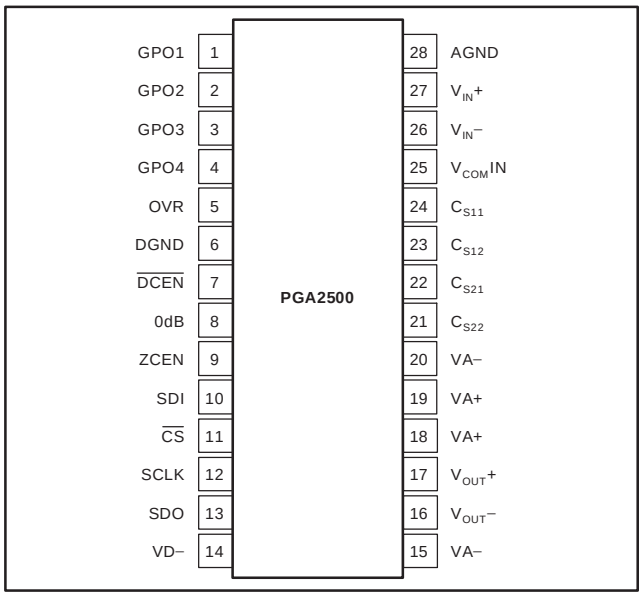
(1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

All parameters specified with T_A = +25°C, VA+ = +5V, VA− = −5V, VD− = −5V, and V_{COM}IN = 0V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	PGA2500			UNIT
		MIN	TYP	MAX	
DC Characteristics					
Step Size	Gain = 10dB through 65dB		1		dB
Gain Error	All Gain Settings		0.5		dB
AC Characteristics					
THD+N with f_{IN} = 1kHz	Gain = 0dB, V_{OUT} = 3.5V_{RMS}, V_{COM}IN = 0V Gain = 30dB, V_{OUT} = 3.5V_{RMS}, V_{COM}IN = 0V		−114 −108	−108 −102	dB dB
Analog Input					
Maximum Input Voltage	Gain = 0dB	VA− +1.5		VA+ −2.0	V
Input Resistance Per Input Pin Differential			 4600 9200		 Ω Ω
Analog Output					
Output Voltage Range	V_{COM}IN = 0V, R_L = 600Ω	VA− +0.9		VA+ −0.9	V
Output Offset Voltage	DC Servo On, Any Gain		±0.04	±1	mV
Input Referred Offset	DC Servo Off, Gain = 30dB		±1		mV
Output Resistive Loading		600			Ω
Load Capacitance Stability			100		pF
Short Circuit Current	10-second duration		100		mA
Digital Characteristics					
High-Level Input Voltage, V_{IH}		+2.0		VA+	V
Low-Level Input Voltage, V_{IL}		−0.3		0.8	V
High-Level Output Voltage, V_{OH}	I_O = 200µA	(VA+) − 1.0			V
Low-Level Output Voltage, V_{OL}	I_O = −3.2mA			0.4	V
Input Leakage Current, I_{IN}			2	10	µA
Switching Characteristics					
Serial Clock (SCLK) Frequency	f_{SCLK}	0		6.25	MHz
Serial Clock (SCLK) Pulse Width Low	t_{PH}	80			ns
Serial Clock (SCLK) Pulse Width High	t_{PL}	80			ns
Input Timing					
SDI Setup Time	t_{SDS}	20			ns
SDI Hold Time	t_{SDH}	20			ns
$\overline{CS}$ Falling to SCLK Rising	t_{CSCR}	90			ns
SCLK Falling to $\overline{CS}$ Rising	t_{CFCS}	35			ns
Output Timing					
$\overline{CS}$ Low to SDO Active	t_{CSO}			35	ns
SCLK Falling to SDO Data Valid	t_{CFDO}			60	ns
$\overline{CS}$ High to SDO High Impedance	t_{CSZ}			100	ns
Power Supply					
Operating Voltage					
VA+		+4.75	+5	+5.25	V
VA−		−4.75	−5	−5.25	V
VD−		−4.75	−5	−5.25	V
Quiescent Current					
IA+	VA+ = +5V		30	40	mA
IA−	VA− = −5V		30	40	mA
ID−	VD− = −5V		1	2	mA

PIN CONFIGURATION



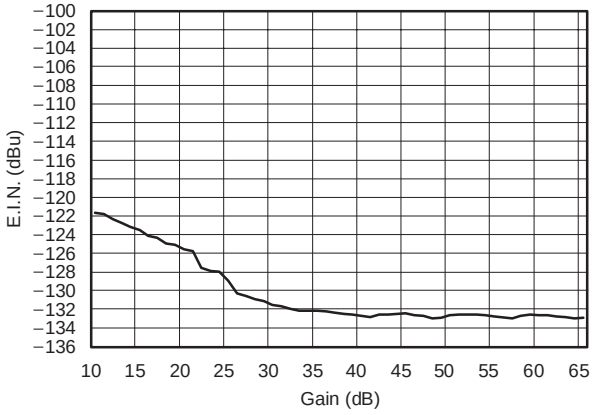
PIN DESCRIPTIONS

PIN NUMBER	NAME	DESCRIPTION
1	GPO1	General-Purpose CMOS Logic Output
2	GPO2	General-Purpose CMOS Logic Output
3	GPO3	General-Purpose CMOS Logic Output
4	GPO4	General-Purpose CMOS Logic Output
5	OVR	Over Range Output (Active High)
6	DGND	Digital Ground
7	$\overline{\text{DCEN}}$	DC Servo Enable (Active Low)
8	0dB	Unity Gain Enable (Active High)
9	ZCEN	Zero Crossing Detector Enable (Active High)
10	SDI	Serial Data Input
11	$\overline{\text{CS}}$	Chip Select Input (Active Low)
12	SCLK	Serial Data Clock Input
13	SDO	Serial Data Output
14	VD−	−5V Digital Supply
15	VA−	−5V Analog Supply
16	V_{OUT}−	Analog Output, Inverting
17	V_{OUT}+	Analog Output, Non-Inverting
18	VA+	+5V Analog Supply
19	VA+	+5V Analog Supply
20	VA−	−5V Analog Supply
21	C_{S22}	DC Servo Capacitor #2, Terminal 2
22	C_{S21}	DC Servo Capacitor #2, Terminal 1
23	C_{S12}	DC Servo Capacitor #1, Terminal 2
24	C_{S11}	DC Servo Capacitor #1, Terminal 1
25	V_{COM}IN	Common Mode Voltage Input, 0V to +2.5V
26	V_{IN}−	Analog Input, Inverting
27	V_{IN}+	Analog Input, Noninverting
28	AGND	Analog Ground

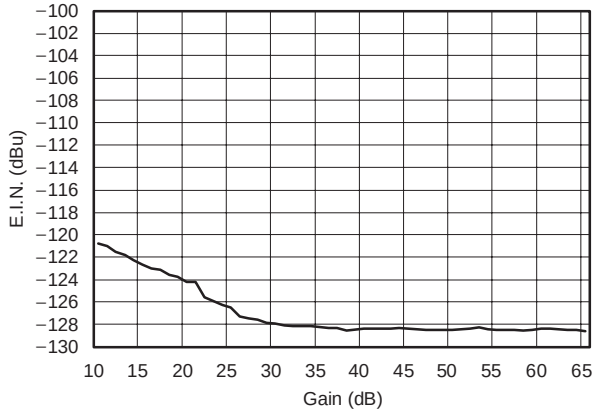
TYPICAL CHARACTERISTICS

All specifications at T_A = +25°C, VA+ = +5V, VA− = −5V, VD− = −5V, and V_{COM}IN = 0V, unless otherwise noted.

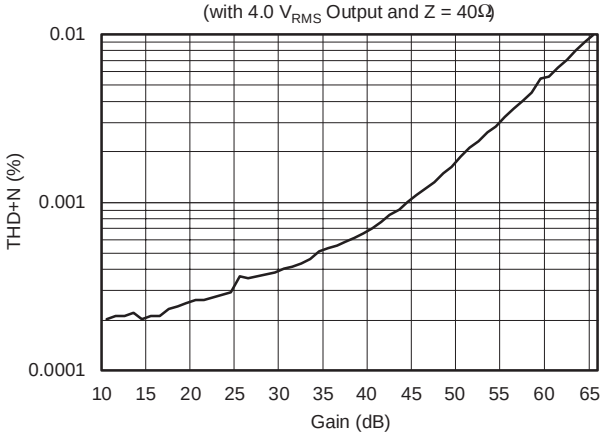
EQUIVALENT INPUT NOISE (E.I.N.) AS A FUNCTION OF GAIN
(with Z = 0Ω)



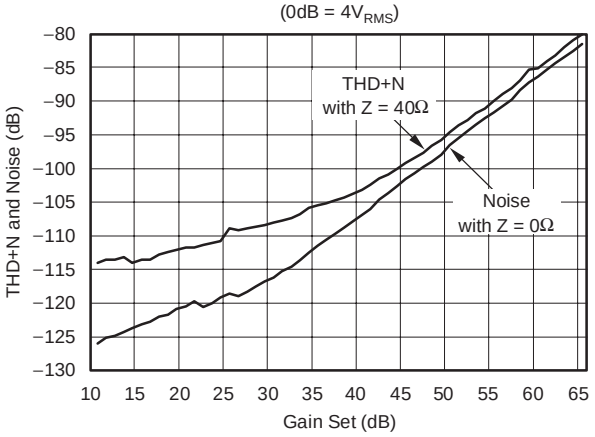
EQUIVALENT INPUT NOISE (E.I.N.) AS A FUNCTION OF GAIN
(with Z = 150Ω)



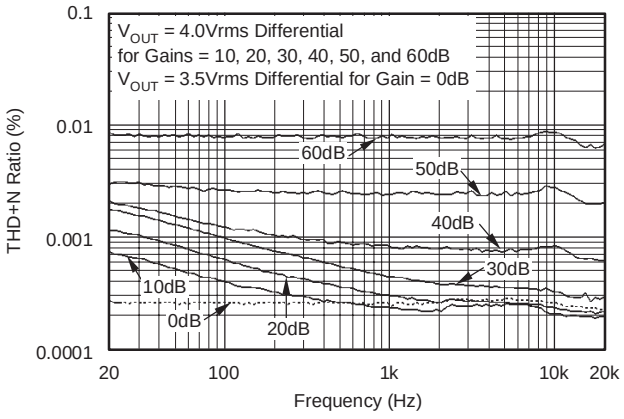
THD+N vs GAIN
(with 4.0 V_{RMS} Output and Z = 40Ω)



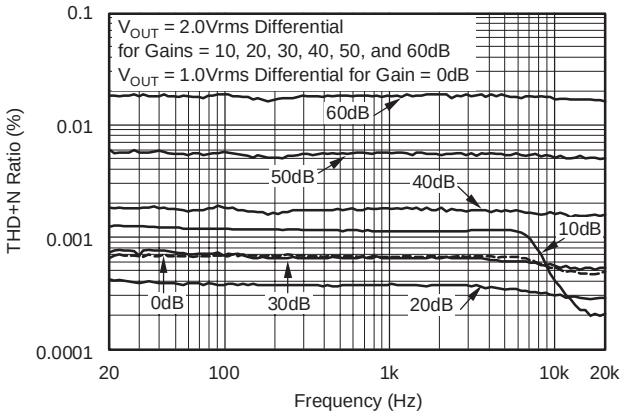
THD+N AND NOISE vs GAIN
(0dB = 4V_{RMS})



THD+N vs FREQUENCY
(R_S = 40Ω, R_L = 600Ω, V_{COM}IN = 0V, BW = 22Hz to 22kHz)



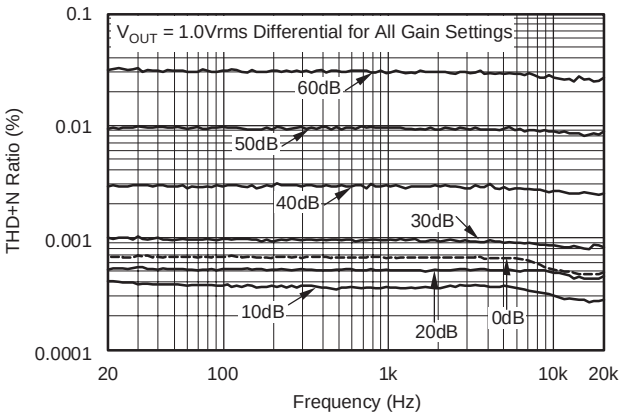
THD+N vs FREQUENCY
(R_S = 40Ω, R_L = 600Ω, V_{COM}IN = +2.5V, BW = 22Hz to 22kHz)



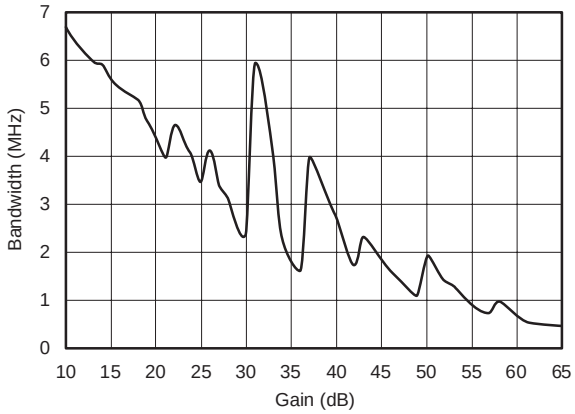
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, VA+ = +5V, VA− = −5V, VD− = −5V, and V_{COM}IN = 0V, unless otherwise noted.

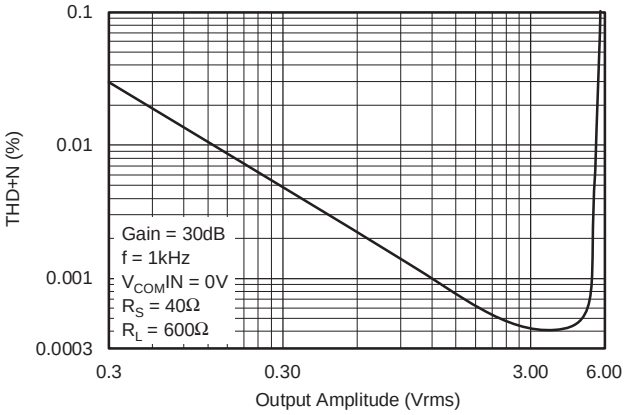
THD+N vs FREQUENCY
(R_S = 40Ω R_L = 600Ω V_{COM}IN = +2.5V, BW = 22Hz to 22kHz)



BANDWIDTH vs GAIN



THD+N vs OUTPUT AMPLITUDE



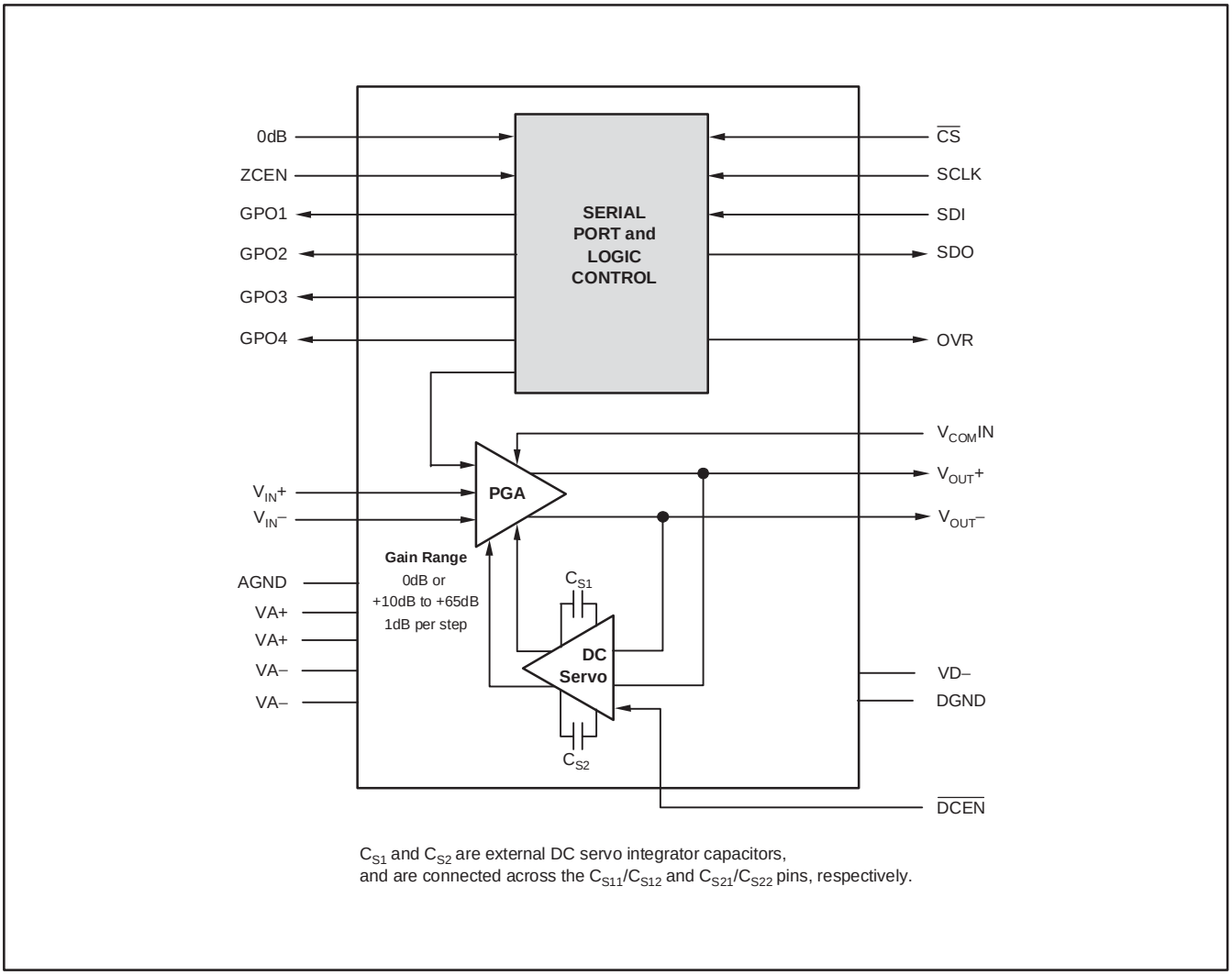
OVERVIEW

The PGA2500 is a digitally controlled microphone preamplifier integrated circuit designed for amplifying the output of dynamic and condenser microphones and driving high performance audio analog-to-digital converters (ADCs). A functional block diagram of the PGA2500 is shown in Figure 1.

The analog input to the preamplifier is provided differentially at the V_{IN}+ and V_{IN}− inputs (pins 27 and 26, respectively). The programmable gain amplifier can be programmed to either pass through the signal at unity gain, or apply 10dB to 65dB of gain to the input signal. The gain of the amplifier is adjustable over the full 10dB to 65dB range in 1dB steps. The differential output of the PGA2500 is made available at V_{OUT}+ and V_{OUT}− (pins 17 and 16, respectively). Gain is controlled using a serial port interface.

The four-wire serial port interface is used to program the PGA2500 gain and support functions. A 16-bit control word is utilized to program these functions (see Figure 2, page 9). A serial data output pin provides support for daisy-chaining multiple PGA2500 devices on a single serial interface bus (see Figure 4, page 10).

The differential analog output of the PGA2500 is constantly monitored by a DC servo amplifier loop. The purpose of the servo loop is to minimize the DC offset voltage present at the analog outputs by feeding back an error signal to the input stage of the programmable gain amplifier. The error signal is then used to correct the offset. The DC servo may be disabled by driving the $\overline{\text{DCEN}}$ input (pin 7) high or setting the $\overline{\text{DC}}$ bit in the serial control word to 1. Normally, the $\overline{\text{DCEN}}$ pin is connected to DGND to enable the DC servo, while the $\overline{\text{DC}}$ bit is set to 0.



C_{S1} and C_{S2} are external DC servo integrator capacitors, and are connected across the C_{S11}/C_{S12} and C_{S21}/C_{S22} pins, respectively.

Figure 1. PGA2500 Functional Block Diagram

Two external capacitors are required for the DC servo function, with one capacitor connected between C_{S11} and C_{S12} (pins 24 and 23), and the second capacitor connected between C_{S21} and C_{S22} (pins 22 and 21). Capacitor values up to 4.7µF may be utilized. However, larger valued capacitors will result in longer settling times for the DC servo loop. A value of 1µF is recommended for use in most microphone preamplifier applications.

The PGA2500 includes a common-mode servo function. This function is enabled and disabled using the CM bit in the serial control word; see Figure 2. When enabled, the servo provides common-mode negative feedback at the input differential pair, resulting in very low common-mode input impedance. The differential input impedance is not affected by this feedback. This function is useful when the source is floating, or has a high common-mode output impedance. In this case, the only connection between the source and the ground will be through the PGA2500 preamplifier input resistance.

In this case, input common-mode parasitic current is determined by high output impedance of the source, not by input impedance of the amplifier. Therefore, input common-mode interference can be reduced by lowering the common-mode input impedance while at the same time not increasing the input common-mode current. Increasing common-mode current degrades common-mode rejection. Using the common-mode servo, overall common-mode rejection can be improved by suppressing low and medium frequency common-mode interference.

The common-mode servo function is designed to operate with a total common-mode input capacitance (including the microphone cable capacitance) of up to 10nF. Beyond this limit, stable servo operation is not ensured.

The common-mode voltage control input, named $V_{COM}IN$ (pin 25), allows the PGA2500 output and input to be DC-biased to a common-mode voltage between 0 and +2.5V. This allows for a DC-coupled interface between the PGA2500 preamplifier output and the inputs of common single-supply audio ADCs.

A dedicated 0dB input (pin 8) is provided so that the gain of the PGA2500 may be forced to unity without using the serial port interface. The 0dB input overrides gain settings made through the serial port. While the 0dB input is active (forced high), the serial port register may be updated or data may passed through the serial interface to other PGA2500 devices in daisy-chain configuration. However, any changes made in the gain will not take effect until the 0dB input is driven low.

The zero crossing control input, named ZCEN (pin 9), is provided for enabling and disabling the internal zero crossing detector function. Forcing the ZCEN input high enables the function. Zero crossing detection is used to force gain changes on zero crossings of the analog input signal. This limits the glitch energy associated with switching gain, thereby minimizing audible artifacts at the preamplifier output. Since zero crossing detection can add some delay when performing gain changes (up to 16ms maximum for a detector timeout event), there may be cases where the user may wish to disable the function. Forcing the ZCEN input low disables zero crossing detection, with gain changes occurring immediately when programmed.

An overflow indicator output, OVR, is provided at pin 5. The OVR pin is an active high, CMOS-logic-level output. The overflow output is forced high when the preamplifier output voltage exceeds one of two preset thresholds. The threshold is programmed through the serial port interface using the OL bit. If OL = 0, then the threshold is set to $5.1V_{RMS}$ differential, which is approximately −1dB below the specified output voltage range. If OL = 1, then the threshold is set to $4.0V_{RMS}$ differential, which is approximately −3dB below the specified output voltage range.

The PGA2500 includes four programmable digital outputs, named GPO1 through GPO4 (pins 1 through 4, respectively), which are controlled via the serial port interface. All four pins are CMOS-logic-level outputs. These pins may be used to control relay drivers or switches used for external preamplifier functions, including input pads, filtering, polarity reversal, or phantom power.

ANALOG INPUTS AND OUTPUTS

An analog signal is input differentially across the $V_{IN}+$ (pin 27) and $V_{IN}−$ (pin 26) inputs. The input voltage range and input impedance are provided in the Electrical Characteristics table. The Applications Information section of this datasheet provides additional details regarding typical input circuit considerations when interfacing the PGA2500 to a microphone input.

Both $V_{IN}+$ and $V_{IN}−$ are biased at approximately 0.65V below the common-mode input voltage, supplied at $V_{COM}IN$ (pin 25). The use of AC-coupling capacitors (see Figure 7, page 12) is highly recommended for the analog inputs of the PGA2500. If DC-coupling is required for a given application, the user must take this offset into account.

It is recommended that a small capacitor be connected from each analog input pin to analog ground. Values of at least 50pF are recommended. See Figure 7 (page 12) for larger capacitors being used for EMI filtering which will satisfy this requirement.

The analog output is presented differentially across $V_{OUT}+$ (pin 17) and $V_{OUT}−$ (pin 16). The output voltage range is provided in the Electrical Characteristics table. The analog output is designed to drive a 600Ω differential load while meeting the published THD+N specifications and typical performance curves.

SERIAL PORT OPERATION

The serial port interface for the PGA2500 is comprised of four wires: $\overline{CS}$ (pin 11), SCLK (pin 12), SDI (pin 10), and SDO (pin 13). Figure 2 illustrates the serial port protocol, while Figure 3 and the Electrical Characteristics table provide detailed timing parameters for the port.

The $\overline{CS}$ input functions as the chip select and word latch clock for the serial port. The $\overline{CS}$ input must be low in order to clock data into and out of the serial port. The control word is latched on a low-to-high transition of the $\overline{CS}$ input. The serial port ignores the SCLK and SDI inputs when $\overline{CS}$ is high, and the SDO output is set to a high impedance state while $\overline{CS}$ is high.

The SCLK input is used to clock serial data into the SDI pin and out of the SDO pin. The SDI pin functions as the serial data input, and is used to write the serial port register. The SDO pin is the shift register serial output, and is used for either register read-back or for daisy-chaining multiple PGA2500 devices. Data on SDI is sampled on the rising edge of SCLK, while data is clocked out of SDO on the falling edge of SCLK.

When the 0dB input (pin 8) is forced high, the gain set by the serial port register will be overridden. The serial port register may be updated while the 0dB input is forced high, but the programmed gain will not take effect until the 0dB input is forced low.

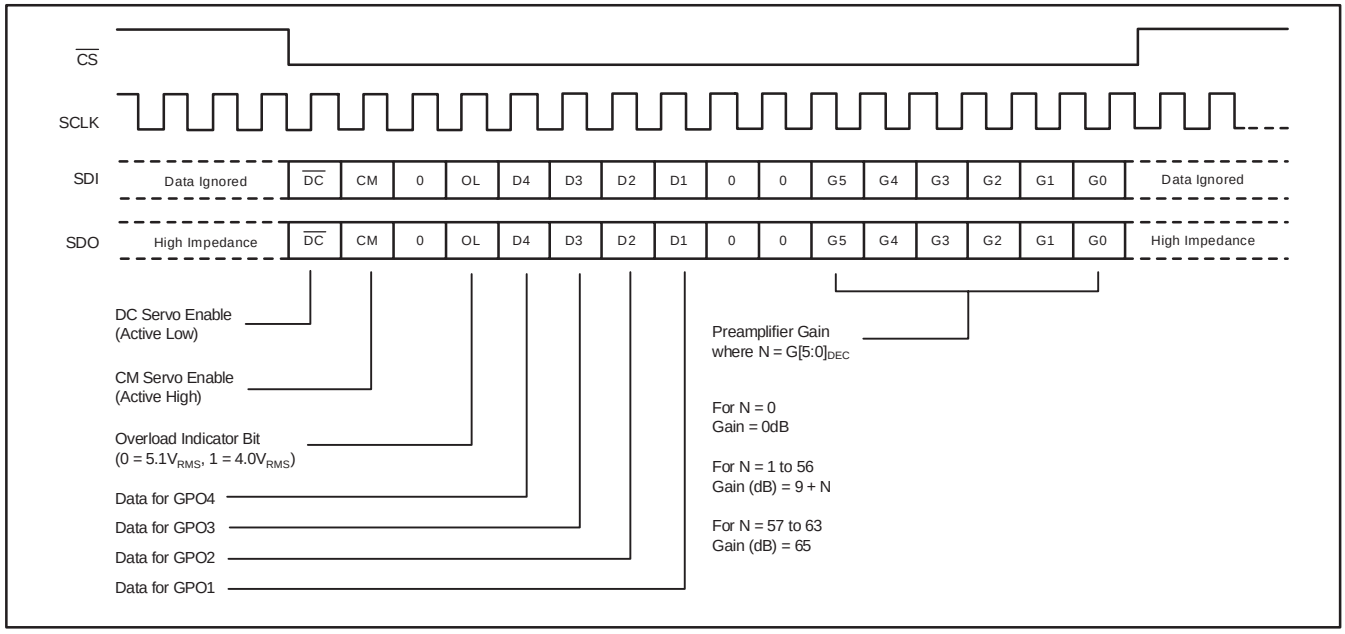


Figure 2. Serial Port Protocol

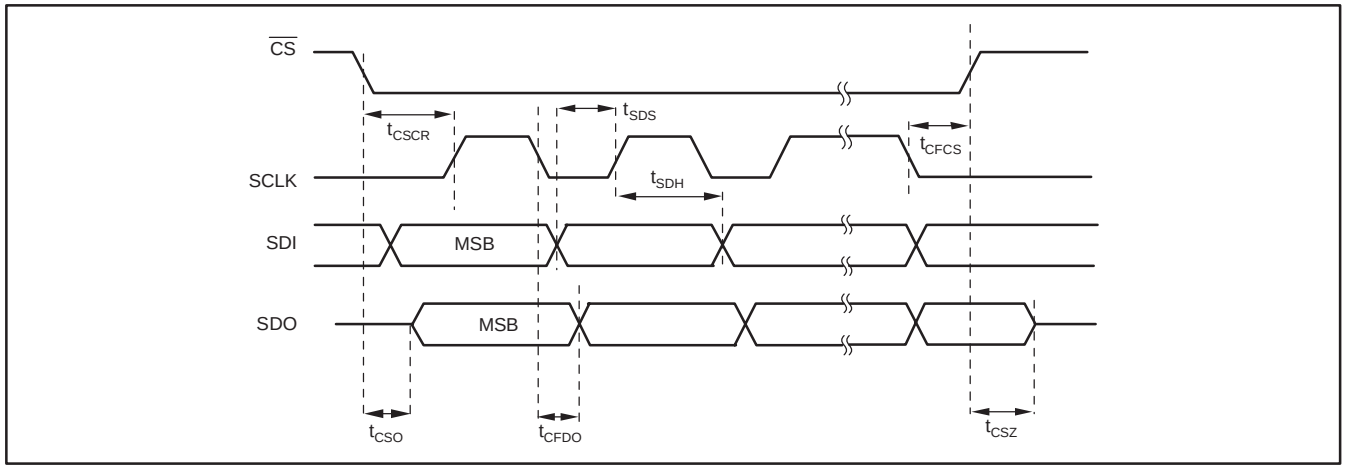


Figure 3. Serial Port Timing Requirements

DAISY-CHAINING MULTIPLE PGA2500 PREAMPLIFIERS

Since the serial port interface may be viewed as a serial in, serial out shift register, multiple PGA2500 preamplifiers may be connected in a cascaded or daisy-chained fashion, as shown in Figure 4. The daisy-chained PGA2500 devices behave as a 16 x *N*-bit shift register, where *N* is the number of cascaded PGA2500 devices. To program all of the devices, simply force $\overline{CS}$ low for 16 x *N* serial clock periods and clock in 16 x *N* bits of control data. The $\overline{CS}$ input is then forced high to latch in the new settings.

A timing diagram for the daisy-chain application is shown in Figure 5.

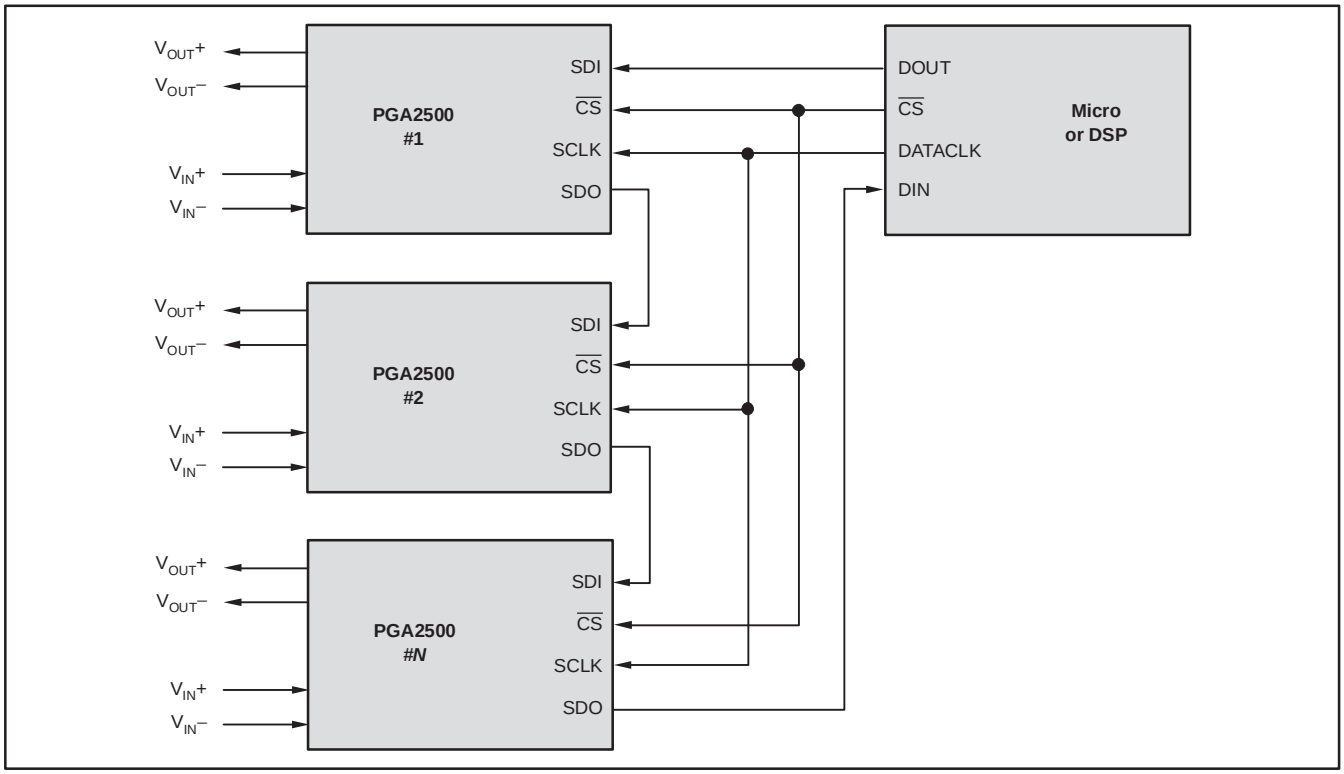


Figure 4. Daisy-Chain Configuration for Multiple PGA2500 Preamplifiers

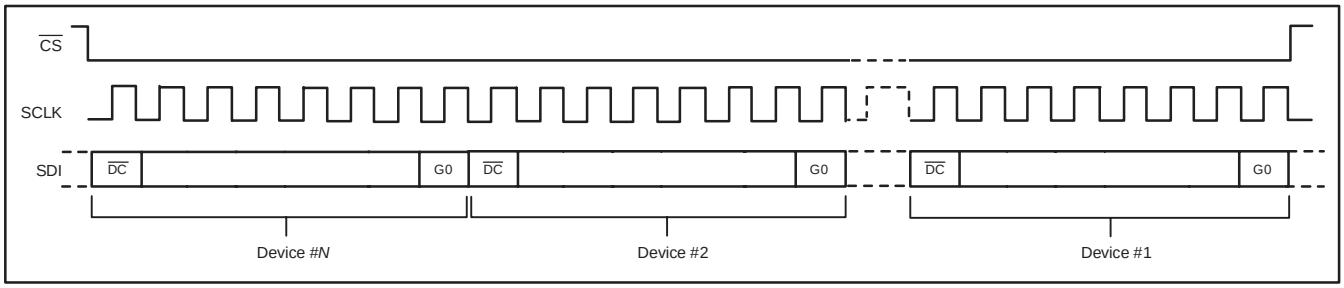


Figure 5. Serial Port Operation for Daisy-Chain Operation

APPLICATION INFORMATION

This section provides practical information for designing the PGA2500 into end applications.

BASIC CIRCUIT CONFIGURATION

A typical applications circuit, without the input and output circuitry, is shown in Figure 6. Power-supply bypass and DC servo capacitors are shown with recommended values. All capacitors should be placed as close as possible to the PGA2500 package to limit inductive noise coupling. Surface-mount capacitors are recommended (X7R ceramic for the 0.1µF and 1µF capacitors, and low ESR tantalum for the 4.7µF capacitors).

The PGA2500 can be placed on a split ground plane, with the package located over the split. However, there must be a low impedance connection between the analog and digital grounds at a common return point.

The DC common-mode input, $V_{COM}IN$ (pin 25), can be connected to analog ground or a DC voltage (such as the reference or common voltage output of an audio ADC). When biasing this input to a DC voltage, keep in mind that both the analog output and input pins are level-shifted by the value of the bias voltage.

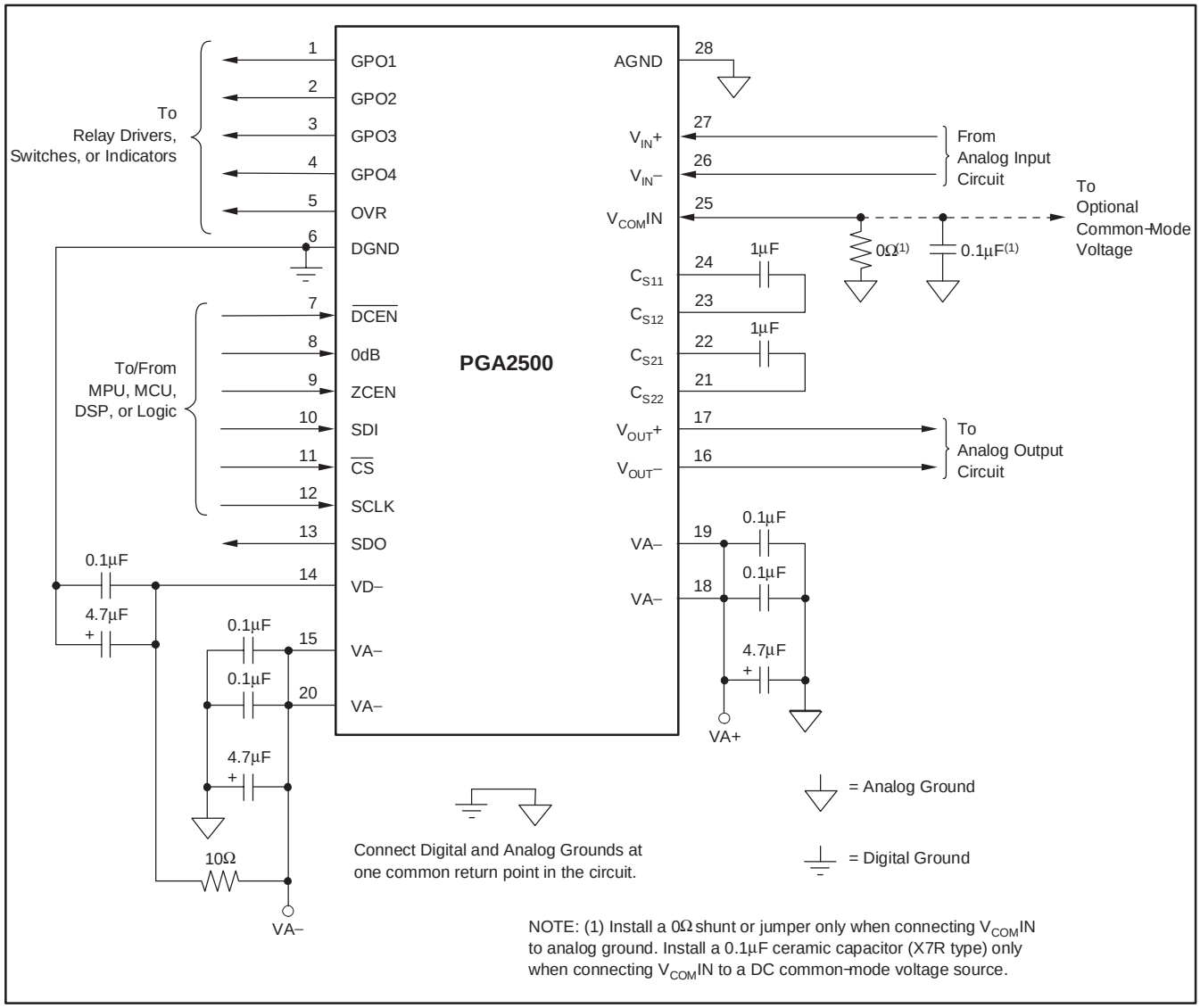


Figure 6. Basic Circuit Configuration for the PGA2500

INPUT CIRCUIT CONSIDERATIONS

The input circuit for the PGA2500 must include several items that are common to most microphone preamplifiers. Figure 7 shows a typical input circuit configuration. Other functions, such as input attenuation (pads), filters, and polarity reversal switches are commonly found in preamplifier circuits, but are not shown here in order to focus on the basic input circuit requirements.

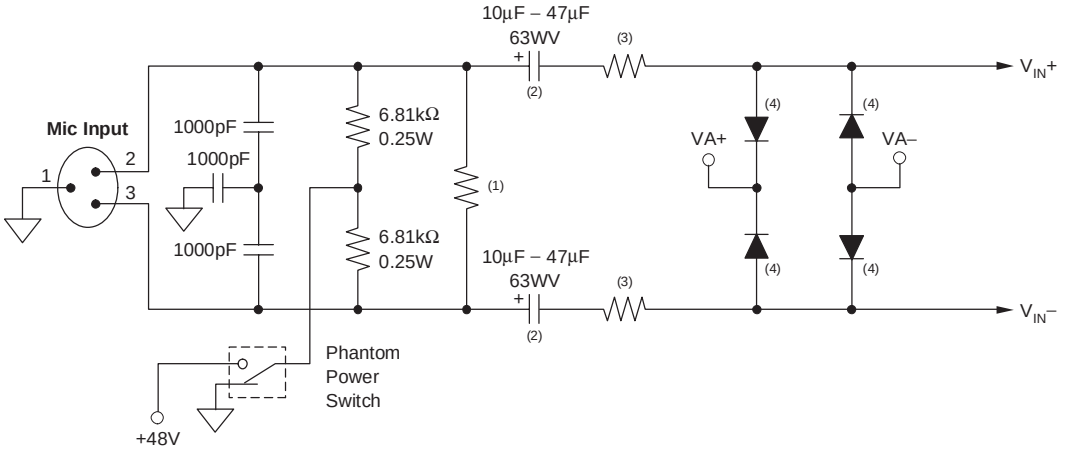
The microphone input is typically taken from a balanced XLR or TRS input connection (XLR shown). The 1000pF capacitors provide simple EMI filtering for the circuit. Additional filtering for low- or high-frequency noise may be added, depending upon the end application environment. A bridging resistor is shown and may be selected to provide the desired overall input impedance required for a given microphone. This resistance will be in parallel with the phantom power bias resistors and the PGA2500 input resistance to set the actual impedance seen by the microphone.

Connections for +48V phantom power, required for condenser microphones, are shown in Figure 7. The phantom power requires an On/Off switch, as dynamic microphones do not require phantom power and may be damaged if power is applied. DC-blocking capacitors are required between the phantom power connections and the PGA2500 inputs. The blocking capacitors are selected to have a high working voltage rating, with 50V being the minimum and 63V recommended for long term reliability.

The blocking capacitors, along with the PGA2500 input resistance, form a high-pass filter circuit. With the typical input resistance of the PGA2500 specified in the Electrical Characteristics table, the value of the capacitor can be chosen to meet the desired low frequency response for the end application. At the same time, the value should be no higher than required, since larger capacitors store more charge and increase the surge current seen at the preamplifier when a short circuit occurs on the microphone input connector.

To protect the PGA2500 from large surge currents, power Schottky diodes are placed on the input pins to both the VA+ and VA− power supplies. Schottky diodes are used due to their lower turn-on voltage compared to standard rectifier diodes. Power devices are required since the surge currents from a large valued blocking capacitor (47µF) can exceed 4.5 amps for a very short duration of time. It is recommended that the Schottky diode chosen for this application be specified for at least a 10A surge current.

The use of a series current-limiting resistor prior to the protection diodes will aid in handling surge currents, although the resistor will add noise to the circuit. Select a current-liming resistor value that is as high as tolerable for the desired noise performance of the preamplifier circuit.



NOTES: (1) Bridging resistor, used to set the impedance seen by the microphone.
(2) The blocking capacitor value is selected based upon the desired low frequency response.
(3) Current-limiting resistor. Select the highest value tolerable based upon input noise requirements.
(4) Schottky diode, selected for fast turn-on and rated for a minimum of a 10A surge current.
Recommended device is the MBRA120LT3 from ON Semiconductor.

Figure 7. Typical Input Circuit for the PGA2500

OPERATION WITH $V_{COM}IN$ = +2.5V

When interfacing the analog outputs of the PGA2500 with audio ADC inputs, the converter will frequently have a common-mode DC output pin. This pin may be connected to the $V_{COM}IN$ pin of the PGA2500 in order to facilitate a DC-coupled interface between the two devices. The common-mode DC voltage level is typically +2.5V, although some converters may have a slightly lower value, usually between +2.1V and +2.5V. There are several issues that must be considered when operating the PGA2500 in this fashion.

Both the analog input and output pins of the PGA2500 will be level shifted by the $V_{COM}IN$ voltage. The analog outputs will be shifted to the $V_{COM}IN$ level, while the analog inputs will be shifted to approximately $V_{COM}IN$ − 0.65V, due to the offset that normally exists on the input pins. The level shifting will limit the input and output swing of the PGA2500, reducing the overall signal-to-noise ratio and degrading the THD+N performance.

Given $V_{COM}IN$ = +2.5V and gains of 10dB through 65dB, the output swing is limited to less than one-half that specified in the Electrical Characteristics table. The output will hard-clip at approximately a diode drop below the VA+ supply rail and a diode drop above analog ground.

Given $V_{COM}IN$ = +2.5V and a gain of 0dB, the practical maximum input or output voltage swing is approximately 1.0Vrms differential. Increasing the signal level much beyond this point will result in a substantial increase in distortion.

Plots of THD+N vs Frequency are shown in the Typical Characteristics section of this datasheet for both $V_{COM}IN$ = 0V and +2.5V. The performance difference can be seen when comparing the plots. The user needs to consider whether the difference is acceptable for the end application.

As a suggested alternative, the PGA2500 analog outputs may be AC-coupled to the ADC inputs, allowing the PGA2500 to operate with $V_{COM}IN$ = 0V in order to achieve best performance. The AC-coupling capacitors will affect the overall low-frequency response of the preamplifier and converter combination, and the user is advised to choose a value that best suits the application requirements.

Figure 8 illustrates a typical PGA2500 to audio ADC interface utilizing AC-coupling. In addition to the coupling capacitors, a passive RC filter is required as an anti-alias filter for the converter. The vast majority of audio ADCs are of the oversampling delta-sigma variety, with a simple single-pole filter meeting the anti-aliasing requirements for this type of converter. Providing at least 6dB of attenuation will also allow the PGA2500 to operate near full signal swing without overdriving the ADC inputs.

Figure 9 illustrates an application where the $V_{COM}IN$ pin of the PGA2500 is connected to the common-mode DC output of the audio ADC, with a DC-coupled interface between the PGA2500 analog outputs and the ADC analog inputs.

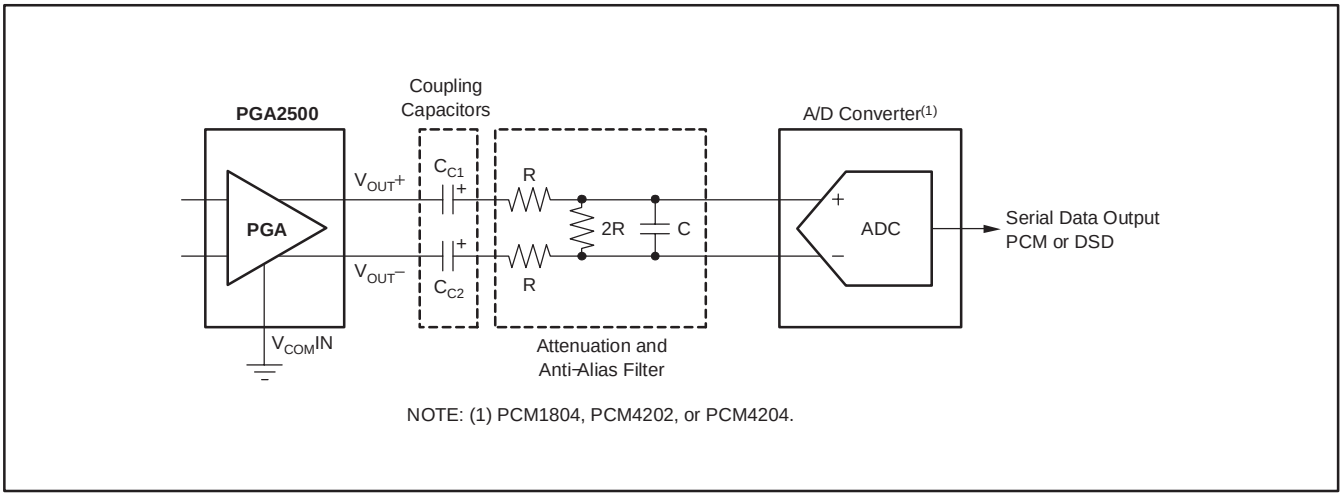


Figure 8. PGA2500 Analog Output to ADC Analog Input Interface, AC-Coupled

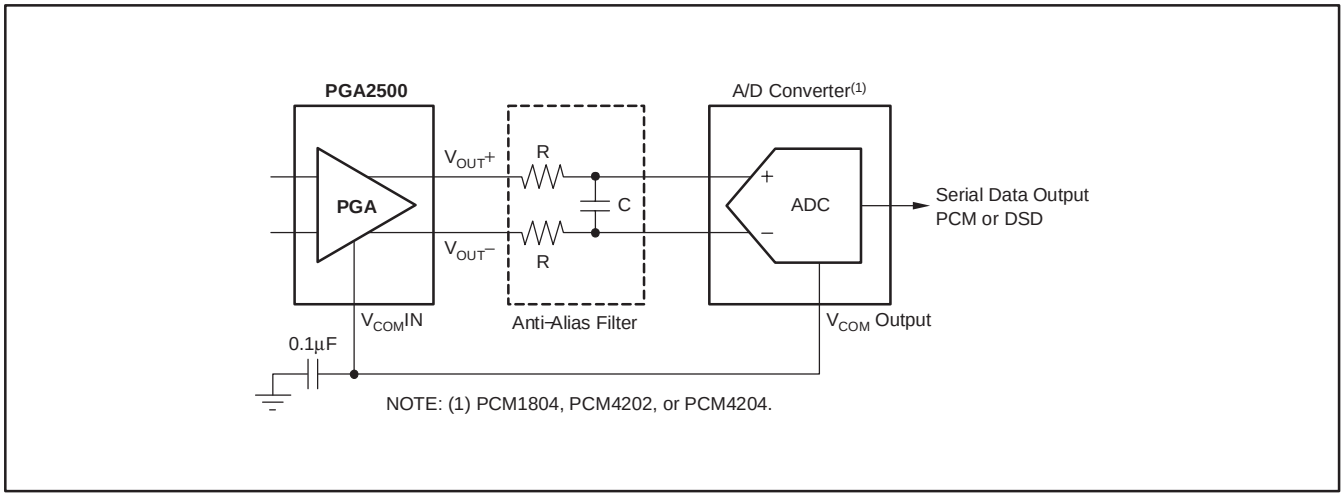


Figure 9. PGA2500 Analog Output to ADC Analog Input Interface, DC-Coupled

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PGA2500IDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA2500IDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA2500IDBR	ACTIVE	SSOP	DB	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PGA2500IDBRG4	ACTIVE	SSOP	DB	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

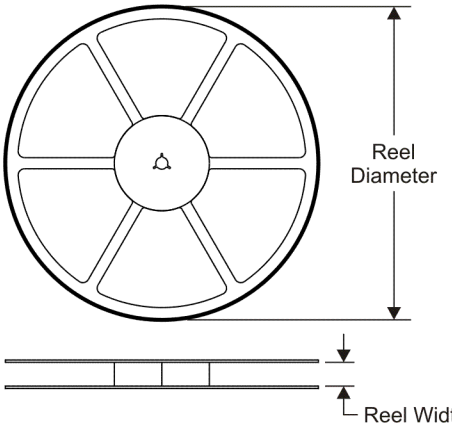
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

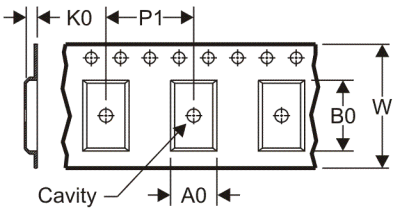
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

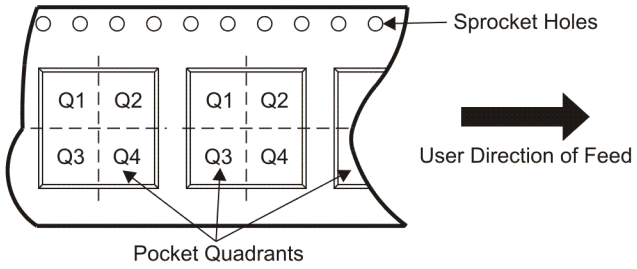


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

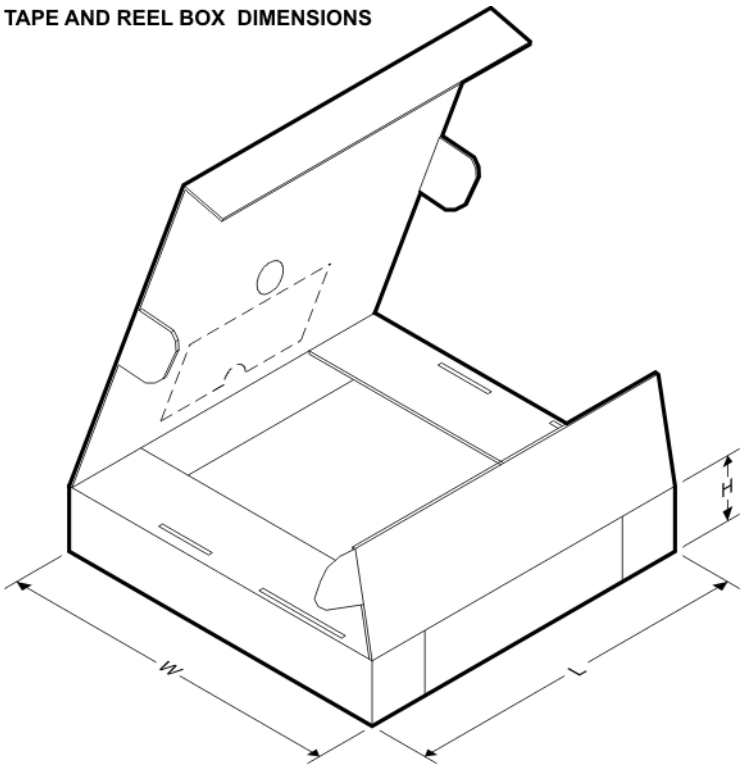
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA2500IDBR	SSOP	DB	28	1000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



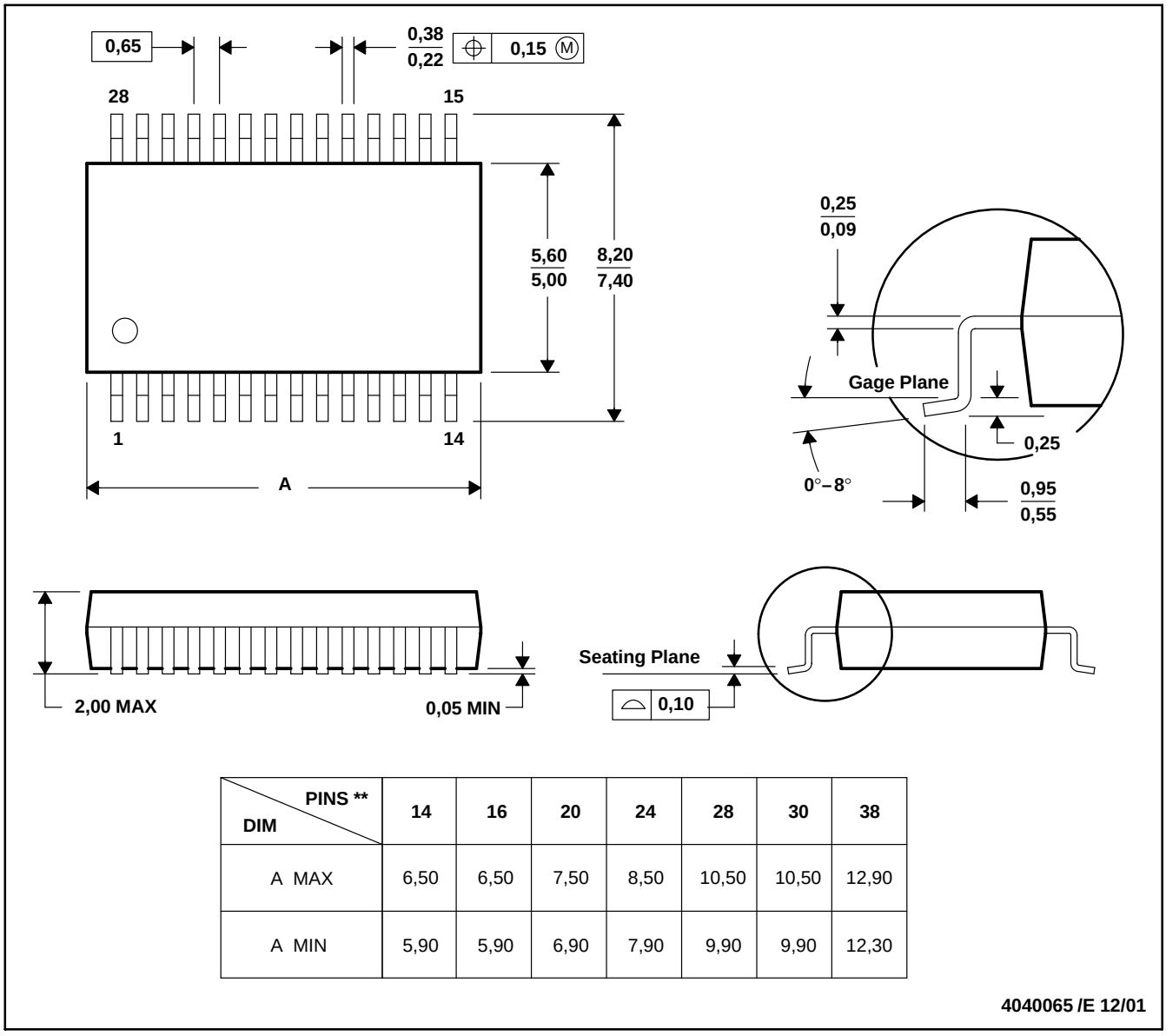
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA2500IDBR	SSOP	DB	28	1000	346.0	346.0	33.0

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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