



**THE DATASHEET OF
PH8030L,115**



Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use salesaddresses@nexperia.com (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

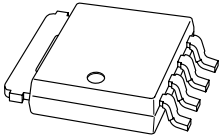
Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via salesaddresses@nexperia.com). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia



PH8030L

N-channel TrenchMOS logic level FET

Rev. 01 — 6 February 2006

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Optimized for use in DC-to-DC converters
- Logic level compatible
- Very low switching and conduction losses
- Lead-free package

1.3 Applications

- DC-to-DC converters
- Voltage regulators
- Switched-mode power supplies
- Notebook computers

1.4 Quick reference data

- $V_{DS} \leq 30\text{ V}$
- $R_{DS(on)} \leq 5.9\text{ m}\Omega$
- $I_D \leq 76.7\text{ A}$
- $Q_{GD} = 3.1\text{ nC (typ)}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)		
4	gate (G)		
mb	mounting base; connected to drain (D)		

SOT669 (LPAK)

3. Ordering information

Table 2: Ordering information

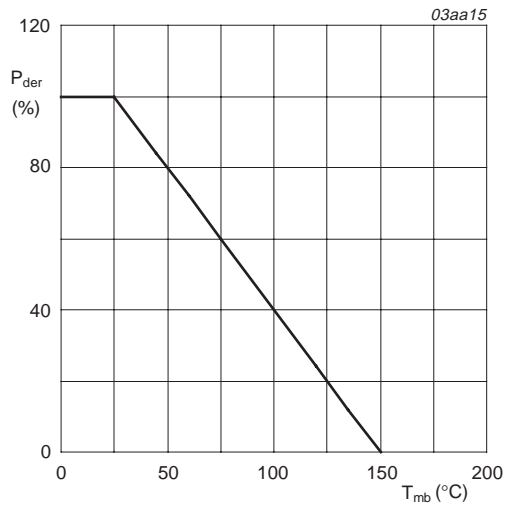
Type number	Package		
	Name	Description	Version
PH8030L	LFPAK	plastic single-ended surface mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 3: Limiting values

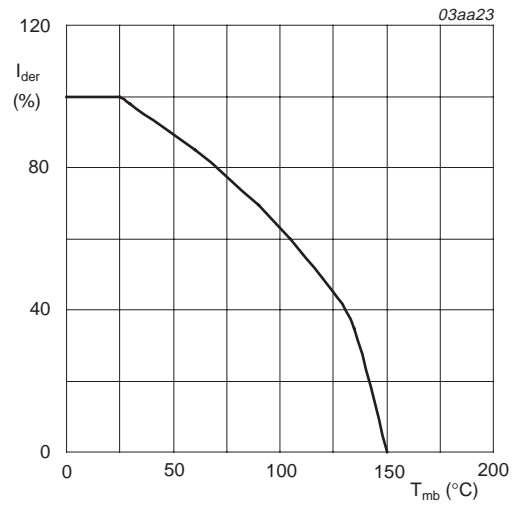
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2 and 3	-	76.7	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2	-	48.5	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	300	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	$^{\circ}\text{C}$
T_j	junction temperature		-55	+150	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	208	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 31\text{ A}$; $t_p = 0.14\text{ ms}$; $V_{DS} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting at $T_j = 25\text{ °C}$	-	95	mJ



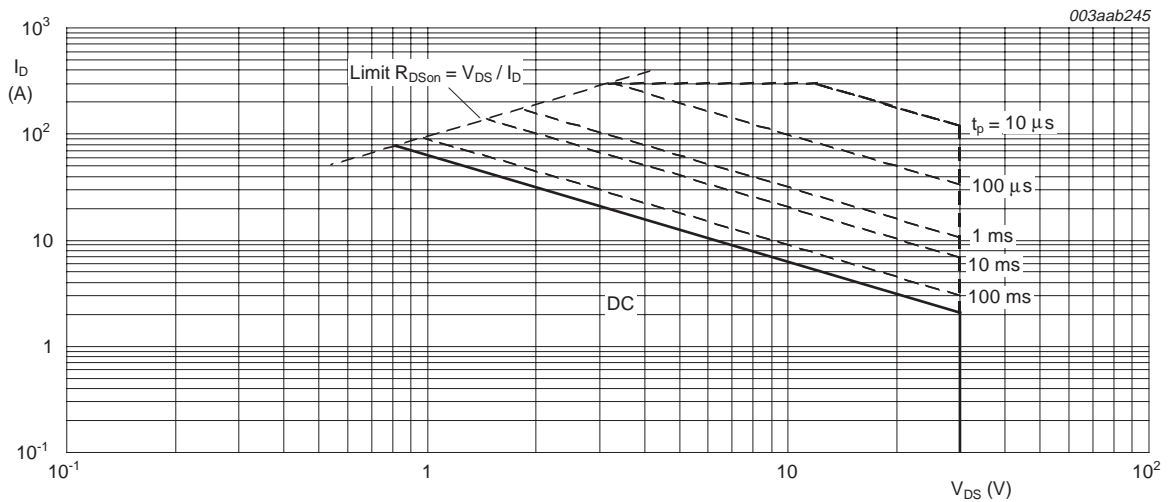
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2	K/W

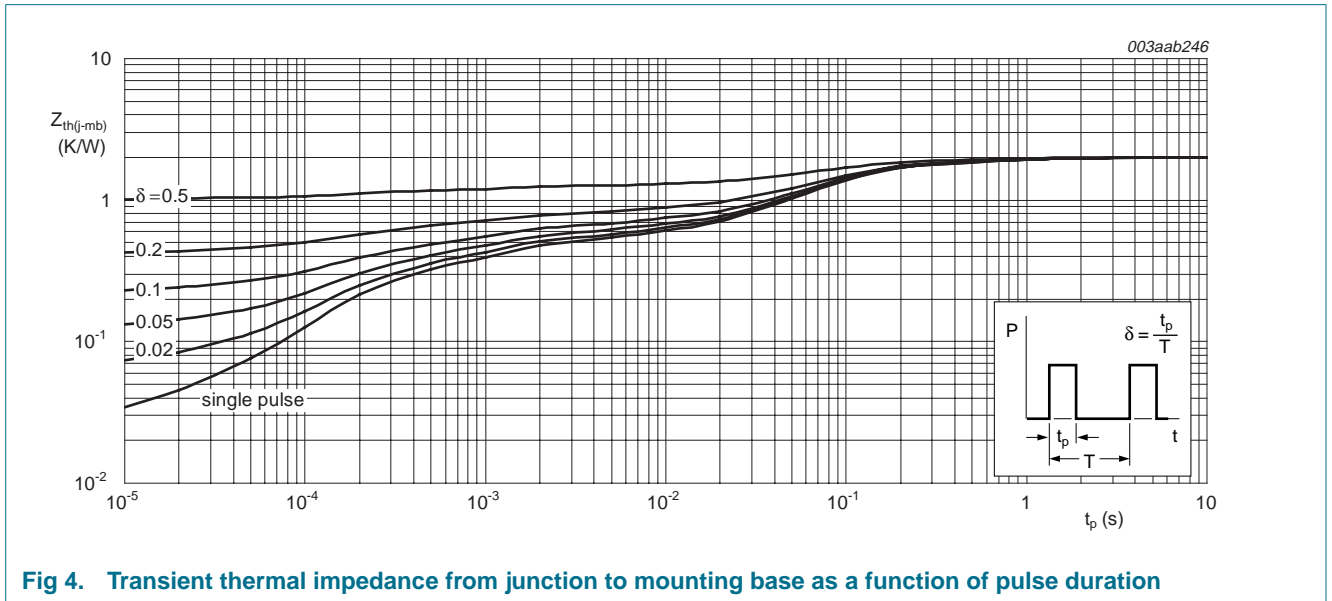
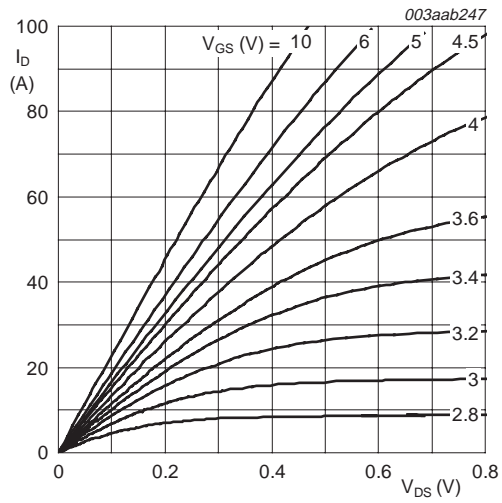


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

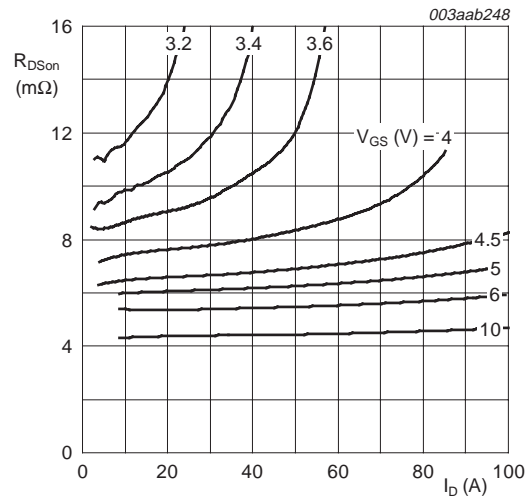
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V T _j = 25 °C	30	-	-	V
		T _j = -55 °C	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; see Figure 9 and 10 T _j = 25 °C	1.3	1.7	2.15	V
		T _j = 150 °C	0.8	-	-	V
		T _j = -55 °C	-	-	2.6	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V T _j = 25 °C	-	-	1	μA
		T _j = 150 °C	-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = ±16 V; V _{DS} = 0 V	-	-	100	nA
R _G	gate resistance	f = 1 MHz	-	1.75	-	Ω
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; see Figure 6 and 8 T _j = 25 °C	-	4.7	5.9	mΩ
		T _j = 150 °C	-	8.5	10.6	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; see Figure 6 and 8	-	7.3	9.7	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; see Figure 11 and 12	-	15.2	-	nC
Q _{GS}	gate-source charge		-	8.5	-	nC
Q _{GS1}	pre-V _{GS(th)} gate-source charge		-	4.1	-	nC
Q _{GS2}	post-V _{GS(th)} gate-source charge		-	4.4	-	nC
Q _{GD}	gate-drain charge		-	3.1	-	nC
V _{GS(pl)}	gate-source plateau voltage		-	3.5	-	V
Q _{G(tot)}	total gate charge	I _D = 0 A; V _{DS} = 0 V; V _{GS} = 4.5 V	-	14	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 12 V; f = 1 MHz; see Figure 14	-	2260	-	pF
C _{oss}	output capacitance		-	460	-	pF
C _{rss}	reverse transfer capacitance		-	210	-	pF
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 0 V; f = 1 MHz	-	2540	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 12 V; R _L = 0.5 Ω; V _{GS} = 4.5 V;	-	25	-	ns
t _r	rise time	R _G = 5.6 Ω	-	53	-	ns
t _{d(off)}	turn-off delay time		-	27	-	ns
t _f	fall time		-	14	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; see Figure 13	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V	-	34	-	ns
Q _r	recovered charge		-	11.5	-	nC



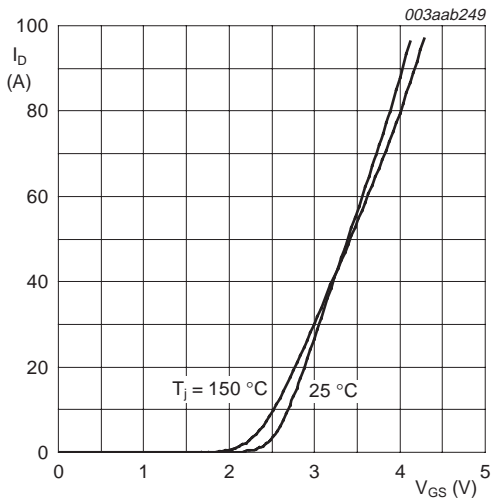
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



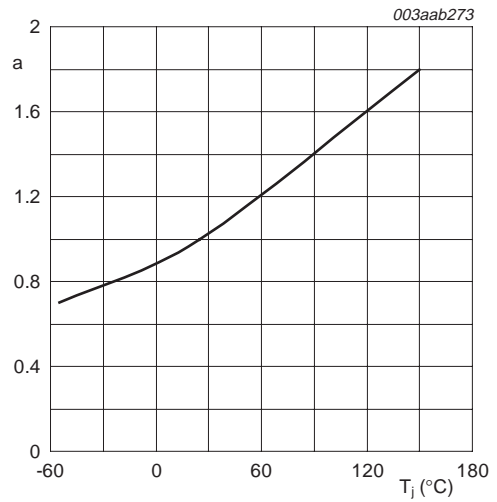
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



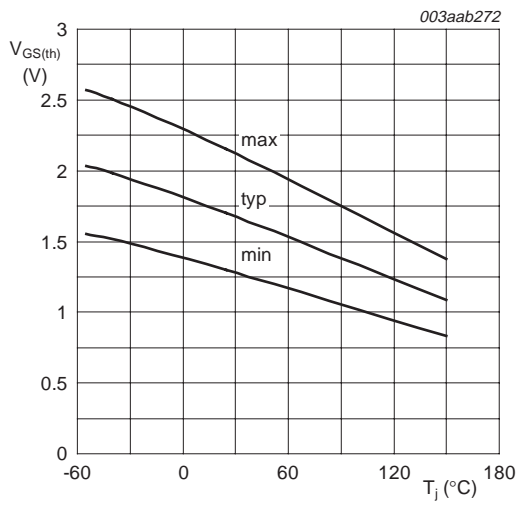
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



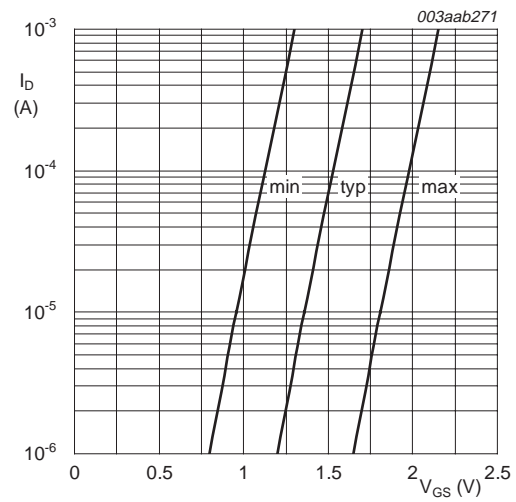
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ }^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



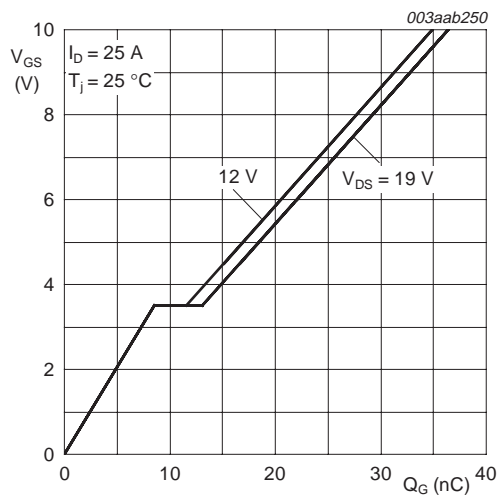
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V and } 19 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

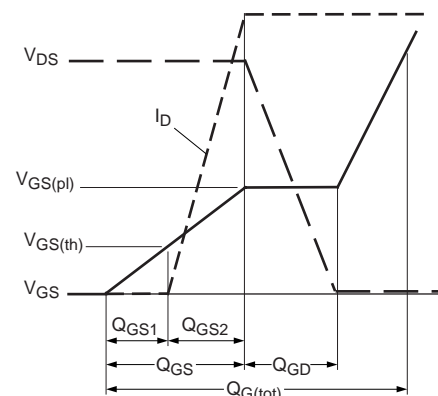
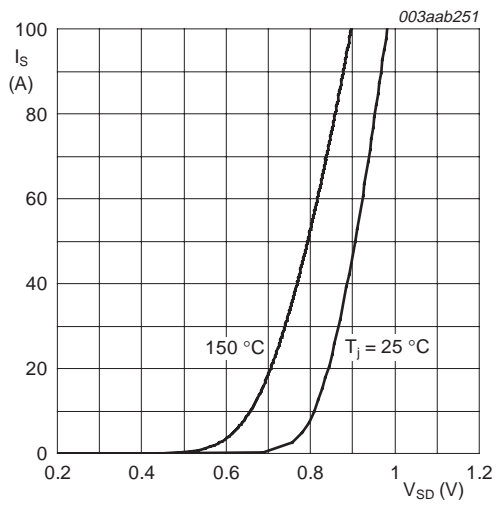
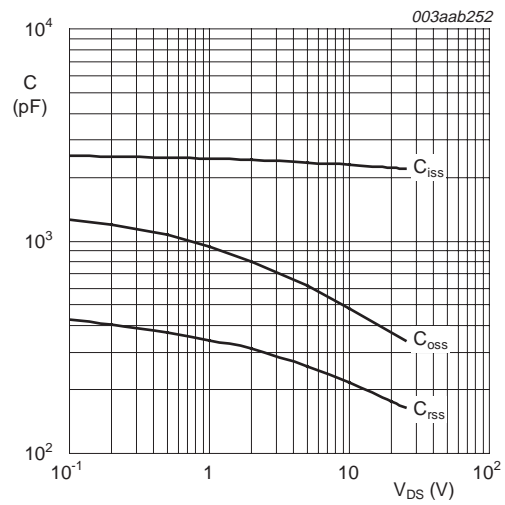


Fig 12. Gate charge waveform definitions



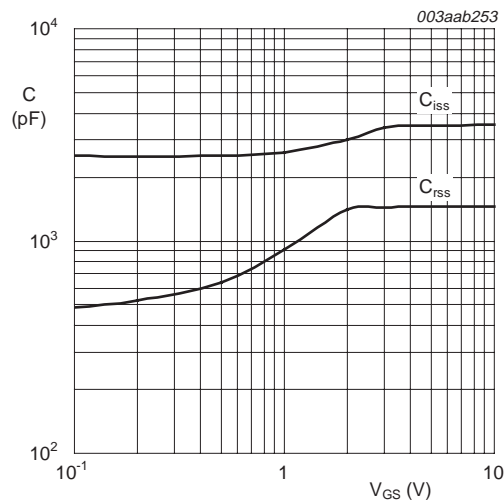
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 15. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

7. Package outline

Plastic single-ended surface mounted package (LPAK); 4 leads

SOT669

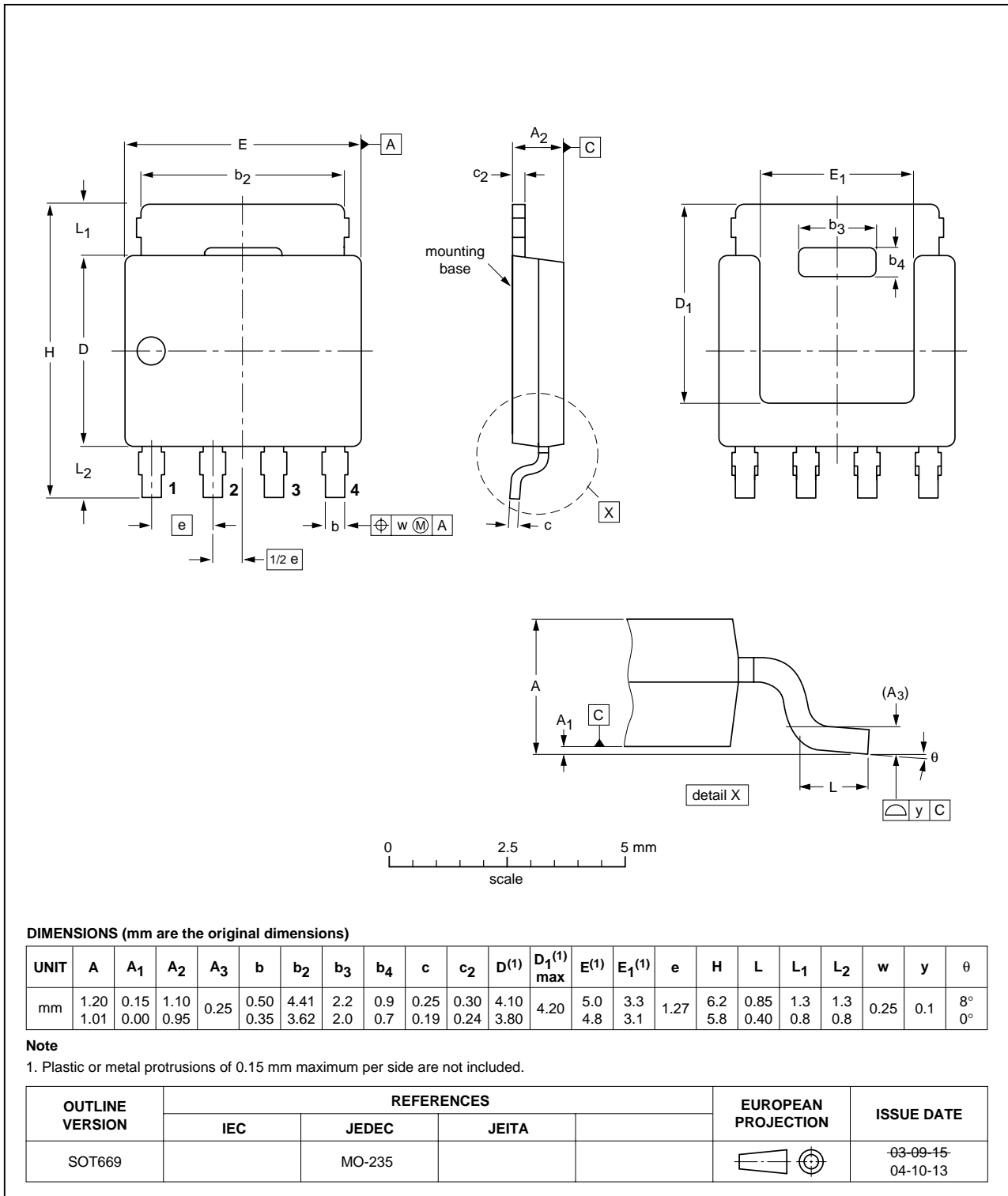


Fig 16. Package outline SOT669 (LPAK)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH8030L_1	20060206	Product data sheet	-	-	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^[2] ^[3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

10. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

11. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors

13. Contact information

For additional information, please visit: <http://www.semiconductors.philips.com>

For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com

customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

12. Trademarks

Notice — All referenced brands, product names, service names and trademarks are the property of their respective owners.

TrenchMOS — is a trademark of Koninklijke Philips Electronics N.V.

14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
6	Characteristics	5
7	Package outline	9
8	Revision history	10
9	Data sheet status	11
10	Definitions	11
11	Disclaimers	11
12	Trademarks	11
13	Contact information	11



© Koninklijke Philips Electronics N.V. 2006



All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Date of release: 6 February 2006
Document number: PH8030L_1

Published in The Netherlands

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View PH8030L,115 on WIN SOURCE](#)
-  [NXP / Nexperia Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management