



# THE DATASHEET OF PLL1700E





# MULTI-CLOCK GENERATOR

## FEATURES

- 27MHz MASTER CLOCK INPUT
- GENERATED AUDIO SYSTEM CLOCK:
  - SCKO1: 33.8688MHz (Fixed)
  - SCKO2:  $256f_S$
  - SCKO3:  $384f_S$
  - SCKO4:  $768f_S$
- ZERO PPM ERROR OUTPUT CLOCKS
- LOW CLOCK JITTER: 150ps at SCKO3
- MULTIPLE SAMPLING FREQUENCIES:
  - $f_S = 32\text{kHz}, 44.1\text{kHz}, 48\text{kHz}, 64\text{kHz},$
  - $88.2\text{kHz}, 96\text{kHz}$
- +3.3V CMOS LOGIC INTERFACE
- DUAL POWER SUPPLIES: +5V and +3.3V
- SMALL PACKAGE: 20-Lead SSOP

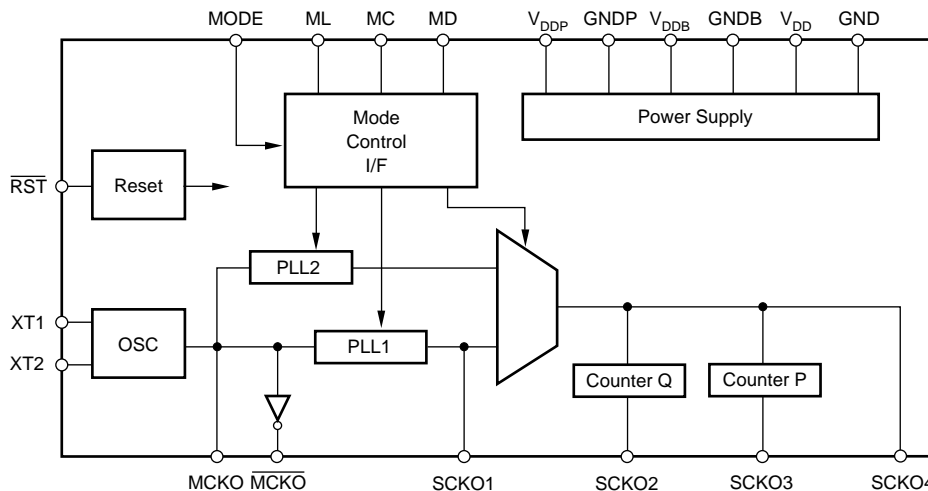
## DESCRIPTION

The PLL1700 is a low cost, multi-clock generator Phase Lock Loop (PLL).

The PLL1700 can generate four systems clocks from a 27MHz reference input frequency.

The device gives customers both cost and space savings by eliminating external components and enables customers to achieve the very low jitter performance needed for high-performance audio digital-to-analog converters (DACs) and/or analog-to-digital converters (ADCs).

The PLL1700 is ideal for MPEG-2 applications that use a 27MHz master clock such as DVD players, DVD add-on cards for multimedia PCs, digital HDTV systems, and set-top boxes.



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# ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage (+V <sub>DD</sub> , +V <sub>DDP</sub> , +V <sub>DDB</sub> )	+6.5V
Supply Voltage Differences (+V <sub>DD</sub> , +V <sub>DDP</sub> )	±0.1V
GND Voltage Differences: GND, GNDP, GNDB	±0.1V
Digital Input Voltage	-0.3V to (V <sub>DD</sub> + 0.3V)
Digital Output Voltage	-0.3V to (V <sub>DDB</sub> + 0.3V)
Input Current (any pins except supply pins)	±10mA
Power Dissipation	300mW
Operating Temperature Range	-25°C to +85°C
Storage Temperature	-55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR reflow, 10s)	+235°C

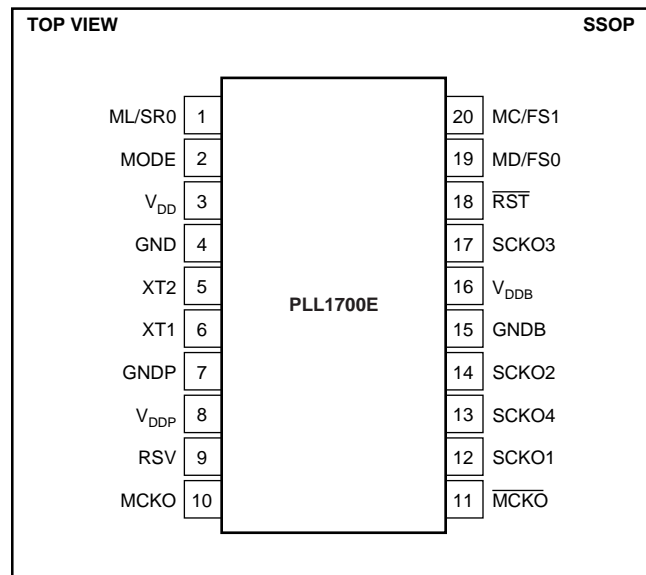
NOTE: (1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## PACKAGE INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE	SPECIFIED TEMPERATURE RANGE	PACKAGE DESIGNATOR
PLL1700E	20-Lead SSOP	-25°C to +85°C	DB

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at [www.ti.com](http://www.ti.com).

## PIN CONFIGURATION



## PIN ASSIGNMENTS

PIN	NAME	I/O	FUNCTION
1	ML/SR0	IN	Latch Enable for Software Mode/Sampling Rate Selection for Hardware Mode. When MODE pin is LOW, ML is selected. <sup>(1)</sup>
2	MODE	IN	Mode Control Select. When this pin is HIGH, device is operated in hardware mode using SR0 (pin 1), FS0 (pin 19), and FS1 (pin 20). When this pin is LOW, device is operated in software mode by three-wire interface using ML (pin 1), MD (pin 19) and MC (pin 20). <sup>(1)</sup>
3	V <sub>DD</sub>	—	Digital Power Supply, +5V.
4	GND	—	Digital Ground.
5	XT2	—	27MHz Crystal. When an external 27MHz clock is applied to XT1 (pin 6), this pin must be connected to GND.
6	XT1	IN	27MHz Oscillator Input/External 27MHz Input.
7	GNDP	—	Ground for PLL.
8	V <sub>DDP</sub>	—	Power Supply for PLL, +5V.
9	RSV	—	Reserved. Must be left open.
10	MCKO	OUT	27MHz Output.
11	MCKO-bar	OUT	Inverted 27MHz Output.
12	SCKO1	OUT	Fixed 33.8688MHz Clock Output.
13	SCKO4	OUT	768f <sub>s</sub> Clock Output.
14	SCKO2	OUT	256f <sub>s</sub> Clock Output.
15	GNDB	—	Digital Ground for V <sub>DDB</sub> .
16	V <sub>DDB</sub>	—	Digital Power Supply for Clock Output Buffers, +3.3V.
17	SCKO3	OUT	384f <sub>s</sub> Output. This output has been optimized for the lowest jitter and should be connected to the audio DAC(s).
18	RST-bar	IN	Reset. When this pin is LOW, device is held in reset. <sup>(1)</sup>
19	MD/FS0	IN	Serial Data Input for Software Mode/Sampling Frequency Selection for Hardware Mode. When MODE pin is LOW, MD is selected. <sup>(1)</sup>
20	MC/FS1	IN	Shift Clock Input for Software Mode/Sampling Frequency Selection for Hardware Mode. When MODE pin is LOW, MC is selected. <sup>(1)</sup>

NOTE: (1) Schmitt-trigger input with internal pull-down resistors.

# ELECTRICAL CHARACTERISTICS

All specifications at  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = V_{DDP} = +5\text{V}$ ,  $V_{DDB} = +3.3\text{V}$ ,  $f_M = 27\text{MHz}$  crystal oscillation, and  $f_S = 48\text{kHz}$ , unless otherwise noted.

PARAMETER	CONDITIONS	PLL1700E			UNITS
		MIN	TYP	MAX	
<b>DIGITAL INPUT/OUTPUT</b> Input Logic Level: $V_{IH}^{(1)}$ $V_{IL}^{(1)}$ $V_{IH}^{(2)}$ $V_{IL}^{(2)}$ Input Logic Current: $I_{IH}^{(1)}$ $I_{IL}^{(1)}$ $I_{IH}^{(2)}$ $I_{IL}^{(2)}$ Output Logic Level: $V_{OH}^{(3)}$ $V_{OL}^{(3)}$ Sampling Frequency ( $f_S$ )			TTL-Compatible		
		2.0		0.8	VDC
		1.2		0.4	VDC
				200	$\mu\text{A}$
				-1	$\mu\text{A}$
				4	mA
				-800	$\mu\text{A}$
			CMOS		
			$V_{DDB} - 0.4\text{V}$		VDC
				0.4	VDC
		32	44.1	48	kHz
		64	88.2	96	kHz
<b>MASTER CLOCK (MCKO, <math>\overline{\text{MCKO}}</math>)</b> Master Clock Frequency Clock Jitter <sup>(4)</sup> Clock Duty Cycle $\overline{\text{MCKO}}$ For Crystal Oscillation $\overline{\text{MCKO}}$ Clock Duty Cycle $\overline{\text{MCKO}}$ For External Clock $\overline{\text{MCKO}}$	$f_M = 27\text{MHz}$ , $C_L = 20\text{pF}$	26.73	27	27.27	MHz
	$C_1 = C_2 = 15\text{pF}$	40	50	60	%
		40	50	60	%
			40	60	%
				60	%
<b>PHASE LOCK LOOP (PLL)</b> Generated System Clock Frequency SCKO1 SCKO2 SCKO3 SCKO4 Generated Clock Rise Time <sup>(3)</sup> Generated Clock Fall Time <sup>(3)</sup> Generated Clock Duty Cycle  Generated Clock Jitter <sup>(4)</sup>  Settling Time Power-Up Time	$f_M = 27\text{MHz}$ , $C_L = 20\text{pF}$		33.8688		MHz
	Fixed	8.192		24.576	MHz
	$256f_S$	12.288		36.864	MHz
	$384f_S$	24.576		36.864	MHz
	$768f_S$		5		ns
	20% to 80% $V_{DDB}$		5		ns
	80% to 20% $V_{DDB}$				
	SCKO1, SCKO3, SCKO4	40	50	60	%
	SCKO2 (standard)	40	50	60	%
	SCKO2 (double) <sup>(5)</sup>	25	33	40	%
	SCKO1, SCKO2 (standard), SCKO4		300		ps
	SCKO3		150		ps
SCKO2 (double)		450		ps	
To Programmed Frequency			20	ms	
To Programmed Frequency			15	ms	
<b>POWER SUPPLY REQUIREMENTS</b> Voltage Range  Supply Current <sup>(6)</sup> : $I_{DD} + I_{DDP}$ $I_{DDB}$ Power Dissipation	$V_{DD}, V_{DDP}$ $V_{DDB}$	+4.5 +2.7	+5 +3.3	+5.5 +3.6	VDC VDC
	$V_{DD} = V_{DDP} = 5\text{V}$ , $f_S = 48\text{kHz}$		11	16	mA
	$V_{DDB} = +3.3\text{V}$ , $f_S = 48\text{kHz}$		6	9	mA
	$f_S = 48\text{kHz}$		75	110	mW
<b>TEMPERATURE RANGE</b> Operation Storage		-25 -55		+85 +125	$^\circ\text{C}$ $^\circ\text{C}$

NOTES: (1) ML, MC, MD, MODE,  $\overline{\text{RST}}$  (Schmitt-trigger input with internal pull-down resistor).

(2) XT1, when an external 27MHz clock is used, the buffer ICs, such as 74HC04, are recommended to interface to XT1.

(3) MCKO,  $\overline{\text{MCKO}}$ , SCKO4, SCKO3, SCKO2, and SCKO1.

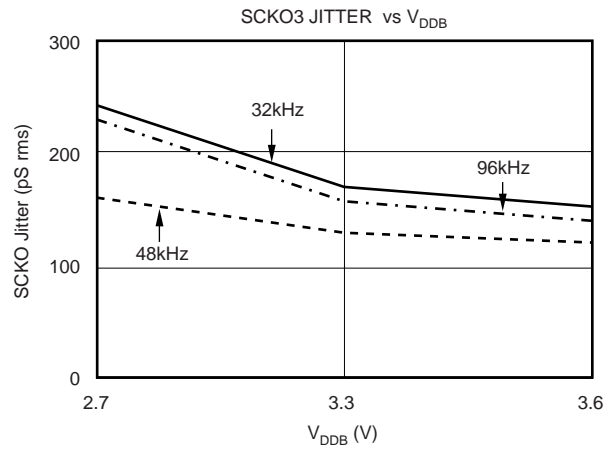
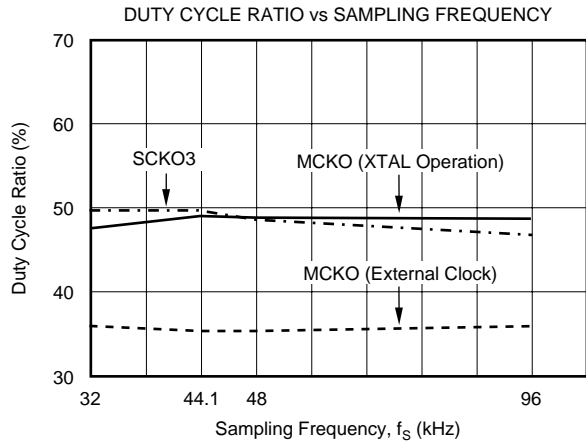
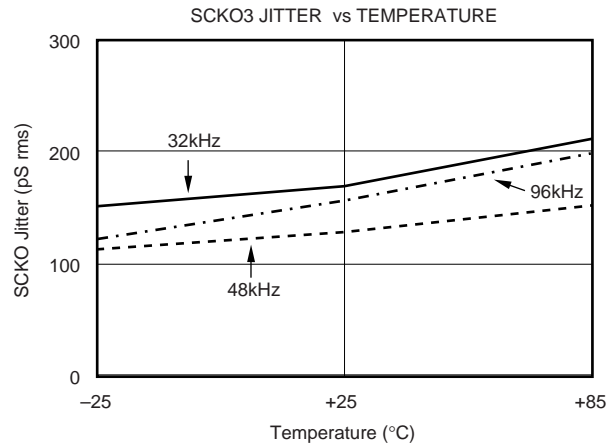
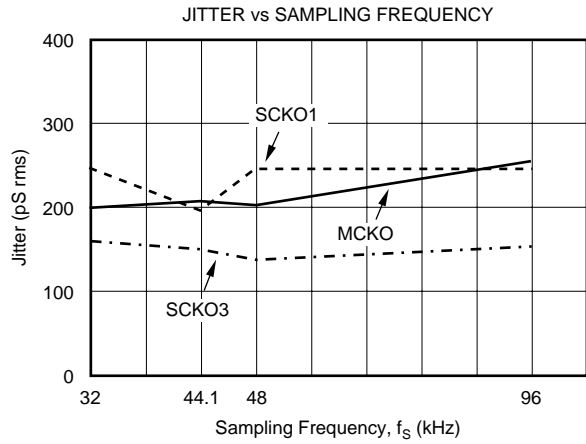
(4) Jitter performance is specified as standard deviation of jitter under 27MHz crystal oscillation.

(5) When SCKO2 is set to double rate clock output, its duty cycle is 33%.

(6)  $f_M = 27\text{MHz}$  crystal oscillation, no load on MCKO,  $\overline{\text{MCKO}}$ , SCKO4, SCKO3, SCKO2, and SCKO1.

# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = V_{DDP} = +5\text{V}$ ,  $V_{DDB} = +3.3\text{V}$ ,  $C_L = 20\text{pF}$ , unless otherwise noted.



# THEORY OF OPERATION

## MASTER CLOCK AND SYSTEM CLOCK OUTPUT

The PLL1700 consists of a dual PLL clock and master clock generator which generates four system clocks and two buffered 27MHz clocks from a 27MHz master clock. Figure 1 shows the block diagram of the PLL1700. The PLL is designed to accept a 27MHz master clock or crystal oscillator. The master clock can be either a crystal

oscillator placed between XT1 (pin 6) and XT2 (pin 5), or an external input to XT1. If an external master clock is used, XT2 must be connected to ground. In both cases, the signal amplitude on XT1 must satisfy the specification described in Figure 3. Therefore, careful  $C_1$  and  $C_2$  determination is required for keeping this specification when using a crystal oscillator.

Figure 2 illustrates possible system clock connection options. Figure 3 illustrates the 27MHz master clock timing requirements.

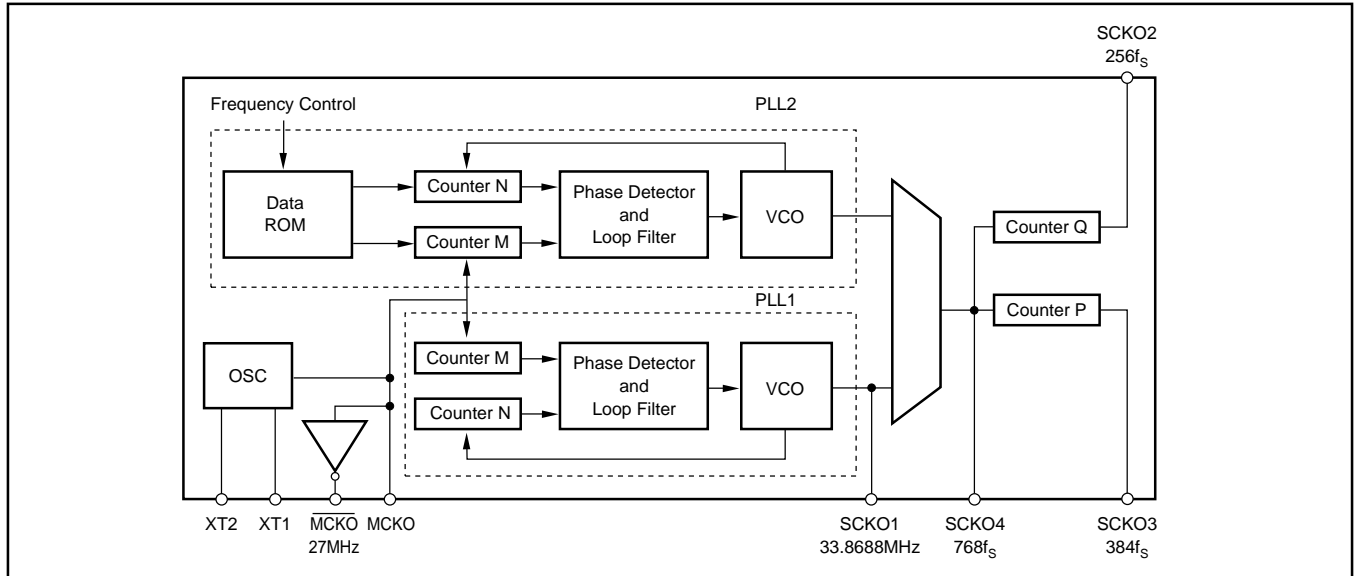


FIGURE 1. Block Diagram of PLL1700.

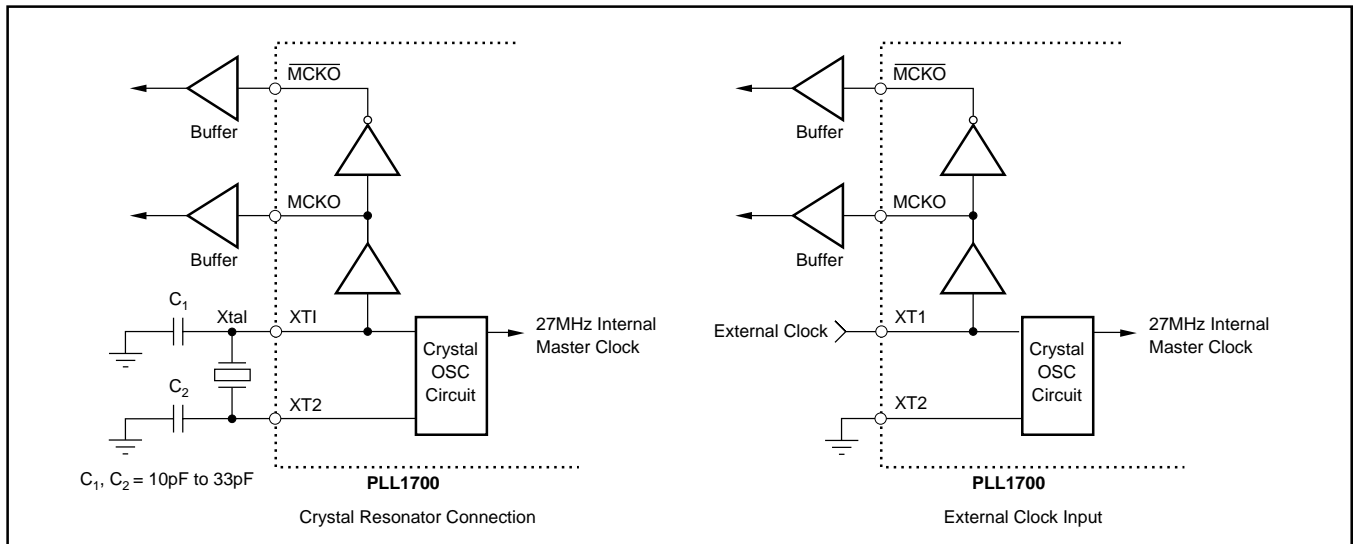


FIGURE 2. Master Clock Generator Connection Diagram.

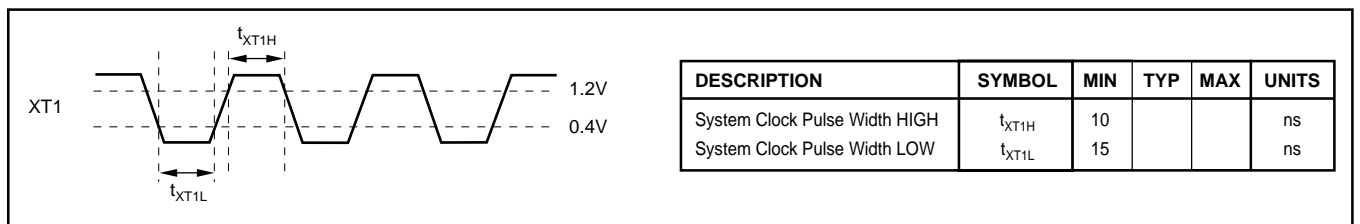


FIGURE 3. External Master Clock Timing Requirement.

The PLL1700 provides a very low jitter, high accuracy clock. SCKO1 is a fixed frequency clock which is 33.8688MHz (768 x 44.1kHz) for a CD-DA DSP. The output frequency of the remaining clocks is determined by the sampling frequency ( $f_s$ ) by software or hardware control. SCKO2 and SCKO3 output  $256f_s$  and  $384f_s$  systems clocks, respectively. SCKO4 output is  $768f_s$  if the sampling frequency is 32kHz, 44.1kHz, 48kHz, or the output is  $384f_s$  if the sampling frequency is 64kHz, 88.2kHz, or 96kHz. Table I shows each sampling frequency. The system clock output frequencies are generated by a 27MHz master clock and programmed sampling frequencies are shown in Table II.

SAMPLING RATE	SAMPLING FREQUENCY (kHz)		
	Standard Sampling Frequencies	32	44.1
Double of Standard Sampling Frequencies	64	88.2	96

TABLE I. Sampling Frequencies.

SAMPLING FREQUENCY (kHz)	SAMPLING RATE	SCKO2 (MHz)	SCKO3 (MHz)	SCKO4 (MHz)
32	Standard	8.192	12.288	24.576
44.1	Standard	11.2896	16.9344	33.8688
48	Standard	12.288	18.4320	36.8640
64	Double	16.384	24.576	24.576
88.2	Double	22.5792	33.8688	33.8688
96	Double	24.576	36.8640	36.8640

TABLE II. Sampling Frequencies and Master Clock Output Frequencies.

Response time from power-on (or applying the clock to XT1) to SCKO settling time is typically 15ms. Delay time from sampling frequency change to SCKO settling time is 20ms maximum. Figure 4 illustrates SCKO transient timing.

External buffers are recommended on all output clocks in order to avoid degrading the jitter performance of the PLL1700.

## RESET

The PLL1700 has an internal power-on reset circuit, as well as an external forced reset (RST, pin 18). Both resets have the same effect on the PLL1700 functions. The mode register default settings for software mode are initialized by reset. Throughout the reset period, all clock outputs are enabled with the default settings. Initialization for the internal power-on reset is done automatically during 1024 master clocks at  $V_{DD} \geq 2.2V$  (1.8V to 2.6V). When using the internal power-on reset, RST should be HIGH. Power-on reset timing is shown in Figure 5. RST (pin 18) accepts an external forced reset by RST = L. Initialization (reset) is done when RST = L and 1024 master clocks after RST = H. External reset timing is shown in Figures 6 and 7.

## FUNCTION CONTROL

The built-in function of the PLL1700 can be controlled in the software mode (serial mode), which uses a three-wire interface by ML (pin 1), MC (pin 20), and MD (pin 19), when MODE (pin 2) = L. They can also be controlled in the hardware mode (parallel mode) which uses SR0 (pin 1), FS1 (pin 20) and FS0 (pin 19), when MODE (pin 2) = H. The selectable functions are shown in Table III.

FUNCTION	HARDWARE MODE (MODE = H)	SOFTWARE MODE (MODE = L)
Sampling Frequency Select (32kHz, 44.1kHz, 48kHz)	Yes	Yes
Sampling Rate Select (Standard/Double)	Yes	Yes
Each Clock Output Enable/Disable	No	Yes

TABLE III. Selectable Functions.

### HARDWARE MODE (MODE = H)

In the hardware mode, the following functions can be selected:

#### Sampling Group Select

The sampling frequency group can be selected by FS1 (pin 20) and FS0 (pin 19). This selection must be made with an interval time greater than 20 $\mu$ s.

FS1 (Pin 20)	FS0 (Pin 19)	SAMPLING GROUP
L	L	48kHz
L	H	44.1kHz
H	L	32kHz
H	H	Reserved

#### Sampling Rate Select

The sampling rate can be selected by SR0 (pin 1).

SR0 (Pin 1)	SAMPLING RATE SELECT
L	Standard
H	Double

### SOFTWARE MODE (MODE = L)

The PLL1700 special function in software mode is shown in Table IV. These functions are controlled using ML, MC, and MD serial control signal.

FUNCTION	DEFAULT
Sampling Frequency Select (32kHz, 44.1kHz, 48kHz)	48kHz Group
Sampling Rate Select (Standard/Double)	Standard
Each Clock Output Enable/Disable	Enable

TABLE IV. Selectable Functions.

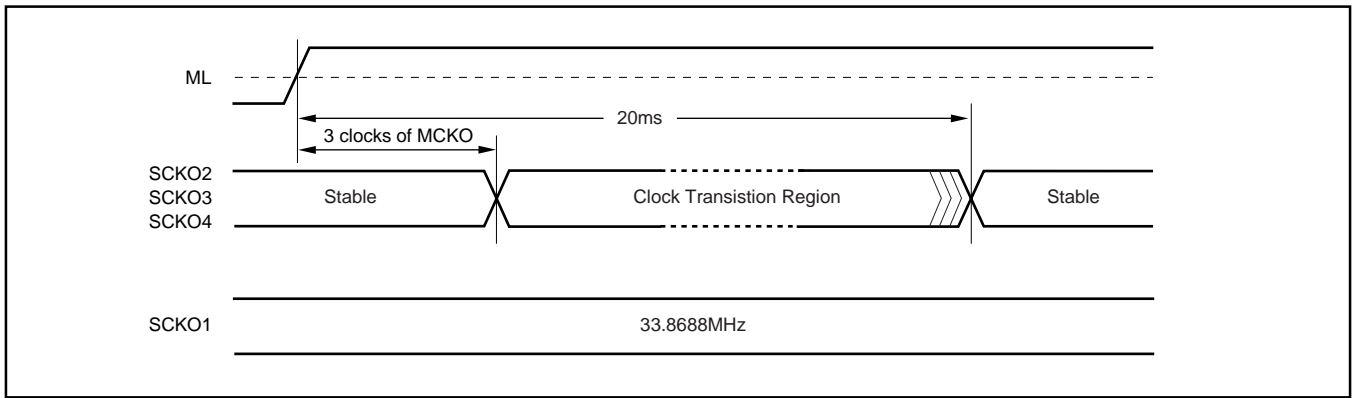


FIGURE 4. System Clock Transient Timing Chart.

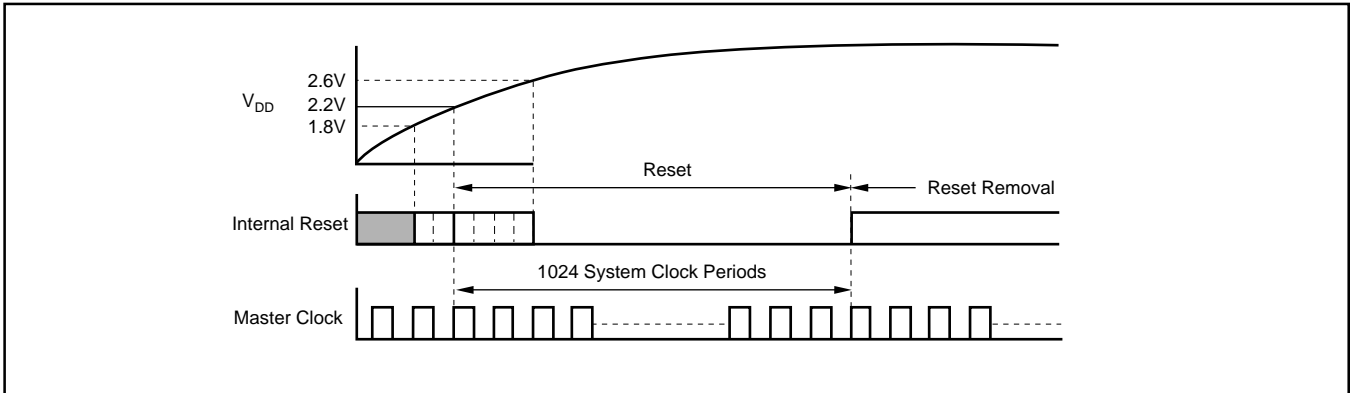


FIGURE 5. Power-On Reset Timing.

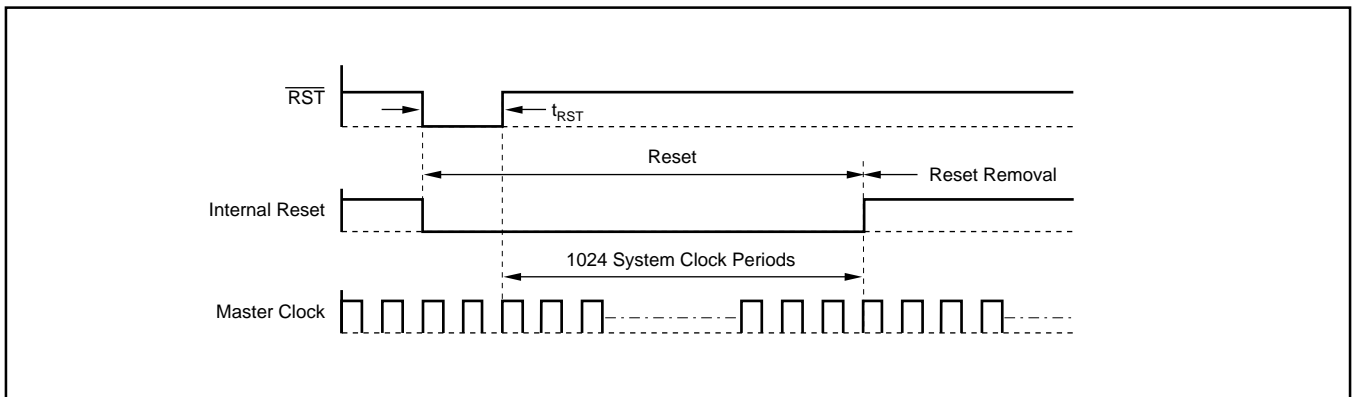


FIGURE 6. External Reset Timing.

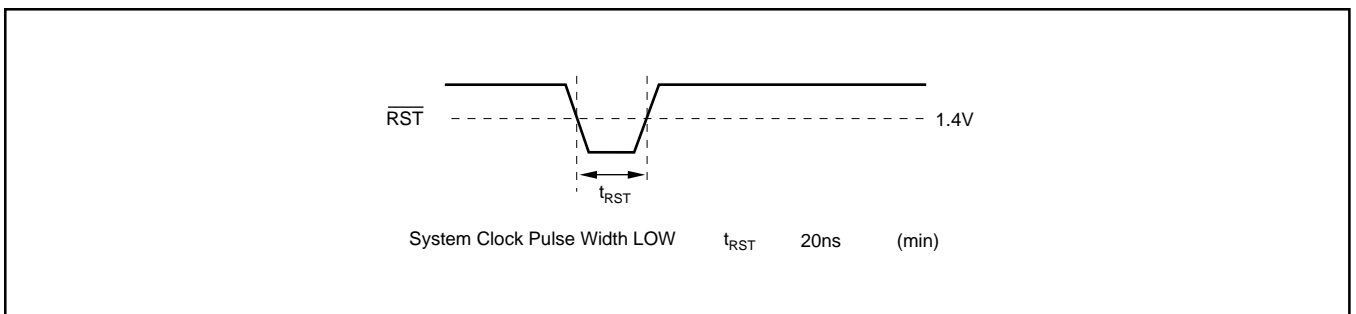


FIGURE 7. Reset Pulse Timing Requirement.

## PROGRAM REGISTER BIT-MAPPING

The built-in functions of the PLL1700 are controlled through a 16-bit program register. This register is loaded using MD. After the 16 data bits are clocked in using the rising edge of MC, ML is used to latch the data into the register. Table V shows the bit-mapping of the registers. The software mode control format and control data input timing is shown in Figures 8 and 9, respectively.

### Mode Register

D15	D14	D13	D12	D11	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	CE6	CE5	CE4	CE3	CE2	CE1	SR1	SR0	FS1	FS0

REGISTER	BIT NAME	DESCRIPTION
MODE	CE6	MCKO Output Enable/Disable
	CE5	MCKO Output Enable/Disable
	CE4	SCKO4 Output Enable/Disable
	CE3	SCKO3 Output Enable/Disable
	CE2	SCKO2 Output Enable/Disable
	CE1	SCKO1 Output Enable/Disable
	SR [1:0]	Sampling Rate Select
	FS [1:0]	Sampling Frequency Select

TABLE V. Register Mapping.

### Mode Register

FS [1:0]: Sampling Frequency Group Select. This selection must be made with an interval time greater than 20µs.

FS1	FS0	SAMPLING FREQUENCY	DEFAULT
0	0	48kHz	0
0	1	44.1kHz	
1	0	32kHz	
1	1	Reserved	

SR [1:0]: Sample Rate Select

SR1	SR0	SAMPLING RATE	DEFAULT
0	0	Standard	0
0	1	Double	
1	0	Reserved	
1	1	Reserved	

CE [1:6]: Clock Output Control

CE1 - CE6	CLOCK OUTPUT CONTROL	DEFAULT
0	Clock Output Disable	
1	Clock Output Enable	0

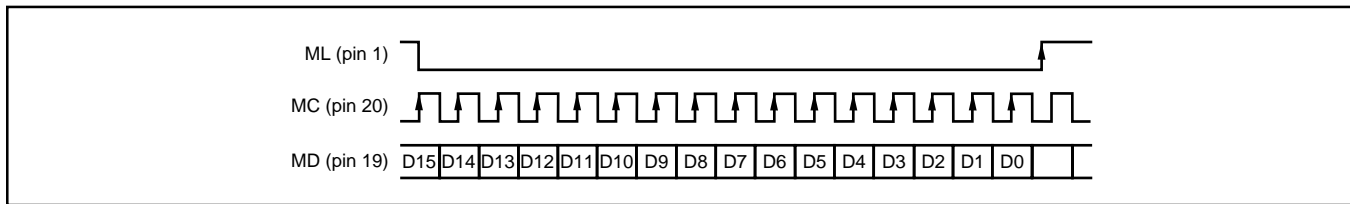


FIGURE 8. Software Mode Control Format.

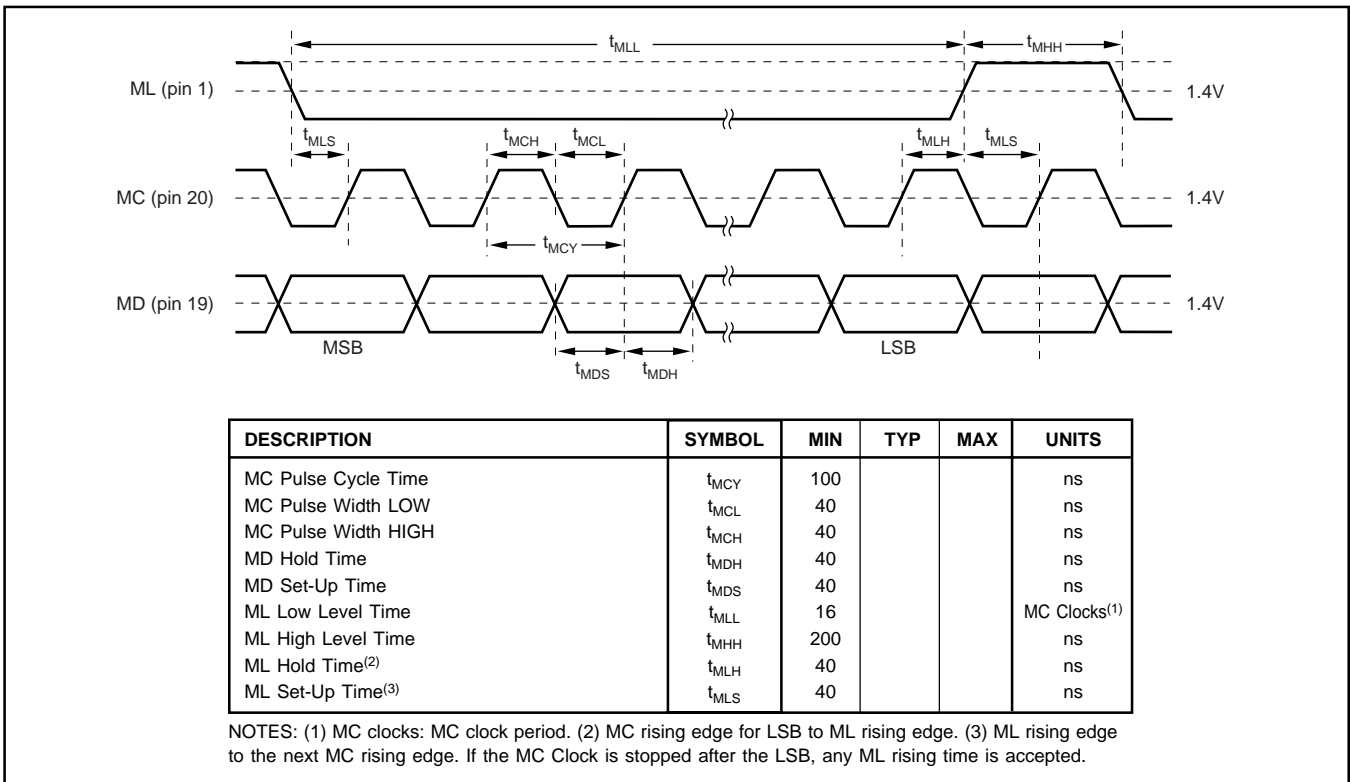


FIGURE 9. Control Data Input Timing.

## CONNECTION DIAGRAM

Figure 10 shows the typical connection circuit for the PLL1700. There are three grounds for digital, analog and PLL power supply. However, the use of one common ground connection is recommended to avoid latch-up problems. Power supplies should be bypassed as close as possible to the device.

## MPEG-2 APPLICATIONS

Typical applications for the PLL1700 are MPEG-2 based systems such as DVD players, DVD add-on cards for multimedia PCs, digital HDTV systems, and set-top boxes. The PLL1700 provides audio system clocks for a CD-DA DSP, DVD DSP, Karaoke DSP, and DAC(s) from a 27MHz video clock.

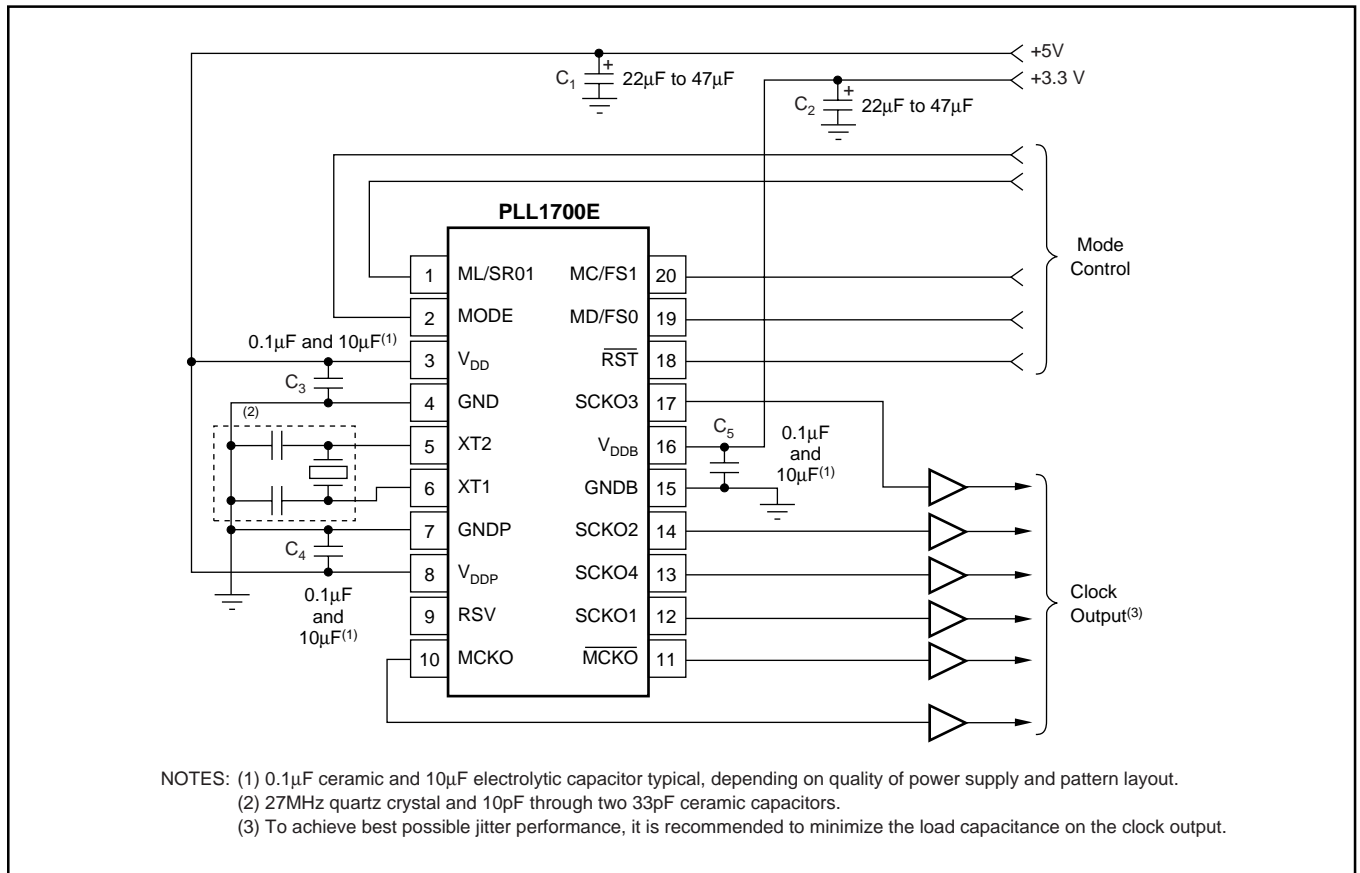


FIGURE 10. Typical Connection Diagram.

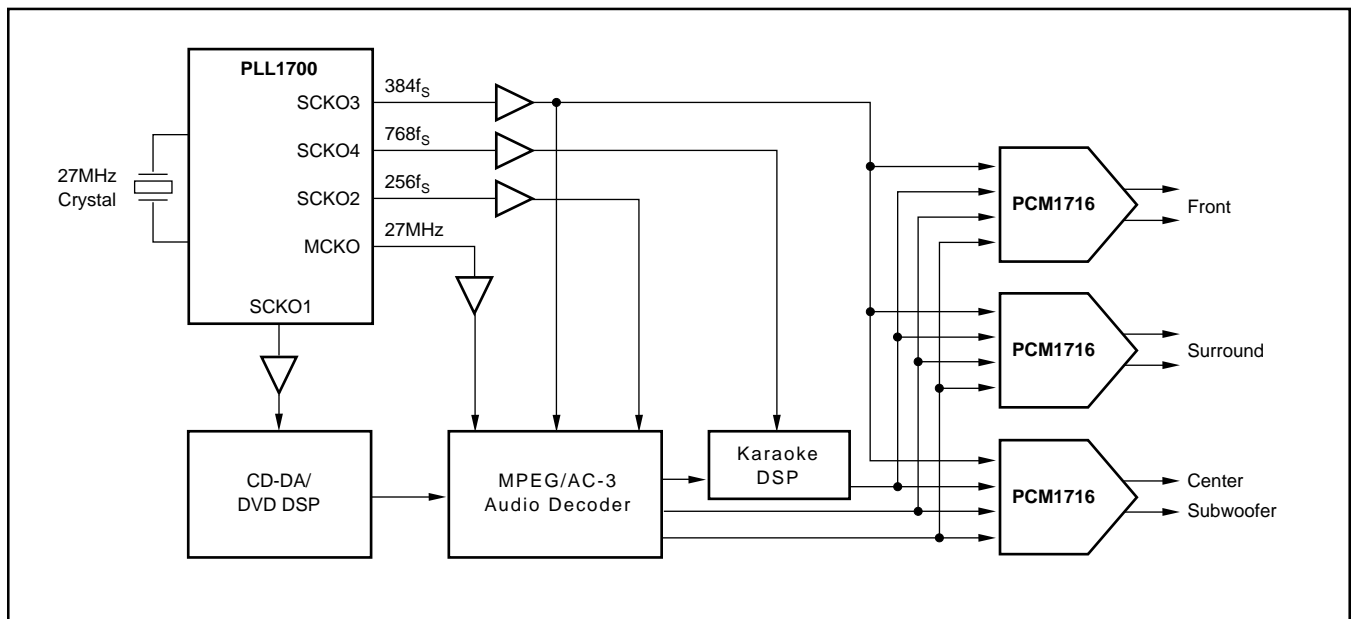


FIGURE 11. PLL1700 System Application Block Diagram.

## Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
5/07	A	—	Entire Document	Updated format to current standard look.
		3	Electrical Characteristics	Added note (1) to $V_{IH}$ and $V_{IL}$ .
				Added two rows to <i>Input Logic Level</i> for $V_{IH}$ and $V_{IL}$ with note (2).
				Added condition to <i>Clock Duty Cycle</i> row stating that $C_1 = C_2 = 15\text{pF}$ .
		5	Master Clock and System Clock Output	Changed "X2 should be connected" to "X2 must be connected."
				Added text regarding signal amplitude.
		5	Figure 5	Changed voltage from 2.0V to 1.2V.
				Changed voltage from 0.8V to 0.4V.
				Changed $t_{XT1H}$ min value from 15 to 10.
		6	Sampling Group Select	Added text regarding interval time.
8	Mode Register	Added text regarding interval time.		
9	Figure 10	Deleted note (1) from $C_1$ and $C_2$ .		
		Changed note text from "tantalum" to "electrolytic" capacitor.		

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
PLL1700E	NRND	SSOP	DB	20	65	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PLL1700E-1/2K	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
PLL1700E-1/2KG4	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
PLL1700E/2K	NRND	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PLL1700E/2KG4	NRND	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PLL1700EG	NRND	SSOP	DB	20	65	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM
PLL1700EG/2K	NRND	SSOP	DB	20	2000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM
PLL1700EG/2KE6	NRND	SSOP	DB	20	2000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM
PLL1700EG4	NRND	SSOP	DB	20	65	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PLL1700EGE6	NRND	SSOP	DB	20	65	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



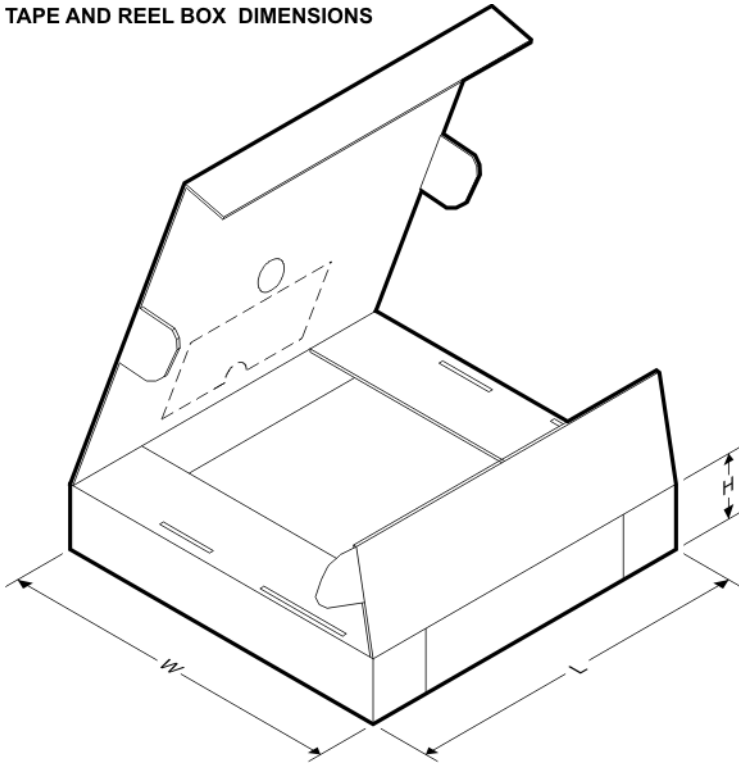
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLL1700E/2K	SSOP	DB	20	2000	330.0	17.4	8.5	7.6	2.4	12.0	16.0	Q1
PLL1700EG/2K	SSOP	DB	20	2000	330.0	17.4	8.5	7.6	2.4	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLL1700E/2K	SSOP	DB	20	2000	336.6	336.6	28.6
PLL1700EG/2K	SSOP	DB	20	2000	336.6	336.6	28.6

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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