



# THE DATASHEET OF PMN40LN,135



## Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of [sales.addresses@www.nxp.com](mailto:sales.addresses@www.nxp.com) or [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com), use [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com) (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

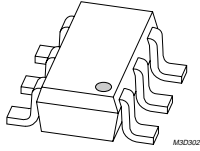
Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia



# PMN40LN

TrenchMOS™ logic level FET

Rev. 01 — 13 November 2002

Product data

## 1. Description

N-channel logic level field-effect power transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PMN40LN in SOT457 (TSOP6).

## 2. Features

- TrenchMOS™ technology
- Logic level compatible
- Surface mount package.

## 3. Applications

- Battery management
- High speed switch
- Low power DC to DC converter.

## 4. Pinning information

Table 1: Pinning - SOT457 (TSOP6), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,5,6	drain (d)	<p>Top view <span style="float: right;">MBK092</span></p> <p><b>SOT457 (TSOP6)</b></p>	<p>MBB076</p>
3	gate (g)		
4	source (s)		



**PHILIPS**

## 5. Quick reference data

**Table 2: Quick reference data**

Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
$I_D$	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 10\text{ V}$	-	5.4	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$	-	1.75	W
$T_j$	junction temperature		-	150	°C
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 2.5\text{ A}; T_j = 25\text{ °C}$	32	38	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 2\text{ A}; T_j = 25\text{ °C}$	40	45	mΩ

## 6. Limiting values

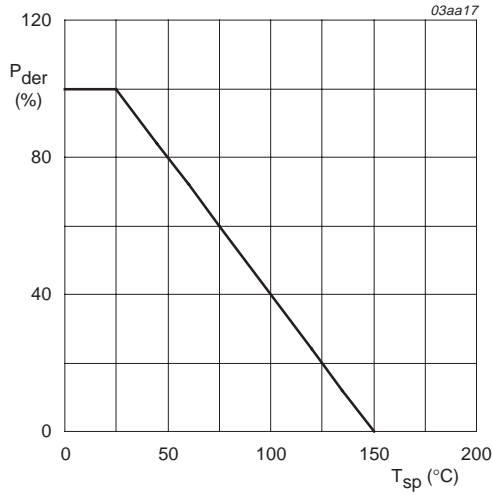
**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage (DC)		-	±15	V
$I_D$	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 10\text{ V};$ <b>Figure 2 and 3</b>	-	5.4	A
		$T_{sp} = 70\text{ °C}; V_{GS} = 10\text{ V};$ <b>Figure 2</b>	-	4	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ <b>Figure 3</b>	-	21.6	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C};$ <b>Figure 1</b>	-	1.75	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C

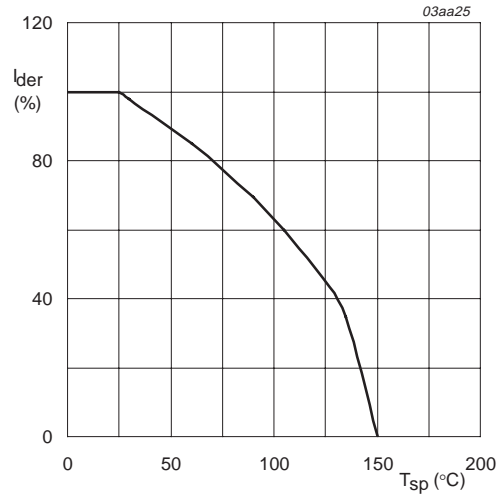
### Source-drain diode

$I_S$	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	1.45	A
$I_{SM}$	peak source (diode forward) current	$T_{sp} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	5.8	A



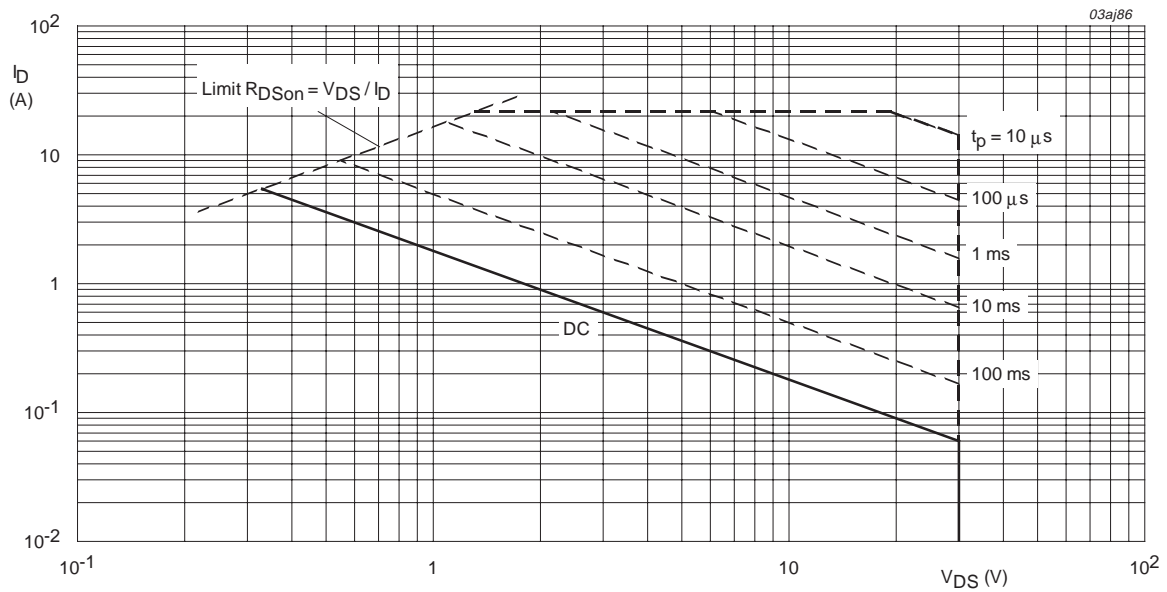
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig. 2. Normalized continuous drain current as a function of solder point temperature.



T<sub>sp</sub> = 25 °C; V<sub>GS</sub> = 10 V; I<sub>DM</sub> is single pulse.

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad board; Figure 4	-	-	70	K/W

### 7.1 Transient thermal impedance

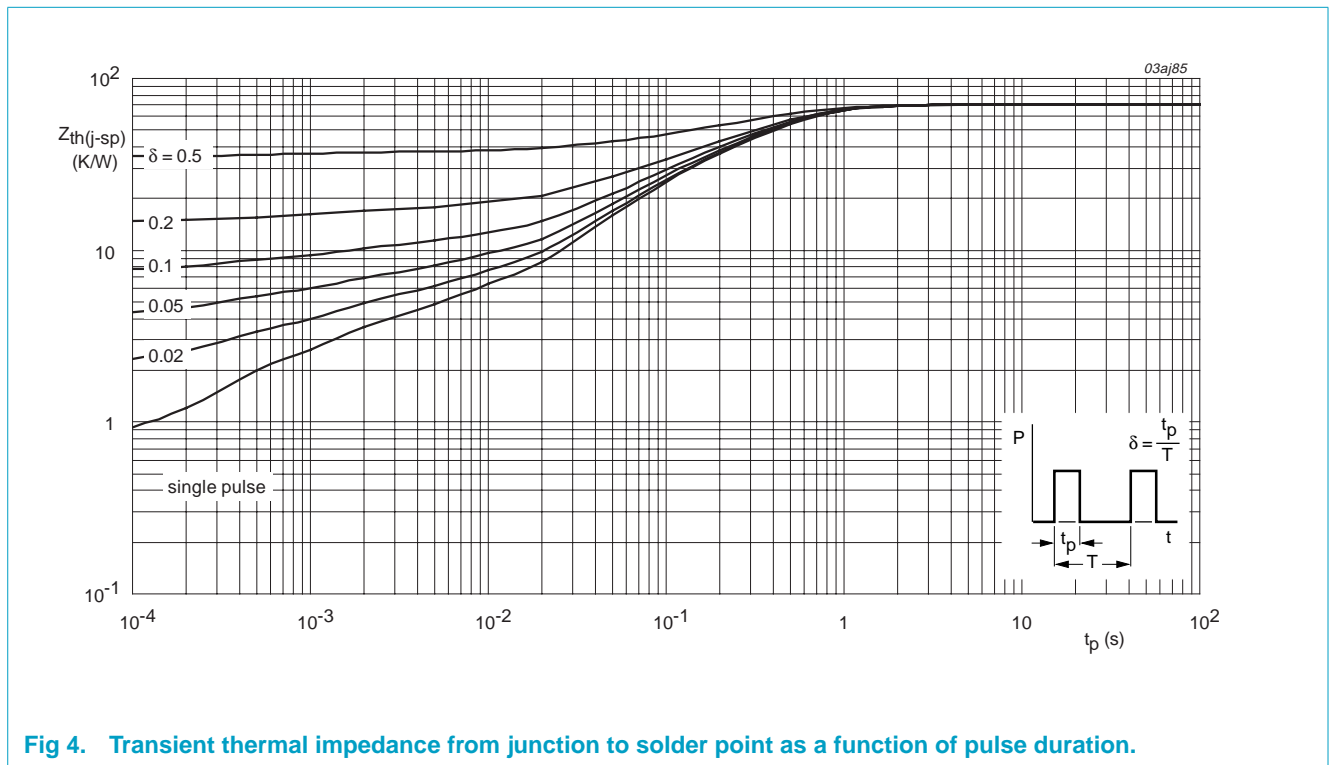
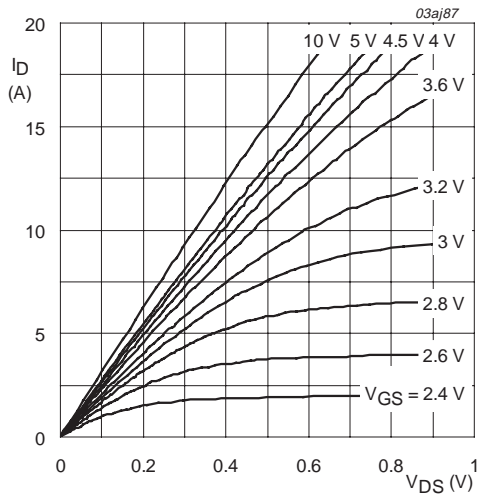


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

## 8. Characteristics

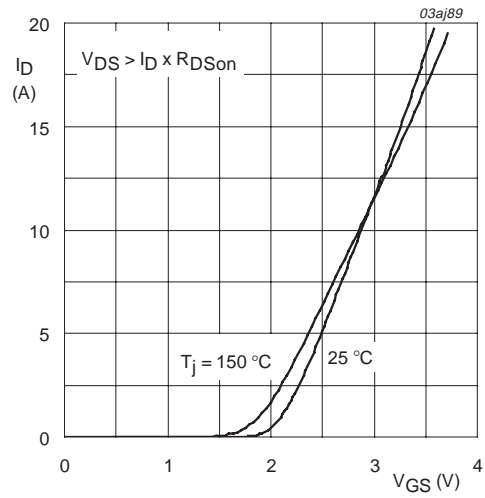
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	30	-	-	V
		T <sub>j</sub> = -55 °C	27	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; <b>Figure 9</b>				
		T <sub>j</sub> = 25 °C	1	1.5	2	V
		T <sub>j</sub> = 150 °C	0.6	-	-	V
		T <sub>j</sub> = -55 °C	-	-	2.2	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 24 V; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	-	0.05	1	μA
		T <sub>j</sub> = 150 °C	-	-	500	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±15 V; V <sub>DS</sub> = 0 V	-	10	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 2 A; <b>Figure 7 and 8</b>				
		T <sub>j</sub> = 25 °C	-	40	45	mΩ
		T <sub>j</sub> = 150 °C	-	64	72	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 2.5 A; <b>Figure 7</b>				
		T <sub>j</sub> = 25 °C	-	32	38	mΩ
<b>Dynamic characteristics</b>						
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 5 A; V <sub>DD</sub> = 15 V; V <sub>GS</sub> = 10 V; <b>Figure 13</b>	-	13.8	-	nC
Q <sub>gs</sub>	gate-source charge		-	1.8	-	nC
Q <sub>gd</sub>	gate-drain (Miller) charge		-	2.4	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; <b>Figure 11</b>	-	555	-	pF
C <sub>oss</sub>	output capacitance		-	105	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	70	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 15 V; R <sub>L</sub> = 12 Ω;	-	5	-	ns
t <sub>r</sub>	rise time	V <sub>GS</sub> = 10 V; R <sub>G</sub> = 6 Ω	-	7	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	19	-	ns
t <sub>f</sub>	fall time		-	8	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 1.7 A; V <sub>GS</sub> = 0 V; <b>Figure 12</b>	-	0.8	1.2	V



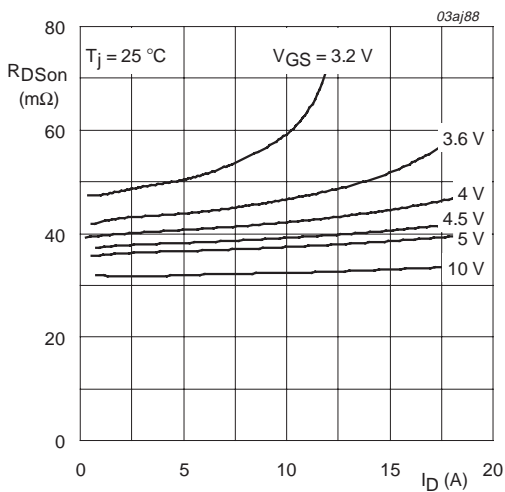
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



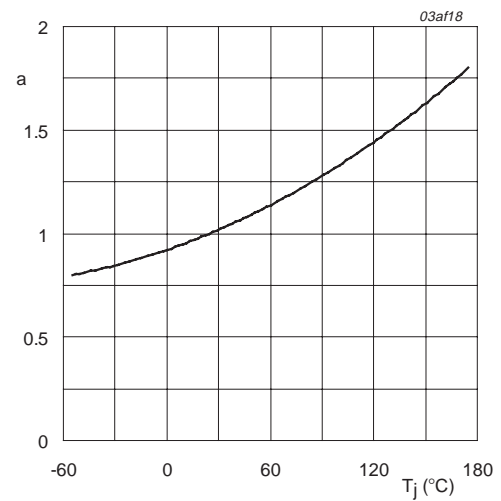
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



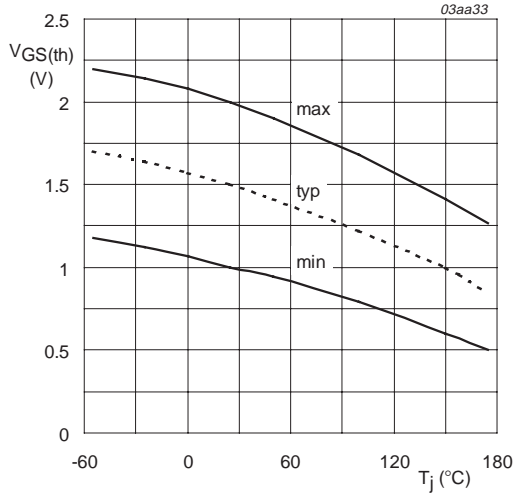
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



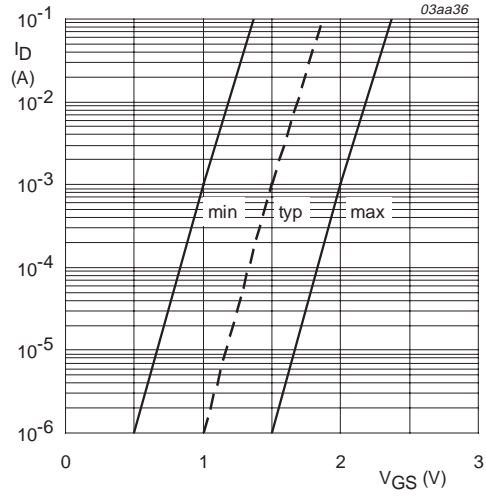
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



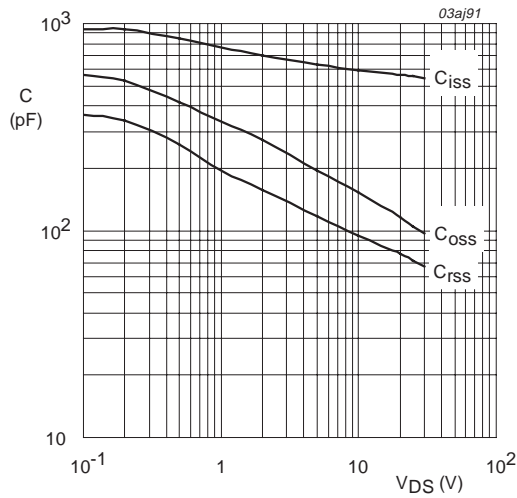
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



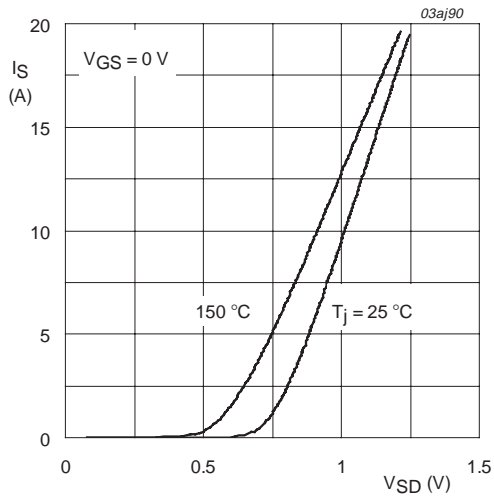
$T_J = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



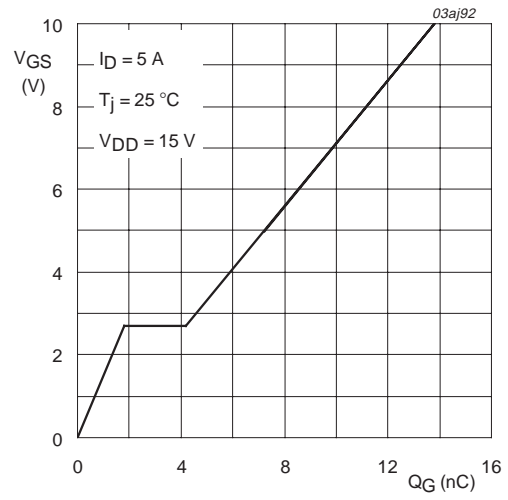
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25$  °C and  $150$  °C;  $V_{GS} = 0$  V

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 5$  A;  $V_{DD} = 15$  V

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**

9. Package outline

Plastic surface mounted package; 6 leads

SOT457

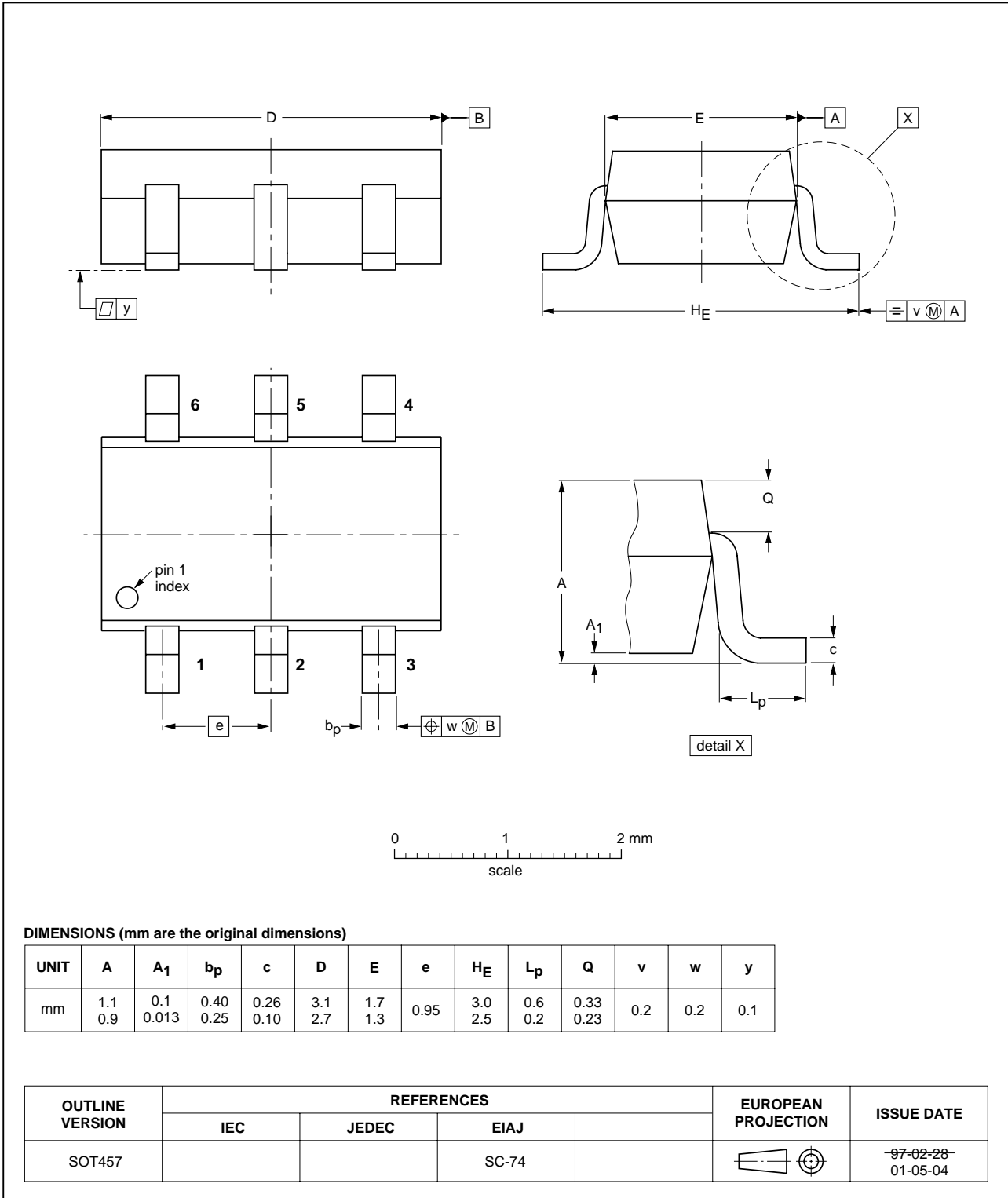


Fig 14. SOT457 (TSOP6).

## 10. Revision history

---

Table 6: Revision history

Rev	Date	CPCN	Description
01	20021113	-	Product data.

---

## 11. Trademarks

---

TrenchMOS — is a trademark of Koninklijke Philips Electronics N.V.

## 12. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 13. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## 14. Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

## Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com).

Fax: +31 40 27 24825

## Contents

1	Description	1
2	Features	1
3	Applications	1
4	Pinning information	1
5	Quick reference data	2
6	Limiting values	2
7	Thermal characteristics	4
7.1	Transient thermal impedance	4
8	Characteristics	5
9	Package outline	9
10	Revision history	10
11	Trademarks	10
12	Data sheet status	11
13	Definitions	11
14	Disclaimers	11

© Koninklijke Philips Electronics N.V. 2002.  
Printed in The Netherlands

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Date of release: 13 November 2002

Document order number: 9397 750 10192





# PHILIPS

*Let's make things better.*

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View PMN40LN,135 on WIN SOURCE](#)
-  [NXP / Nexperia Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management