THE DATASHEET OF

PTH12060WAH

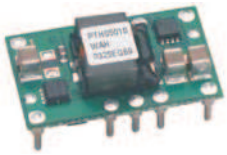
10-A, 12-V INPUT NON-ISOLATED WIDE-OUTPUT ADJUST POWER MODULE

FEATURES

- **Up to 10-A Output Current**
- **12-V Input Voltage**
- **Wide-Output Voltage Adjust (1.2 V to 5.5 V/(0.8 V to 1.8 V)**
- **Efficiencies up to 95%**
- **225 W/in^3 Power Density**
- **Output Voltage Sense**
- **Margin Up/Down Controls**
- **Undervoltage Lockout**
- **Auto-Track™ Sequencing**
- **Pre-Bias Start-up Capability using On/Off Inhibit**
- **Output Overcurrent Protection (Non-latching, Auto-Reset)**
- **Operating Temperature: –40°C to 85°C**
- **Safety Agency Approvals: UL/IEC/CSA C22.2 60950-1**
- **Point-of-Load Alliance (POLA™) Compatible**

APPLICATIONS

- **Complex Digital Systems**



Nominal Size = 1 in x 0.62 in (25,4 mm x 15,75 mm)

DESCRIPTION

The PTH12060 series is a non-isolated power module, and part of a new class of complete dc/dc converters from Texas Instruments. These modules are small in size, and are an alternative for applications requiring up to 10 A of load current.

The small footprint, (1 inch × 0.62 inch) and industry leading features makes this module suitable for space conscious digital systems that incorporate multiple processors.

This series of modules operate from a 12-V input bus voltage to provide step-down power conversion to a wide range of output voltages. The output voltage of the W-suffix device may be set to any voltage over the adjust range, 1.2 V to 5.5 V. The L-suffix device has an adjustment range of 0.8 V to 1.8 V. The output voltage is set within the adjust range using a single external resistor.

This product includes Auto-Track™ Sequencing. Auto-Track simplifies the task of supply voltage sequencing in a power system, by enabling modules to track each other, or any other external voltage, during power up and power down.

Other features include an on/off inhibit and margin up/down controls. An output voltage sense ensures tight load regulation. Non-latching overcurrent trip protects against load faults.

For start-up into a non-prebiased output, review page 14 in the *Application Information* section.

For start-up into a prebiased output, review page 18 in the *Application Information* section.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Auto-Track, POLA, TMS320 are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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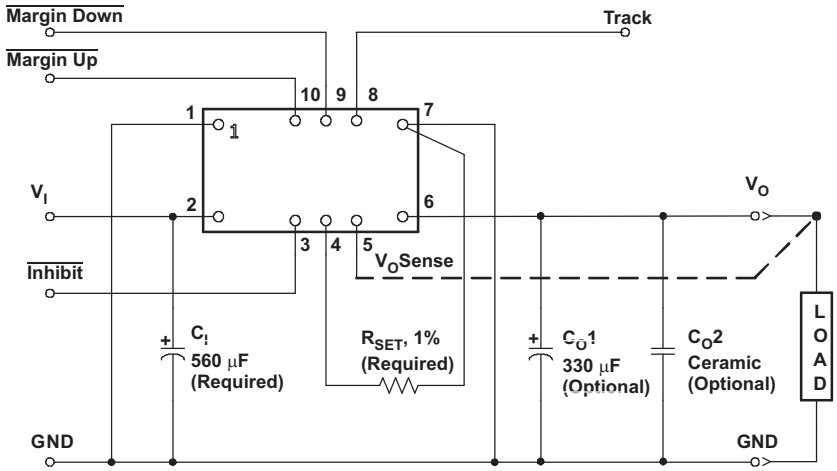
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

STANDARD APPLICATION



A. R_{SET} = Required to set the output voltage to a value higher than the minimum value. See the Application Information section for values.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

voltages are with respect to GND

				UNIT
V_I	Input voltage	Track		–0.3 V to V_I +0.3 V
T_A	Operating temperature range	Over V_I range		–40°C to 85°C (1)
T_{wave}	Wave solder temperature	Surface temperature of module body or pins **(5 seconds)**	PTH12060WAH	260°C (2)
			PTH12060WAD	
T_{reflow}	Solder reflow temperature	Surface temperature of module body or pins	PTH12060WAS	235°C (2)
			PTH12060WAZ	260°C (2)
T_{stg}	Storage temperature			–55°C to 125°C (3)
	Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 msec, Sine, mounted		500 G
	Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz		20 G
	Weight			5 grams
	Flammability	Meets UL 94V-O		

(1) For operation below 0°C, the external capacitors must have stable characteristics. Use either a low ESR tantalum, Os-Con, or ceramic capacitor.
(2) During soldering of package version, do not elevate peak temperature of the module, pins or internal components above the stated maximum.
(3) The shipping tray or tape & reel cannot be used to bake parts at temperatures higher than 65°C.

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ELECTRICAL CHARACTERISTICS

T_A = 25C; V_I = 12 V; V_O = 3.3 V; C_I = 560 µF, C_O = 0 µF, and I_O = $I_O$max (unless otherwise stated)

PARAMETER		TEST CONDITIONS		PTH12060W			UNIT
				MIN	TYP	MAX	
I_O	Output current	Over ΔV_{adj} range	T_A = 60°C, 200 LFM airflow	0		10(1)	A
			T_A = 25°C, natural convection			10(1)	A
V_I	Input voltage range	Over I_O range		10.8		13.2	V
$V_{O\ tol}$	Set-point voltage tolerance					±2(2)	%V_O
ΔReg_{temp}	Temperature variation	–40°C < T_A < 85°C			±0.5		%V_O
ΔReg_{line}	Line regulation	Over V_{in} range			±10		mV
ΔReg_{load}	Load regulation	Over I_o range			±12		mV
ΔReg_{tot}	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C				±3	%V_O
ΔV_{adj}	Output voltage adjust range	Over V_{in} range		1.2		5.5	V
η	Efficiency	I_O = 8 A	R_{SET} = 280 Ω, V_O = 5.0 V		94%		
			R_{SET} = 2.0 kΩ, V_O = 3.3 V		92%		
			R_{SET} = 4.32 kΩ, V_O = 2.5 V		90%		
			R_{SET} = 11.5 kΩ, V_O = 1.8 V		87%		
			R_{SET} = 24.3 kΩ, V_O = 1.5 V		85%		
			R_{SET} = open circuit, V_O = 1.2 V		83%		
	V_O ripple (peak-to-peak)	20-MHz bandwidth, with C_O2 = 10 µF ceramic	V_O ≤ 2.5 V		25(3)		mV_{PP}
			V_O > 2.5 V		1(3)		%V_O
I_O trip	Overcurrent threshold	Reset, followed by auto-recovery			20		A
t_{tr}	Transient response	1 A/µs load step, 50 to 100% $I_o$max, C_O1 = 330 µF	Recovery time		70		µS
ΔV_{tr}			V_o over/undershoot		100		mV
$V_O$adj	Margin up/down adjust				±5%		
I_{IL}margin	Margin input current (pins 9/10)	Pin to GND			–8 (4)		µA
I_{IL}track	Track input current (pin 8)	Pin to GND				–0.11(5)	mA
dV_{track}/dt	Track slew rate capability	C_O ≤ C_O (max)				1	V/ms
UVLO	Undervoltage lockout	V_I increasing			9.5	10.4	V
		V_I decreasing		8.8	9		
V_{IH}	Inhibit Control (pin 3)	Input high voltage, Referenced to GND				Open(5)	V
V_{IL}		Input low voltage, Referenced to GND		–0.2		0.5	
I_{IL}		Input low current, Pin 3 to GND			0.24		mA
I_I	Input standby current	Inhibit (pin 3) to GND, Track (pin 8) open			10		mA
f_s	Switching frequency	Over V_I and I_O ranges		300	350	400	kHz
C_I	External input capacitance			560(6)			µF
C_O	External output capacitance	Capacitance value	Nonceramic	0	330(7)	5500(8)	µF
			Ceramic	0		300	
		Equivalent series resistance (nonceramic)		4(9)			mΩ
MTBF	Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign		6.4			10^6 Hr

(1) See SOA curves or consult factory for appropriate derating.
(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.
(3) The peak-to-peak output ripple voltage is measured with an external 10-µF ceramic capacitor. See the standard application schematic.
(4) A small, low leakage (<100 nA) MOSFET is recommended to control this pin. The open-circuit voltage is less than 1 Vdc.
(5) This control pin has an internal pull-up to the input voltage V_I. If it is left open-circuit, the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET or open-drain/collector voltage supervisor IC is recommended for control. Do not place an external pull-up on this pin. For further information, see the related application information section.
(6) A 560 µF input capacitor are required for proper operation. The electrolytic capacitor must be rated for a minimum of 1050 mA rms of ripple current.
(7) An external output capacitor is not required for basic operation. Adding 330 µF of distributed capacitance at the load improves the transient response.
(8) This is the calculated maximum. The minimum ESR limitation oftens result in a lower value. When controlling the Track pin using a voltage supervisor, C_O(max) is reduced to 2200 µF. See the application notes for further guidance.
(9) This is the typical ESR for all the electrolytic (nonceramic) output capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.

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ELECTRICAL CHARACTERISTICS

T_A = 25C; V_I = 12 V; V_O = 1.8 V; C_I = 560 µF, C_O = 0 µF, and I_O = $I_O$max (unless otherwise stated)

PARAMETER		TEST CONDITIONS		PTH12060L			UNIT
				MIN	TYP	MAX	
I_O	Output current	Over ΔV_{adj} range	85°C, 200 LFM airflow	0		10(1)	A
			25°C, natural convention	0		10(1)	
V_I	Input voltage range	Over I_O range		10.8		13.2	V
$V_{O\ tol}$	Set-point voltage tolerance					±2(2)	%V_O
ΔReg_{temp}	Temperature variation	–40°C < T_A < 85°C			±0.5		%V_O
ΔReg_{line}	Line regulation	Over V_I range			±10		mV
ΔReg_{load}	Load regulation	Over I_O range			±12		mV
ΔReg_{tot}	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C				±3	%V_O
ΔV_{adj}	Output voltage adjust range	Over V_I range		0.8		1.8	V
η	Efficiency	I_O = 8 A	R_{SET} = 130 Ω, V_O = 1.8 V		88%		
			R_{SET} = 3.57 kΩ, V_O = 1.5 V		87%		
			R_{SET} = 12.1 kΩ, V_O = 1.2 V		84%		
			R_{SET} = 32.4 kΩ, V_O = 1 V		82%		
			R_{SET} = open circuit, V_O = 0.8 V		81%		
	V_O ripple (peak-to-peak)	20-MHz bandwidth, with C_O2 = 10 µF ceramic	V_O > 1 V		20(3)		mV_{PP}
			V_O ≤ 1 V		30(3)		
I_O trip	Overcurrent threshold	Reset, followed by auto-recovery			20		A
t_{tr}	Transient response	1 A/µs load step, 50 to 100% $I_O$max, C_O1 = 330 µF	Recovery time		70		µS
ΔV_{tr}			V_O over/undershoot		100		mV
$V_O$adj	Margin up/dow adjust				±5%		
I_{IL}margin	Margin input current (pins 9/10)	Pin to GND			–8(4)		µA
I_{IL}track	Track input current (pin 8)	Pin to GND				–0.11(5)	mA
dV_{track}/dt	Track slew rate capability	C_O ≤ C_O (max)				1	V/ms
UVLO	Under-voltage lockout	V_I increasing			9.5	10.4	V
		V_I decreasing		8.8	9		
V_{IH}	Inhibit Control (pin 3)	Input high voltage, Referenced to GND				Open(5)	V
V_{IL}		Input low voltage, Referenced to GND		–0.2		0.5	
I_{IL}		Input low current, Pin 3 to GND			0.24		mA
I_I	Input standby current	Inhibit (pin 3) to GND, Track (pin 8) open			10		mA
f_s	Switching frequency	Over V_I and I_O ranges		200	250	300	kHz
C_I	External input capacitance			560(6)			µF
C_O	External output capacitance	Capacitance value	Nonceramic	0	330(7)	5500(8)	µF
			Ceramic	0		300	
		Equivalent series resistance (nonceramic)		4(9)			mΩ
MTBF	Reliability	Per Bellcore TR-332 50% stress, T_A = 40°C, ground benign		6.4			10^6 Hr

(1) See SOA curves or consult factory for appropriate derating.
(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.
(3) The peak-to-peak output ripple voltage is measured with an external 10-µF ceramic capacitor. See the standard application schematic.
(4) A small, low-leakage (<100 nA) MOSFET is recommended to control this pin. The open-circuit voltage is less than 1 Vdc.
(5) This control pin has an internal pull-up to the input voltage V_I. If it is left open-circuit, the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET or open-drain/collector voltage supervisor IC is recommended for control. Do not place an external pull-up on this pin. For further information, see the application information section.
(6) A 560-µF input capacitor are required for proper operation. The electrolytic capacitor must be rated for a minimum of 1050 mA rms of ripple current.
(7) An external output capacitor is not required for basic operation. Adding 330 µF of distributed capacitance at the load improves the transient response.
(8) This is the calculated maximum. The minimum ESR limitation oftens result in a lower value. When controlling the Track pin using a voltage supervisor, C_O(max) is reduced to 2200 µF. See the application notes for further guidance.
(9) This is the typical ESR for all the electrolytic (nonceramic) output capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.

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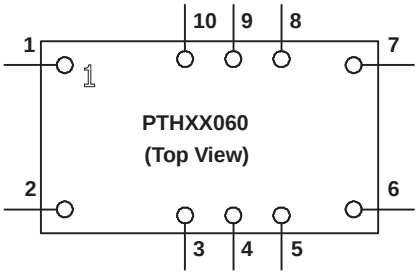
DEVICE INFORMATION

Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
V_I	2	The positive input voltage power node to the module, which is referenced to common GND.
V_O	6	The regulated positive power output with respect to the GND node.
GND	1, 7	This is the common ground connection for the V_I and V_O power connections. It is also the 0 Vdc reference for the control inputs.
Inhibit	3	The Inhibit pin is an open-collector/drain negative logic input that is referenced to GND. Applying a low level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever a valid input source is applied. Do not place an external pull-up on this pin. *For power-up into a non-prebiased output, it is recommended that AutoTrack be utilized for On/Off control. See the Application Information for additional details.*
V_O Adjust	4	A 1% resistor must be directly connected between this pin and GND (pin 1) to set the output voltage of the module to a value higher than its lowest value. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range is 1.2 V to 5.5 V for W-suffix devices, and 0.8 V to 1.8 V for L-suffix devices. The resistor value required for a given output voltage may be calculated using a formula. If left open circuit, the output voltage defaults to its lowest value. For further information on output voltage adjustment, see the application information section. Table 2 gives the preferred resistor values for a number of standard output voltages.
V_O Sense	5	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy, V_O Sense should be connected to V_O. It can also be left disconnected.
Track	8	This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from zero volts, up to the nominal set-point voltage. Within this range, the output follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to V_I. *Note: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, see the application information section.*
Margin Down	9	When this input is asserted to GND, the output voltage is decreased by 5% from the nominal. The input requires an open-collector (open-drain) interface. It is not TTL compatible. A lower percent change can be accommodated with a series resistor. For further information, see the application information section.
Margin Up	10	When this input is asserted to GND, the output voltage is increased by 5%. The input requires an open-collector (open-drain) interface. It is not TTL compatible. The percent change can be reduced with a series resistor. For further information, see the application information section.



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PTH12060W TYPICAL CHARACTERISTICS (V_I = 12 V)(1)(2)(3)

EFFICIENCY vs OUTPUT CURRENT

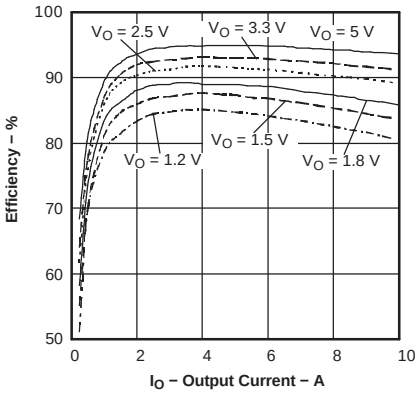

Figure 1.

OUTPUT RIPPLE vs OUTPUT CURRENT (see Note 3 below)

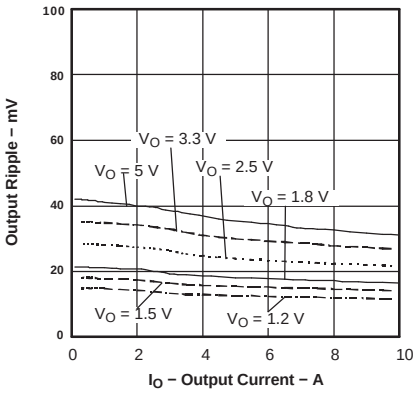

Figure 2.

POWER DISSIPATION vs OUTPUT CURRENT

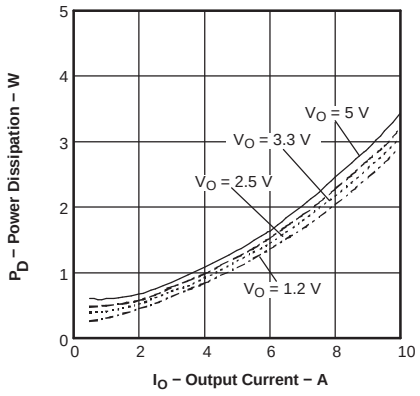

Figure 3.

TEMPERATURE DERATING vs OUTPUT CURRENT

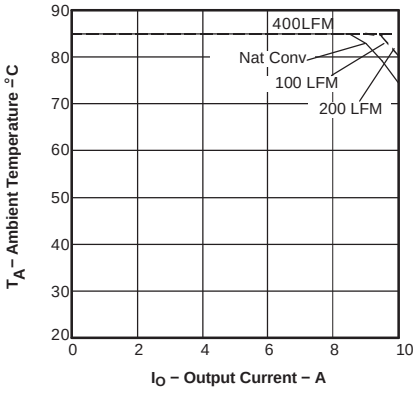

Figure 4.

(1) Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) SOA graphs represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in., double-sided PCB with 1 oz copper. For surface mount products (AS and AZ suffix), multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 4.

(3) The peak-to-peak output ripple voltage is measure with an external 10 µF ceramic capacitor on the output.

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PTH12060L TYPICAL CHARACTERISTICS (V_I = 12 V)(1)(2)(3)

EFFICIENCY VS OUTPUT CURRENT

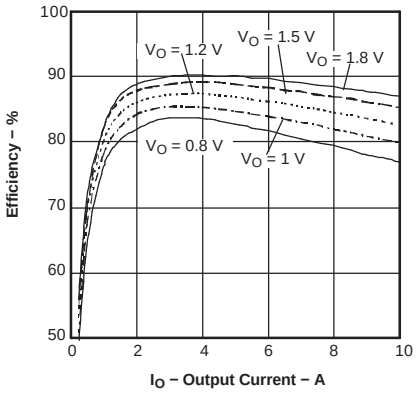

Figure 5.

OUTPUT RIPPLE VS OUTPUT CURRENT (see Note 3 below)

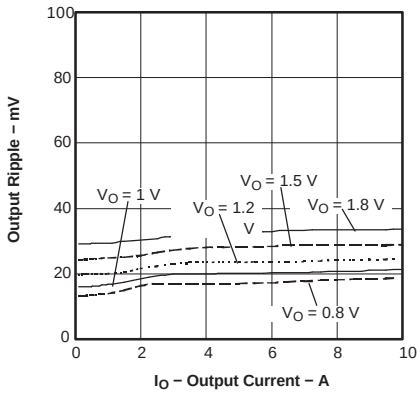

Figure 6.

POWER DISSIPATION VS OUTPUT CURRENT

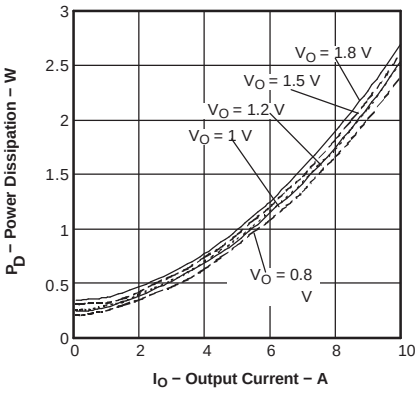

Figure 7.

TEMPERATURE DERATING VS OUTPUT CURRENT

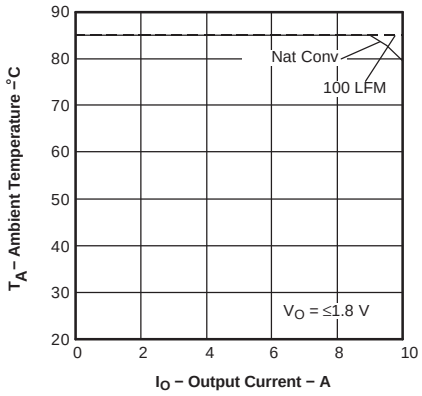

Figure 8.

(1) Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter. Applies to Figure 5, Figure 6, and Figure 7.

(2) SOA graphs represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in., double-sided PCB with 1 oz copper. For surface mount products (AS and AZ suffix), multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 8.

(3) The peak-to-peak output ripple voltage is measure with an external 10 µF ceramic capacitor on the output.

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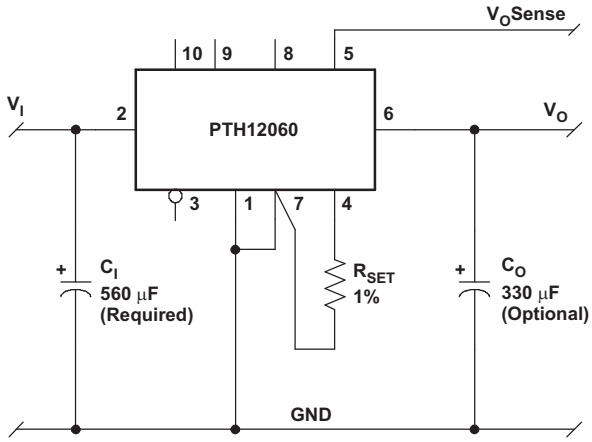
APPLICATION INFORMATION

ADJUSTING THE OUTPUT VOLTAGE

The V_OAdjust control (pin 4) sets the output voltage of the PTH12060W/L. The adjustment range is from 1.2V to 5.5V for the W-suffix modules, and 0.8V to 1.8V for L-suffix modules. The adjustment method requires the addition of a single external resistor, R_{SET}, that must be connected directly between the V_OAdjust and GND pins(1). Table 1 gives the standard value of the external resistor for a number of standard voltages, along with the actual output voltage that the resistance value provides. For other output voltages the value of the required resistor can either be calculated using Equation 1, or simply selected from the range of values given in Table 3. Figure 9 shows the placement of the required resistor.

Table 1. Standard Values of R_{SET} for Standard Output Voltages

	PTH12060W		PTH12060L	
V_O(V) (Required)	R_{SET} (kΩ)	V_O(V) (Actual)	R_{SET}(kΩ)	V_O(V) (Actual)
5	0.280	5.009	N/A	N/A
3.3	2	3.294	N/A	N/A
2.5	4.32	2.503	N/A	N/A
2	8.06	2.01	N/A	N/A
1.8	11.5	1.801	0.130	1.8
1.5	24.3	1.506	3.57	1.499
1.2	Open	1.2	12.1	1.201
1.1	N/A	N/A	18.7	1.101
1.0	N/A	N/A	32.4	0.999
0.9	N/A	N/A	71.5	0.901
0.8	N/A	N/A	Open	0.8



(1) **R_{SET}:** Use a 0.05-W rated resistor with a 1% tolerance and temperature stability of 100 ppm/°C or better. Place the resistor directly between pins 4 and 7, as close to the regulator as possible, using dedicated PCB traces.

(2) Never connect capacitors from V_O Adjust to either GND or V_O. Any capacitance added to the V_O Adjust pin affects the stability of the regulator.

Figure 9. V_O Adjust Resistor Placement

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Use Equation 1 to calculate the adjust resistor value. See Table 2 for parameters, R_S and V_{min}.

Equation 1. Output Voltage Adjust

$$R_{SET} = 10\ k\Omega \times \frac{0.8\ V}{V_O - V_{min}} - R_S\ k\Omega \quad (1)$$

Table 2. Adjust Equation Parameters

Parameter	PTH12060W	PTH12060L
V_{min} (V)	1.2	0.8
V_{max} (V)	5.5	1.8
R_S (kΩ)	1.82	7.87

Table 3. Output Voltage Set-Point Resistor Values

PTH12060W				PTH12060L	
V_O (V)	R_{SET} (kΩ)	V_O(V)	R_{SET} (kΩ)	V_O(V)	R_{SET} (kΩ)
1.20	Open	2.70	3.51	0.80	Open
1.225	318	2.75	3.34	0.825	312
1.25	158	2.80	3.18	0.85	152
1.275	105	2.85	3.03	0.875	98.8
1.30	78.2	2.90	2.89	0.90	72.1
1.325	62.2	2.95	2.75	0.925	56.1
1.35	51.5	3.0	2.62	0.95	45.5
1.375	43.9	3.05	2.5	0.975	37.8
1.40	38.2	3.10	2.39	1.0	32.1
1.425	33.7	3.15	2.28	1.025	27.7
1.45	30.2	3.20	2.18	1.05	24.1
1.475	27.3	3.25	2.08	1.075	21.2
1.50	24.8	3.30	1.99	1.10	18.8
1.55	21	3.35	1.9	1.125	16.7
1.60	18.2	3.40	1.82	1.15	15
1.65	16	3.50	1.66	1.175	13.5
1.70	14.2	3.60	1.51	1.20	12.1
1.75	12.7	3.70	1.38	1.225	11
1.80	11.5	3.80	1.26	1.25	9.91
1.85	10.5	3.90	1.14	1.275	8.97
1.90	9.61	4.0	1.04	1.30	8.13
1.95	8.85	4.10	0.939	1.325	7.37
2.0	8.18	4.20	0.847	1.35	6.68
2.05	7.59	4.30	0.761	1.375	6.04
2.10	7.07	4.40	0.680	1.40	5.46
2.15	6.6	4.50	0.604	1.425	4.93
2.20	6.18	4.60	0.533	1.45	4.44
2.25	5.8	4.70	0.466	1.475	3.98
2.30	5.45	4.80	0.402	1.50	3.56
2.35	5.14	4.90	0.342	1.55	2.8
2.40	4.85	5.0	0.285	1.60	2.13
2.45	4.58	5.10	0.231	1.65	1.54

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Table 3. Output Voltage Set-Point Resistor Values (continued)

PTH12060W				PTH12060L	
V_O (V)	R_{SET} (kΩ)	V_O(V)	R_{SET} (kΩ)	V_O(V)	R_{SET} (kΩ)
2.50	4.33	5.20	0.180	1.70	1.02
2.55	4.11	5.30	0.131	1.75	0.551
2.60	3.89	5.40	0.085	1.80	0.130
2.65	3.7	5.50	0.041		

CAPACITOR RECOMMENDATIONS FOR THE PTH12060 SERIES OF POWER MODULES

Input Capacitor

The recommended input capacitance is determined by the 560 µF minimum capacitance and 1050 mArms minimum ripple current rating. A 10 µF X5R/X7R ceramic capacitor can be added to reduce the reflected input ripple current. The ceramic capacitor should be located between the input electrolytic and the module.

Ripple current, less than 100 mΩ equivalent series resistance (ESR) and temperature, are major considerations when selecting input capacitors. Unlike polymer-tantalum capacitors, regular tantalum capacitors have a recommended minimum voltage rating of 2 × (max. dc voltage + ac ripple). No tantalum capacitors were found with sufficient voltage rating to meet this requirement. At temperatures below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, Os-Con, polymer-tantalum, and polymer-aluminum types should be considered.

Output Capacitors (Optional)

For applications with load transients (sudden changes in load current), regulator response benefits from external output capacitance. The value of 330 µF is used to define the transient response specification. For most applications, a high quality, computer-grade aluminum electrolytic capacitor is adequate. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable for ambient temperatures above 0°C. Below 0°C, tantalum, ceramic, or Os-Con type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 4 mΩ (7 mΩ using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR type capacitors are identified in Table 4.

In addition to electrolytic capacitance, adding a 10 µF X5R/X7R ceramic capacitor to the output reduces the output ripple voltage and improves the regulator's transient response. The measurement of both the output ripple and transient response is also best achieved across a 10 µF ceramic capacitor.

Ceramic Capacitors

Above 150 kHz, the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input, and improve the transient response of the output. When used on the output, their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 300 µF. Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 µF or greater.

Tantalum Capacitors

Tantalum type capacitors are most suited for use on the output bus, and are recommended for applications where the ambient operating temperature can be less than 0°C. The AVX TPS, Sprague 593D/594/595, and Kemet T495/T510 capacitor series are suggested over other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR, reduced power dissipation, and lower ripple current capability. These capacitors are also less reliable as they have lower power dissipation and surge current ratings. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications.

When specifying Os-con and polymer tantalum capacitors for the output, the minimum ESR limit is encountered well before the maximum capacitance value is reached.

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Capacitor Table

Table 4 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

Note: This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

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Table 4. Input/Output Capacitors(1)

Capacitor Vendor, Type/Series (Style)	Capacitor Characteristics					Quantity		Vendor Number
	Working Voltage (V)	Value (µF)	Max ESR at 100 kHz (Ω)	Max Ripple Current at 85°C (Irms) (mA)	Physical Size (mm)	Input Bus	Output Bus	
Panasonic, Aluminum	35	680	0.060	1100	12,5 × 13,5	1	1	EEVFK1V681Q
FK (SMD)	25	1000	0.060	1100	12,5 × 13,5	1	1	EEVFK1E102Q
FC (Radial)	25	560	0.065	1205	12,5 × 15	1	1	EEUFC1E561S
United Chemi-Con								
PS, Poly-Aluminum (Radial)	16	330	0.0014	5050	10 × 12,5	2	≤2	16PS330MJ12
LXZ, Aluminum	16	680	0.068	1050	10 × 16	1	1	LXZ16VB681M10X16LL
PXA, Poly-Aluminum (SMD)	16	330	0.014	5050	10 × 12,2	2	≤2	PXA16VC331MJ12
Nichicon Aluminum								
PM (Radial)	25	560	0.060	1060	12,5 × 15	1	1	UPM1E561MHH6
HD (Radial)	16	680	0.038	1430	10 × 16	1	1	UHD1C681MHR
PM (Radial)	35	560	0.048	1360	16 × 15	1	1	UPM1V561MHH6
Panasonic, Poly-Aluminum								
S/SE (SMD)	6.3	180	0.005	4000	7,3 × 4,3 × 4,2	N/R(2)	≤1(3)	EEFSE0J181R(V_O≤5.1V)
Sanyo								
TPE, POSCAP (SMD)	10	330	0.025	3000	7,3 × 5,7	N/R(2)	≤4	10TPE330M
SEPC, OS-CON (Radial)	16	470	0.010	>9700	10 × 13	2	≤1	16SEPC470M
SVP, OS-CON (SMD)	16	330	0.016	4700	11 × 12	2	≤3	16SVP330M
AVX								
TPS, Tantalum (SMD)	10	470	0.045	>1723	7,3 × 5,7 × 4,1	N/R(2)	≤5(3)	TPSE477M019R0045(V_O≤5.1V)
TPS, Tantalum (SMD)	10	330	0.045	>1723		2	≤5(3)	TPSE337M019R0045(V_O≤5.1V)
Kemet								
T520, Poly-Tantalum (SMD)	10	330	0.040	1800		N/R(2)	≤5(3)	T520X337M010AS
T530, Tantalum/Organic	10	330	0.015	>3800	4,3 × 7,3 × 4,0	N/R(2)	≤2	T53X337M010AS
	6.3	470	0.012	4200		N/R(2)	≤2(3)	T530X477M0061S(V_O≤5.1V)
Vishay-Sprague 594D, Tantalum (SMD)	10	470	0.100	1440	7,2 × 6 × 4,1	N/R(2)		595D477X0010R2T(V_O≤5.1V)
94SP, Organic (Radial)	16	270	0.018	4200	10 × 10,5	2(4)	≤3	94SP277X0016FBP
94SVP, Organic (SMD)	16	330	0.017	4500	10 × 12.7	2	≤2	94SVP337X0016F12
Kemet, Ceramic X5R (SMD)	16	10	0.002		1210 case	1(5)	≤5	C1210C106M4PAC
	6.3	47	0.002		3225 mm	N/R(2)	≤5	C1210C476K9PAC
Murata, Ceramic X5R (SMD)	6.3	100	0.002		1210 case	N/R(2)	≤3	GRM32ER60J107M
	6.3	47			3225 mm	N/R(2)	≤5	GRM32ER60J476M
	16	22				1(5)	≤5	GRM32ER61C226K
	16	10				1(5)	≤5	GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3	100	0.002		1210 case	N/R(2)	≤3	C3225X5R0J107MT
	6.3	47			3225 mm	N/R(2)	≤5	C3225X5R0J476MT
	16	22				1(5)	≤5	C3225X5R1C226MT
	16	10				1(5)	≤5	C3225X5R1C106MT

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table. Capacitor suppliers may recommend alternative part numbers because of limited availability or obsolete products. In some instances, the capacitor product life cycle may be in decline and have short-term consideration for obsolescence.
RoHS, Lead-free and Material Details
Please consult capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements. Component designators or part number deviations can occur when material composition or soldering requirements are updated.
(2) N/R – Not recommended. The capacitor voltage rating does not meet the minimum operating limits.
(3) The voltage rating of this capacitor only allows it to be used for output voltages that are equal to or less than 5.1 V.
(4) A total capacitance of 540 µF is acceptable based on the combined ripple current rating.
(5) Ceramic capacitors are required to complement electrolytic types at the input and to reduce high-frequency ripple current.

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Designing for Very Fast Load Transients

The transient response of the dc/dc converter is characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement is met with additional output capacitor decoupling. In these cases, special attention must be paid to the type, value, and ESR of the capacitors selected.

If the transient performance requirements exceed that specified in this data sheet, or the total amount of load capacitance is above 3,000 µF, the selection of output capacitors becomes more important.

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Features of the PTH Family of Non-Isolated Wide Output Adjust Power Modules

Introduction

The PTH/PTV family of non-isolated, wide-output adjustable power modules are optimized for applications that require a flexible, high performance module that is small in size. Each of these products are POLA™ compatible. POLA-compatible products are produced by a number of manufacturers, and offer customers advanced, nonisolated modules with the same footprint and form factor. POLA parts are also ensured to be interoperable, thereby, providing customers with second-source availability.

From the basic, *Just Plug it In* functionality of the 6-A modules, to the 30-A rated feature-rich PTHxx030, these products were designed to be very flexible, yet simple to use. The features vary with each product. Table 5 provides a quick reference to the features by product series and input bus voltage.

Table 5. Operating Features by Series and Input Bus Voltage

Series	Input Bus (V)	I_O (A)	Adjust (Trim)	On/Off Inhibit	Over-Current	Prebias Startup	Auto-Track™	Margin Up/Down	Output Sense	Thermal Shutdown
PTHxx050	3.3	6	•	•	•	•	•			
	5	6	•	•	•	•	•			
	12	6	•	•	•	•	•			
PTHxx060	3.3 / 5	10	•	•	•	•	•	•	•	
	12	10	•	•	•	•	•	•	•	
PTHxx010	3.3 / 5	15	•	•	•	•	•	•	•	
	12	12	•	•	•	•	•	•	•	
PTVxx010	5	8	•	•	•	•	•			
	12	8	•	•	•	•	•			
PTHxx020	3.3 / 5	22	•	•	•	•	•	•	•	•
	12	18	•	•	•	•	•	•	•	•
PTVxx020	3.3 / 5	18	•	•	•	•	•		•	•
	12	16	•	•	•	•	•		•	•
PTHxx030	3.3 / 5	30	•	•	•	•	•	•	•	•
	12	26	•	•	•	•	•	•	•	•

For simple point-of-use applications, the PTH12050 (6 A) provides operating features such as an on/off inhibit, output voltage trim, prebias start-up and overcurrent protection. The PTH12060 (10 A), and PTH12010 (12 A) include an output voltage sense, and margin up/down controls. Then the higher output current, PTH12020 (18 A) and PTH12030 (26 A) products incorporate overtemperature shutdown protection.

The PTV12010 and PTV12020 are similar parts offered in a vertical, single in-line pin (SIP) profile, at slightly lower current ratings.

All of the products referenced in Table 5 include Auto-Track™. This feature was specifically designed to simplify the task of sequencing the supply voltages in a power system. This and other features are described in the following sections.

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POWER-UP INTO A NON-PREBIASED OUTPUT — AUTO-TRACK™ FUNCTION

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications that use dual-voltage VLSI ICs such as the TMS320™ DSP family, microprocessors, and ASICs.

Basic Power-Up using Auto-Track™

For applications requiring output voltage on/off control, each series of the PTH family incorporates the track control pin. The Auto-Track feature should be used instead of the inhibit feature wherever there is a requirement for the output voltage from the regulator to be turned on/off.

Figure 10 shows the typical application for basic start-up. Note the discrete transistor (Q1). The track input has its own internal pull-up to a potential of 5 V to 13.2 V The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor or supply voltage supervisor (TPS3808 or TPS7712) is recommended for control.

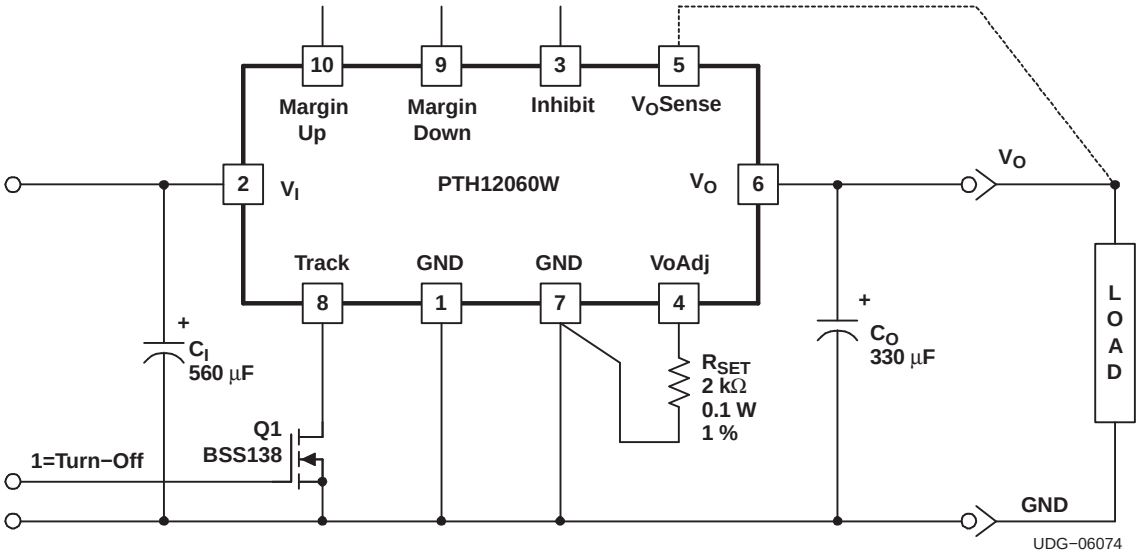

Figure 10. Basic Start-up Control Circuit

Turning on Q1 applies a low voltage to the track control pin and disables the output of the module. If Q1 is then turned off, the output ramps immediately to the regulated output voltage. A regulated output voltage is produced within 35 ms. With the initial application of the input source voltage, the track pin must be held low (Q1 turned ON) for at least 40 ms. Figure 11 shows the typical rise in both the output voltage and input current, following the turn off of Q1. The turn off of Q1 corresponds to the rise in the waveform, Q1 Vds. The waveforms were measured with a 10-A constant current load.

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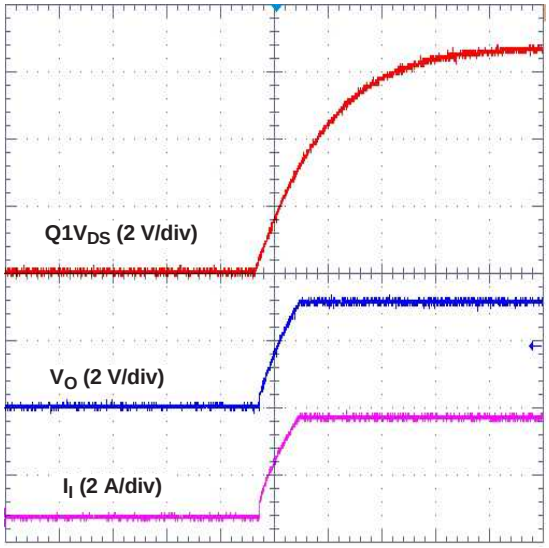

Figure 11. Power-Up from Track Control

NOTE:

If a prebias condition is not present, it is highly recommended that the Track control pin be used for controlled power-up and power-down. If Track control is not used, the output voltage starts up and overshoots by as much as 10%, before settling at the output voltage setpoint.

How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the *Track* control pin (1). This control range is limited to between 0 V and the module set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module output remains at its set-point (2). As an example, if the *Track* pin of a 2.5-V regulator is at 1 V, the regulated output is 1 V. If the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 2.5 V.

When under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit (3). For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.

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Typical Auto-Track Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the *Track* inputs of two or more modules forces their track input to follow the same collective RC-ramp waveform, and allows their power-up sequence to be coordinated from a common Track control signal. This can be an open-collector (or open-drain) device, such as a power-up reset voltage supervisor IC. See U3 in Figure 12.

To coordinate a power-up sequence, the Track control must first be pulled to ground potential through R_{TRK} as defined in Figure 12. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 40 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization (4), enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, that includes a built-in time delay, is an ideal component for automatically controlling the Track inputs at power up.

Figure 12 shows how the TL7712A supply voltage supervisor IC (U3) can be used to coordinate the sequenced power up of two 12-V input Auto-Track modules. The output of the TL7712A supervisor becomes active above an input voltage of 3.6 V, enabling it to assert a ground signal to the common track control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 43 ms after the input voltage has risen above U3's voltage threshold, which is 10.95 V. The 43-ms time period is controlled by the capacitor C3. The value of 3.3 µF provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the track control voltage is allowed to rise. When U3 removes the ground signal, the track control voltage automatically rises. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.

Figure 13 shows the output voltage waveforms from the circuit of Figure 12 after input voltage is applied to the circuit. The waveforms, V_O1 and V_O2, represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively. V_{TRK}, V_O1, and V_O2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is re-applied to the common track control. This pulls the track inputs to zero volts, forcing the output of each module to follow, as shown in Figure 14. In order for a simultaneous power-down to occur, the track inputs must be pulled low before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that a valid input voltage is no longer present, their outputs can no longer follow the voltage applied at their track input. During a power-down sequence, the fall in the output voltage from the modules is limited by the maximum output capacitance and the Auto-Track slew rate. If the *Track* pin is pulled low at a slew rate greater than 1 V/ms, the discharge of the output capacitors will induce large currents which could exceed the peak current rating of the module. This will result in a reduction in the maximum allowable output capacitance as listed in the Electrical Characteristics table. When controlling the *Track* pin of the PTH12060W using a voltage supervisor IC, the slew rate is increased, therefore $C_O$max is reduced to 2200 µF.

Notes on Use of Auto-Track™

1. The *Track* pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the *Track* pin is the input voltage V_I.
4. The module cannot follow a voltage at its track control input until it has completed its soft-start initialization. This takes about 40 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the *Track* pin be held at ground potential.
5. The Auto-Track function is disabled by connecting the *Track* pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises at a quicker and more linear rate after input power has been applied.

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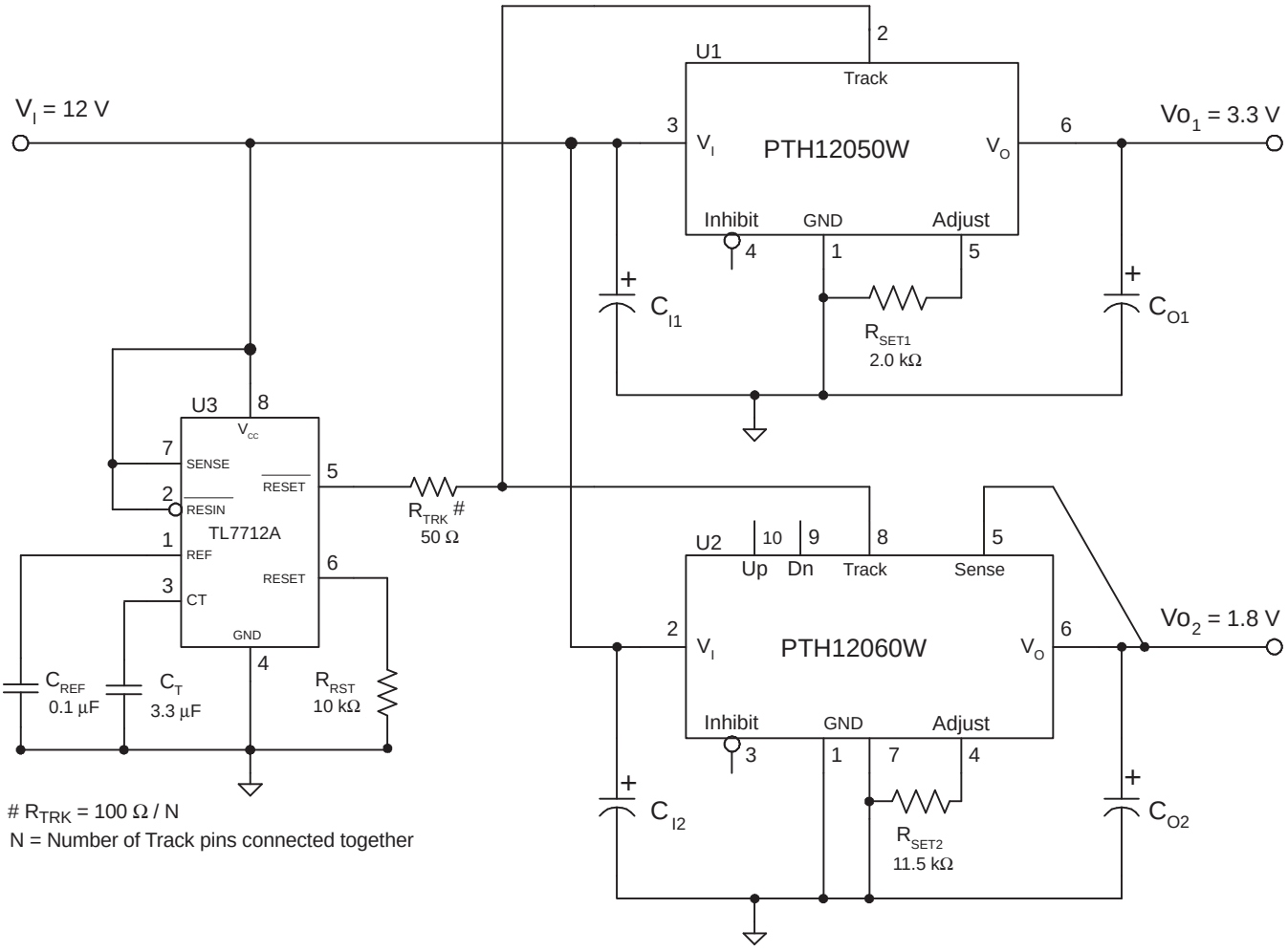

Figure 12. Sequenced Power Up and Power Down Using Auto-Track

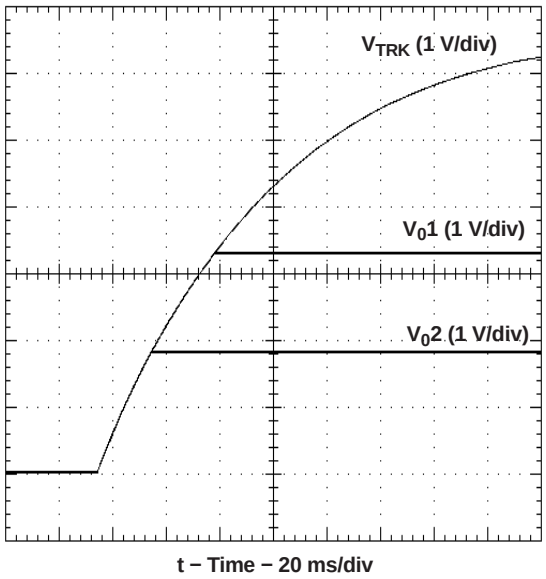

Figure 13. Simultaneous Power Up With Auto-Track Control

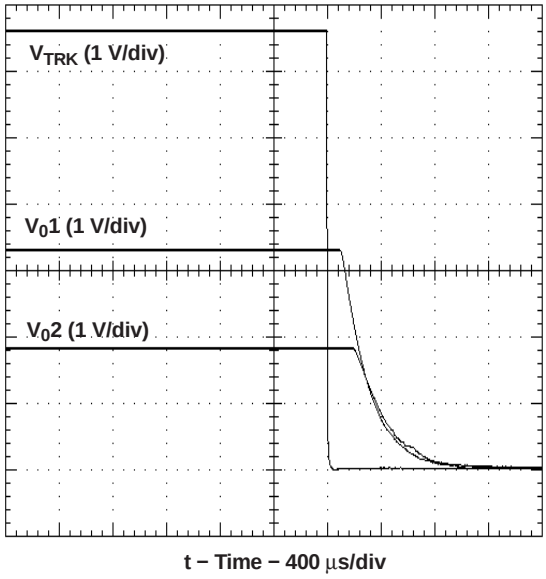

Figure 14. Simultaneous Power Down with Auto-Track Control

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POWER-UP INTO A PREBIASED OUTPUT — START-UP USING INHIBIT CONTROL

The capability to start up into an output prebias condition is now available to all the 12-V input, PTH series of power modules. (Note that this is a feature enhancement for the many of the W-suffix products) [1].

A prebias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes, sometimes used as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, such modules can sink as well as source output current. The 12-V input PTH modules all incorporate synchronous rectifiers, but does not sink current during startup, or whenever the Inhibit pin is held low.

Conditions for Prebias Holdoff

In order for the module to allow an output prebias voltage to exist (and not sink current), certain conditions must be maintained. The module holds off a prebias voltage when the Inhibit pin is held low, and whenever the output is allowed to rise under soft-start control. Power up under soft-start control occurs upon the removal of the ground signal to the Inhibit pin (with input voltage applied), or when input power is applied with Auto-Track disabled [2]. To further ensure that the regulator doesn't sink output current, (even with a ground signal applied to its Inhibit), the input voltage must always be greater than the applied prebias source. This condition must exist throughout the power-up sequence [3].

The soft-start period is complete when the output begins rising above the prebias voltage. Once it is complete the module functions as normal, and sinks current if a voltage higher than the nominal regulation value is applied to its output.

Note: If a prebias condition is not present, the soft-start period is complete when the output voltage has risen to either the set-point voltage, or the voltage applied at the module's Track control pin, whichever is lowest. to its output.

Prebias Demonstration Circuit

Figure 15 shows the startup waveforms for the demonstration circuit shown in Figure 16. The initial rise in V_O2 is the prebias voltage, which is passed from the VCCIO to the VCORE voltage rail through the ASIC. Note that the output current from the PTH12010L module (I_O2) is negligible until its output voltage rises above the applied prebias.

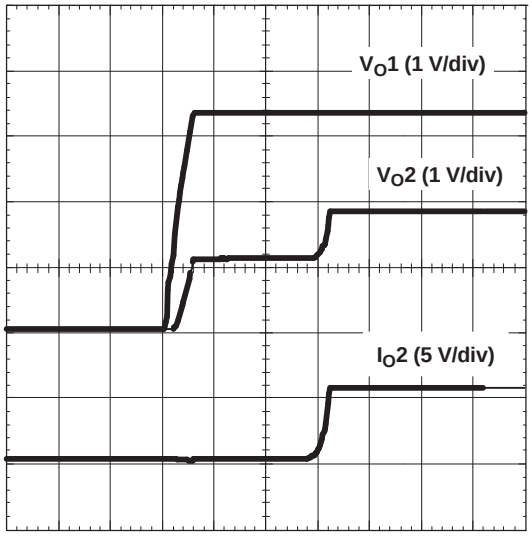

Figure 15. Prebias Startup Waveforms

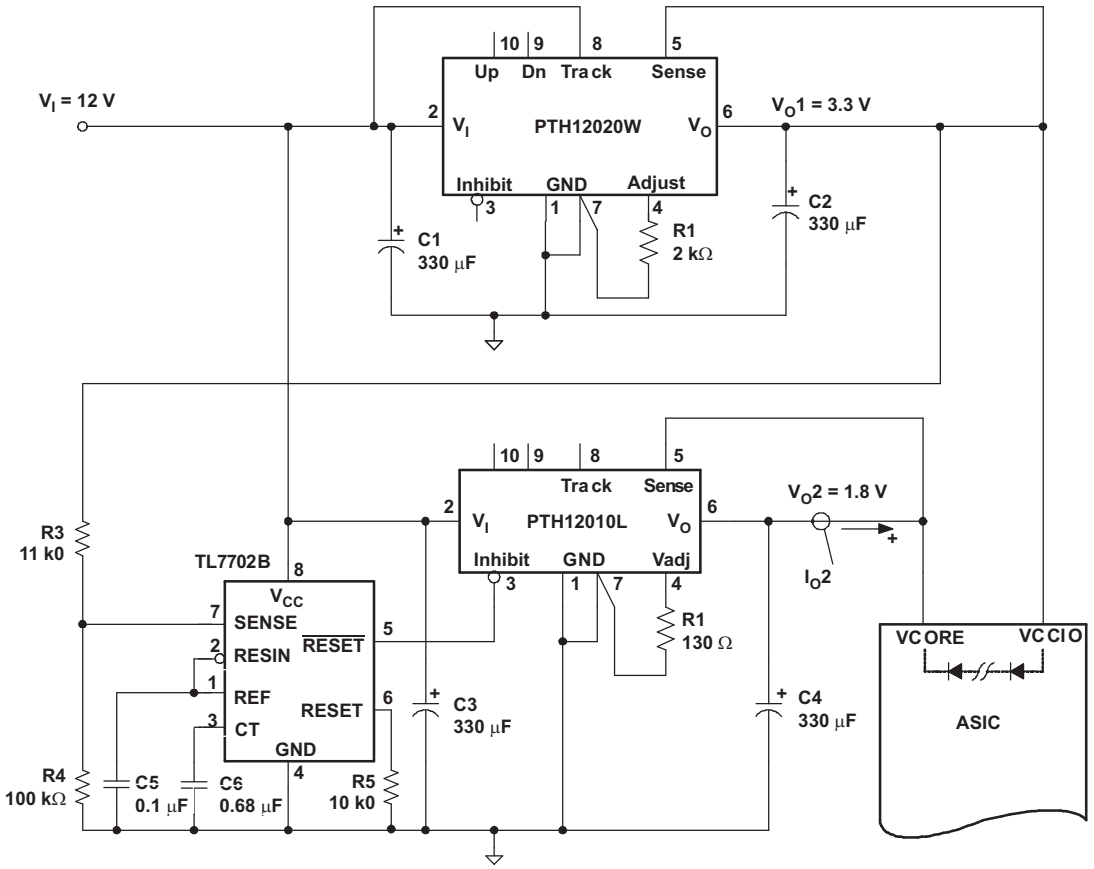

Figure 16. Application Circuit Demonstrating Prebias Startup

Notes:

1. Output prebias holdoff is an inherent feature to all PTH120x0L and PTV120x0W/L modules. It has now been incorporated into all modules (including W-suffix modules with part numbers of the form PTH120x0W), with a production lot date code of *0423* or later.
2. The prebias start-up feature is not compatible with Auto-Track. If the rise in the output is limited by the voltage applied to the Track control pin, the output sinks current during the period that the track control voltage is below that of the back-feeding source. For this reason, it is recommended that Auto-Track be disabled when not being used. This is accomplished by connecting the Track pin to the input voltage, V_I. This raises the Track pin voltage well above the set-point voltage prior to the module's start up, thereby, defeating the Auto-Track feature.
3. To further ensure that the regulator's output does not sink current when power is first applied (even with a ground signal applied to the Inhibit control pin), the input voltage must always be greater than the applied prebias source. This condition must exist *throughout* the power-up sequence of the power system.

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Remote Sense

Products with this feature incorporate an output voltage sense pin, V_O Sense. A remote sense improves the load regulation performance of the module by allowing it to compensate for any *IR* voltage drop between its output and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance.

To use this feature simply connect the V_O Sense pin to the V_O node, close to the load circuit (see data sheet standard application circuit). If a sense pin is left open-circuit, an internal low-value resistor (15-Ω or less) connected between the pin and the output node, ensures the output remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the V_O and GND pins, and that measured from V_O Sense to GND, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

Note: The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

Overcurrent Protection

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, a module periodically attempts to recover by initiating a soft-start power-up. This is described as a *hiccup* mode of operation, whereby, the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Overtemperature Protection (OTP)

The PTH12020, PTV12020, and PTH12030 products have overtemperature protection. These products have an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's Inhibit control is internally pulled low. This turns the output off. The output voltage drops as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the sensed temperature decreases by about 10°C below the trip point.

Note: The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

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Margin Up/Down Controls

The PTH12060, PTH12010, PTH12020, and PTH12030 products incorporate Margin Up and Margin Down control inputs. These controls allow the output voltage to be momentarily adjusted [1], either up or down, by a nominal 5%. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. The ±5% change is applied to the adjusted output voltage, as set by the external resistor, R_{SET} at the V_O Adjust pin.

The 5% adjustment is made by pulling the appropriate margin control input directly to the GND terminal [2]. A low-leakage, open-drain device, such as an n-channel MOSFET or p-channel JFET is recommended for this purpose [3]. Adjustments of less than 5% can also be accommodated by adding series resistors to the control inputs. The value of the resistor can be selected from Table 6, or calculated using Equation 2.

Margin Up/Down Adjust Resistance Calculation

To reduce the margin adjustment to a value less than 5%, series resistors are required (See R_D and R_U in Equation 2). For the same amount of adjustment, the resistor value calculated for R_U and R_D is the same. The formula is as follows.

$$R_U = \left(\frac{499}{\Delta\%}\right) - 99.8\,k\Omega$$

$$R_D = \left(\frac{499}{\Delta\%}\right) - 99.8\,k\Omega \quad (2)$$

Where Δ% = The desired amount of margin adjust in percent.

Notes:

1. The Margin Up and Margin Down controls were not intended to be activated simultaneously. If they are activated simultaneously, the affect on the output voltage may not completely cancel, resulting in the possibility of a slightly higher error in the output voltage set point.
2. The ground reference should be a direct connection to the module GND. This produces a more accurate adjustment at the load circuit terminals. The transistors Q1 and Q2 should be located close to the regulator.
3. The Margin Up and Margin Down control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true open-drain device (preferably a discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8 µA when grounded, and has an open-circuit voltage of 0.8 V.

Table 6. Margin Up/Down Resistor Values

% Adjust	5%	4%	3%	2%	1%
R_U / R_D(kΩ)	0.0	24.9	66.5	150.0	397.0

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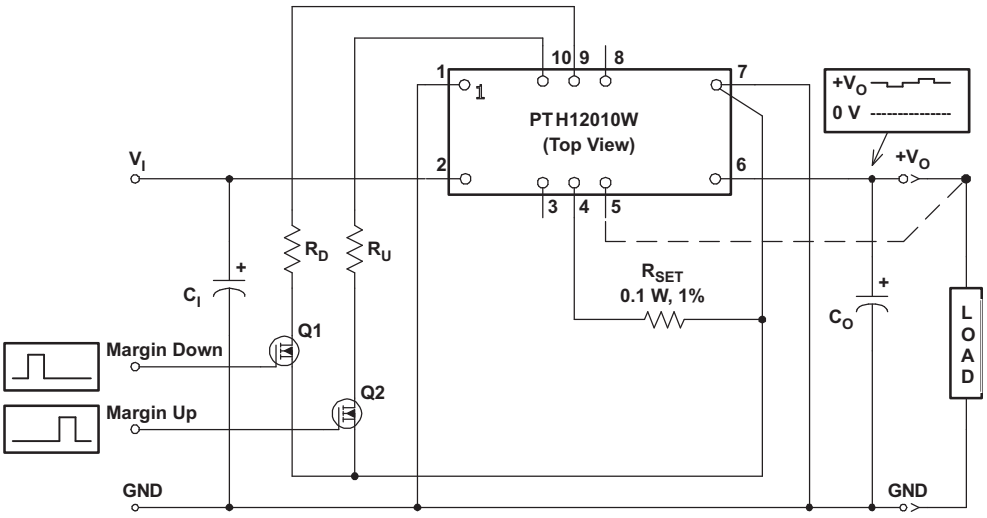
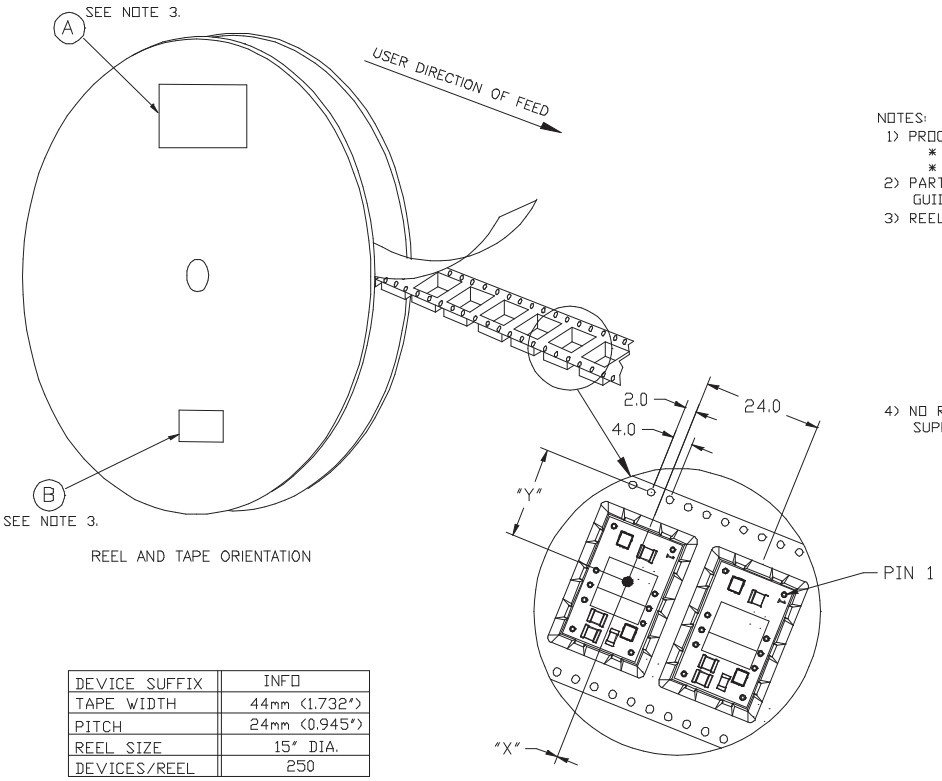


Figure 17. Margin Up/Down Application Schematic

TAPE AND REEL SPECIFICATIONS



REEL AND TAPE ORIENTATION

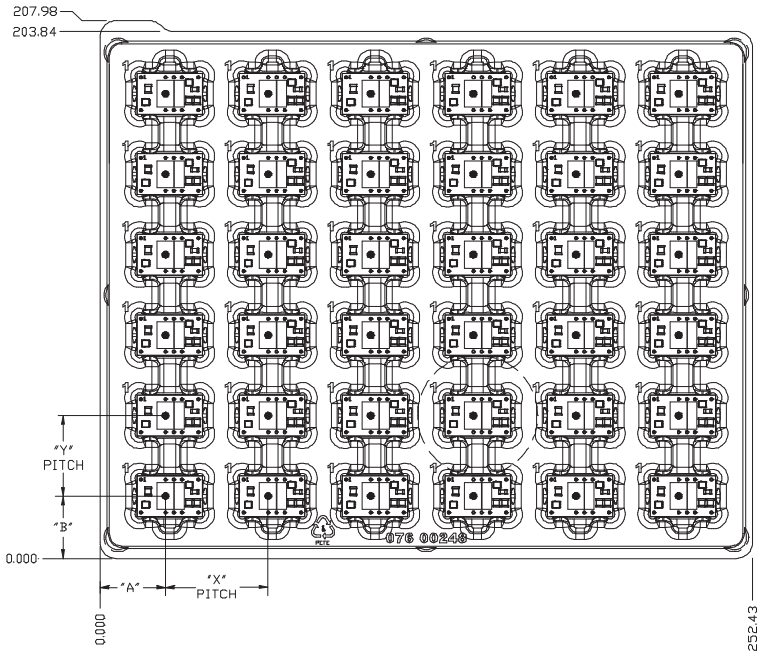
NOTES:
1) PROCESS IN ACCORDANCE WITH EIA-481-2
   * TAPE LEADER DIMENSION 15.30" MIN.
   * TAPE TRAILER DIMENSION 6.30" MIN.
2) PARTS SHOULD BE PACKAGED IN ACCORDANCE WITH ESD GUIDELINES IN EIA-541.
3) REEL LABEL: "A"- * TI PART NUMBER.
   * QUANTITY
   * DATE CODE
   * LOT NUMBER
   * MSL DATA
   * MADE IN
   * ASSY SITE ORIGIN
   * COUNTRY OF ORIGIN
   * SUPPLIER

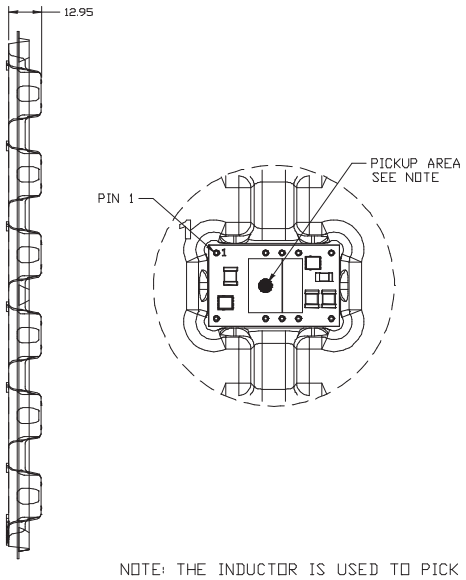
   "B"- ANTI-STATIC CAUTION LABEL
4) NO REQUIREMENT FOR TAPE DIRECTION OF FEED FROM SUPPLIER REEL.

PTXXXX6X	"X"	"Y"
PTH03060/05060	0.0mm	18.4mm
PTH12060	0.0mm	17.9mm
PTN78060	1.2mm	21.8mm

DEVICE SUFFIX	INFO
TAPE WIDTH	44mm (1.732")
PITCH	24mm (0.945")
REEL SIZE	15" DIA.
DEVICES/REEL	250

TRAY SPECIFICATIONS





NOTE: THE INDUCTOR IS USED TO PICK AND PLACE THE MODULE. IT'S LOCATION MAY VARY FROM PACKAGE STYLE. SEE PRODUCT TABLE

PTXXXX6X	"A"	"B"	"X"	"Y"
PTH03060/05060	25.46	24.13	39.52	31.12
PTH12060	24.66	24.13		
PTN78060	28.61	25.35		
ALL DIMENSIONS ARE IN MILLIMETER.				

DEVICES/TRAY	36

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTH12060LAH	ACTIVE	Through-Hole Module	EUW	10	36	RoHS (In Work) & Green (In Work)	SN	N / A for Pkg Type	-40 to 85		Samples
PTH12060LAS	ACTIVE	Surface Mount Module	EUY	10	36	Non-RoHS & Green (In Work)	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH12060LAST	ACTIVE	Surface Mount Module	EUY	10	250	Non-RoHS & Green (In Work)	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH12060LAZ	ACTIVE	Surface Mount Module	EUY	10	36	RoHS (In Work) & Green (In Work)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH12060LAZT	ACTIVE	Surface Mount Module	EUY	10	250	RoHS (In Work) & Green (In Work)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH12060WAD	ACTIVE	Through-Hole Module	EUW	10	36	RoHS (In Work) & Green (In Work)	SN	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH12060WAH	ACTIVE	Through-Hole Module	EUW	10	36	RoHS (In Work) & Green (In Work)	SN	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH12060WAS	ACTIVE	Surface Mount Module	EUY	10	36	Non-RoHS & Green (In Work)	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH12060WAST	ACTIVE	Surface Mount Module	EUY	10	250	Non-RoHS & Green (In Work)	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH12060WAZ	ACTIVE	Surface Mount Module	EUY	10	36	RoHS (In Work) & Green (In Work)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH12060WAZT	ACTIVE	Surface Mount Module	EUY	10	250	RoHS (In Work) & Green (In Work)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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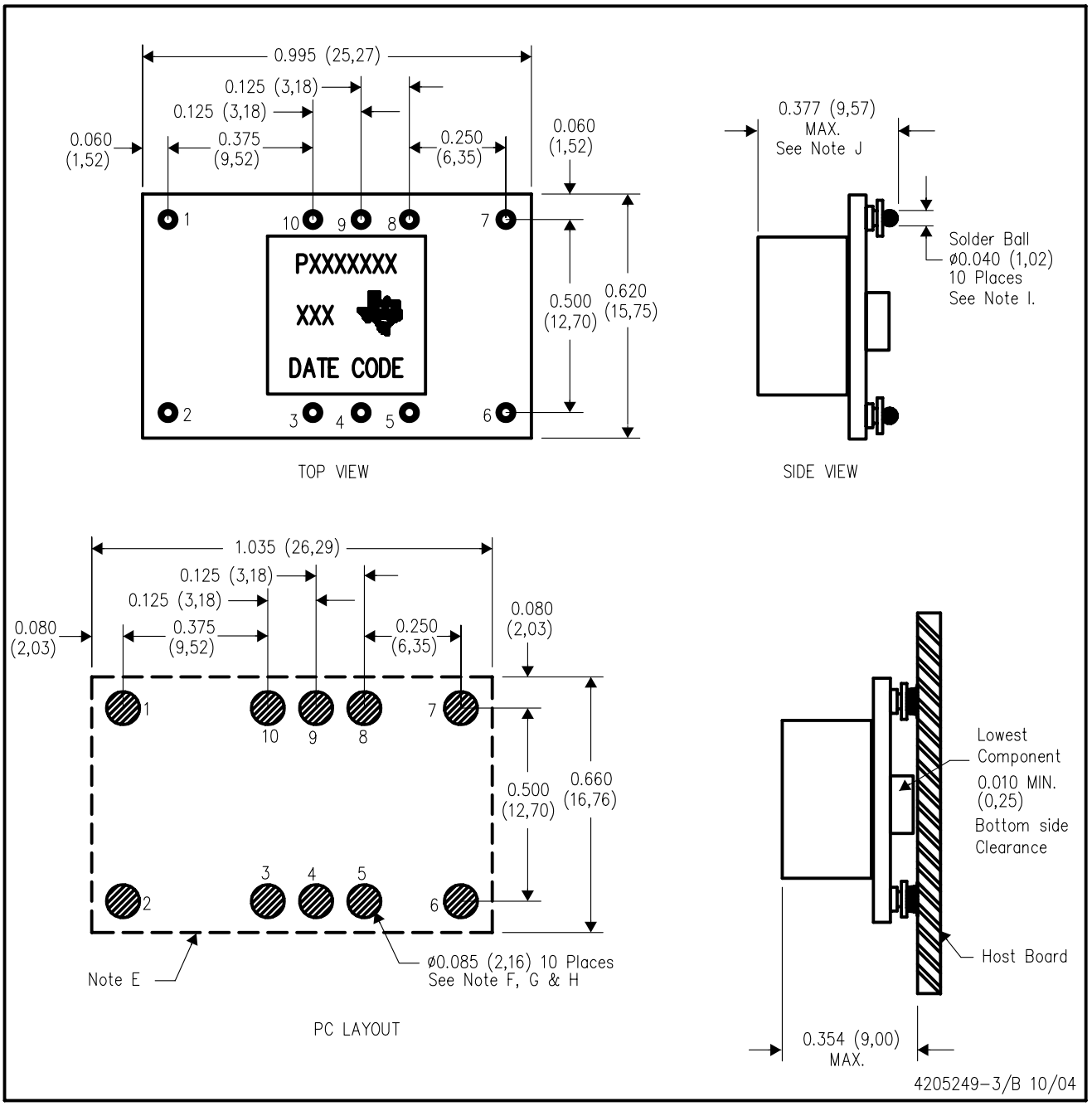
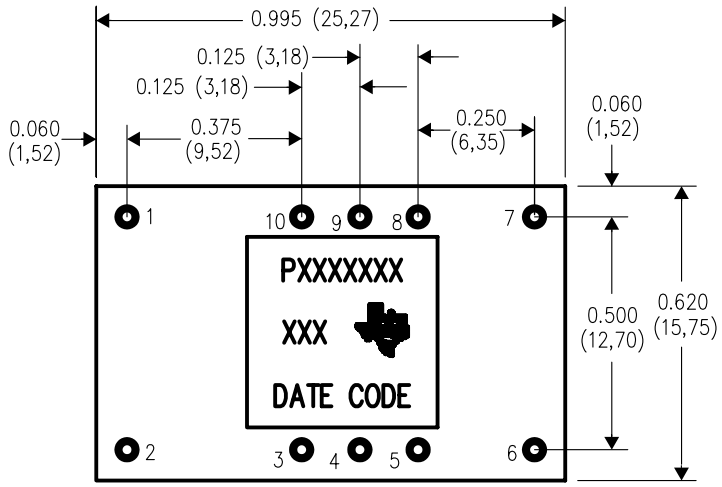
EUY (R–PDSS–B10) DOUBLE SIDED MODULE

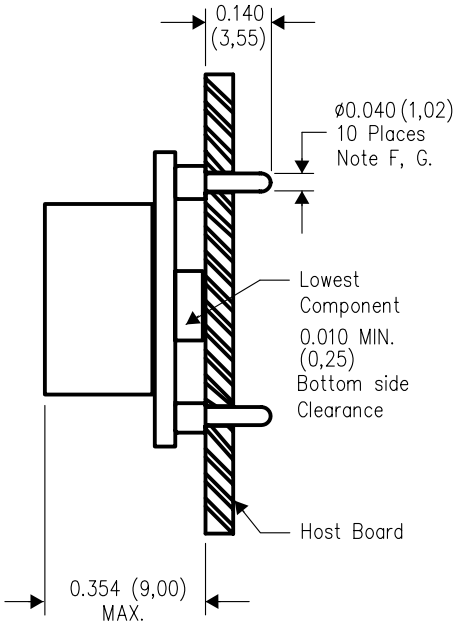


NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

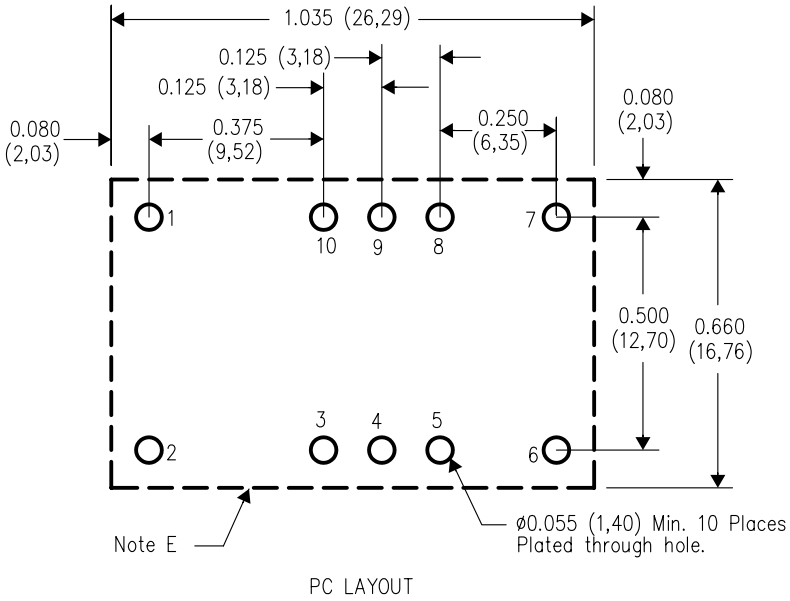
EUW (R–PDSS–T10) DOUBLE SIDED MODULE



TOP VIEW



SIDE VIEW



PC LAYOUT

4205248–3/B 10/04

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B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

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