



# THE DATASHEET OF RC4558IDR



## RC4558 Dual General-Purpose Operational Amplifier

### 1 Features

- Continuous Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Unity-Gain Bandwidth: 3 MHz Typ
- Gain and Phase Match Between Amplifiers
- Low Noise: 8 nV/ $\sqrt{\text{Hz}}$  Typ at 1 kHz

### 2 Applications

- DVD Recorders and Players
- Pro Audio Mixers

### 3 Description

The RC4558 device is a dual general-purpose operational amplifier, with each half electrically similar to the  $\mu\text{A}741$ , except that offset null capability is not provided.

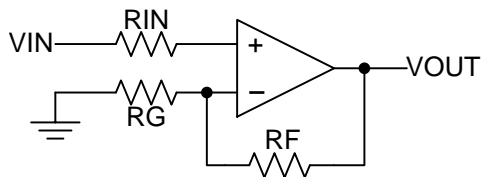
The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected, and the internal frequency compensation ensures stability without external components.

#### Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE
RC4558	SOIC (8)	4.90 mm x 3.91 mm
	SOIC (8)	3.00 mm x 3.00 mm
	PDIP (8)	9.81 mm x 6.35 mm
	TSSOP (8)	3.00 mm x 4.40 mm
	SOP (8)	6.20 mm x 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Noninverting Amplifier Schematic



## Table of Contents

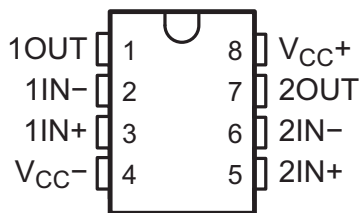
<b>1 Features</b> .....	<b>1</b>	7.2 Functional Block Diagram .....	<b>9</b>
<b>2 Applications</b> .....	<b>1</b>	7.3 Feature Description .....	<b>9</b>
<b>3 Description</b> .....	<b>1</b>	7.4 Device Functional Modes .....	<b>9</b>
<b>4 Revision History</b> .....	<b>2</b>	<b>8 Application and Implementation</b> .....	<b>10</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	8.1 Typical Application .....	<b>10</b>
<b>6 Specifications</b> .....	<b>4</b>	<b>9 Power Supply Recommendations</b> .....	<b>13</b>
6.1 Absolute Maximum Ratings .....	<b>4</b>	<b>10 Layout</b> .....	<b>14</b>
6.2 Handling Ratings .....	<b>4</b>	10.1 Layout Guidelines .....	<b>14</b>
6.3 Recommended Operating Conditions .....	<b>4</b>	10.2 Layout Example .....	<b>14</b>
6.4 Thermal Information .....	<b>4</b>	<b>11 Device and Documentation Support</b> .....	<b>15</b>
6.5 Electrical Characteristics .....	<b>5</b>	11.1 Trademarks .....	<b>15</b>
6.6 Operating Characteristics .....	<b>5</b>	11.2 Electrostatic Discharge Caution .....	<b>15</b>
6.7 Typical Characteristics .....	<b>6</b>	11.3 Glossary .....	<b>15</b>
<b>7 Detailed Description</b> .....	<b>9</b>	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>15</b>
7.1 Overview .....	<b>9</b>		

## 4 Revision History

<b>Changes from Revision F (September 2010) to Revision G</b>	<b>Page</b>
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Handling Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....	<b>1</b>
• Removed <i>Ordering Information</i> table. ....	<b>1</b>

## 5 Pin Configuration and Functions

**D, DGK, P, PS, OR PW PACKAGE  
(TOP VIEW)**



**Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input
1IN-	2	I	Inverting Input
1OUT	1	O	Output
2IN+	5	I	Noninverting input
2IN-	6	I	Inverting Input
2OUT	7	O	Output
V <sub>CC</sub> +	8	—	Positive Supply
V <sub>CC</sub> -	4	—	Negative Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC+</sub>	Supply voltage <sup>(2)</sup>		18	V
V <sub>CC-</sub>			-18	
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>		±30	V
V <sub>I</sub>	Input voltage (any input) <sup>(2)(4)</sup>		±15	V
	Duration of output short circuit to ground, one amplifier at a time <sup>(5)</sup>		Unlimited	
T <sub>J</sub>	Operating virtual junction temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, unless otherwise noted, are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC-</sub>.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
- (5) Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

### 6.2 Handling Ratings

		MIN	MAX	UNIT	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	0	500	V
		Charged device model (CDM), per AEC Q100-011 <sup>(2)</sup>	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>CC+</sub>	Supply voltage	5	15	V	
V <sub>CC-</sub>		-5	-15		
T <sub>A</sub>	Operating free-air temperature	RC4558	0	70	°C
		RC4558I	-40	85	

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	RC4558					UNIT	
	D	DGK	P	PS	PW		
	8 PINS						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	97	172	85	95	149	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

at specified free-air temperature,  $V_{CC+} = 15\text{ V}$ ,  $V_{CC-} = -15\text{ V}$ 

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	$T_A$ <sup>(2)</sup>	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_O = 0$	25°C		0.5	6	mV
			Full range			7.5	
$I_{IO}$	Input offset current	$V_O = 0$	25°C		5	200	nA
			Full range			300	
$I_{IB}$	Input bias current	$V_O = 0$	25°C		150	500	nA
			Full range			800	
$V_{ICR}$	Common-mode input voltage range		25°C	±12	±14		V
$V_{OM}$	Maximum output voltage swing	$R_L = 10\text{ k}\Omega$	25°C	±12	±14		V
			Full range	±10	±13		
		$R_L = 2\text{ k}\Omega$	Full range	±10			
$A_{VD}$	Large-signal differential voltage amplification	$R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}$	25°C	20	300		V/mV
			Full range	15			
$B_1$	Unity-gain bandwidth		25°C		3		MHz
$r_i$	Input resistance		25°C	0.3	5		M $\Omega$
CMRR	Common-mode rejection ratio		25°C	70	90		dB
$k_{SVS}$	Supply-voltage sensitivity ( $\Delta V_{IO}/\Delta V_{CC}$ )	$V_{CC} = \pm 15\text{ V}$ to $\pm 9\text{ V}$	25°C		30	150	$\mu\text{V/V}$
$V_n$	Equivalent input noise voltage (closed loop)	$A_{VD} = 100$ , $R_S = 100\ \Omega$ , $f = 1\text{ kHz}$ , $BW = 1\text{ Hz}$	25°C		8		$\text{nV}/\sqrt{\text{Hz}}$
$I_{CC}$	Supply current (both amplifiers)	$V_O = 0$ , No load	25°C		2.5	5.6	mA
			$T_A$ min		3	6.6	
			$T_A$ max		2.3	5	
$P_D$	Total power dissipation (both amplifiers)	$V_O = 0$ , No load	25°C		75	170	mW
			$T_A$ min		90	200	
			$T_A$ max		70	150	
$V_{O1}/V_{O2}$	Crosstalk attenuation	Open loop	25°C		85		dB
		$A_{VD} = 100$					

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified.

(2) Full range is 0°C to 70°C for RC4558 and –40°C to 85°C for RC4558L.

## 6.6 Operating Characteristics

 $V_{CC+} = 15\text{ V}$ ,  $V_{CC-} = -15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_r$	Rise time	$V_I = 20\text{ mV}$ ,	$R_L = 2\text{ k}\Omega$ ,	$C_L = 100\text{ pF}$		0.13		ns
	Overshoot	$V_I = 20\text{ mV}$ ,	$R_L = 2\text{ k}\Omega$ ,	$C_L = 100\text{ pF}$		5%		
SR	Slew rate at unity gain	$V_I = 10\text{ V}$ ,	$R_L = 2\text{ k}\Omega$ ,	$C_L = 100\text{ pF}$	1.1	1.7		V/ $\mu\text{s}$

## 6.7 Typical Characteristics

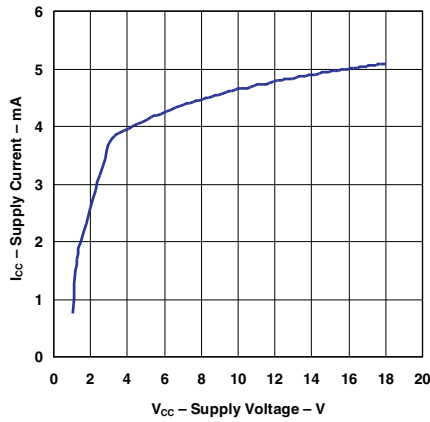


Figure 1. Supply Current vs Supply Voltage  
( $T_A = 25^\circ\text{C}$ )

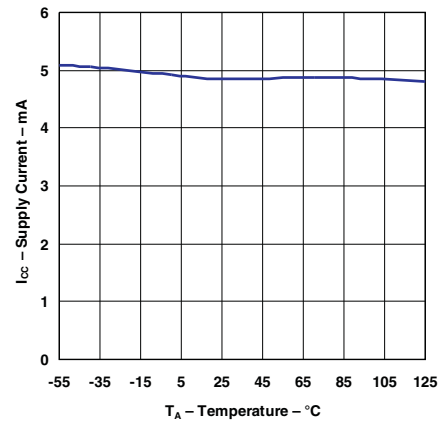


Figure 2. Supply Current vs Temperature  
( $V_{CC} = \pm 15\text{ V}$ )

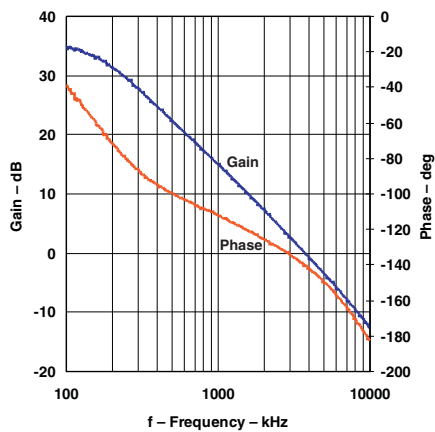


Figure 3. Gain and Phase vs Frequency  
( $V_{CC} = \pm 15\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ ,  $C_L = 22\text{ pF}$ )

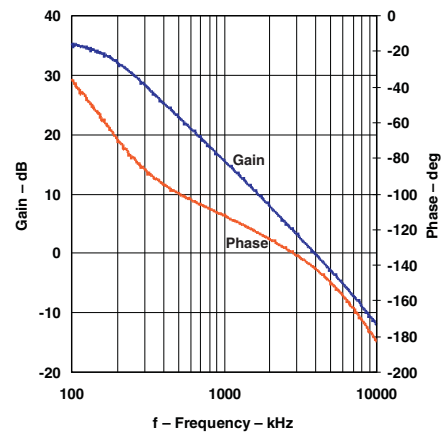


Figure 4. Gain and Phase vs Frequency  
( $V_{CC} = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ ,  $C_L = 22\text{ pF}$ )

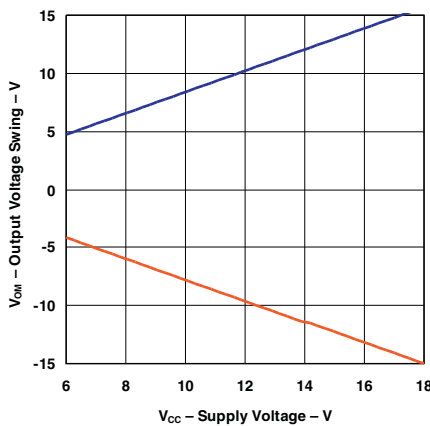


Figure 5. Output Voltage Swing vs Supply Voltage  
( $R_L = 2\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$ )

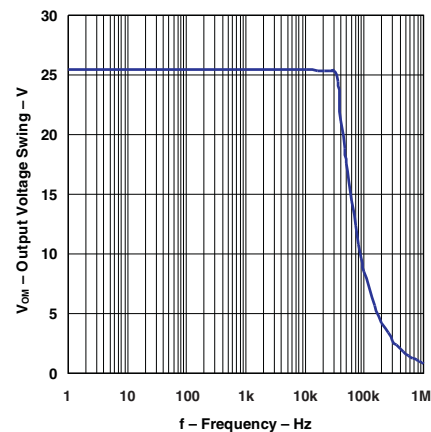


Figure 6. Output Voltage Swing vs Frequency  
( $V_{CC} = \pm 15\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$ )

Typical Characteristics (continued)

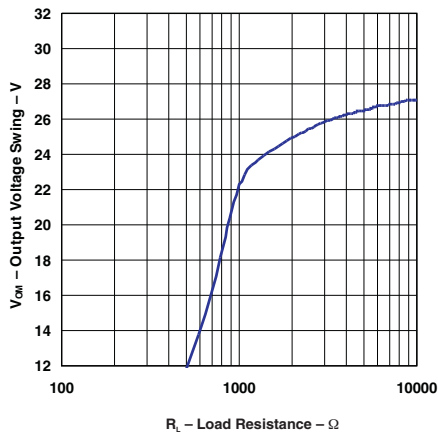


Figure 7. Output Voltage Swing vs Load Resistance ( $V_{CC} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ )

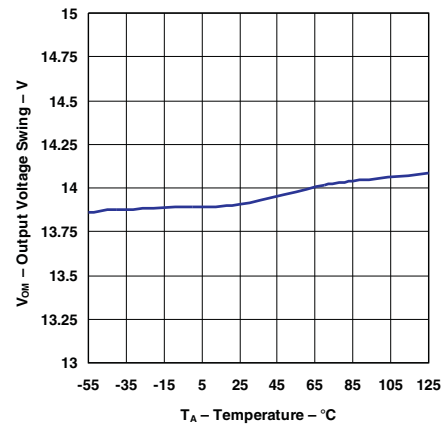


Figure 8. Output Voltage Swing vs Temperature ( $V_{CC} = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ )

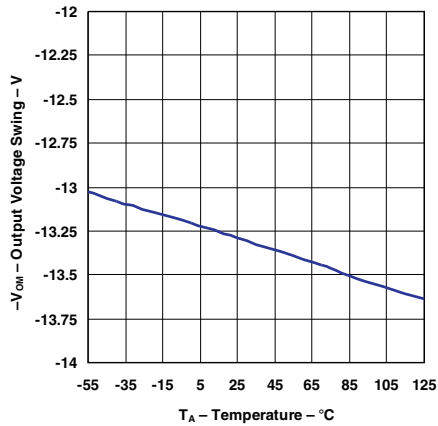


Figure 9. Negative Output Voltage Swing vs Temperature ( $V_{CC} = \pm 15\text{ V}$ ,  $R_L = 10\text{ k}\Omega$ )

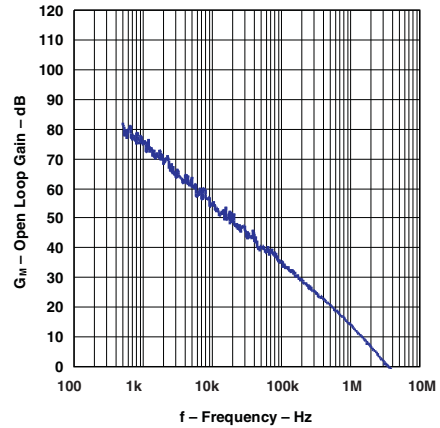


Figure 10. Open Loop Gain vs Frequency ( $V_{CC} = \pm 15\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ ,  $C_L = 22\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

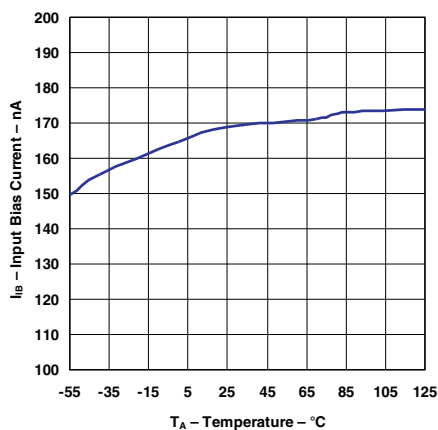


Figure 11. Input Bias Current vs Temperature ( $V_{CC} = \pm 15\text{ V}$ )

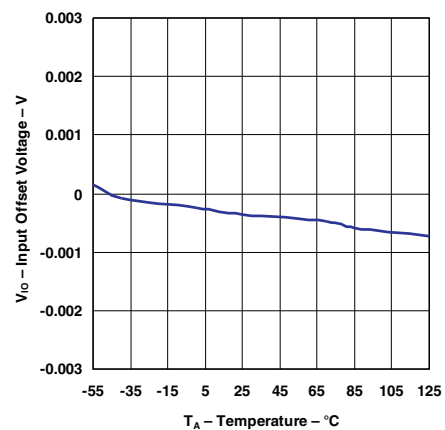
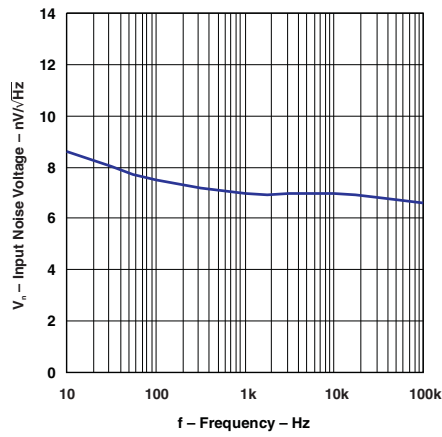


Figure 12. Input Offset Voltage vs Temperature ( $V_{CC} = \pm 15\text{ V}$ )

**Typical Characteristics (continued)**



**Figure 13. Input Noise Voltage vs Frequency**  
( $V_{CC} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ )

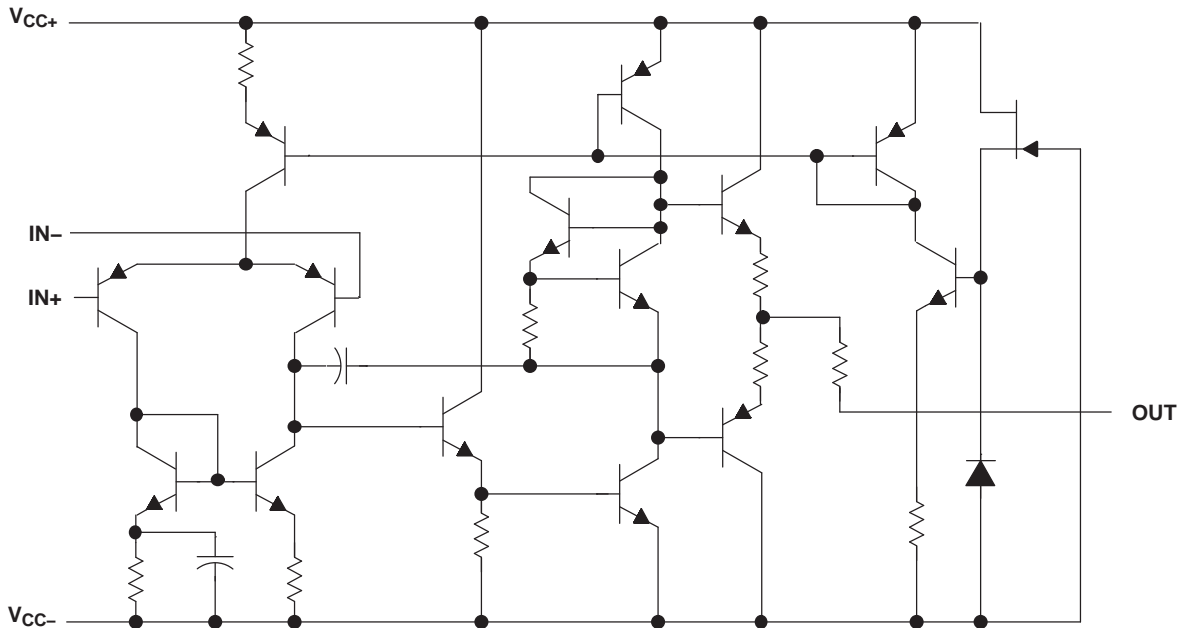
## 7 Detailed Description

### 7.1 Overview

The RC4558 device is a dual general-purpose operational amplifier, with each half electrically similar to the  $\mu$ A741, except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected, and the internal frequency compensation ensures stability without external components.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The RC4558 device has a 3-MHz unity-gain bandwidth.

#### 7.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage, then converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of the RC4558 device is 90 dB.

#### 7.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The RC4558 device has a 1.7 V/ $\mu$ s slew rate.

### 7.4 Device Functional Modes

The RC4558 device is powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

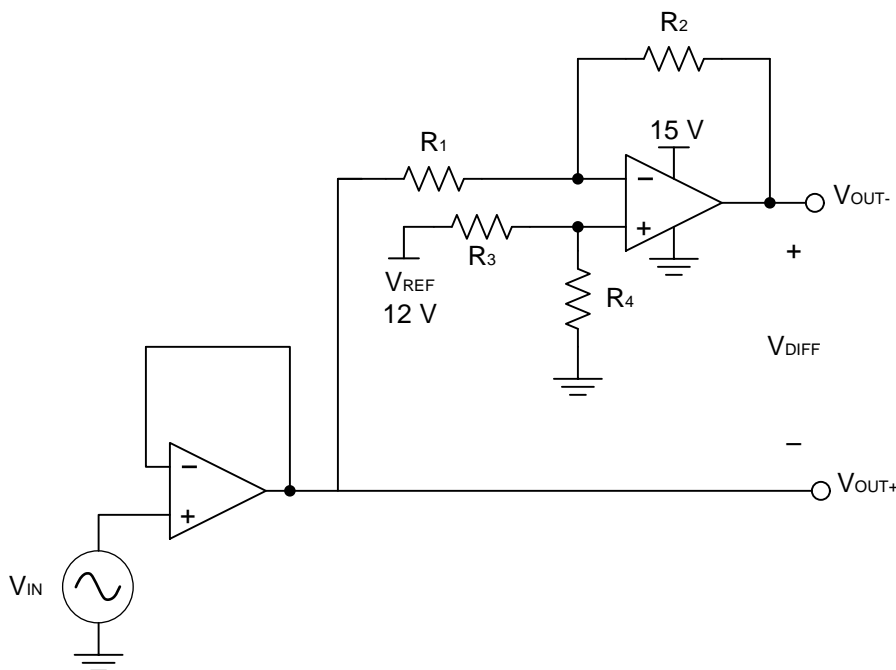
## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Typical Application

Some applications require differential signals. [Figure 14](#) shows a simple circuit to convert a single-ended input of 2 V to 10 V into differential output of  $\pm 8$  V on a single 15-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage,  $V_{OUT+}$ . The second amplifier inverts the input and adds a reference voltage to generate  $V_{OUT-}$ . Both  $V_{OUT+}$  and  $V_{OUT-}$  range from 2 V to 10 V. The difference,  $V_{DIFF}$ , is the difference between  $V_{OUT+}$  and  $V_{OUT-}$ .



**Figure 14. Schematic for Single-Ended Input to Differential Output Conversion**

## Typical Application (continued)

### 8.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15 V
- Reference voltage: 12V
- Input: 2 V to 10 V
- Output differential:  $\pm 8$  V

### 8.1.2 Detailed Design Procedure

The circuit in [Figure 14](#) takes a single-ended input signal,  $V_{IN}$ , and generates two output signals,  $V_{OUT+}$  and  $V_{OUT-}$  using two amplifiers and a reference voltage,  $V_{REF}$ .  $V_{OUT+}$  is the output of the first amplifier and is a buffered version of the input signal,  $V_{IN}$  (see [Equation 1](#)).  $V_{OUT-}$  is the output of the second amplifier which uses  $V_{REF}$  to add an offset voltage to  $V_{IN}$  and feedback to add inverting gain. The transfer function for  $V_{OUT-}$  is [Equation 2](#).

$$V_{OUT+} = V_{IN} \quad (1)$$

$$V_{OUT-} = V_{REF} \times \left( \frac{R_4}{R_3 + R_4} \right) \times \left( 1 + \frac{R_2}{R_1} \right) - V_{IN} \times \frac{R_2}{R_1} \quad (2)$$

The differential output signal,  $V_{DIFF}$ , is the difference between the two single-ended output signals,  $V_{OUT+}$  and  $V_{OUT-}$ . [Equation 3](#) shows the transfer function for  $V_{DIFF}$ . By applying the conditions that  $R_1 = R_2$  and  $R_3 = R_4$ , the transfer function is simplified into [Equation 6](#). Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the  $V_{REF}$ . The differential output range is  $2 \times V_{REF}$ . Furthermore, the common mode voltage will be one half of  $V_{REF}$  (see [Equation 7](#)).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left( 1 + \frac{R_2}{R_1} \right) - V_{REF} \times \left( \frac{R_4}{R_3 + R_4} \right) \left( 1 + \frac{R_2}{R_1} \right) \quad (3)$$

$$V_{OUT+} = V_{IN} \quad (4)$$

$$V_{OUT-} = V_{REF} - V_{IN} \quad (5)$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \quad (6)$$

$$V_{cm} = \left( \frac{V_{OUT+} + V_{OUT-}}{2} \right) = \frac{1}{2} V_{REF} \quad (7)$$

#### 8.1.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Because RC4558 has a bandwidth of 3 MHz, this circuit will only be able to process signals with frequencies of less than 3 MHz.

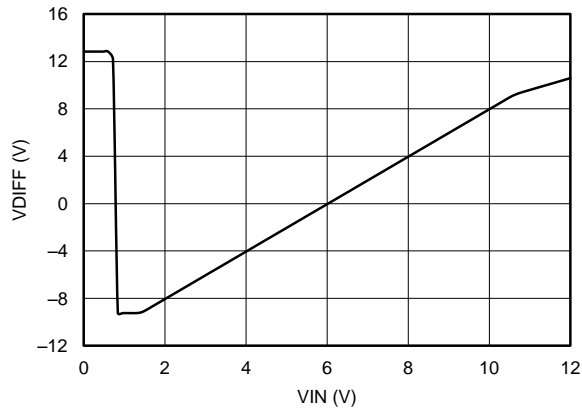
#### 8.1.2.2 Passive Component Selection

Because the transfer function of  $V_{OUT-}$  is heavily reliant on resistors ( $R_1$ ,  $R_2$ ,  $R_3$ , and  $R_4$ ), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 k $\Omega$  with tolerances measured to be within 2%. But, if the noise of the system is a key parameter, the user can select smaller resistance values (6 k $\Omega$  or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

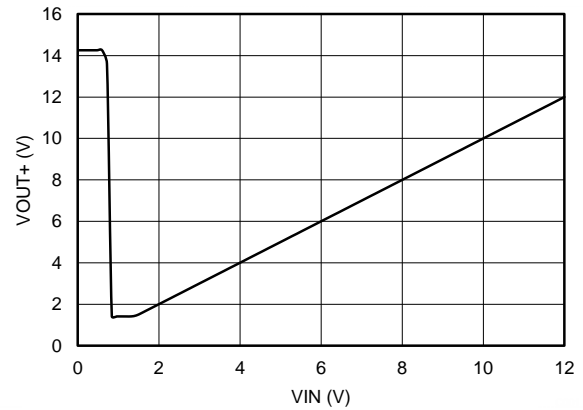
## Typical Application (continued)

### 8.1.3 Application Curves

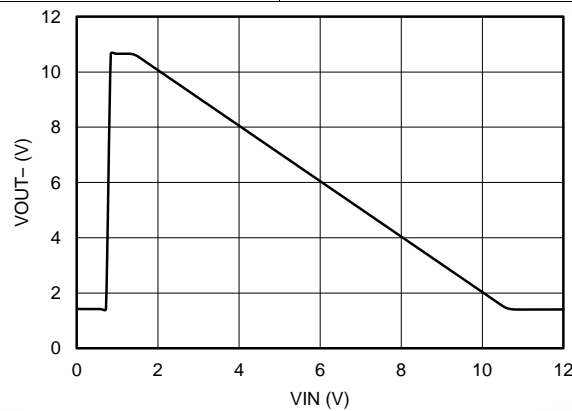
The measured transfer functions in [Figure 15](#), [Figure 16](#), and [Figure 17](#) were generated by sweeping the input voltage from 0 V to 12 V. However, this design should only be used between 2 V and 10 V for optimum linearity.



**Figure 15. Differential Output Voltage Node vs Input Voltage**



**Figure 16. Positive Output Voltage Node vs Input Voltage**



**Figure 17. Positive Output Voltage Node vs Input Voltage**

## 9 Power Supply Recommendations

The RC4558 device is specified for operation from  $\pm 5$  V to  $\pm 15$  V; many specifications apply from  $-0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

### CAUTION

Supply voltages outside of the  $\pm 18$ -V range can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout Guidelines](#).

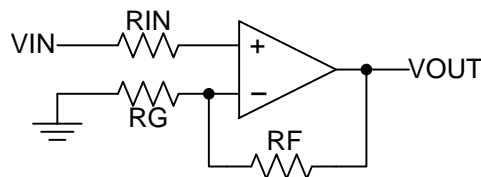
## 10 Layout

### 10.1 Layout Guidelines

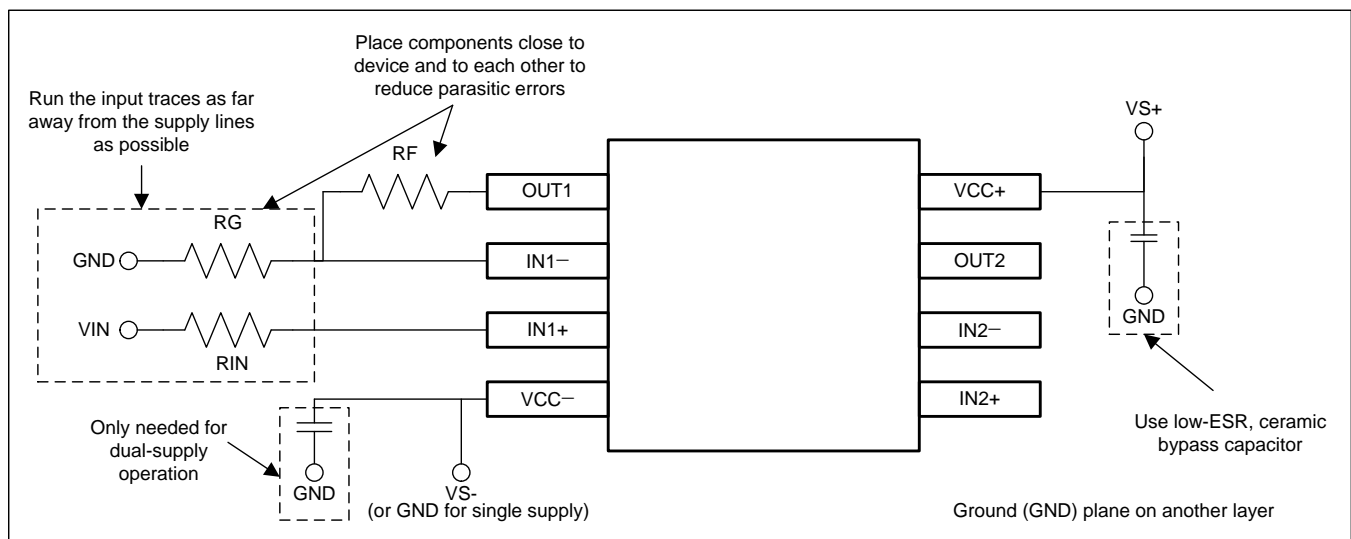
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, ([SLOA089](#)).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 10.2 Layout Example



**Figure 18. Operational Amplifier Schematic for Noninverting Configuration**



**Figure 19. Operational Amplifier Board Layout for Noninverting Configuration**

## 11 Device and Documentation Support

### 11.1 Trademarks

All trademarks are the property of their respective owners.

### 11.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RC4558DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(YRP, YRS, YRU)	<a href="#">Samples</a>
RC4558DGKRG4	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	0 to 70		<a href="#">Samples</a>
RC4558DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	RC4558	<a href="#">Samples</a>
RC4558IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YSP, YSS, YSU)	<a href="#">Samples</a>
RC4558IDGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YSP, YSS, YSU)	
RC4558IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4558I	<a href="#">Samples</a>
RC4558IDRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4558I	
RC4558IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	RC4558IP	<a href="#">Samples</a>
RC4558IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	R4558I	<a href="#">Samples</a>
RC4558P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	RC4558P	<a href="#">Samples</a>
RC4558PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	R4558	<a href="#">Samples</a>
RC4558PSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	R4558	<a href="#">Samples</a>
RC4558PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	R4558	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

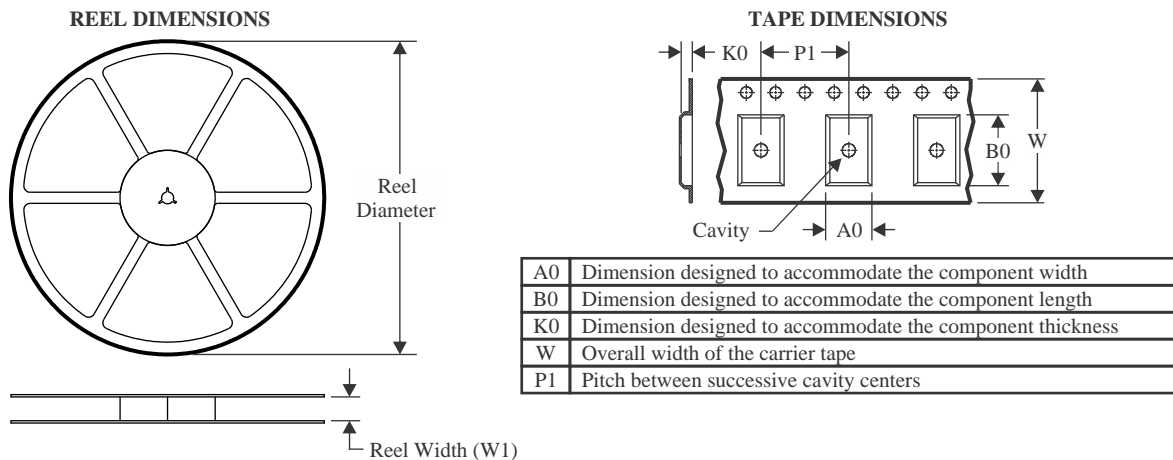
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4558DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
RC4558DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
RC4558IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
RC4558IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
RC4558PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
RC4558PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
RC4558PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4558DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
RC4558DR	SOIC	D	8	2500	340.5	338.1	20.6
RC4558DRG3	SOIC	D	8	2500	364.0	364.0	27.0
RC4558DRG4	SOIC	D	8	2500	340.5	338.1	20.6
RC4558IDGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
RC4558IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
RC4558IDR	SOIC	D	8	2500	340.5	338.1	20.6
RC4558IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
RC4558PSR	SO	PS	8	2000	356.0	356.0	35.0
RC4558PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
RC4558PWR	TSSOP	PW	8	2000	364.0	364.0	27.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
RC4558D	D	SOIC	8	75	507	8	3940	4.32
RC4558D	D	SOIC	8	75	506.6	8	3940	4.32
RC4558DE4	D	SOIC	8	75	506.6	8	3940	4.32
RC4558DE4	D	SOIC	8	75	507	8	3940	4.32
RC4558ID	D	SOIC	8	75	507	8	3940	4.32
RC4558IP	P	PDIP	8	50	506	13.97	11230	4.32
RC4558IP	P	PDIP	8	50	506	13.97	11230	4.32
RC4558IPW	PW	TSSOP	8	150	530	10.2	3600	3.5
RC4558P	P	PDIP	8	50	506	13.97	11230	4.32
RC4558PW	PW	TSSOP	8	150	530	10.2	3600	3.5

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

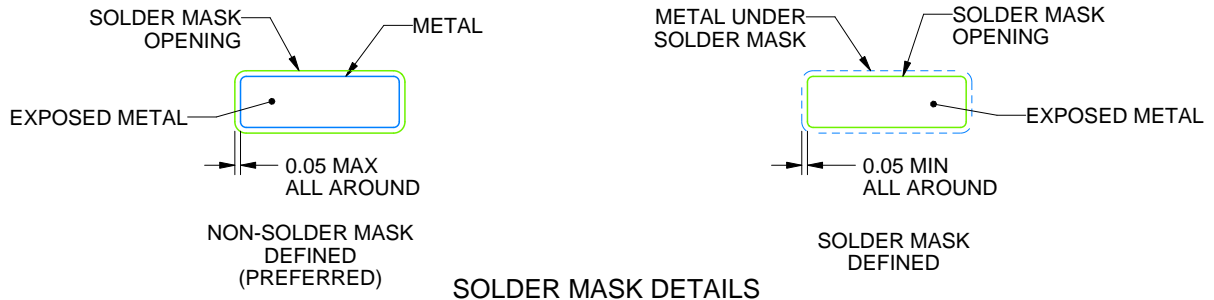
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

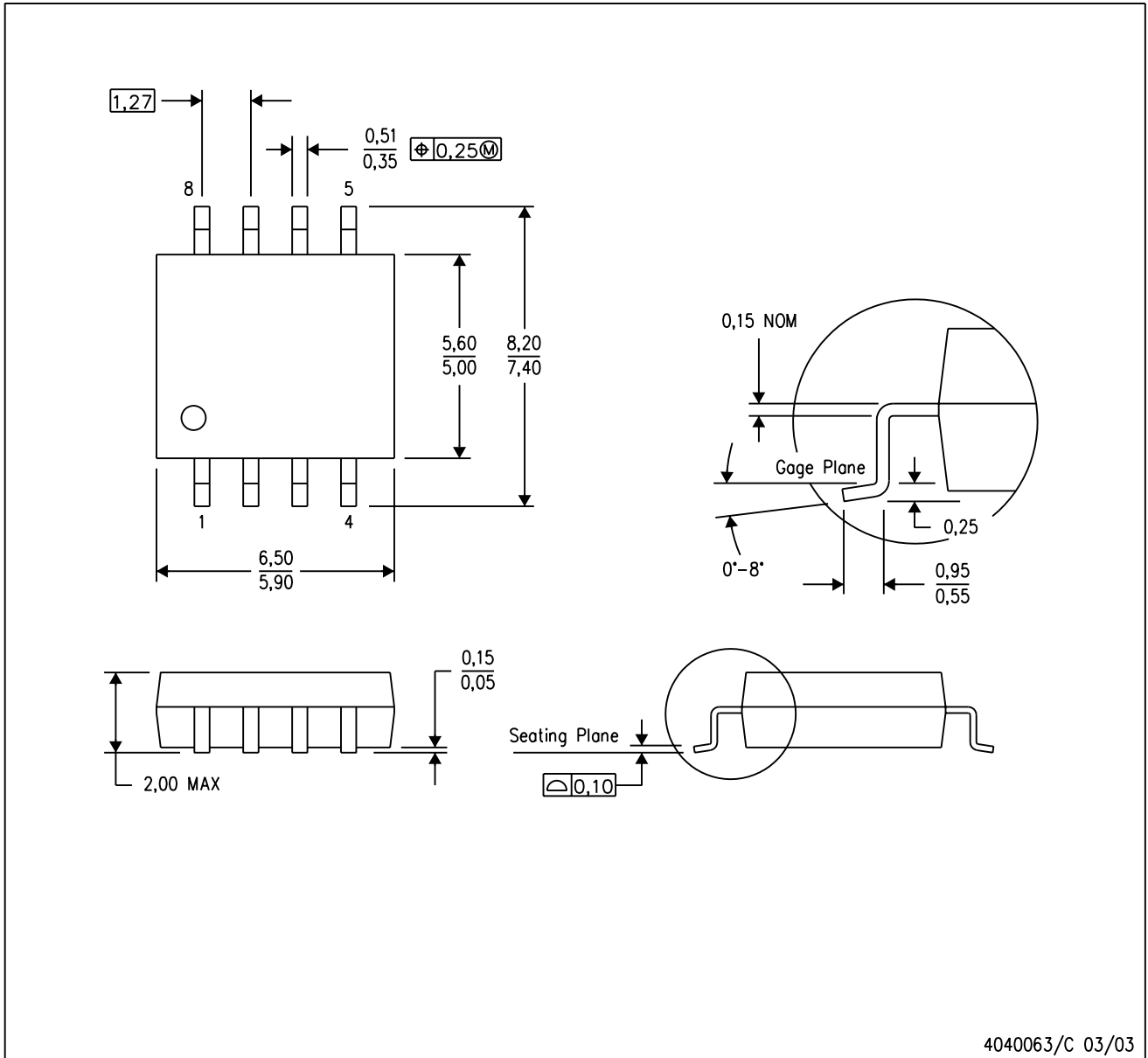
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

PS (R-PDSO-G8)

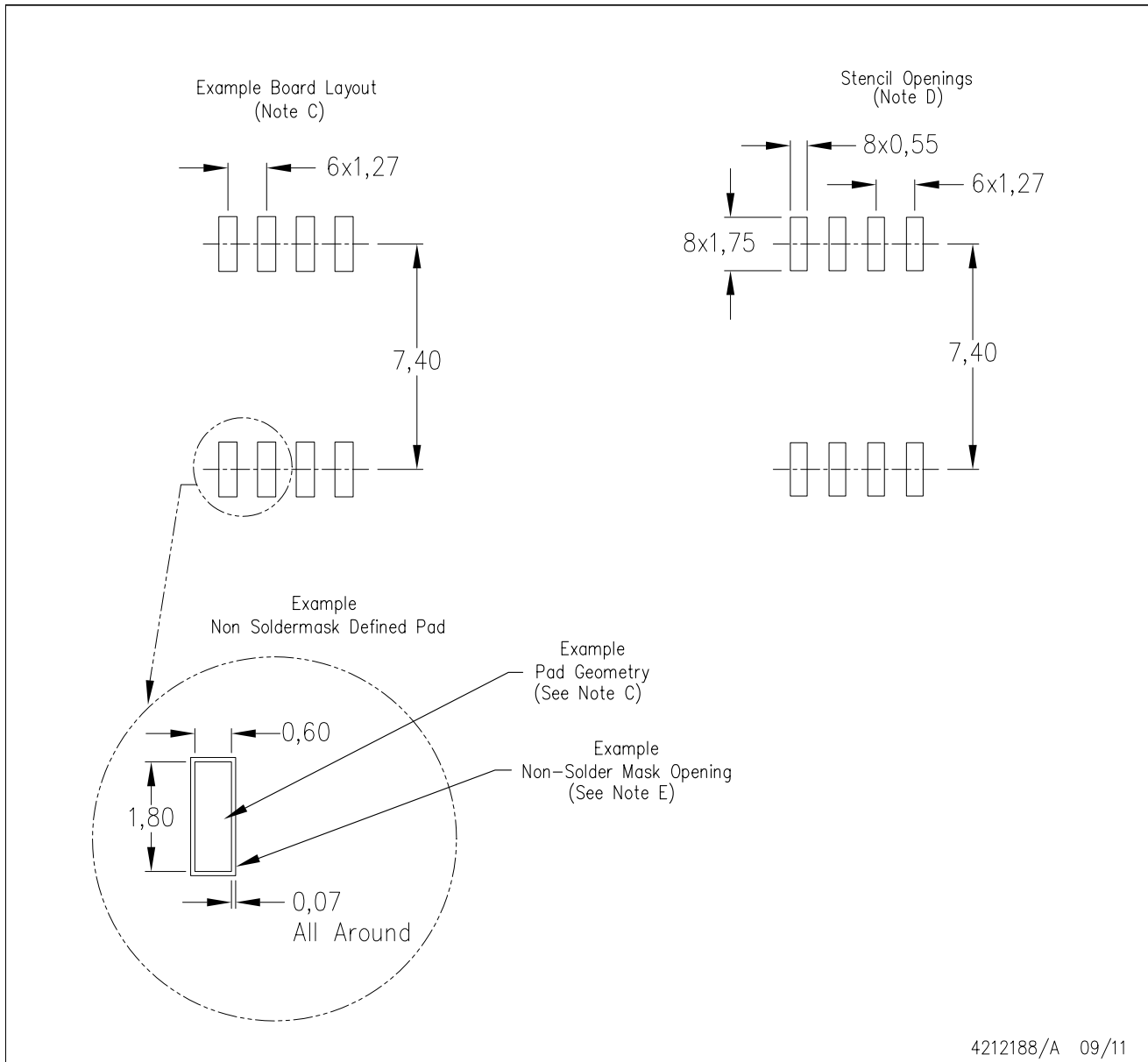
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

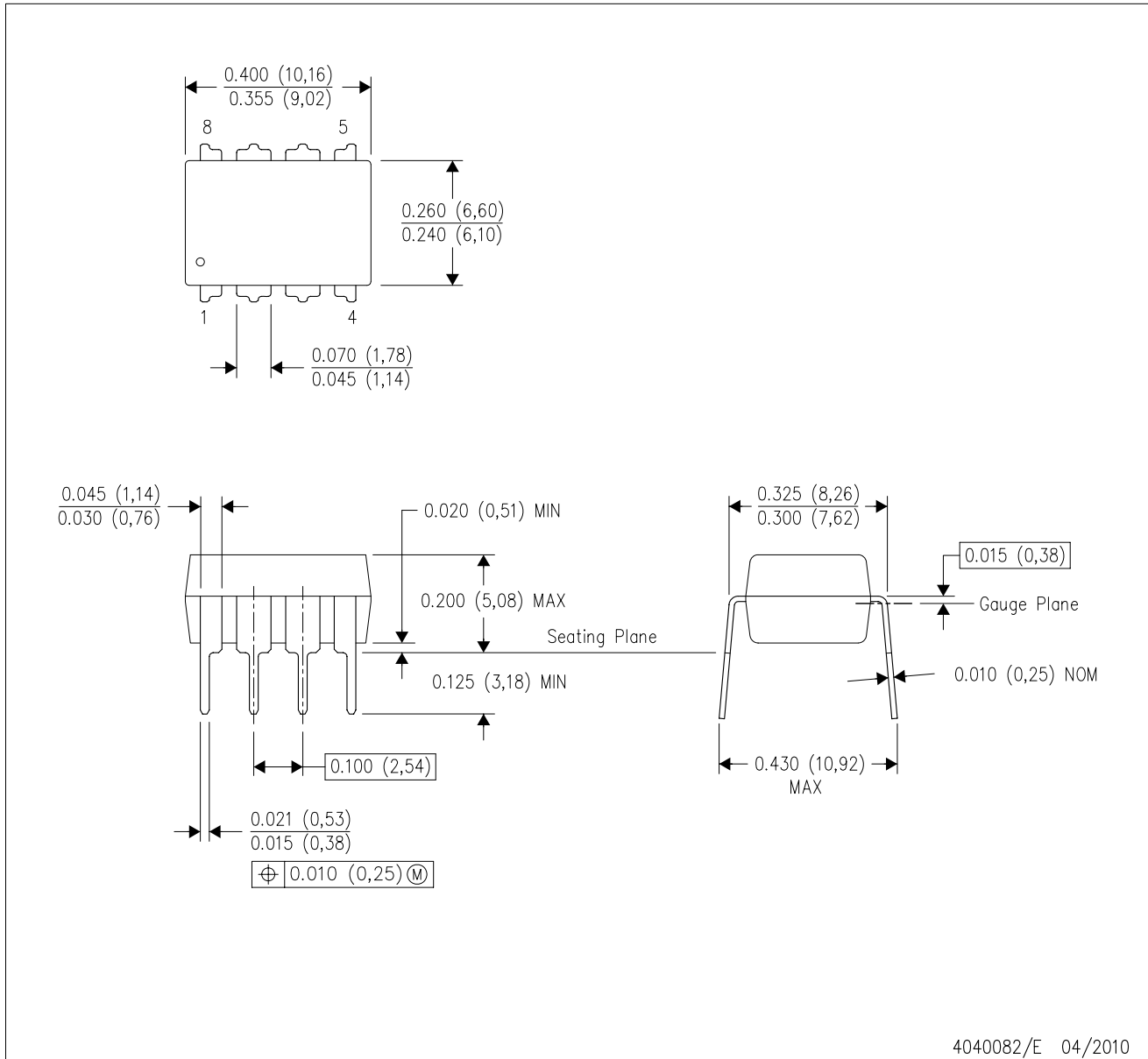
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



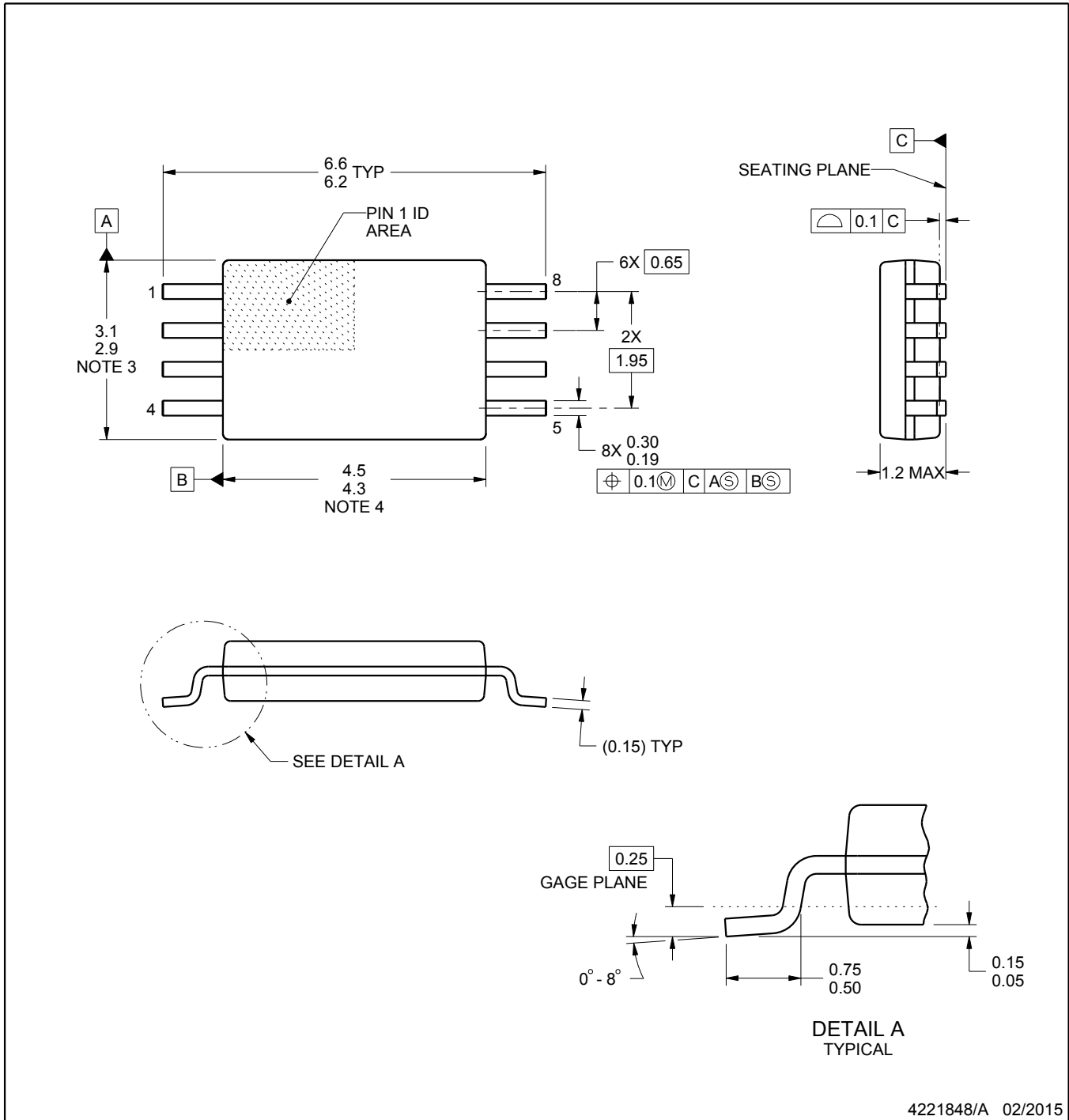
4040082/E 04/2010

PW0008A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

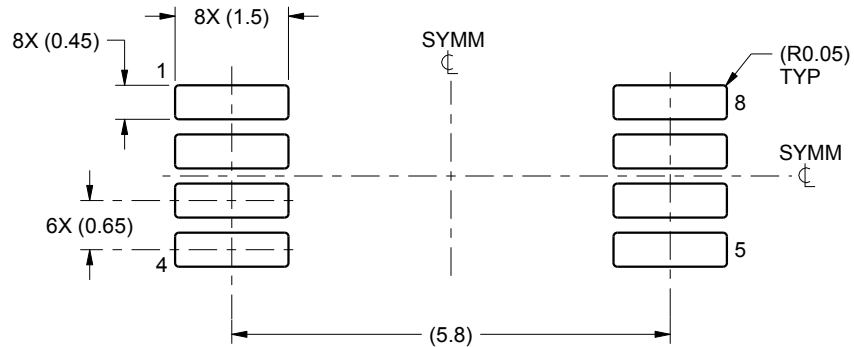
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

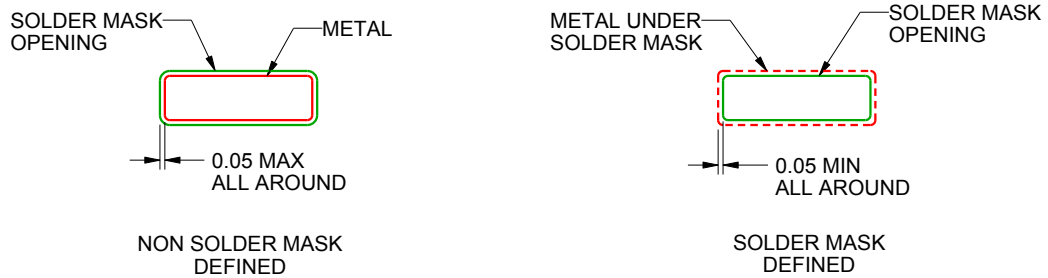
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

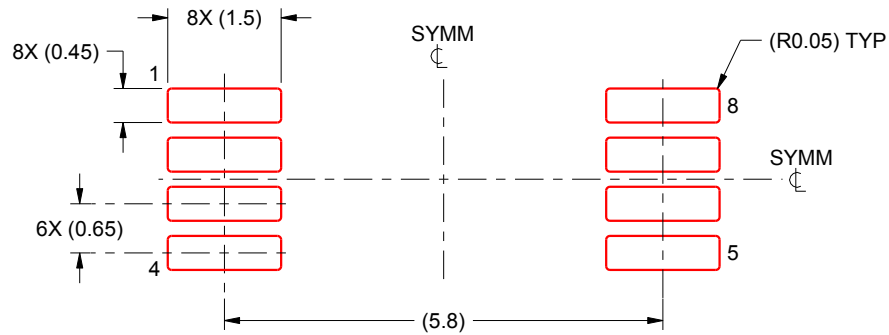
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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