THE DATASHEET OF

5V9885TPFGI

3.3V EEPROM PROGRAMMABLE CLOCK GENERATOR

IDT5V9885T

FEATURES:

- **Three internal PLLs**
- **Internal non-volatile EEPROM**
- **JTAG and FAST mode I²C serial interfaces**
- **Input Frequency Ranges: 1MHz to 400MHz**
- **Output Frequency Ranges: 4.9kHz to 500MHz**
- **Reference Crystal Input with programmable oscillator gain and programmable linear load capacitance**
  - *Crystal Frequency Range: 8MHz to 50MHz*
- **Each PLL has an 8-bit pre-scaler and a 12-bit feedback-divider**
- **10-bit post-divider blocks**
- **Fractional Dividers**
- **Two of the PLLs support Spread Spectrum Generation capability**
- **I/O Standards:**
  - *Outputs - 3.3V LVTTL/ LVCMOS, LVPECL, and LVDS*
  - *Inputs - 3.3V LVTTL/ LVCMOS*
- **Programmable Slew Rate Control**
- **Programmable Loop Bandwidth Settings**
- **Programmable output inversion to reduce bimodal jitter**
- **Redundant clock inputs with glitchless auto and manual switchover options**
- **JTAG Boundary Scan**
- **Individual output enable/disable**
- **Power-down mode**
- **3.3V V_{DD}**
- **Available in TQFP and VFQFPN packages**

DESCRIPTION:

The IDT5V9885T is a programmable clock generator intended for high performance data-communications, telecommunications, consumer, and networking applications. There are three internal PLLs, each individually programmable, allowing for three unique non-integer-related frequencies. The frequencies are generated from a single reference clock. The reference clock can come from one of the two redundant clock inputs. A glitchless automatic or manual switchover function allows any one of the redundant clocks to be selected during normal operation.

The IDT5V9885T can be programmed through the use of the I²C or JTAG interfaces. The programming interface enables the device to be programmed when it is in normal operation or what is commonly known as in-system programmable. An internal EEPROM allows the user to save and restore the configuration of the device without having to reprogram it on power-up. JTAG boundary scan is also implemented.

Each of the three PLLs has an 8-bit pre-scaler and a 12-bit feedback divider. This allows the user to generate three unique non-integer-related frequencies. The PLL loop bandwidth is programmable to allow the user to tailor the PLL response to the application. For instance, the user can tune the PLL parameters to minimize jitter generation or to maximize jitter attenuation. Spread spectrum generation and fractional divides are allowed on two of the PLLs.

There are 10-bit post dividers on five of the six output banks. Two of the six output banks are configurable to be LVTTL, LVPECL, or LVDS. The other four output banks are LVTTL. The outputs are connected to the PLLs via the switch matrix. The switch matrix allows the user to route the PLL outputs to any output bank. This feature can be used to simplify and optimize the board layout. In addition, each output's slew rate and enable/disable function can be programmed.

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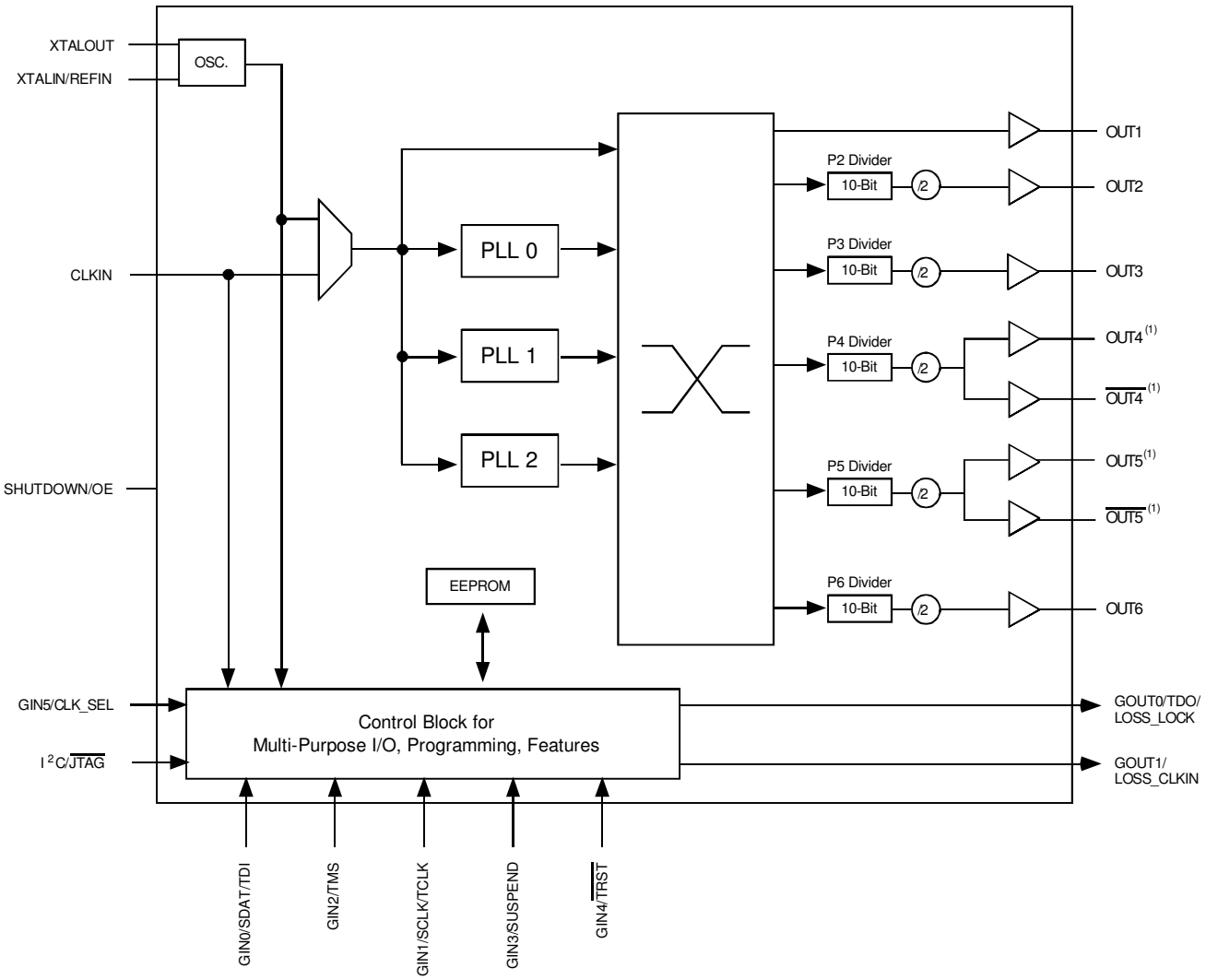
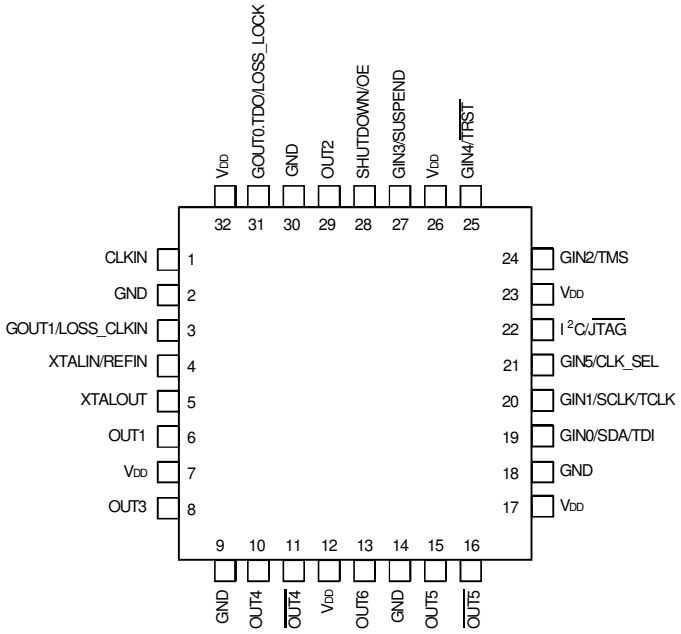
FUNCTIONAL BLOCK DIAGRAM

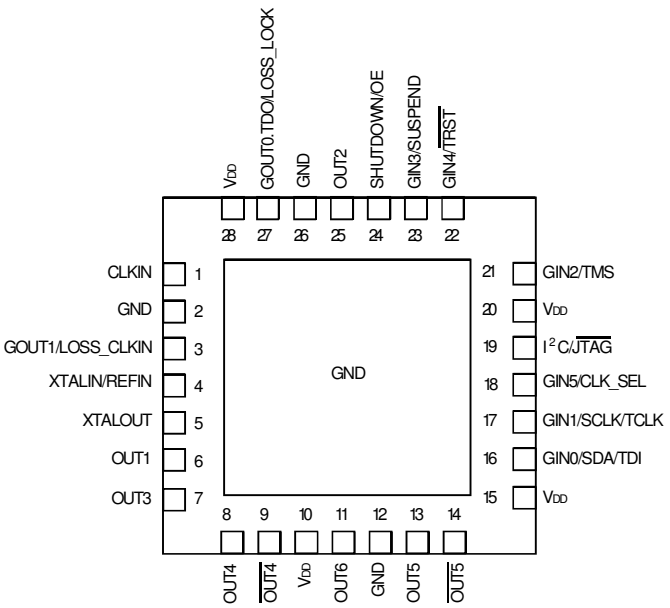


NOTE:
1. OUT4 and OUT5 pairs can be configured to be LVDS, LVPECL, or two single-ended LVTTL outputs. As LVTTL, OUT4 and OUT5 can be configured to be non-inverting.

PIN CONFIGURATION



TQFP
TOP VIEW



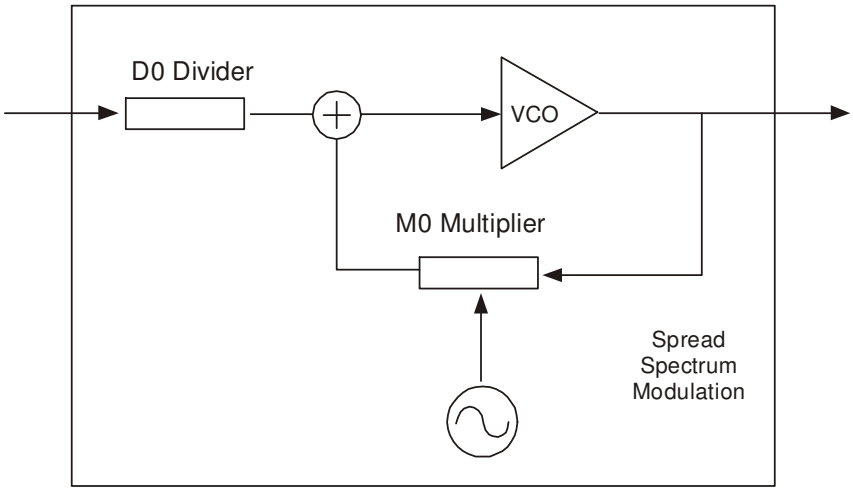
VFQFPN
TOP VIEW

PIN DESCRIPTION

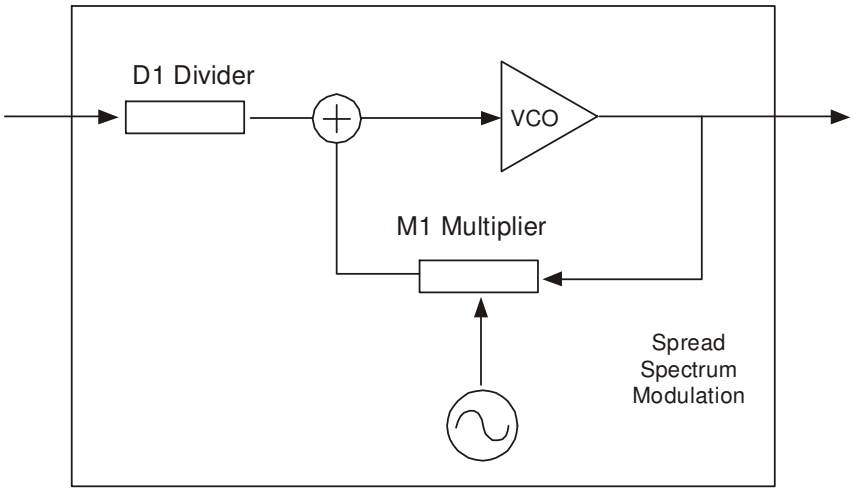
Pin Name	PF32 Pin#	NL28 Pin#	I/O	Type	Description
CLKIN	1	1	I	LVTTL	Input Clock
XTALIN/REFIN	4	4	I	LVTTL	CRYSTAL_IN - Reference crystal input or external reference clock input
XTALOUT	5	5	O	LVTTL	CRYSTAL_OUT -Reference crystal feedback
GIN0/SDAT/TDI	19	16	I	LVTTL(1,2)	Multi-purpose inputs. Can be used for Frequency Control, SDAT(I^2C), or TDI(JTAG).
GIN1/SCLK/TCK	20	17	I	LVTTL(1,2)	Multi-Purpose inputs. Can be used for Frequency Control, SCLK(I^2C), or TCK(JTAG).
GIN2/TMS	24	21	I	LVTTL(1,2)	Multi-Purpose inputs. Can be used for Frequency Control or TMS (JTAG)
GIN3/SUSPEND	27	23	I	LVTTL(1,2)	Multi-Purpose inputs. Can be used for Frequency Control or as a suspend mode control input (active HIGH).
GIN4/TRST	25	22	I	LVTTL(1,2)	Multi-Purpose inputs. Can be used for Frequency Control or TRST (JTAG)
GIN5/CLK_SEL	21	18	I	LVTTL(1,2)	Multi-Purpose inputs. Can be used for Frequency Control or input clock selector.
SHUTDOWN/OE	28	24	I	LVTTL(1,2)	Enables/disables the outputs or powers down the chip. The SP bit (0x1C) controls the polarity of the signal to be either active HIGH or LOW. (Default is active HIGH.)
I^2C/$\overline{JTAG}$	22	19	I	3-level(3)	I^2C (HIGH) or MFC Mode (MID) or JTAG Programming (LOW)
OUT1	6	6	O	LVTTL	Configurable clock output 1. Can also be used to buffer the reference clock.
OUT2	29	25	O	LVTTL	Configurable clock output 2
OUT3	8	7	O	LVTTL	Configurable clock output 3
OUT4	10	8	O	Adjustable(4)	Configurable clock output 4, Single-Ended or Differential when combined with OUT4
OUT4	11	9	O	Adjustable(4)	Configurable complementary clock output 4, Single-Ended or Differential when combined with OUT4
OUT5	15	13	O	Adjustable(4)	Configurable clock output 5, Single-Ended or Differential when combined with OUT5
OUT5	16	14	O	Adjustable(4)	Configurable complementary clock output 5, Single-Ended or Differential when combined with OUT5
OUT6	13	11	O	LVTTL	Configurable clock output 6
GOUT0/TDO/LOSS_LOCK	31	27	O	LVTTL(1)	Multi-Purpose Output. Can be programmed to use as PLL LOCK signal, LOSS_LOCK or TDO in JTAG mode
GOUT1/LOSS_CLKIN	3	3	O	LVTTL	Multi-Purpose Output. Can be programmed to use as LOSS_CLKIN
V_{DD}	7,12,17, 23,26,32	10,15,20 28			3.3V Power Supply
GND	2,9,14, 18,30	2,12,26			Ground

NOTES:
1. The JTAG (TDO, TMS, TCLK, TRST, and TDI) and I^2C (SCLK and SDAT) signals share the same pins with GIN signals.
2. Weak internal 100KΩ pull-down resistor.
3. 3-level inputs are static inputs and must be tied to V_{DD} or GND or left floating. These inputs are internally biased to $V_{DD}/2$. They are not hot-insertable or over voltage tolerant.
4. Outputs are user programmable to drive single-ended 3.3V LVTTL, differential LVDS, or differential LVPECL interface levels.

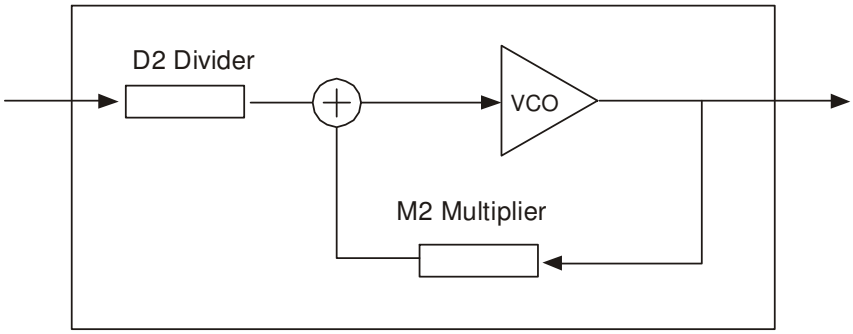
PLL FEATURES AND DESCRIPTIONS



PLL0 Block Diagram



PLL1 Block Diagram



PLL2 Block Diagram

	Pre-Divider (D) Values	Multiplier (M) Values	Programmable Loop Bandwidth	Spread Spectrum Generation Capability
PLL0	1 - 255	2 - 8190	yes	yes
PLL1	1 - 255	2 - 8190	yes	yes
PLL2	1 - 255	1 - 4095	yes	no

REFERENCE CLOCK INPUT PINS AND SELECTION

The 5V9885T supports up to two clock inputs. One of the clock inputs (XTALIN/ REFIN) can be driven by either an external crystal or a reference clock. The second clock input (CLKIN) can only be driven from an external reference clock. Either clock input can be set as a the primary clock. The primary clock designation is to establish which is the main reference clock to the PLLs. The non-primary clock is designated as the secondary clock in case the primary clock goes absent and a backup is needed. The PRIMCLK bit (0x34) determines which clock input will be the primary clock. When PRIMCLK bit is "0", it will select XTALIN/REFIN as the primary, and when "1", it will select CLKIN as the primary. The two external reference clocks can be manually selected using the GIN5/CLK_SEL pin, except in Manual Frequency Control (MFC) mode 2, or via programming by hard wiring the CLK_SEL pin and toggling the PRIMCLK bit. For more details on the MFC modes, refer to the CONFIGURING MULTI-PURPOSE I/Os section. When CLK_SEL is LOW, the primary clock is selected and when HIGH, the secondary clock is selected. The SM bits (0x34) must be set to "0x" for manual switchover which is detailed in SWITCHOVER MODES section.

GIN5/CLK_SEL	Selected Clock Input
L	Primary
H	Secondary

Crystal Input (XTALIN/REFIN)

The crystal oscillators should be fundamental mode quartz crystals: overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 50Ωmaximum equivalent series resonance.

When the XTALIN/REFIN pin is driven by a crystal, it is important to set the internal oscillator inverter drive strength and internal tuning/load capacitor values correctly to achieve the best clock performance. These values are programmable through either I^2C or JTAG interface to allow for maximum compatibility with crystals from various manufacturers, processes, performances, and qualities. The internal load capacitors are true parallel-plate capacitors for ultra-linear performance. Parallel-plate capacitors were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. External non-linear crystal load capacitors should not be used for applications that are sensitive to absolute frequency requirements. The value of the internal load capacitors are determined by XTALCAP[7:0] bits, (0x07). The load capacitance can be set with a resolution of 0.125 pF for a total crystal load range of 3.5pF to 35.5pF. This value should be set to two times the crystal load capacitance value stated by the vendor, subtracting out board capacitance value. Check with the vendor's crystal load capacitance specification for the exact setting to tune the internal load capacitor. The following equation governs how the total internal load capacitance is set.

Ex.: For crystal capacitance = 12pF
For board capacitance = 3pF each leg
XTALCAP = 2x [12-3] = 18pF

XTAL load cap = 3.5pF + XTALCAP[7:0] * 0.125pF (Eq. 1)

Parameter	Bits	Step	Min	Max	Units
XTALCAP	8	0.125	0	32	pF

When using an external reference clock instead of a crystal on the XTAL/ REFIN pin, the input load capacitors may be completely bypassed. This allows for the input frequency to be up to 200MHz. When using an external reference clock, the XTALOUT pin must be left floating, XTALCAP must be programmed to the default value of "0", and crystal drive strength bit, XDRV (0x06), must be set to the default value of "11".

CLKIN Pin

CLKIN pin is a regular clock input pin, and can be driven up to 400MHz.

PRE-SCALER, FEEDBACK-DIVIDER, AND POST-DIVIDER

Each PLL incorporates an 8-bit pre-scaler and a 12-bit feedback divider which allows the user to generate three unique non-integer-related frequencies. For output banks OUT2-OUT6, each bank has a 10-bit post-divider. The following equation governs how the frequency on output banks OUT2-6 is calculated.

$$F_{OUT} = \frac{F_{IN} * \left(\frac{M}{D}\right)}{P * 2} \qquad \text{(Eq. 2)}$$

Where F_{IN} is the reference frequency, M is the total feedback-divider value, D is the pre-scaler value, P is the total post-divider value, and F_{OUT} is the resulting output bank frequency. The value 2 in the denominator is due to the divide-by-2 on each of the output banks OUT2-6. Note that OUT1 does not have any type of post-divider. Also, programming any of the dividers may cause glitches on the outputs.

Pre-Scaler

D[7:0] are the bits used to program the pre-scaler for each PLL, D0 for PLL0, D1 for PLL1, and D2 for PLL2. The pre-scalers divide down the reference clock with integer values ranging from 1 to 255. To maintain low jitter, the divided down clock must be higher than 400KHz; it is best to use the smallest D divider value possible. If D is set to '0x00', then this will power down the PLL and all the outputs associated with that PLL.

Feedback-Divider

N[11:0] and A[3:0] are the bits used to program the feedback-divider for PLL0 (N0 and A0) and PLL1 (N1 and A1). If spread spectrum generation is enabled for either PLL0 or PLL1, then the SS_OFFSET[5:0] bits (0x61, 0x69) would be factored into the overall feedback divider value. See the SPREAD SPECTRUM GENERATION section for more details on how to configure PLL0 and PLL1 when spread spectrum is enabled. The two PLLs can also be configured for fractional divide ratios. See FRACTIONAL DIVIDER for more details. For PLL2, only the N[11:0] bits (N2) are used to program its feedback divider and there is no spread spectrum generation and fractional divides capability. The 12-bit feedback-divider integer values range from 1 to 4095.

The following equations govern how the feedback divider value is set. Note that the equations are different for PLL0/PLL1 and PLL2

PLL0 and PLL1:

M = 2*N[11:0] + A[3:0] + 1 + SS_OFFSET[5:0] * 1/64 (Eq. 3)

M = 2*N[11:0] + A[3:0] + 1 (spread spectrum disabled) (Eq. 4)

A[3:0] = 0000 = -1
= 0001 = 1
= 0010 = 2
= 0011 = 3
.
.
.
= 1111 = 15

Note: A[3:0] < (N[11:0] - 5), must be met when using A. N cannot be programmed with a value of 4, 8, or 16 when using A.

PLL2:

M = N[11:0] (Eq. 5)

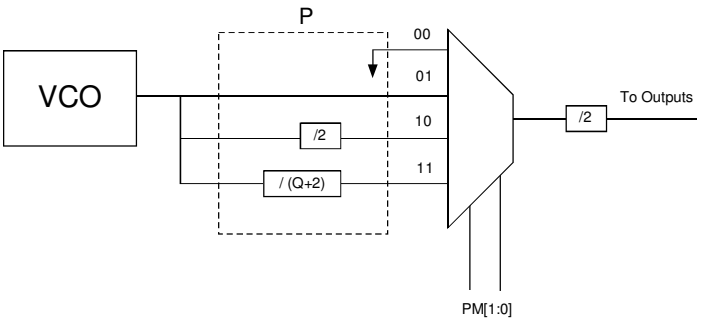
The user can achieve an even or odd integer divide ratio for both PLL0 and PLL1 by setting the A[3:0] bits accordingly and disabling the spread spectrum. A fractional divide can also be set for PLL0 and PLL1 by using the A[3:0] bits in conjunction with the SS_OFFSET[5:0] bits, which is detailed in the FRACTIONAL DIVIDER section. Note that the VCO has a frequency range of 10MHz to 1200MHz. To maintain low jitter, it is best to maximize the VCO frequency. For example, if the reference clock is 100MHz and a 200MHz clock is required, to achieve the best jitter performance, multiply the 100MHz by 12 to get the VCO running at the highest possible frequency of 1200MHz and then divide it down to get 200MHz. Or if the reference clock is 25MHz and 20MHz is the required clock, multiply the 25MHz by 40 to get the VCO running at 1000MHz and then divide it down to get 20MHz. If N is set to '0x00', the VCO will slew to the minimum frequency.

Post-Divider

Q[9:0] are the bits used to program the 10-bit post-dividers on output banks OUT2-6. OUT1 bank does not have a 10-bit post-divider or any other post-divide along its path. The 10-bit post-dividers will divide down the output banks' frequency with integer values ranging from 1 to 1023.

There is the option to choose between disabling the post-divider, utilizing a div/1, a div/2, or the 10-bit post-divider by using the PM[1:0] bits. Each bank, except for OUT1, has a set of PM bits. When disabling the post-divider, no clock will appear at the outputs, but will remain powered on. The values are listed in the table below.

PM[1:0]	P Post-Divider
00	disabled
01	div/1
10	div/2
11	Q[9:0] + 2 (Eq. 6)



Post-Divider Diagram

Note that the actual 10-bit post-divider value has a 2 added to the integer value Q and the outputs are routed through another div/2 block. The post-divider should never be disabled unless the output bank will never be used during normal operation. The output frequency range for LVTTL outputs are from 4.9KHz to 200MHz. The output frequency range for LVPECL/LVDS outputs are from 4.9KHz to 500MHz.

SPREAD SPECTRUM GENERATION

PLL0 and PLL1 support spread spectrum generation capability, which users have the option of turning on and off. Spread spectrum profile, frequency, and spread are fully programmable (within limits). The programmable spread spectrum generation parameters are TSSC[3:0], NSSC[3:0], SS_OFFSET[5:0], SD[3:0], DITH, and X2 bits. These bits are in the memory address range of 0x60 to 0x67 for PLL0 and 0x68 to 0x6F for PLL1. The spread spectrum generation on PLL0 & PLL1 can be enabled/disabled using the TSSC[3:0] bits. To enable spread spectrum, set TSSC > '0' and set NSSC, SD[3:0], SD[5:0], and the A[3:0] in the total M value accordingly. And to disable, set TSSC = '0'.

TSSC[3:0]
These bits are used to determine the number of phase/frequency detector cycles per spread spectrum cycle (ssc) steps. The modulation frequency can be calculated with the TSSC bits in conjunction with the NSSC bits. Valid TSSC integer values for the modulation frequency range from 5 to 14.

NSSC[3:0]
These bits are used to determine the number of delta-encoded samples used for a single quadrant of the spread spectrum waveform. All four quadrants of the spread spectrum waveform are mirror images of each other. The modulation frequency is also calculated based off the NSSC bits in conjunction with the TSSC bits. Valid NSSC integer values range from 1 to 6.

SS_OFFSET[5:0]
These bits are used to program the fractional offset with respect to the nominal M integer value. For center spread, the SS_OFFSET should be set to '0' so the spread spectrum waveform is about the nominal M (Mnom) value. For down spread, the SS_OFFSET > '0' so the spread spectrum wavform is about the (Mideal -1 = Mnom) value. The downspread percentage can be thought of in terms of center spread. For example, a downspread of -1% can also be considered as a center spread of ±0.5% but with Mnom shifted down by one and offset. The SS_OFFSET has integer values ranging from 0 to 63.

SD[3:0]
These bits are used to shape the profile of the spread spectrum waveform. These are delta-encoded samples of the waveform. There are twelve sets of SD samples for each PLL. The NSSC bits determine how many of these samples are used for the waveform. The sum of these delta-encoded samples (sigma-delta-encoded samples) determine the amount of spread and should not exceed (63 - SS_OFFSET). The maximum spread is inversely proportional to the nominal M integer value.

DITH
This bit is for dithering the sigma-delta-encoded samples. This will randomize the least-significant bit of the input to the spread spectrum modulator. Set the bit to '1' to enable dithering.

X2
This bit will double the total value of the sigma-delta-encoded-samples which will increase the amplitude of the spread spectrum waveform by a factor of two. When X2 is '0', the amplitude remains nominal but if set to '1', the amplitude is increased by x2.

The following equations govern how the spread spectrum is set:

T_{SSC} = TSSC[3:0] + 2 (Eq. 7)

N_{SSC} = NSSC[3:0] * 2 (Eq. 8)

$SD[3:0]_K = S_{J+1}$(unencoded) - S_J(unencoded) (Eq. 9)
where S_J is the unencoded sample out of a possible 12 and SD_K is the delta-encoded sample out of a possible 12.

$$\text{Amplitude} = \frac{(2*N[11:0] + A[3:0] + 1) * \text{Spread\%} / 100}{2} \quad \text{(Eq. 10)}$$

if 1 < Amp < 2, then set X2 bit to '1'.

Modulation frequency:

$F_{PFD} = F_{IN} / D$ (Eq. 11)

$F_{VCO} = F_{PFD} * M_{NOM}$ (Eq. 12)

$F_{SSC} = F_{PFD} / (4 * Nssc * Tssc)$ (Eq. 13)

Spread:

$\Sigma\Delta = SD_0 + SD_1 + SD_2 + \ldots + SD_{11}$

the number of samples used depends on the N_{SSC} value

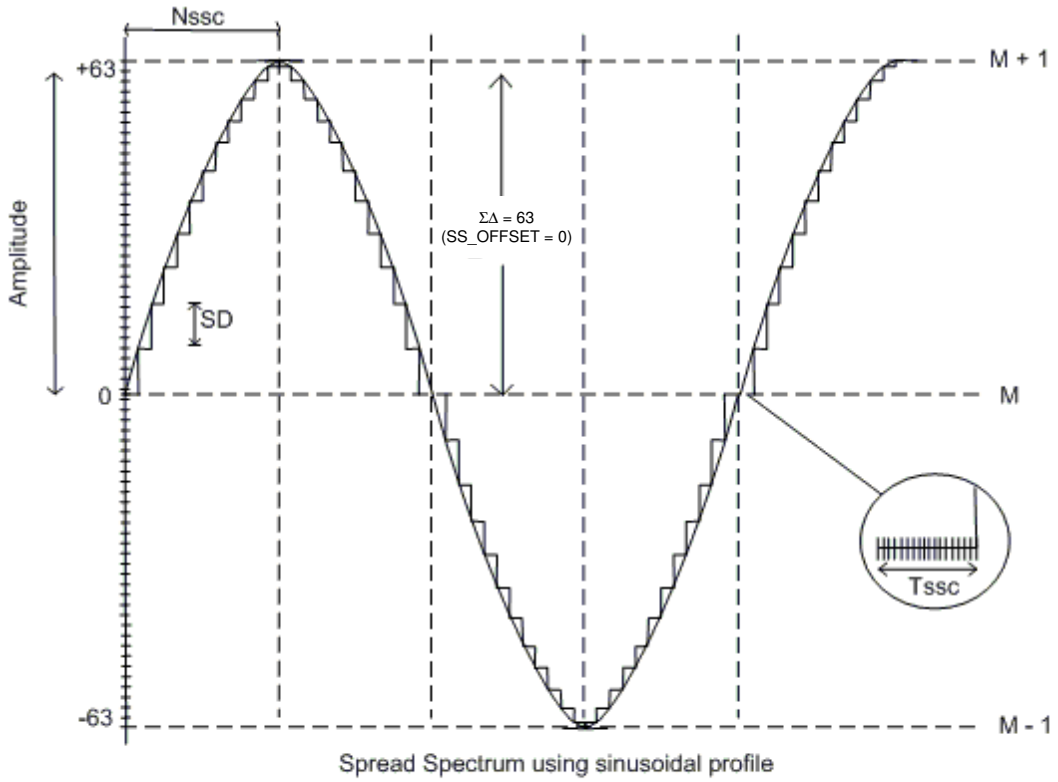
$\Sigma\Delta \leq 63 - SS_OFFSET$

$$\pm Spread\% = \frac{\Sigma\Delta * 100}{64 * (2*N[11:0] + A\{3:0\} + 1)} \quad \text{(Eq. 14)}$$

$\pm$Max Spread% / 100 = 1 / M_{NOM} or 2 / M_{NOM} (X2=1)

Profile:

Waveform starts with SS_OFFSET, SS_OFFSET + SD_J, SS_OFFSET + SD_{J+1}, etc.



Spread Spectrum Using Sinusoidal Profile

Example
F_{IN} = 25MHz, F_{OUT} = 100MHz, Fssc = 33KHz with center spread of ±2%. Find the necessary spread spectrum register settings.

Since the spread is center, the SS_OFFSET can be set to '0'. Solve for the nominal M value; keep in mind that the nominal M should be chosen to maximize the VCO. Start with D = 1, using Eq.10 and Eq.11.

M_{NOM} = 1200MHz / 25MHz = 48

Using Eq.4, we arbitrarily choose N = 22, A = 3. Now that we have the nominal M value, we can determine TSSC and NSSC by using Eq.12.

Nssc * Tssc = 25MHz / (33KHz * 4) = 190

However, using Eq. 7 and Eq.8, we find that the closest value is when TSSC = 14 and NSSC = 6. Keep in mind to maximize the number of samples used to enhance the profile of the spread spectrum waveform.

Tssc = 14 + 2 = 16
Nssc = 6 * 2 = 12
Nssc * Tssc = 192

Use Eq.14 to determine the value of the sigma-delta-encoded samples.

$$\pm 2\% = \frac{\Sigma\Delta * 100}{64 * 48}$$

$\Sigma\Delta$ = 61.44

Either round up or down to the nearest integer value. Therefore, we end up with 61 or 62 for sigma-delta-encoded samples. Since the sigma-delta-encoded samples must not exceed 63 with SS_OFFSET set to '0', 61 or 62 is well within the limits. It is the discretion of the user to define the shape of the profile that is better suited for the intended application.
Using Eq.14 again, the actual spread for the sigma-delta-encoded samples of 61 and 62 are ±1.99% and ±2.02%, respectively.

Use Eq.10 to determine if the X2 bit needs to be set;

$$\text{Amplitude} = \frac{48 * (1.99 \text{ or } 2.02) / 100}{2} = 0.48 < 1$$

Therefore, the X2 = '0 '. The dither bit is left to the discretion of the user.

The example above was of a center spread using spread spectrum. For down spread, the nominal M value can be set one integer value lower to 43.
Note that the 5V9885T should not be programmed with TSSC > '0', SS_OFFSET = '0', and SD = '0' in order to prevent an unstable state in the modulator. The PLL loop bandwidth must be at least 10x the modulation frequency along with higher damping (larger ω_{LZ}) to prevent the spread spectrum from being filtered and reduce extraneous noise. Refer to the LOOP FILTER section for more detail on ω_{LZ}. The A[3:0] must be used for spread spectrum, even if the total multiplier value is an even integer.

FRACTIONAL DIVIDER

There is the option for the feedback-divider to be programmed as a fractional divider for only PLL0 and PLL. By setting TSSC > '0' and SD bits to '0', the SS_OFFSET bits would determine the fractional divide value. See the SPREAD SPECTRUM GENERATION section for more details on the TSSC, SD, and SS_OFFSET bits. The following equation governs how the fractional divide value is set.

M = 2*N[11:0] + A[3:0] + 1 + SS_OFFSET[5:0] *1/64

The spread spectrum parameters such as the modulation frequency and profile will not be enabled nor will it have any impact on the PLL output when the PLL is programmed for fractional divide.

The following is an example of how to set the fractional divider.

Example

F_{IN} = 20MHz, $F_{OUT}1$ = 168.75MHz, $F_{OUT}2$ = 350MHz

Solving for 350MHz using Eq.2 and Eq.3 with PLL0 and spread spectrum off,

350MHz = 20MHz * (M / D)/ (P * 2)

For better jitter performance, keep D as small as possible

(350MHz * 2/20MHz)= (M/P) = 35

Therefore, we have D = 1, M = 35 (N = 16, A = 2) for PLL0 with P = 1 on output bank4 resulting in 350MHz.

Solving for 168.75MHz with PLL1 and fractional divide enabled:

168.75MHz = 20MHz * (M / D)/(P * 2)

168.75MHz * 2/20MHz = M/P = 16.875/1 or 33.75/2

The 33.75 value is chosen to achieve the highest VCO frequency possible. Next step is to figure out the setting for the fractional divide using Eq.3.

33.75 = 2*N + A + 1 + SS_OFFSET * 1/64

Integer value 33 can be determined by N and A, thus leaving 0.75 left to be solved.

2*N + A + 1 = 33
SS_OFFSET = 64 * 0.75 = 48

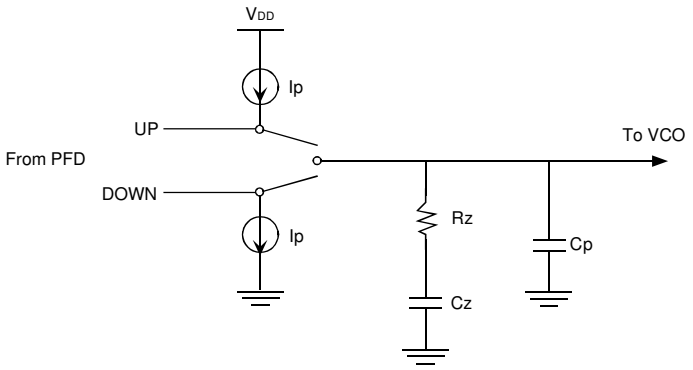
Therefore, we have D=1, M=33.75 (N=15, A=2, SS_OFFSET=48) for PLL1 with P=2 on an output bank resulting in 168.75MHz.

The fractional divider can be determined if it is needed by following the steps in the previous example. Note that the 5V9885T should not be programmed with TSSC > '0', SS_OFFSET = '0', and SD = '0' in order to prevent an unstable state in the modulator. The A[3:0] must be used and set to be greater than '2' for a more accurate fractional divide.

LOOP FILTER

The loop filter for each PLL can be programmed to optimize the jitter performance. The low-pass frequency response of the PLL is the mechanism that dictates the jitter transfer characteristics. The loop bandwidth can be extracted from the jitter transfer. A narrow loop bandwidth is good for jitter attenuation while a wide loop bandwidth is best for low jitter generation. The specific loop filter components that can be programmed are the resistor via the RZ[3:0] bits, pole capacitor via the CZ[3:0] bits, zero capacitor via the CP[3:0] bits, and the charge pump current via the IP[2:0] bits.

The following equations govern how the loop filter is set.



Charge Pump and Loop Filter Configuration

Resistor (Rz) = 0.3KΩ + RZ[3:0] * 1KΩ (Eq. 15)

Zero capacitor (Cz) = 6pF + CZ[3:0] * 27.2pF (Eq. 16)

Pole capacitor (Cp) = 1.3pF + CP[3:0] * 0.75pF (Eq. 17)

Charge pump current (Ip) = $5 * 2^{IP[2:0]}$ µA (Eq. 18)

Parameter	Bits	Step	Min	Max	Units
RZ	4	1	0.3	15.3	K Ω
CZ	4	27.2	6	414	pF
CP	4	0.75	1.3	12.55	pF
IP	3	2^n	5	640	µA

PLL loop filter design is beyond the scope of this datasheet. Refer to design procedures for 3-order charge-pump based PLLs. For the sake of simplicity, the fastest and easiest way to calculate the PLL loop bandwidth (Fc) given the programmable loop filter parameters is as follows.

PLL Loop Bandwidth:

Charge pump gain ($K\phi$) = Ip / 2π (Eq. 19)

VCO gain (K_{VCO}) = 950MHz/V * 2π (Eq. 20)

M = Total multiplier value (See the PRE-SCALERS, FEEDBACK-DIVIDERS, POST-DIVIDERS section for more detail)

$$\omega c = \frac{Rz * K\phi * K_{VCO} * Cz}{M * (Cz + Cp)} \quad \text{(Eq. 21)}$$

$$Fc = \omega c / 2\pi \quad \text{(Eq. 22)}$$

Note, the phase/frequency detector frequency (F_{PFD}) is typically seven times the PLL closed-loop bandwidth (Fc) but too high of a ratio will reduce your phase margin thus compromising loop stability.

To determine if the loop is stable, the phase margin (ωm) would need to be calculated as follows.

Phase Margin:

$\omega z = 1 / (Rz * Cz)$ (Eq. 23)

$\omega p = \frac{Cz + Cp}{Rz * Cz * Cp}$ (Eq. 24)

$\phi m = (360 / 2\pi) * [\tan^{-1}(\omega c / \omega z) - \tan^{-1}(\omega c / \omega p)]$ (Eq. 25)

To ensure stability in the loop, the phase margin is recommended to be > 60° but too high will result in the lock time being excessively long. Certain loop filter parameters would need to be compromised to not only meet a required loop bandwidth but to also maintain loop stability.

Example

Fc = 150KHz is the desired loop bandwidth. The total M value is 850. The ratio of $\omega p/\omega c$ should be at least 4. A rule of thumb that will help to aid the way, the $\omega p / \omega c$ ratio should be at least 4. Given Fc and M, an optimal loop filter setting needs to be solved for that will meet both the PLL loop bandwidth and maintain loop stability.

The charge pump gain should be relatively small as possible to achieve a low loop bandwidth.

Ip = 40uA .

$K\phi * K_{VCO}$ = 950MHz/V * 40uA = 38000A/Vs

Loop Bandwidths

$\omega c = 2\pi * Fc = 9.42x10^5\ s^{-1}$

$\omega z = \omega p / \omega c = 4$ (Eq. 26)

$\omega c^2 = \omega p * \omega z$ (Eq. 27)

$\omega p = \frac{Cz + Cp}{Rz * Cz * Cp} = \omega z (1 + Cz / Cp)$

Solving for Cz, Cp, and Rz

Knowing $\omega c = \frac{Rz * K\phi * K_{VCO} * Cz}{M * (Cz + Cp)}$ and substituting in the equations from above,

Cz >>> Cp, therefore, we can easily derive Cp to be

$Cp = \frac{K\phi * K_{VCO}}{M * \omega c^2 * \omega z} = 12.60pF$

Similarly for Cz and Rz

$Cz = \frac{K\phi * K_{VCO} * (\omega z^2 - 1) = Cp * (\omega z^2 - 1)}{M * \omega c^2 * \omega z} = 189pF$

$Rz = \frac{M * \omega c * \omega z^2}{K\phi * K_{VCO} * (\omega z^2 - 1)} = 22.48K\Omega$

Based on the loop filter parameter equations from above, since there are no possible values of 12.60pF for Cp, 189pF for Cz, and 22.48KΩfor Rz, the next possible values within the loop filter settings are 12.55pF (CP[3:0]=1111), 196.4pF (CZ[3:0]=0111), and 15.3KΩ(RZ[3:0]=1111), respectively. This loop filter setting will yield a loop bandwidth of about 102KHz. The phase margin must be checked for loop stability.

$\phi m = (360 / 2\pi) * [\tan^{-1}(6.41x10^5\ s^{-1} / 3.33x10^5\ s^{-1}) - \tan^{-1}(6.41x10^5\ s^{-1} / 5.54x10^6\ s^{-1})] = 56°$

Although slightly below 60°, the phase margin would be acceptable with a fairly stable loop.

CONFIGURING THE MULTI-PURPOSE I/Os

The 5V9885T can operate in four distinct modes. These modes are controlled by the MFC bit (0x04) and the I²C/$\overline{\text{JTAG}}$ pin. The general purpose I/O pins (GIN0, GIN1, GIN2, GIN3, GIN4, GIN5) have different uses depending on the mode of operation. The four available modes of operation are:

1) Manual Frequency Control (MFC) Mode for PLL0 Only
2) Manual Frequency Control (MFC) Mode for all three PLLs
3) I²C Programming Mode
4) JTAG Programming Mode

Along with the GINx pins are also GOUTx output pins that can take up a different function depending on the mode of operation. See table below for description.

Multi-Purpose Pins	Other Signal Functions	Signal Description
GIN0	SDAT / TDI	I²C serial data input / JTAG serial data input
GIN1	SCLK / TCK	I²C clock input / JTAG clock input
GIN2	TMS	JTAG control signal to the TAP controller state machine
GIN3	SUSPEND	Suspends all outputs of PLL (Active High)
GIN4	$\overline{\text{TRST}}$	JTAG active LOW input to asynchronously reset the BST
GIN5	CLK_SEL	Reference clock select between XTALIN/REFIN and CLKIN
GOUT0	TDO / LOSS_LOCK	JTAG serial data output / Detects loss of PLL lock(1)
GOUT1	LOSS_CLKIN	Detects loss of the primary clock source(1)

NOTE:

1. Please see detail description in Loss of Lock and Input Clock section.

Each PLL's programming registers can store up to four different Dx and Mx configurations in combination with two different P configurations in MFC modes. The post-divider should never be disabled in any of the two P configurations unless the output bank will never be used during normal operation. The PLL's loop filter settings also has four different configurations to store and select from. This will be explained in the MODE1 and MODE2 sections. The use of the GINx pins in MFC mode control the selection of these configurations.

MODE1 - Manual Frequency Control (MFC=1) Mode for PLL0 Only

In this mode, only 8 configurations of PLL0 can be changed during operation. The GIN0, GIN1 and GIN2 pins control the selection of eight different configurations (D, M, Rz, Cz, Cp and Ip) of PLL0. GIN3 becomes PLL SUSPEND pin, GIN4 is not available to users, and GIN5 becomes CLK_SEL pin. The output GOUT0 will become an indicator for loss of PLL lock (LOSS_LOCK). GOUT1 pin will become an indicator for loss of the primary clock (LOSS_CLKIN).

The PLL0 has 4 sets of dedicated registers for D, M, Rz, Cz, Cp, Ip and ODIV. For additional 4 sets of registers, the PLL0 uses registers from CONFIG2 and CONFIG3 of PLL1 and PLL2. The PLL1 and PLL2 will still be fully operational, but have only one fixed configuration in this mode, and the default configuration will be set to CONFIG0 of PLL1 and CONFIG0 of PLL2. (Please see page 18 for register location.)

The output banks will each have two P configurations that can be associated with each of the PLL configurations. Each of the two P configurations has its own set of PM bits (See the PRE-SCALERS, FEEDBACK-DIVIDERS, POST-DIVIDERS section for more detail on the PM bits). Use the ODIV bit to choose which post-divider configuration to associate with a specific PLL configuration.

To enter this mode, users must set MFC bit to "1", and I2C/JTAG pin must be left floating.

GIN2 Pin	GIN1 Pin	GIN0 Pin	PLL0 Configuration Selection (Mode 1)
0	0	0	Configuration 0
0	0	1	Configuration 1
0	1	0	Configuration 2
0	1	1	Configuration 3
1	0	0	Configuration 4
1	0	1	Configuration 5
1	1	0	Configuration 6
1	1	1	Configuration 7

MODE2 - Manual Frequency Control (MFC=0) Mode for all PLLs

In this mode, the configuration of PLL0, PLL1, and PLL2 can be changed during operation. The GINx pins are used to control the selection of up to four different Dx, Mx, RZx, CZx, CPx, and IPx configurations for each PLL. GIN0 and GIN1 become configuration selection pins for D0 and M0 of PLL0, GIN2 and GIN3 become configuration selection pins for PLL1, and GIN4 and GIN5 become configuration selection pins for D2 and M2 of PLL2. The output GOUT0 will become an indicator for loss of PLL lock (LOSS_LOCK). GOUT1 pin will become an indicator for loss of the primary clock (LOSS_CLKIN).

The output banks will have two different P configurations to choose from for each of the four PLL configurations. Each of the two P configurations has its own set of PM bits (See the PRE-SCALERS, FEEDBACK-DIVIDERS, POST-DIVIDERS section for more detail on the PM bits). Use the ODIV bit to choose which post-divider configuration to associate with a specific PLL configuration. For example, if ODIV2_CONFIG2=1, then when Config2 is selected Qx[9:0]_CONFIG1 is selected as the post-divider value to be used. Note that there is an ODIVx bit for each of the PLL configurations. In this way, the post-divider values can change with the configuration.

To enter this mode, users must set MFC bit to "0", and $I^2C/\overline{JTAG}$ pin must be left floating.

GIN1 Pin	GIN0 Pin	PLL0 Configuration Selection (Mode 2)
0	0	Configuration 0
0	1	Configuration 1
1	0	Configuration 2
1	1	Configuration 3

GIN5 Pin	GIN4 Pin	PLL2 Configuration Selection (Mode 2)
0	0	Configuration 0
0	1	Configuration 1
1	0	Configuration 2
1	1	Configuration 3

GIN3 Pin	GIN2 Pin	PLL1 Configuration Selection (Mode 2)
0	0	Configuration 0
0	1	Configuration 1
1	0	Configuration 2
1	1	Configuration 3

MODE3 - I^2C Programming Mode

In this mode, GIN0, GIN1, GIN3 and GIN5 become SDAT (I^2C data), SCLK (I^2C clock), SUSPEND and CLK_SEL signal pins, respectively. The output GOUT0 will become an indicator for loss of PLL lock (LOSS_LOCK). GOUT1 pin will become an indicator for loss of the primary clock (LOSS_CLKIN). GIN2 and GIN4 are not available to users.

To enter this mode, $I^2C/\overline{JTAG}$ pin must be set HIGH.

MODE4 - JTAG Programming Mode

In this mode, GIN0, GIN1, GIN2, GIN3, GIN4 and GIN5 will become TDI (JTAG data in), TCK (JTAG clock), TMS (JTAG control signal), SUSPEND, $\overline{TRST}$ (JTAG reset) and CLK_SEL signal pins, respectively. The output GOUT0 will become JTAG TDO signal, and GOUT1 will be an indicator for loss of the selected clock (LOSS_CLKIN).

To enter this mode, $I^2C/\overline{JTAG}$ pin must be set LOW.

Multi-Purpose pins	Manual Frequency Control modes			
	Mode1	Mode2	JTAG	I^2C
GIN0	GIN0	GIN0	TDI	SDAT
GIN1	GIN1	GIN1	TCK	SCLK
GIN2	GIN2	GIN2	TMS	n/a
GIN3	SUSPEND	GIN3	SUSPEND	SUSPEND
GIN4	n/a	GIN4	$\overline{TRST}$	n/a
GIN5	CLK_SEL	GIN5[1]	CLK_SEL	CLK_SEL
GOUT0	LOSS_LOCK	LOSS_LOCK	TDO	LOSS_LOCK
GOUT1	LOSS_CLKIN	LOSS_CLKIN	LOSS_CLKIN	LOSS_CLKIN

NOTE:

1. The PLL(s) will lock onto the primary clock and the manual switchover can be controlled by the PRIMCLK bit.

Understanding the GIN Signals

During power up, the part will virtually be in MFC mode2, therefore, the values of GIN4, GIN3, GIN2, GIN1 and GIN0 will be latched and used for PLL configuration selection, regardless of the state of the $I^2C/\overline{JTAG}$ pin. GIN5 is not latched, and will assume the LOW state internally when in programming mode. This means that when in programming mode, the PLL configuration can only be changed by writing directly to the registers of the currently selected configuration. When in MFC mode 2, configuration 0 or 1 (GIN5=0) should be selected if you do not want to change configurations when entering or leaving programming mode. The GIN pins should be held LOW during power up to select configuration0 as default.

When not in programming mode, the GIN inputs directly control the selected configuration. The internal GINx signals can be individually disabled via programming the GINEN bits (0x06). When disabled by setting GINENx to "0", the GINx inputs may be left floating, but during power up, the GIN pins will still latch. Disabled inputs are interpreted as LOW by the internal state machines. Even if disabled, GIN2, GIN1, GIN0 and GIN4 pins will be enabled if required for I^2C or JTAG programming functions when in programming mode. The SUSPEND and CLK_SEL functions on the GIN3 and GIN5 pins, respectively, will be rendered completely non-functional when disabled.

SHUTDOWN/SUSPEND/ENABLE OF OUTPUTS

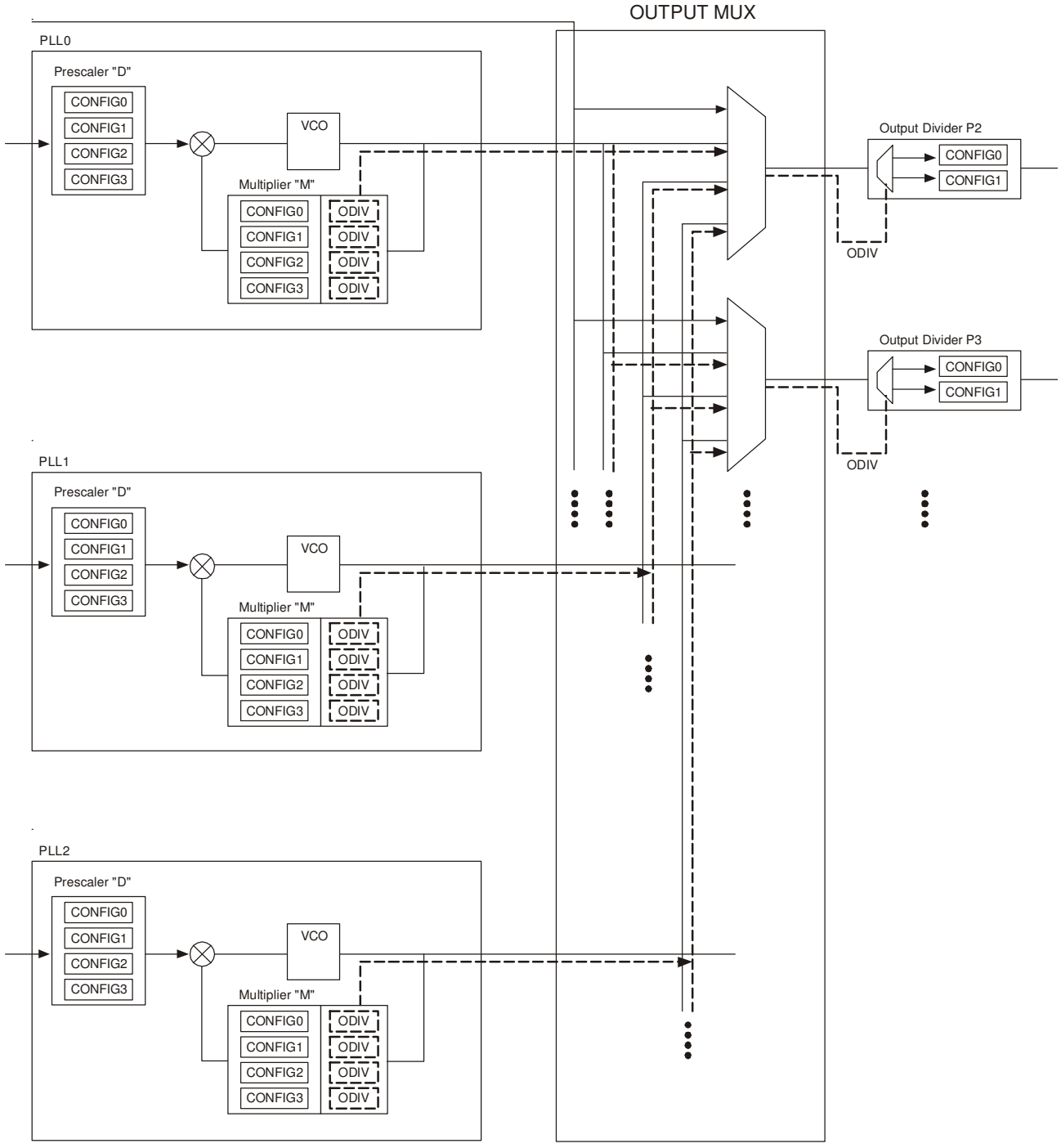
There are two external pins along with internal bits that control the enabling/disabling of the output banks. The two pins are the SHUTDOWN/OE pin and the GIN3/SUSPEND pin. The SHUTDOWN/OE pin can be programmed to function as an output enable or global shutdown. The polarity of the SHUTDOWN/OE signal pin can be programmed to be either active HIGH or LOW with the SP bit (0x1C). When SP is "0", the pin becomes active HIGH and when SP is "1", the pin becomes active LOW. The SH bit(0x1C) determines the function of the SHUTDOWN/OE signal pin. If SH is "1", the signal pin is SHUTDOWN and functions as a global shutdown. This will override the OEx (0x1C), OSx (0x1D), and PLLSx (0x1E) bits. If SH is "0", the signal pin is OE and functions as an enable/disable of the output banks. If used as an output enable/disable, each output bank can be individually programmed to be enabled or disabled by the OE pin.by setting OEx bits to "1". If the OE signal pin is asserted, the output banks that has their corresponding OEx bit set to "1" will be disabled. The OEMx bits determine the outputs' disable state. When set to "0x" the outputs will be tristated. When set to "10", the outputs will be pulled low. When set to "11", the outputs will be pulled high. Inverted outputs will be parked in the opposite state. If the OEx bits are set to "0", the states of the corresponding output banks will not be impacted by the state of the OE pin. To individually enable/disable via programming instead of the OE pin, hard wire the OE pin to Vdd or GND (depending if it is active HIGH or LOW) as if to disable the outputs. Then toggle the OEx bits to either "0" to enable or "1" to disable.

When the chip is in shutdown, the outputs, the reference oscillator, and the I^2C /JTAG pin are powered down. The outputs will be tristated and the I^2C /JTAG pin will be set to MFC mode (MID level). Programming will not be allowed. The GINx pins and clock inputs remain operational. The PLL is not disabled. The SHUTDOWN pin must be reasserted in order to program the part or to resume operation.

The GIN3/SUSPEND pin, when used as a SUSPEND function, can be used to power down the PLL and/or output banks.. Each output bank can be individually programmed to be enabled or disabled by the SUSPEND signal pin by setting the OSx bits to "1". If the SUSPEND signal pin is asserted, the output banks that has their corresponding OSx bit set to "1" will be powered down and outputs tristated. If the OSx bits are set to "0", the states of the corresponding output banks will not be impacted by the state of the SUSPEND pin. There is also an option to suspend individual PLLs by setting the PLLSx bits (0x1E) to "1". This will associate the PLL to the SUSPEND pin. When the pin is asserted, the corresponding PLLs will be powered down. It will not only power down the PLL but also any output bank associated with it. The PLLSx bits will override the OSx bits.

In the event of a PLL suspend, the PLL must achieve lock again after it has been re-enabled, In the event of a global shutdown, the PLL does not have to re-acquire lock since it is not disabled.

MANUAL FREQUENCY CONTROL (MFC) BLOCK DIAGRAM



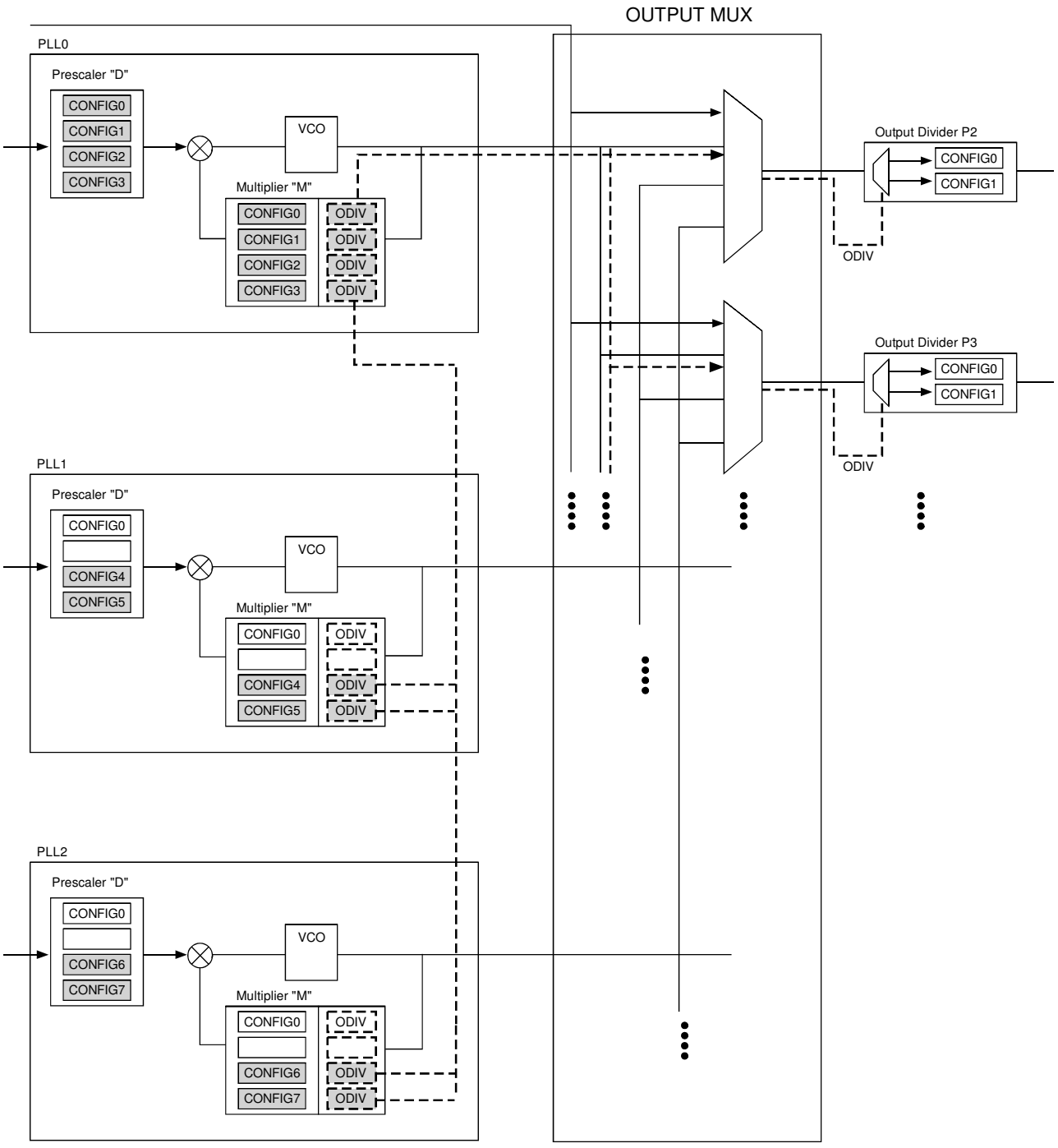
MFC = 0

NOTES:

This illustration shows how the configurations are arranged for each PLL. There is an ODIV bit associated with each of the four configurations.

- GIN0 and GIN1 control four configurations from PLL0.
- GIN2 and GIN3 control four configurations from PLL1.
- GIN4 and GIN4 control four configurations from PLL2.
- ODIV from each configuration determines the selection of two Output Divider Px Configurations.

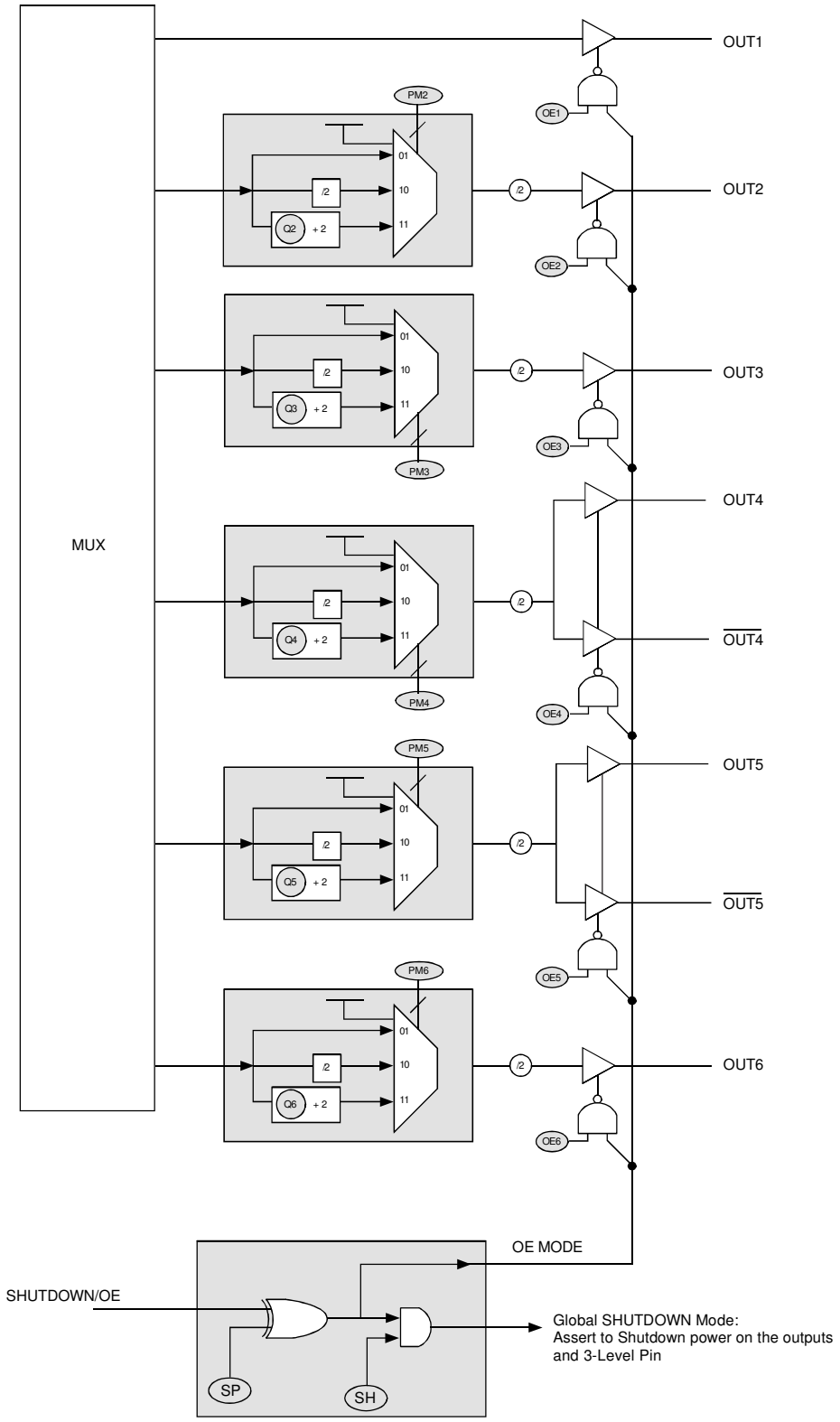
MANUAL FREQUENCY CONTROL (MFC) BLOCK DIAGRAM



MFC = 1

NOTES:
This illustration shows how the configurations are arranged for PLL0. Register location for Config_4 and Config_5 are taken from PLL1, and Config_6 and Config_7 are taken from PLL2. There is an ODIV bit associated with each of the configurations.
- GIN0, GIN1, and GIN2 control eight shaded configurations for PLL0.
- ODIV from each configuration determines the selection of two Output Divider Px Configurations.

BLOCK DIAGRAM FOR SHUTDOWN/OE CONTROL SIGNAL



NOTE:
This illustration shows the internal logic behind the SHUTDOWN/OE pin and the bits associated with it.

POWER UP AND POWER SAVING FEATURES

If a global shutdown is enabled, SHUTDOWN pin asserted, most of the chip except for the PLLs will be powered down. In order to have a complete power down of the chip, the PLLs must be powered down via the SUSPEND function or by setting the pre-scaler bits to '0x00' and disable the internal GINx signals via the enable bits at memory address 0x05. Note that the register bits will not lose their state in the event of a chip power-down. The only possibility that the register bits will lose their state is if the part was power-cycled. After coming out of shutdown mode, the PLLs will require time to relock.

During power up, the values of GIN4, GIN3, GIN2, GIN1 and GIN0 will be latched and used for PLL configuration selection, regardless of the state of the $I^2C/\overline{JTAG}$ pin and GINx being disabled via the GINENx bits. GIN5 will have an internal state of LOW. The GIN pins should be held LOW during power up to select configuration0 as default. The output levels will be at an undefined state during power up.

The post-divider should never be disabled via PM bits after power up, or else it will render the output bank completely non-functional during normal operation, (unless the output bank itself will not be used at all).

During power up, the V_{DD} ramp must be monotonic.

LOSS OF LOCK AND INPUT CLOCK

The device employs a loss of lock and loss of input clock detection circuitry. The GOUT0/LOSS_LOCK and GOUT1/LOSS_CLKIN are the outputs that indicate such failures. LOSS_LOCK signal will be asserted if any of the three powered up PLLs loses frequency lock for any event other than PLL shutdown. Lock is determined by checking that the reference and feedback clocks are within 1/2 period of each other.Loss_LOCK signal may be falsely asserted when

- Spread Spectrum is turned on for any of the PLLs
- Fractional divider is used for any of the PLLs
- the reference and feedback clocks are not within 1/2 period of each other.

LOSS_CLKIN is asserted when the currently selected clock is lost or is asserted when both clocks are lost. In the event of the selected clock being absent up on power up, the loss of the selected clock detection circuitry will reference an internal oscillator. LOSS_LOCK and LOSS_CLKIN cannot be used as reliable inputs to other devices.

SWITCHOVER MODES

The IDT5V9885T features redundant clock inputs which supports both Automatic and Manual switchover mode. These two modes are determined by the configuration bits, SM (0x34). The primary clock source can be programmed, via the PRIMCLK bit, to be either XTALIN/REFIN or CLKIN, which is determined by the PRIMCLK bit. The other clock source input will be considered as the secondary source. This is more detailed in the 'REFERENCE CLOCK INPUT PINS AND SELECTION'. Note that the switchover modes are asynchronous. If the reference clocks are directly routed to OUTx with no phase relationship, short pulses can be generated during switchover. The automatic switchover mode will work only when the primary clock source is XTALIN/REFIN.

MANUAL SWITCHOVER MODE

When SM[1:0] is "0x", the redundant inputs are in manual switchover mode. In this mode, CLK_SEL pin is used to switch between the primary and secondary clock sources. As previously mentioned, the primary and secondary clock source setting is determined by the PRIMCLK bit. During the switchover, no glitches will occur at the output of the device, although there may be frequency and phase drift, depending on the exact phase and frequency relationship between the primary and secondary clocks. If GOUT1 is used as LOSS_CLKIN, it indicates loss of primary clock.

AUTOMATIC SWITCHOVER MODE

When SM[1:0] is "11", the redundant inputs are in automatic revertive switchover mode.

Revertive

The input clock selection will switch to the secondary clock source when there are no transitions on the primary clock source. LOSS_CLKIN signals will be asserted. After a stable and valid primary clock source is present, the input clock selection will automatically switch back to the primary clock source and LOSS_CLKIN signal will be deasserted. The CLK_SEL pin can be left floating in this auto-revertive mode. Note that both clock inputs must be at the same frequency (within 1000 ppm) in order for the auto-revertive switchover to function properly. If both reference clocks are at different frequencies, the device will always remain on the primary clock unless it is absent for two secondary clock cycles.

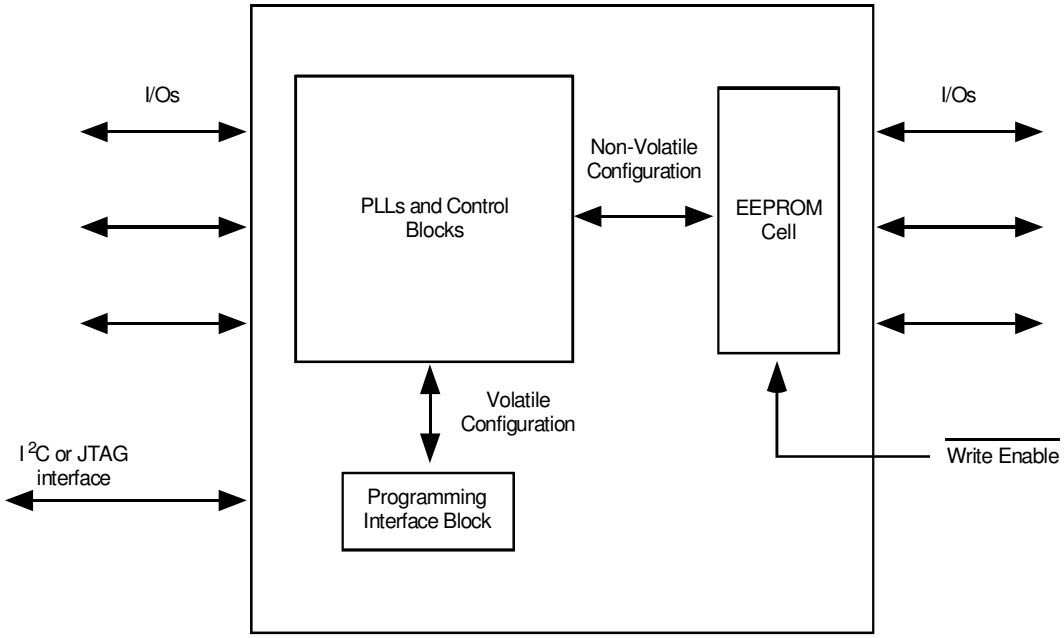
CLOCK SWITCH MATRIX AND OUTPUTS

All three PLL outputs and the currently selected input clock source are routed into and through a clock matrix. The user is able to select which PLL output and clock source is routed to which output bank via the SRCx bits (0x34, 0x35). Each output bank has its own set of SRC bits. Refer to the RAM table for more information. Note that OUT1 will be based off the reference clock and the only output bank toggling under the default RAM bit settings.

Outputs 1, 2 and 3 are 3.3V LVTTL. Outputs banks 4 and 5 can be 3.3V LVTTL, LVPECL or LVDS. The LVDS and LVPECL selection is determined by the LVLx bits (0x54, 0x58). Each output bank has individual slew-rate control (SLEWx bits). Each output can be individually inverted (INVx bits); when using LVPECL or LVDS modes, one of the outputs in each LVPECL/LVDS pair should be inverted. All output banks except OUT1 have a programmable 10-bit post-divider (Qx bits) with two selectable divide configurations via the ODIVx bits.

There are four settings for the programmable slew rate, 0.7V/ns, 1.25V/ns, 2V/ns, and 2.75V/ns; this only applies to the 3.3V LVTTL outputs. The differential outputs are not slew rate programmable in LVPECL or LVDS modes. SLEW4 and/or SLEW5 must be set to 2.75V/ns for stable output operation . For LVTTL output frequency rates higher than 100MHz, a slew rate of 2V/ns or greater should be selected. The post-dividers can be disabled using the PMx bit, which is described in the PRE-SCALER, FEEDBACK-DIVIDER, AND POST-DIVIDER section. Each output can also be enabled/disabled, which is described in the 'SHUTDOWN/SUSPEND/ENABLE of OUTPUTS' section. Refer to the RAM table for all binary settings.

HIGH LEVEL BLOCK DIAGRAM FOR CONFIGURATION SCHEME



NOTE: Diagram does not represent actual number of die on chip.

PROGRAMMING THE DEVICE

I²C and JTAG may be used to program the 5V9885T. The I²C/$\overline{\text{JTAG}}$ pin selects the I²C when HIGH and JTAG when LOW. Note that the TRST pin needs to be LOW for I²C mode.

Hardwired Parameters for the IDT5V9885T
JTAG identification number = 32'b0000_0000001110101100_00000110011_1
Device (slave) address = 7'b1101010
ID Byte for the 5V9885T = 8'b00010000

I²C PROGRAMMING

The 5V9885T is programmed through an I²C-Bus serial interface, and is an I²C slave device. The read and write transfer formats are supported. The first byte of data after a write frame to the correct slave address is interpreted as the register address; this address auto-increments after each byte written or read. The frame formats are shown below.

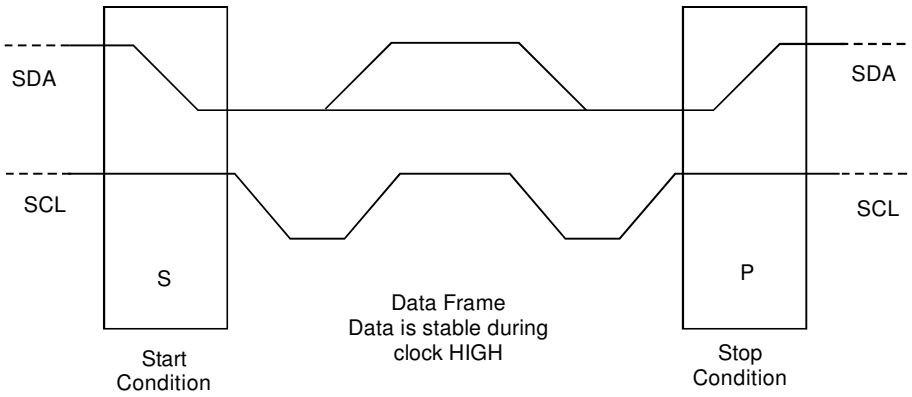
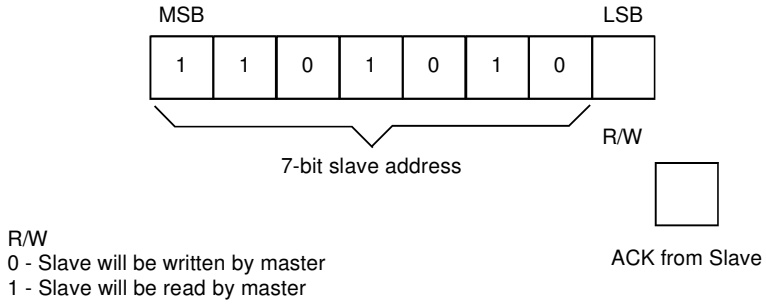


Figure 1: Framing

Each frame starts with a "Start Condition" and ends with an "End Condition". These are both generated by the Master device.



R/W
0 - Slave will be written by master
1 - Slave will be read by master

The first byte transmitted by the Master is the Slave Address followed by the R/W bit.
The Slave acknowledges by sending a "1" bit.

Figure 2: First Byte Transmittetd on I²C Bus

EXTERNAL I²C INTERFACE CONDITION

KEY:

From Master to Slave

From Master to Slave, but can be omitted if followed by the correct sequence
Normally data transfer is terminated by a STOP condition generated by the Master. However, if the Master still wishes to communicate on the bus, it can generate a repeated START condition, and address another Slave address without first generating a STOP condition.

From Slave to Master

SYMBOLS:

ACK - Acknowledge (SDA LOW)
NACK - Not Acknowledge (SDA HIGH)
Sr - Repeated Start Condition
S - START Condition
P - STOP Condition

PROGWRITE

S	Address	R/W	ACK	Command Code	ACK	Register	ACK	Data	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx00	1-bit	8-bits	1-bit	8-bits	1-bit	

Figure 3: Progwrite Command Frame

Writes can continue as long as a Stop condition is not sent and each byte will increment the register address.

PROGREAD

Note: If the expected read command is not from the next higher register to the previous read or write command, then set a known "read" register address prior to a read operation by issuing the following command:

S	Address	R/W	ACK	Command Code	ACK	Register	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx00	1-bit	8-bits	1-bit	

Figure 4a: Prior to Progread Command Set Register Address

The user can ignore the STOP condition above and use a repeated START condition instead, straight after the slave acknowledgement bit (i.e., followed by the Progread command):

Sr	Address	R/W	ACK	ID Byte	ACK	Data_1	ACK	Data_2	ACK	Data_last	NACK	P
	7-bits	1	1-bit	8 bits	1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit	

Figure 4b: Progread Command Frame

Note: Figure 4b above by itself is the Progread command format. The ID byte for the 5V9885T is 10hex. Each byte recieved increments the register address.

PROGSAVE

S	Address	R/W	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits:xxxxxx01	1-bit	

NOTE:
PROGWRITE is for writing to the 5V9885T registers.
PROGREAD is for reading the 5V9885T registers.
PROGSAVE is for saving all the contents of the 5V9885T registers to the EEPROM.
PROGRESTORE is for loading the entire EEPROM contents to the 5V9885T registers.

PROGRESTORE

S	Address	R/W	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits:xxxxxx10	1-bit	

JTAG INTERFACE

In addition to the IEEE 1149.1 instructions EXTEST, SAMPLE/PRELOAD, CLAMP, HIGH-Z and BYPASS, the 5V9885T allows access to internal programming registers using the REGADDR (set register address), REGDATAR (read register) and REGDATW (write register instructions. Data is always accessed by byte, and the register address increments after each read or write. The full instruction set follows. The IDT5V9885T will be updating the registers during programming.

The JTAG TAP controller can be reset in one of four ways:

1) Power up in JTAG mode
2) Power up in I^2C mode and then go into JTAG mode, or go out of and back into JTAG mode with the $I^2C/\overline{JTAG}$ pin
3) Apply TRST while in JTAG mode
4) Apply five rising edges of TCK with TMS high while in JTAG mode

JTAG INSTRUCTION REGISTER DESCRIPTION

IR (3)	IR (2)	IR (1)	IR (0)	Instructions
0	0	0	0	EXTEST(1)
0	0	0	1	SAMPLE/PRELOAD(1)
0	0	1	0	IDCODE(1)
0	0	1	1	REGADDR(2)
0	1	0	0	REGDATAW / PROGWRITE(3)
0	1	0	1	REGDATAR / PROGREAD(4)
0	1	1	0	PROGSAVE(5)
0	1	1	1	PROGRESTORE(6)
1	0	0	0	CLAMP(1)
1	0	0	1	HIGHZ(1,7)
1	1	1	1	BYPASS(1)

NOTES:
1. IEEE 1149.1 definition
2. REGADDR is for setting a specific 5V9885T register address.
3. REGDATAW/PROGWRITE is for writing to the 5V9885T registers.
4. REGDATAR/PROGREAD is for reading the 5V9885T registers.
5. PROGSAVE is for saving all the contents of the 5V9885T registers to the EEPROM.
6. PROGRESTORE is for loading the entire EEPROM contents to the 5V9885T registers.
7. The OEMs bits for OUT1-6 must be set for tri-state when using the HIGHZ instruction

EEPROM INTERFACE

The IDT5V9885T can also store its configuration in an internal EEPROM. The contents of the device's internal programming registers can be saved to the EEPROM by issuing a save instruction (ProgSave) and can be loaded back to the internal programming registers by issuing a restore instruction (ProgRestore).

To initiate a save or restore using I^2C, only two bytes are transferred. The Device Address is issued with the read/write bit set to "0", followed by the appropriate command code. The save or restore instruction executes after the STOP condition is issued by the Master, during which time the IDT5V9885T will not generate Acknowledge bits. The IDT5V9885T will acknowledge the instructions after it has completed execution of them. During that time, the I^2C bus should be interpreted as busy by all other users of the bus.

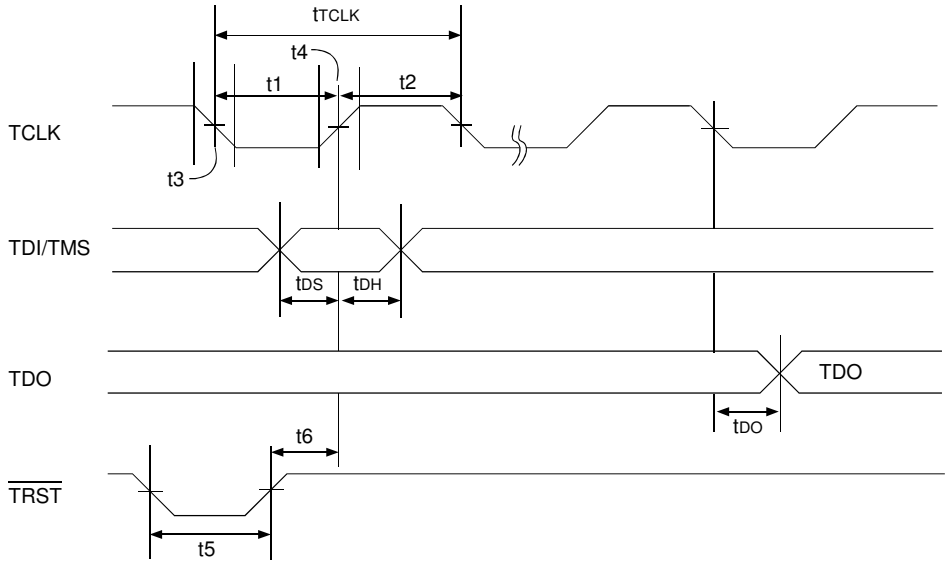
Using JTAG, the ProgSave and ProgRestore instructions selects the BYPASS register path for shifting the data from TDI to TDO during the data register scanning. During the execution of a ProgSave or ProgRestore instruction, the IDT5V9885T will not accept a new programming instruction (read, write, save, or restore). All non-programming JTAG instructions will function properly, but the user should wait until the save or restore is complete before issuing a new programming instruction. If a new programming instruction is issued before the save or restore completes, the new instruction is ignored, and the BYPASS register path remains in effect for shifting data from TDI to TDO during data register scanning.

The time it takes for the save (T_{SAVE}) and restore ($T_{RESTORE}$) instructions to complete is:

T_{SAVE} = 100ms max, $T_{RESTORE}$ = 10 ms max

In order for the save and restore instructions to function properly, the IDT5V9885T must not be in shutdown mode (SHUTDOWN pin asserted). In the event of an interrupt of some sort such as a power down of the part in the middle of a save or restore operation, the contents to or from the EEPROM will be partially loaded, and a CRC error will be generated. The CERR bit (0x81) will be asserted to indicate that an error has occurred. The LOSS_LOCK signal will also be asserted.

On power-up of the IDT5V9885T, an automatic restore is performed to load the EEPROM contents into the internal programming registers. The auto-restore will not function properly if the device is in shutdown mode (SHUTDOWN pin asserted). The IDT5V9885T will be ready to accept a programming instruction once it acknowledges its 7-bit I²C address.



Standard JTAG Timing

NOTE:
t1 = tTCLKLOW
t2 = tTCLKHIGH
t3 = tTCLKFALL
t4 = tTCLKRISE
t5 = tRST (reset pulse width)
t6 = tRSR (reset recovery)

JTAG AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units
tTCLK	JTAG Clock Input Period	100	—	ns
tTCLKHIGH	JTAG Clock HIGH	40	—	ns
tTCLKLOW	JTAG Clock Low	40	—	ns
tTCLKRISE	JTAG Clock Rise Time	—	5(1)	ns
tTCLKFALL	JTAG Clock Fall Time	—	5(1)	ns
tRST	JTAG Reset	50	—	ns
tRSR	JTAG Reset Recovery	50	—	ns

NOTE:
1. Guaranteed by design.

SYSTEM INTERFACE PARAMETERS

Symbol	Parameter	Min.	Max.	Units
tDO	Data Output(1)	—	20	ns
tDOH	Data Output Hold(1)	0	—	ns
tDS	Data Input, tRISE = 3ns	10	—	ns
tDH	Data Input, tFALL = 3ns	10	—	ns

NOTE:
1. 50pF loading on external output signals.

I²C BUS DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Level		0.7 * V_{DD}			V
V_{IL}	Input LOW Level				0.3 * V_{DD}	V
V_{HYS}	Hysteresis of Inputs		0.05 * V_{DD}			V
I_{IN}	Input Leakage Current				±1.0	µA
V_{OL}	Output LOW Voltage	I_{OL} = 3 mA			0.4	V

I²C BUS AC CHARACTERISTICS FOR STANDARD MODE

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Serial Clock Frequency (SCLK)	0		100	KHz
t_{BUF}	Bus free time between STOP and START	4.7			µs
$t_{SU:START}$	Setup Time, START	4.7			µs
$t_{HD:START}$	Hold Time, START	4			µs
$t_{SU:DATA}$	Setup Time, data input (SDAT)	250			ns
$t_{HD:DATA}$	Hold Time, data input (SDAT)(1)	0			µs
t_{OVD}	Output data valid from clock			3.45	µs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, data and clock (SDAT, SCLK)			1000	ns
t_F	Fall Time, data and clock (SDAT, SCLK)			300	ns
t_{HIGH}	HIGH Time, clock (SCLK)	4			µs
t_{LOW}	LOW Time, clock (SCLK)	4.7			µs
$t_{SU:STOP}$	Setup Time, STOP	4			µs

NOTE:
1. A device must internally provide a hold time of at least 300ns for the SDAT signal (referred to the V_{IHMIN} of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

I²C BUS AC CHARACTERISTICS FOR FAST MODE

Symbol	Parameter	Min	Typ	Max	Unit
F_{SCLK}	Serial Clock Frequency (SCLK)	0		400	KHz
t_{BUF}	Bus free time between STOP and START	1.3			µs
$t_{SU:START}$	Setup Time, START	0.6			µs
$t_{HD:START}$	Hold Time, START	0.6			µs
$t_{SU:DATA}$	Setup Time, data input (SDAT)	100			ns
$t_{HD:DATA}$	Hold Time, data input (SDAT)(1)	0			µs
t_{OVD}	Output data valid from clock			0.9	µs
C_B	Capacitive Load for Each Bus Line			400	pF
t_R	Rise Time, data and clock (SDAT, SCLK)	20 + 0.1 * C_B		300	ns
t_F	Fall Time, data and clock (SDAT, SCLK)	20 + 0.1 * C_B		300	ns
t_{HIGH}	HIGH Time, clock (SCLK)	0.6			µs
t_{LOW}	LOW Time, clock (SCLK)	1.3			µs
$t_{SU:STOP}$	Setup Time, STOP	0.6			µs

NOTE:
1. A device must internally provide a hold time of at least 300ns for the SDAT signal (referred to the V_{IHMIN} of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{DD}	Internal Power Supply Voltage	-0.5 to +4.6	V
V_I	Input Voltage	-0.5 to +4.6	V
V_O	Output Voltage(2)	-0.5 to V_{DD} + 0.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	–65 to +150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Not to exceed 4.6V.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	—	4	—	pF
Crystal Specifications					
XTAL_FREQ	Crystal Frequency	8	—	50	MHz
XTAL_MIN	Minimum Crystal Load Capacitance	—	3.5	—	pF
XTAL_MAX	Maximum Crystal Load Capacitance	—	35.4	—	pF
	Crystal Load Capacitance Resolution	—	0.125	—	
XTAL_V_{PP}	Voltage Swing (peak-to-peak, nominal)	—	2.3	—	V

NOTE:
1. Capacitance levels characterized but not tested.

RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage for LVTTL	3	3.3	3.6	V
	Power Supply Voltage for LVDS/LVPECL	3.135	3.3	3.465	
T_A	Operating Temperature, Ambient	–40	—	+85	°C
C_{LOAD_OUT}	Maximum Load Capacitance (LVTTL only)	—	—	15	pF
F_{IN}	External Reference Crystal	8	—	50	MHz
	External Reference Clock, Industrial	1	—	400	
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	—	5	ms

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{IHH}	Input HIGH Voltage Level[1]	I²C/JTAG 3-Level Input		V_{DD} – 0.4	—	—	V
V_{IMM}	Input MID Voltage Level[1]	I²C/JTAG 3-Level Input		V_{DD}/2 – 0.2	—	V_{DD}/2 + 0.2	V
V_{ILL}	Input LOW Voltage Level[1]	I²C/JTAG 3-Level Input		—	—	0.4	V
I_3	3-Level Input DC Current	V_{IN} = V_{DD}	HIGH Level	—	—	200	µA
		V_{IN} = V_{DD}/2	MID Level	–50	—	+50	
		V_{IN} = GND	LOW Level	–200	—	—	
I_{DD}	Total Power Supply Current (3.3V Supply, V_{DD})	2 outputs @166MHz; 4 outputs @ 83MHz		—	120	—	mA
		2 outputs @20MHz; 4 outputs @ 40MHz		—	40	—	
I_{DDS}	Total Power Supply Current in Shutdown Mode[2]	Global Shutdown Mode (PLLs, dividers, outputs, etc. powered down)		—	2	—	mA

NOTES:

1. These inputs are normally wired to V_{DD}, GND, or left floating. If these inputs are switched dynamically after powerup, the function and timing of the outputs may be glitched, and the PLL may require additional t_{AQ} time before all datasheet limits are achieved.
2. Dividers must reload reprogrammed values via power-on reset or terminal count reload in order to ensure low-power mode.

DC ELECTRICAL CHARACTERISTICS FOR 3.3V LVTTL[1]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output HIGH Current	V_{OH} = V_{DD} - 0.5, V_{DD} = 3.3V ± 0.3V	12	24	—	mA
I_{OL}	Output LOW Current	V_{OL} = 0.5V, V_{DD} = 3.3V ± 0.3V	12	24	—	mA
V_{IH}	Input Voltage HIGH		2	—	—	V
V_{IL}	Input Voltage LOW		—	—	0.8	V
I_{IH}	Input HIGH Current[2]	V_{IN} = V_{DD}	—	—	10	µA
I_{IL}	Input LOW Current	V_{IN} = 0V	—	—	10	µA
I_{OZD}	Output Leakage Current	3-state outputs	—	—	10	µA

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. I_{IH} specification does not apply to inputs with internal pull-down.

POWER SUPPLY CHARACTERISTICS FOR LVTTL OUTPUTS

Symbol	Parameter	Test Conditions	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	REF = LOW Outputs enabled, All outputs unloaded	6	12	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., C_L = 0pF	40	60	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current	$F_{REFERENCE\ CLOCK}$ = 33MHz, C_L = 15pf	26	40	mA
		$F_{REFERENCE\ CLOCK}$ = 133MHz, C_L = 15pf	80	120	
		$F_{REFERENCE\ CLOCK}$ = 200MHz, C_L = 15pf	112	170	

DC ELECTRICAL CHARACTERISTICS FOR LVDS

Symbol	Parameter	Min.	Typ.	Max	Unit
V_{OT} (+)	Differential Output Voltage for the TRUE binary state	247	—	454	mV
V_{OT} (-)	Differential Output Voltage for the FALSE binary state	-247	—	-454	mV
Δ V_{OT}	Change in V_{OT} between Complimentary Output States	—	—	50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)	1.125	1.2	1.375	V
Δ V_{OS}	Change in V_{OS} between Complimentary Output States	—	—	50	mV
I_{OS}	Outputs Short Circuit Current, V_{OUT}+ or V_{OUT}- = 0V or V_{DD}	—	9	24	mA
I_{OSD}	Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT}-	—	6	12	mA

POWER SUPPLY CHARACTERISTICS FOR LVDS OUTPUTS(1)

Symbol	Parameter	Test Conditions(2)	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	REF = LOW Outputs enabled, All outputs unloaded	68	90	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., C_L = 0pF	30	45	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current	$F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 5pf	86	130	mA
		$F_{REFERENCE\ CLOCK}$ = 200MHz, C_L = 5pf	100	150	
		$F_{REFERENCE\ CLOCK}$ = 400MHz, C_L = 5pf	122	190	

NOTES:

1. Output banks 4 and 5 are toggling. Other output banks are powered down.
2. The termination resistors are excluded from these measurements.

DC ELECTRICAL CHARACTERISTICS FOR LVPECL

Symbol	Parameter	Min.	Typ.	Max	Unit
V_{OH}	Output Voltage HIGH, terminated through 50Ω tied to V_{DD} - 2V	V_{DD} - 1.2	—	V_{DD} - 0.9	V
V_{OL}	Output Voltage LOW, terminated through 50Ω tied to V_{DD} - 2V	V_{DD} - 1.95	—	V_{DD} - 1.61	V
V_{SWING}	Peak to Peak Output Voltage Swing	0.55	—	0.93	V

POWER SUPPLY CHARACTERISTICS FOR LVPECL OUTPUTS(1)

Symbol	Parameter	Test Conditions(2)	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	REF = LOW Outputs enabled, All outputs unloaded	86	110	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., C_L = 0pF	35	50	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current	$F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 5pf	120	180	mA
		$F_{REFERENCE\ CLOCK}$ = 200MHz, C_L = 5pf	130	190	
		$F_{REFERENCE\ CLOCK}$ = 400MHz, C_L = 5pf	140	210	

NOTES:

1. Output banks 4 and 5 are toggling. Other output banks are powered down.
2. The termination resistors are excluded from these measurements.

AC TIMING ELECTRICAL CHARACTERISTICS

(SPREAD SPECTRUM GENERATION = OFF)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max	Unit
f_{IN}	Input Frequency	Input Frequency Limit		1[1]	—	400	MHz
1/t1	Output Frequency	Single Ended Clock output limit (LVTTL)		0.0049	—	200	MHz
		Differential Clock output limit (LVPECL/LVDS)		0.0049	—	500	
f_{VCO}	VCO Frequency	VCO operating Frequency Range		10	—	1200	MHz
f_{PFD}	PFD Frequency	PFD operating Frequency Range		0.4[1]	—	400	MHz
f_{BW}	Loop Bandwidth	Based on loop filter resistor and capacitor values		0.03	—	40	MHz
t2	Input Duty Cycle	Duty Cycle for Input		40	—	60	%
t3	Output Duty Cycle	Measured at $V_{DD}/2$, $F_{OUT} \leq 200$MHz		45	—	55	%
		Measured at $V_{DD}/2$, $F_{OUT} > 200$MHz		40	—	60	
t4[2]	Slew Rate SLEWx(bits) = 00	Single-Ended Output clock rise and fall time, 20% to 80% of V_{DD} (Output Load = 15pf)		—	2.75	—	V/ns
	Slew Rate SLEWx(bits) = 01	Single-Ended Output clock rise and fall time, 20% to 80% of V_{DD} (Output Load = 15pf)		—	2	—	
	Slew Rate SLEWx(bits) = 10	Single-Ended Output clock rise and fall time, 20% to 80% of V_{DD} (Output Load = 15pf)		—	1.25	—	
	Slew Rate SLEWx(bits) = 11	Single-Ended Output clock rise and fall time, 20% to 80% of V_{DD} (Output Load = 15pf)		—	0.75	—	
t5	Rise Times	LVDS, 20% to 80%		—	850	—	ps
	Fall Times			—	850	—	
	Rise Times	LVPECL, 20% to 80%		—	500	—	
	Fall Times			—	500	—	
t6	Output three-state Timing	Time for output to enter or leave three-state mode after SHUTDOWN/OE switches		—	—	150 + 1/F_{OUTX}	ns
t7	Clock Jitter[3,7]	Peak-to-peak period jitter, CLK outputs measured at $V_{DD}/2$	f_{PFD} > 20MHz	—	—	150	ps
			f_{PFD} < 20MHz	—	200	—	
t8	Output Skew	Skew between output to output on the same bank (bank 4 and bank 5 only)[4, 5]		—	—	150	ps
t9	Lock Time	PLL Lock Time from Power-up[6]		—	10	20	ms
t10	Lock time[8]	PLL Lock time from shutdown mode		—	20	100	µs

NOTES:

1. Practical lower input frequency is determined by loop filter settings.
2. A slew rate of 2V/ns or greater should be selected for output frequencies of 100MHz and higher.
3. Input frequency is the same as the output with all output banks running at the same frequency.
4. Skew measured between all in-phase outputs in the same bank.
5. Skew measured between the cross points of all differential output pairs under identical input and output interfaces, transitions and load conditions on any one device.
6. Includes loading the configuration bits from EEPROM to PLL registers. It does not include EEPROM programming/write time.
7. Guaranteed by design but not production tested. Actual jitter performance may vary depending on the configuration.
8. Actual PLL lock time depends on the loop configuration.

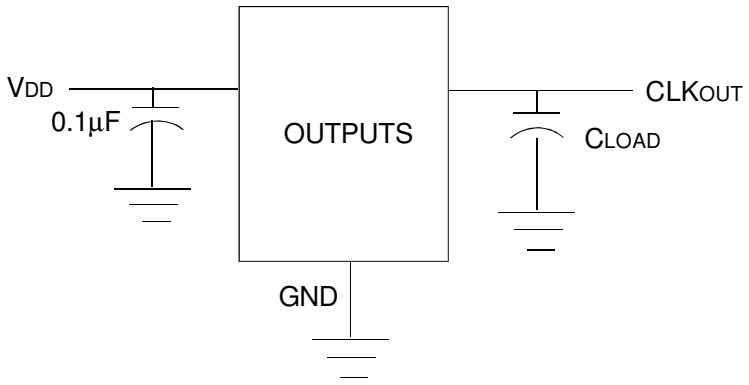
SPREAD SPECTRUM GENERATION SPECIFICATIONS

Symbol	Parameter	Description	Min.	Typ.	Max	Unit
f_{IN}	Input Frequency	Input Frequency Limit	1[1]	—	400	MHz
f_{MOD}	Mod Freq	Modulation Frequency	—	33	—	kHz
f_{SPREAD}	Spread Value	Amount of Spread Value (Programmable) - Down Spread	-0.5, -1, -2.5, -3.5, -4			%f_{OUT}
		Amount of Spread Value (Programmable) - Center Spread	-2.0 to +2.0			

NOTE:

1. Practical lower input frequency is determined by loop filter settings.

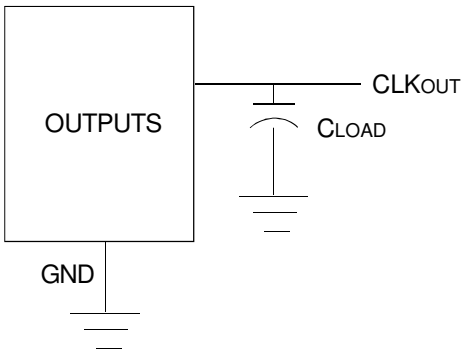
TEST CIRCUITS AND CONDITIONS(1)



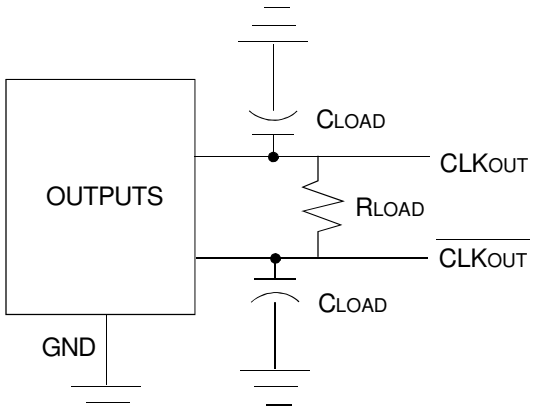
NOTE:
1. All VDD pins must be tied together.

Test Circuits for DC Outputs

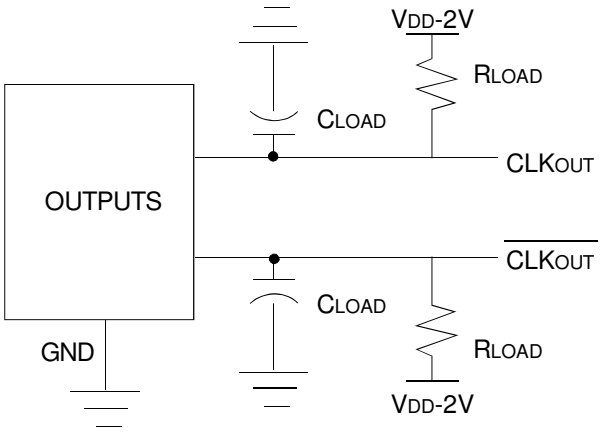
OTHER TERMINATION SCHEME (BLOCK DIAGRAM)



LVTTL: -15pF for each output



LVDS: - 100Ω between differential outputs with 5pF



LVPECL: - 50Ω to VDD-2V for each output with 5pF

RAM (PROGRAMMING REGISTER) TABLES

	BIT #									BIT #								
ADDR	7	6	5	4	3	2	1	0	Register Hex Value	7	6	5	4	3	2	1	0	DESCRIPTION
0x00																		No registers exist
0x01																		
0x02																		
0x03																		
0x04	0	0	0	0	0	0	0	0	00	Reserved							MFC	MFC=Manual Frequency Control Mode ('0'=All PLL Control (Default), "1"=PLL0 Control Only); GINEN0 to GINEN5=GINx Pins Enable Bits, ("1"=Enable (Default), "0"=No Connect (Internal State will be "Low"));
0x05	1	1	1	1	1	1	1	1	FF			GINEN5	GINEN4	GINEN3	GINEN2	GINEN1	GINEN0	
0x06	0	0	1	1	0	0	0	0	30			XDRV[1:0]						XDRV=crystal drive strength ("00" = 1.4V, "01" = 2.3V, "10"= 3.2V pk-pk swing typical, "11"=XTAL_IN with external clock-default); When "11", XTALCAP[7:0] value must also be set to "0". Bits 7,6, 3, 2, 1, 0 are reserved and should be set to "0"
0x07	0	0	0	0	0	0	0	0	00	XTALCAP[7:0]								XTAL load cap = 3.5pF+ (0.125 x XTALCAP[7:0]) , 3.5pF to 35.4pF; Each XTAL pin to GND; (For example, "00000001"=0.125pF, "00000010"=0.25pF, "00000100"=0.5pF); Default = "00000000";
0x08	0	0	0	0	0	0	0	0	00	ODIV0_CONFIG0	IP0[2:0]_CONFIG0			RZ0[3:0]_CONFIG0				
0x09	0	0	0	0	0	0	0	0	00	ODIV0_CONFIG1	IP0[2:0]_CONFIG1			RZ0[3:0]_CONFIG1				
0x0A	0	0	0	0	0	0	0	0	00	ODIV0_CONFIG2	IP0[2:0]_CONFIG2			RZ0[3:0]_CONFIG2				
0x0B	0	0	0	0	0	0	0	0	00	ODIV0_CONFIG3	IP0[2:0]_CONFIG3			RZ0[3:0]_CONFIG3				PLL0 LOOP FILTER SETTING
0x0C	0	0	0	0	0	0	0	0	00	CP0[3:0]_CONFIG0				CZ0[3:0]_CONFIG0				ODIV0_CONFIGx=Determines which one of the 2 "Qx-Divider" Configurations to use wi
0x0D	0	0	0	0	0	0	0	0	00	CP0[3:0]_CONFIG1				CZ0[3:0]_CONFIG1				
0x0E	0	0	0	0	0	0	0	0	00	CP0[3:0]_CONFIG2				CZ0[3:0]_CONFIG2				
0x0F	0	0	0	0	0	0	0	0	00	CP0[3:0]_CONFIG3				CZ0[3:0]_CONFIG3				
0x10	0	0	0	0	0	0	0	0	00	D0[7:0]_CONFIG0								**PLL0 INPUT DIVIDER D0 SETTING**
0x11	0	0	0	0	0	0	0	0	00	D0[7:0]_CONFIG1								
0x12	0	0	0	0	0	0	0	0	00	D0[7:0]_CONFIG2								
0x13	0	0	0	0	0	0	0	0	00	D0[7:0]_CONFIG3								
0x14	0	0	0	0	0	0	0	0	00	N0[7:0]_CONFIG0								PLL0 MULTIPLIER SETTING CONFIG0 will be selected if GINx are disabled and operating in MFC mode. N0[11:0]_CONFIGx - Part of PLL0 M Integer Feedback Divider Values (see equation below) - For 4 Configurations (Default value is '0'); A0[3:0]_CONFIGx - Part of PLL0 M Integer Feedback Divider Values (see equation below) - For 4 Configurations (Default value is '0'); SSC_OFFSET0[5:0] - Spread Spectrum Fractional Multiplier Offset Value. See Spread Spectrum Settings in register address range 0x60-0x67 Total Multiplier Value M0 = 2 * N0[11:0] + A0 + 1 + SS_OFFSET0 * 1/64 When A0[3:0] = 0 and spread spectrum disabled, M0= 2 * N0[11:0]; When A0[3:0] > 0 and spread spectrum disabled, M0 = 2 * N0[11:0] + A0 + 1; (Note: A < N-1, i.e. valid M values are 2, 4, 6, 8, 9, 10, 11, 12, 13, ..., 4095 assuming within fPFD and fVCO spec);
0x15	0	0	0	0	0	0	0	0	00	N0[7:0]_CONFIG1								
0x16	0	0	0	0	0	0	0	0	00	N0[7:0]_CONFIG2								
0x17	0	0	0	0	0	0	0	0	00	N0[7:0]_CONFIG3								
0x18	0	0	0	0	0	0	0	0	00	A0[3:0]_CONFIG0				N0[11:8]_CONFIG0				
0x19	0	0	0	0	0	0	0	0	00	A0[3:0]_CONFIG1				N0[11:8]_CONFIG1				
0x1A	0	0	0	0	0	0	0	0	00	A0[3:0]_CONFIG2				N0[11:8]_CONFIG2				
0x1B	0	0	0	0	0	0	0	0	00	A0[3:0]_CONFIG3				N0[11:8]_CONFIG3				
0x1C	0	0	0	0	0	0	0	0	00	SP	SH	OE6	OE5	OE4	OE3	OE2	OE1	SP=Shutdown/OE Polarity for SHUTDOWN/OE signal pin, ("0"= Active High (Default), "1"= Active Low); OEx=Output Disable Function for OUTx, ("1"=OUTx disabled based on OE pin (Default for OUT2-6, Disable mode is defined by OEMx bits), "0"= Outputs enabled and no association with OE pin (Default)); OSx=Output Power Suspend function for OUTx, ("1"=OUTx will be suspended on GIN3/SUSPEND pin (MFC="1"), "0"= Always Enabled (Default)); PLLSx=Determines which PLLx to suspend when GIN3 is programmed to be used as SUSPEND, It suspends all the outputs associated with that PLL, ("1"= suspends based on SUSPEND pin, "0"= PLL enabled and no association with SUSPEND pin (Default)); It over-rides OSx bits; SH=Determines the function of the SHUTDOWN/OE signal pin. ("1"=Global Shutdown; this over-rides OEx and OSx bits, "0"=Ouput Enable/Disable (Default)) OKC=clock OK count, "0"=8 cycles, "1"=1024 cycles (Default) of Input Clocks for Revertive Switchover Mode: Address 0x1D, Bit 7; Address 0x1E, Bits [7:3] are reserved and should be set to "0"
0x1D	0	1	0	0	0	0	0	0	40		OKC	OS6	OS5	OS4	OS3	OS2	OS1	
0x1E	0	0	0	0	0	0	0	0	00						PLLS2	PLLS1	PLLS0	

RAM (PROGRAMMING REGISTER) TABLES

	BIT # (Default Settings)									BIT #								
ADDR	7	6	5	4	3	2	1	0	Default Register Hex Value	7	6	5	4	3	2	1	0	DESCRIPTION
0x1F	0	0	0	0	0	0	0	0	00	OEM1[1:0]		SLEW1[1:0]			INV1			Configuring Output OUT1 INV1=Output Inversion for OUT1 ("0"= Non-Invert (Default), "1"=Invert); SLEW1=Slew Rate Settings for OUT1 output ("00"= 2.75V/ns (Default), "01"=2V/ns, "10"=1.25V/ns, "11"=0.7V/ns); OEM1= Output Enable Mode for OUT1 output, when used with OE1 bit and SHUTDOWN/OE pin ("0x" = Tri-state (Default), "10"=Park Low, "11"=Park High); Address 0x1F, Bits 3, 1, 0 are reserved and should be set to "0"
0x20	0	0	0	0	0	0	0	0	00	ODIV1_CONFIG0	IP1[2:0]_CONFIG0			RZ1[3:0]_CONFIG0				PLL1 LOOP FILTER SETTING Loop Filter Values for PLL1 - For 4 Configurations (Default value is '0'); CONFIG0 will be selected if GINx are disabled and operating in MFC mode. ODIV1_CONFIGx=Determines which one of the 2 "Qx-Divider" Configurations to use with, for any of the "Qx-Divider" block associated with PLL1; Used in MFC mode; Default ODIV value is "0", and use CONFIG0 of Qx-Divider; Resistor = 0.3KΩ + RZ1[3:0] * 1KΩ, 0.3 to 15.3kOhm with 1kOhm Step, ("0000"=0.3kOhm, "0001"=1.3kOhm, "0010"=2.3kOhm, ...); Zero capacitor = 6pF + CZ1[3:0] * 27.2pF, 6pF to 414pF with 27.2pF Step, ("0000"=6pF, "0001"=33.2pF, "0010"=60.4pF", ...); Pole capacitor = 1.3pF + CP1[3:0] * 0.75pF, 1.3pF to 12.55pF with 0.75pF Step, ("0000"=1.3pF, "0001"=2.05pF, "0010"=2.8pF, ...) Charge pump current = 5 * 2^IP1[2:0] µA, 5uA to 640uA with 5, 10, 20, 40, ... binary step;
0x21	0	0	0	0	0	0	0	0	00	ODIV1_CONFIG1	IP1[2:0]_CONFIG1			RZ1[3:0]_CONFIG1				
0x22	0	0	0	0	0	0	0	0	00	ODIV1_CONFIG2	IP1[2:0]_CONFIG2			RZ1[3:0]_CONFIG2				
0x23	0	0	0	0	0	0	0	0	00	ODIV1_CONFIG3	IP1[2:0]_CONFIG3			RZ1[3:0]_CONFIG3				
0x24	0	0	0	0	0	0	0	0	00	CP1[3:0]_CONFIG0				CZ1[3:0]_CONFIG0				
0x25	0	0	0	0	0	0	0	0	00	CP1[3:0]_CONFIG1				CZ1[3:0]_CONFIG1				
0x26	0	0	0	0	0	0	0	0	00	CP1[3:0]_CONFIG2				CZ1[3:0]_CONFIG2				
0x27	0	0	0	0	0	0	0	0	00	CP1[3:0]_CONFIG3				CZ1[3:0]_CONFIG3				
0x28	0	0	0	0	0	0	0	0	00	D1[7:0]_CONFIG0								**PLL1 INPUT DIVIDER D1 SETTING** PLL1 D-Divider Values (Prescaler) - For 4 Configurations (Default value is '0');
0x29	0	0	0	0	0	0	0	0	00	D1[7:0]_CONFIG1								
0x2A	0	0	0	0	0	0	0	0	00	D1[7:0]_CONFIG2								
0x2B	0	0	0	0	0	0	0	0	00	D1[7:0]_CONFIG3								
0x2C	0	0	0	0	0	0	0	0	00	N1[7:0]_CONFIG0								PLL1 MULTIPLIER SETTING CONFIG0 will be selected if GINx are disabled and operating in MFC mode. N1[11:0]_CONFIGx - Part of PLL1 M Integer Feedback Divider Values (see equation below) - For 4 Configurations (Default value is '0'); A1[3:0]_CONFIGx - Part of PLL1 M Integer Feedback Divider Values (see equation below) - For 4 Configurations (Default value is '0'); SSC_OFFSET1[5:0] - Spread Spectrum Fractional Multiplier Offset Value. See Spread Spectrum Settings in register address range 0x68-0x6F Total Multiplier Value M1 = 2 * N1[11:0] + A1 + 1 + SS_OFFSET1 * 1/64 When A1[3:0] = 0 and spread spectrum disabled, M1= 2 * N1[11:0]; When A1[3:0] > 0 and spread spectrum disabled, M1 = 2 * N1[11:0] + A1 + 1 ; (Note: A < N-1, i.e. valid M values are 2, 4, 6, 8, 9, 10, 11, 12, 13, ..., 4095 assuming within fPFD and fVCO spec);
0x2D	0	0	0	0	0	0	0	0	00	N1[7:0]_CONFIG1								
0x2E	0	0	0	0	0	0	0	0	00	N1[7:0]_CONFIG2								
0x2F	0	0	0	0	0	0	0	0	00	N1[7:0]_CONFIG3								
0x30	0	0	0	0	0	0	0	0	00	A1[3:0]_CONFIG0				N1[11:8]_CONFIG0				
0x31	0	0	0	0	0	0	0	0	00	A1[3:0]_CONFIG1				N1[11:8]_CONFIG1				
0x32	0	0	0	0	0	0	0	0	00	A1[3:0]_CONFIG2				N1[11:8]_CONFIG2				
0x33	0	0	0	0	0	0	0	0	00	A1[3:0]_CONFIG3				N1[11:8]_CONFIG3				
0x34	0	1	0	0	0	1	1	0	46	SRC2[1:0]		SRC1[1:0]			SM[1:0]		PRIMCLK	PRIMCLK=Priority Selection for Input Clock ("0"=XTALIN/REF_IN becomes Primary (Default), "1"=CLK_IN becomes Primary); SM = Switchover Mode ("0x"=Manual, "10"= Auto-NonRevertive, "11"=Auto-Revertive (Default)); Bit 3 is reserved and should be set to "0".
0x35	0	1	0	1	0	1	0	1	55	SRC6[1:0]		SRC5[1:0]		SRC4[1:0]			SRC3[1:0]	SRCx[1:0]=Input Source Selection for Output Dividers "Qx" blocks ("00"=Selected Input CLK, "01"=PLL0, "10"=PLL1, "11"=PLL2); Default on SRC1 is the selected input clock. Default on SRC2-6 is PLL0 which will be powered down.
0x36																		**No Registers Exist**
0x37																		
0x38	0	0	0	0	0	0	0	0	00	ODIV2_CONFIG0	IP2[2:0]_CONFIG0			RZ2[3:0]_CONFIG0				PLL2 LOOP FILTER SETTING Loop Filter Values for PLL2 - For 4 Configurations (Default value is '0'); CONFIG0 will be selected if GINx are disabled and operating in MFC mode. ODIV2_CONFIGx=Determines which one of the 2 "Qx-Divider" Configurations to use with, for any of the "Qx-Divider" block associated with PLL2; Used in MFC mode; Default ODIV value is "0", and use CONFIG0 of Qx-Divider; Resistor = 0.3KΩ + RZ2[3:0] * 1KΩ, 0.3 to 15.3kOhm with 1kOhm Step, ("0000"=0.3kOhm, "0001"=1.3kOhm, "0010"=2.3kOhm, ...); Zero capacitor = 6pF + CZ2[3:0] * 27.2pF, 6pF to 414pF with 27.2pF Step, ("0000"=6pF, "0001"=33.2pF, "0010"=60.4pF", ...); Pole capacitor = 1.3pF + CP2[3:0] * 0.75pF, 1.3pF to 12.55pF with 0.75pF Step, ("0000"=1.3pF, "0001"=2.05pF, "0010"=2.8pF, ...) Charge pump current = 5 * 2^IP2[2:0] µA, 5uA to 640uA with 5, 10, 20, 40, ... binary step;
0x39	0	0	0	0	0	0	0	0	00	ODIV2_CONFIG1	IP2[2:0]_CONFIG1			RZ2[3:0]_CONFIG1				
0x3A	0	0	0	0	0	0	0	0	00	ODIV2_CONFIG2	IP2[2:0]_CONFIG2			RZ2[3:0]_CONFIG2				
0x3B	0	0	0	0	0	0	0	0	00	ODIV2_CONFIG3	IP2[2:0]_CONFIG3			RZ2[3:0]_CONFIG3				
0x3C	0	0	0	0	0	0	0	0	00	CP2[3:0]_CONFIG0				CZ2[3:0]_CONFIG0				
0x3D	0	0	0	0	0	0	0	0	00	CP2[3:0]_CONFIG1				CZ2[3:0]_CONFIG1				
0x3E	0	0	0	0	0	0	0	0	00	CP2[3:0]_CONFIG2				CZ2[3:0]_CONFIG2				
0x3F	0	0	0	0	0	0	0	0	00	CP2[3:0]_CONFIG3				CZ2[3:0]_CONFIG3				

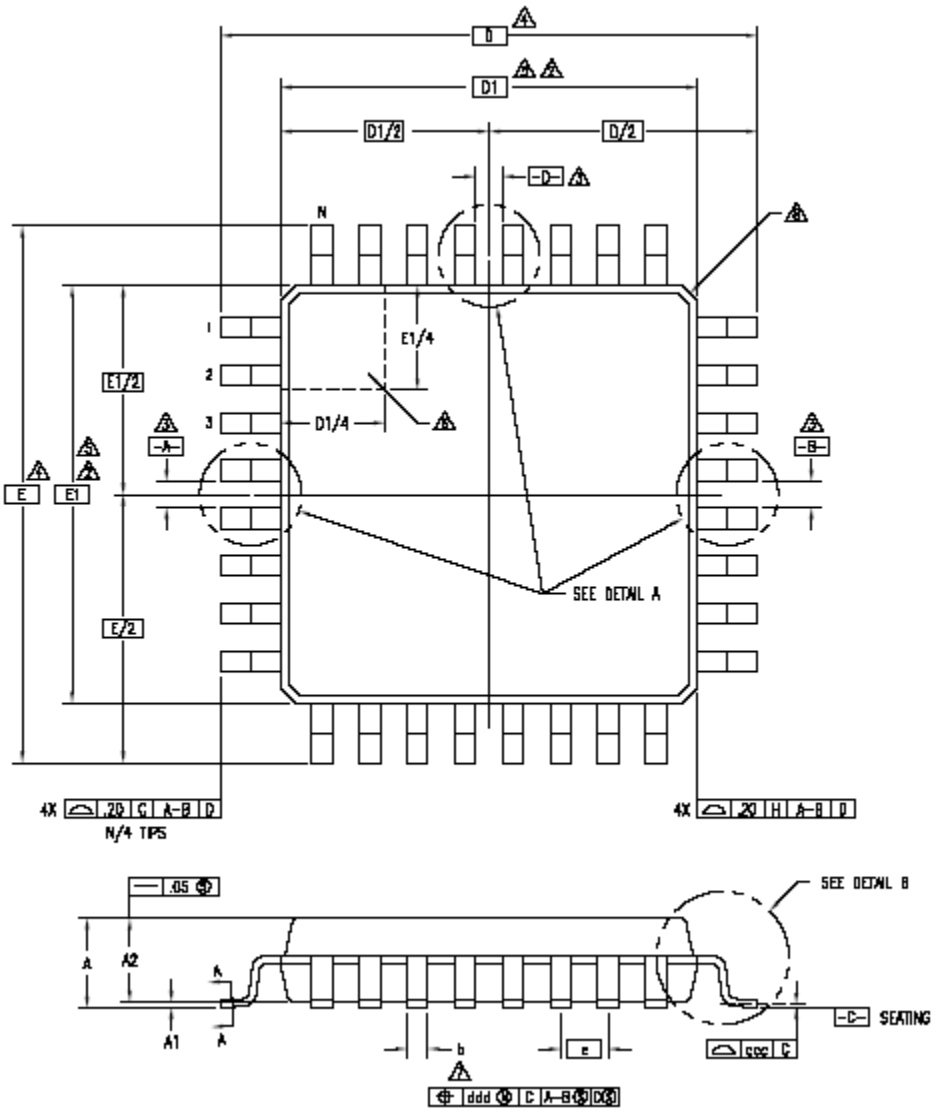
RAM (PROGRAMMING REGISTER) TABLES

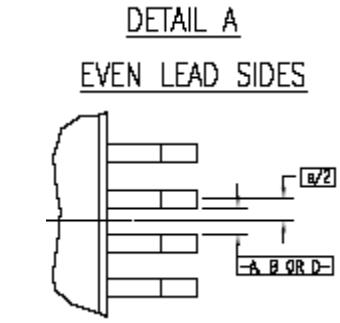
	BIT #								BIT #								
ADDR	7	6	5	4	3	2	1	0	Register Hex Value	7	6	5	4	3	2	1	0	DESCRIPTION
0x40	0	0	0	0	0	0	0	0	00	D2[7:0]_CONFIG0								PLL2 INPUT DIVIDER D2 SETTING
0x41	0	0	0	0	0	0	0	0	00	D2[7:0]_CONFIG1								
0x42	0	0	0	0	0	0	0	0	00	D2[7:0]_CONFIG2								
0x43	0	0	0	0	0	0	0	0	00	D2[7:0]_CONFIG3								
0x44	0	0	0	0	0	0	0	0	00	N2[7:0]_CONFIG0								PLL2 MULTIPLIER SETTING Total Multiplier Value
0x45	0	0	0	0	0	0	0	0	00	N2[7:0]_CONFIG1								
0x46	0	0	0	0	0	0	0	0	00	N2[7:0]_CONFIG2								
0x47	0	0	0	0	0	0	0	0	00	N2[7:0]_CONFIG3								
0x48	0	0	0	0	0	0	0	0	00					N2[11:8]_CONFIG0				
0x49	0	0	0	0	0	0	0	0	00					N2[11:8]_CONFIG1				
0x4A	0	0	0	0	0	0	0	0	00					N2[11:8]_CONFIG2				
0x4B	0	0	0	0	0	0	0	0	00					N2[11:8]_CONFIG3				
0x4C	0	0	0	0	0	0	0	0	00	OEM2[1:0]		SLEW2[1:0]			INV2			INVx PMx OEMx Qx SLEWx Configuring Output OUT2 INV2=Output Inversion for OUT2 ("0"= Non-Invert (Default), "1"=Invert); SLEW2=Slew Rate Settings for OUT2 output ("00"= 2.75V/ns (Default), "01"=2V/ns, "10"=1.25V/ns, "11"=0.7V/ns); INV5_1=Output Inversion for /OUT5 ("0"= Invert, "1"=Non-Invert (Default)); INV5_0=Output Inversion for OUT5 ("0"= Invert, "1"=Non-Invert (Default)); SLEW5=Slew rate settings for OUT5 output ("00"= 2.75V/ns (Default), "01"=2V/ns, "10"=1.25V/ns, "11"=0.7V/ns); OEM5= Output Enable Mode for OUT5 output, when used with OE5 bit and SHUTDOWN/OE pin ("0x" = Tri-state (Default), "10"=Park Low, "11"=Park High); LVL5=Output IO Standard Selection, ("00"=LVTTL (Default), "01"=LVDS, "10"=LVPECL, "11"=Reserved); Q5[x:x]=Output Divider "Q5" Values (Default value is '2') - Support 2 output configurations when used in MFC mode; PM5[xx]=Divide Mode, ("00"=Divider Disabled;"01"=Divide by '1';"10"=Divide by 2; "11"=Divide by (Q+2) (Default)); (Note: To enable OUT5, PM5 register bit values for both CONFIG0 and CONFIG1 configurations must be non-zero.)
0x4D	1	0	1	1	1	0	1	1	BB	Q2[1:0]_CONFIG1		PM2[1:0]_CONFIG1		Q2[1:0]_CONFIG0			PM2[1:0]_CONFIG0	
0x4E	0	0	0	0	0	0	0	0	00	Q2[9:2]_CONFIG0								
0x4F	0	0	0	0	0	0	0	0	00	Q2[9:2]_CONFIG1								
0x50	0	0	0	0	0	0	0	0	00	OEM3[1:0]		SLEW3[1:0]			INV3			Configuring Output OUT3 INV3=Output Inversion for OUT3 ("0"= Non-Invert (Default), "1"=Invert); SLEW3=Slew Rate Settings for OUT3 output ("00"= 2.75V/ns (Default), "01"=2V/ns, "10"=1.25V/ns, "11"=0.7V/ns);
0x51	1	0	1	1	1	0	1	1	BB	Q3[1:0]_CONFIG1		PM3[1:0]_CONFIG1		Q3[1:0]_CONFIG0			PM3[1:0]_CONFIG0	
0x52	0	0	0	0	0	0	0	0	00	Q3[9:2]_CONFIG0								
0x53	0	0	0	0	0	0	0	0	00	Q3[9:2]_CONFIG1								
0x54	0	0	0	0	1	1	0	0	0C	OEM4[1:0]		SLEW4[1:0]		INV4_1	INV4_0		LVL4[1:0]	Configuring Output OUT4 INV4_1=Output Inversion for /OUT4 ("0"= Invert , "1"=Non-Invert (Default)); INV4_0=Output Inversion for OUT4 ("0"= Invert , "1"=Non-Invert (Default));
0x55	1	0	1	1	1	0	1	1	BB	Q4[1:0]_CONFIG1		PM4[1:0]_CONFIG1		Q4[1:0]_CONFIG0			PM4[1:0]_CONFIG0	
0x56	0	0	0	0	0	0	0	0	00	Q4[9:2]_CONFIG0								
0x57	0	0	0	0	0	0	0	0	00	Q4[9:2]_CONFIG1								
0x58	0	0	0	0	1	1	0	0	0C	OEM5[1:0]		SLEW5[1:0]		INV5_1	INV5_0		LVL5[1:0]	Configuring Output OUT5 INV5_1=Output Inversion for /OUT5 ("0"= Invert, "1"=Non-Invert (Default)); INV5_0=Output Inversion for OUT5 ("0"= Invert, "1"=Non-Invert (Default)); When using LVPECL or LVDS outputs, SLEW5 must be set to '00'.
0x59	1	0	1	1	1	0	1	1	BB	Q5[1:0]_CONFIG1		PM5[1:0]_CONFIG1		Q5[1:0]_CONFIG0			PM5[1:0]_CONFIG0	
0x5A	0	0	0	0	0	0	0	0	00	Q5[9:2]_CONFIG0								
0x5B	0	0	0	0	0	0	0	0	00	Q5[9:2]_CONFIG1								
0x5C	0	0	0	0	0	0	1	1	03	OEM6[1:0]		SLEW6[1:0]			INV6			
0x5D	1	0	1	1	1	0	1	1	BB	Q6[1:0]_CONFIG1		PM6[1:0]_CONFIG1		Q6[1:0]_CONFIG0			PM6[1:0]_CONFIG0	
0x5E	0	0	0	0	0	0	0	0	00	Q6[9:2]_CONFIG0								
0x5F	0	0	0	0	0	0	0	0	00	Q6[9:2]_CONFIG1								

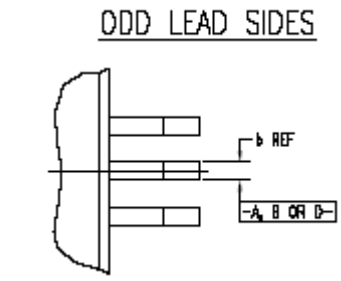
RAM (PROGRAMMING REGISTER) TABLES

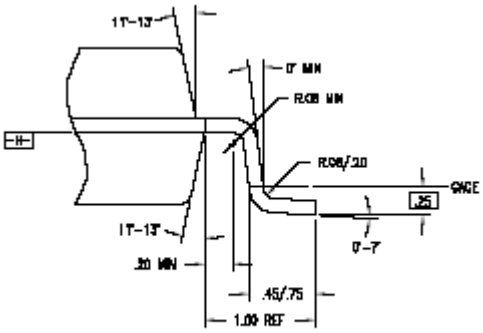
	BIT # (Default Settings)									BIT #								
ADDR	7	6	5	4	3	2	1	0	Default Register Hex Value	7	6	5	4	3	2	1	0	DESCRIPTION
0x60	0	0	0	0	0	0	0	0	00	TSSC0[3:0]				NSSC0[3:0]				
0x61	0	0	0	0	0	0	0	0	00	DITH0	X2_0	SS_OFFSET0[5:0]						
0x62	0	0	0	0	0	0	0	0	00	SD0[3:0][1]				SD0[3:0][0]				
0x63	0	0	0	0	0	0	0	0	00	SD0[3:0][3]				SD0[3:0][2]				**SPREAD SPRECTRUM SETTINGS FOR PLL0** SS_OFFSET0=SS Fractional Offset/ First Sample (Unsigned); TSSC0=# of PFD Cycles Per SS Cycle Step, TSSC="0000" for SSC off (Default); NSSC0=# of SS Samples to Use from SS Memory (Default is "0"); DITH0=LSB DITHER on Σ, ("1"=dither on, "0"=off (Default)); X2_0=ΣΔ output x2, ("1"=x2, "0"=normal (Default)); SD0=Delta-encoded samples (unsigned); Waveform start with SS_OFFSET0, then SS_OFFSET0+SD0[0], etc. (Default is "0");
0x64	0	0	0	0	0	0	0	0	00	SD0[3:0][5]				SD0[3:0][4]				
0x65	0	0	0	0	0	0	0	0	00	SD0[3:0][7]				SD0[3:0][6]				
0x66	0	0	0	0	0	0	0	0	00	SD0[3:0][9]				SD0[3:0][8]				
0x67	0	0	0	0	0	0	0	0	00	SD0[3:0][11]				SD0[3:0][10]				
0x68	0	0	0	0	0	0	0	0	00	TSSC1[3:0]				NSSC1[3:0]				
0x69	0	0	0	0	0	0	0	0	00	DITH1	X2_1	SS_OFFSET1[5:0]						
0x6A	0	0	0	0	0	0	0	0	00	SD1[3:0][1]				SD1[3:0][0]				
0x6B	0	0	0	0	0	0	0	0	00	SD1[3:0][3]				SD1[3:0][2]				**SPREAD SPRECTRUM SETTINGS FOR PLL1** SS_OFFSET1=SS Fractional Offset/ First Sample (Unsigned); TSSC1=# of PFD Cycles Per SS Cycle Step, TSSC="0000" for SSC off (Default); NSSC1=# of SS Samples to Use from SS Memory (Default is "0"); DITH1=LSB DITHER on ΣΔ, ("1"=dither on, "0"=off (Default)); X2_1=ΣΔ output x2, ("1"=x2, "0"=off (Default)); SD1=Delta-encoded samples (unsigned); Waveform start with SS_OFFSET1, then SS_OFFSET1+SD1[0], etc. (Default is "0");
0x6C	0	0	0	0	0	0	0	0	00	SD1[3:0][5]				SD1[3:0][4]				
0x6D	0	0	0	0	0	0	0	0	00	SD1[3:0][7]				SD1[3:0][6]				
0x6E	0	0	0	0	0	0	0	0	00	SD1[3:0][9]				SD1[3:0][8]				
0x6F	0	0	0	0	0	0	0	0	00	SD1[3:0][11]				SD1[3:0][10]				
0x70																		No Registers Exist
0x71																		
0x72																		
0x73																		
0x74																		
0x75																		
0x76																		
0x77																		
0x78																		
0x79																		
0x7A																		
0x7B																		
0x7C																		
0x7D																		
0x7E																		
0x7F																		
0x80																		
0x81												CERR						CRC error in EEPROM CERR = CRC error bit indicator ("1" = CRC error) Read-Only

Package Outline and Package Dimensions (32-pin TQFP)



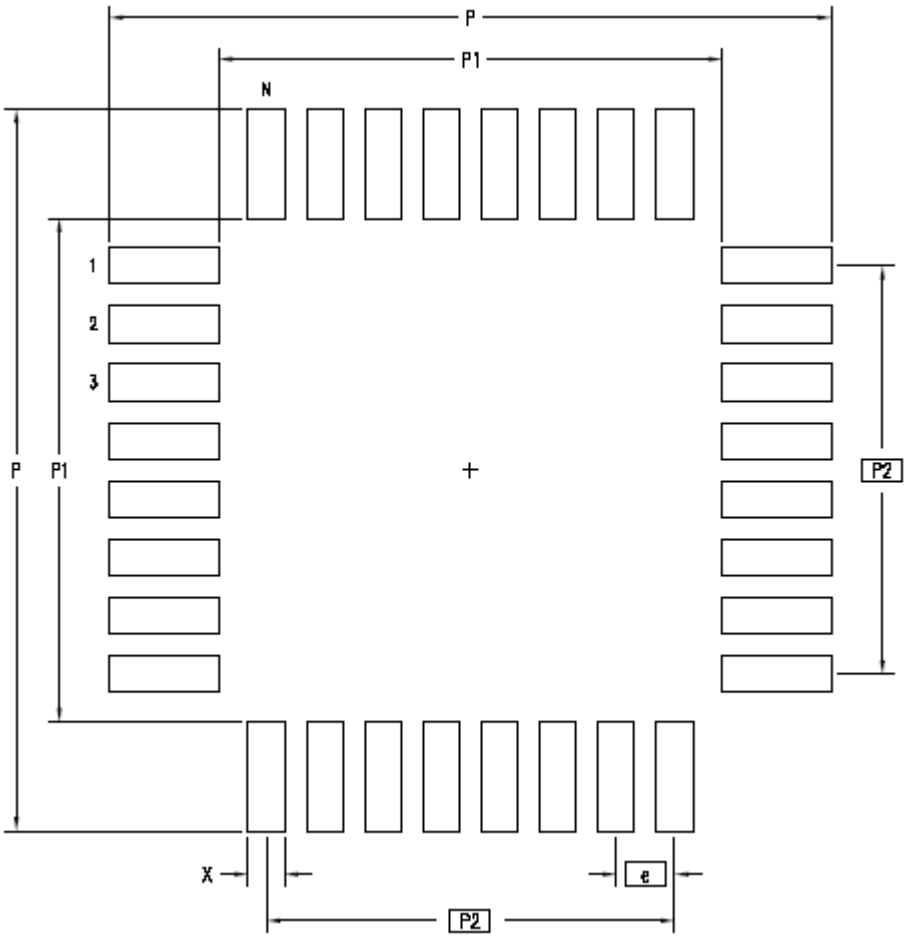






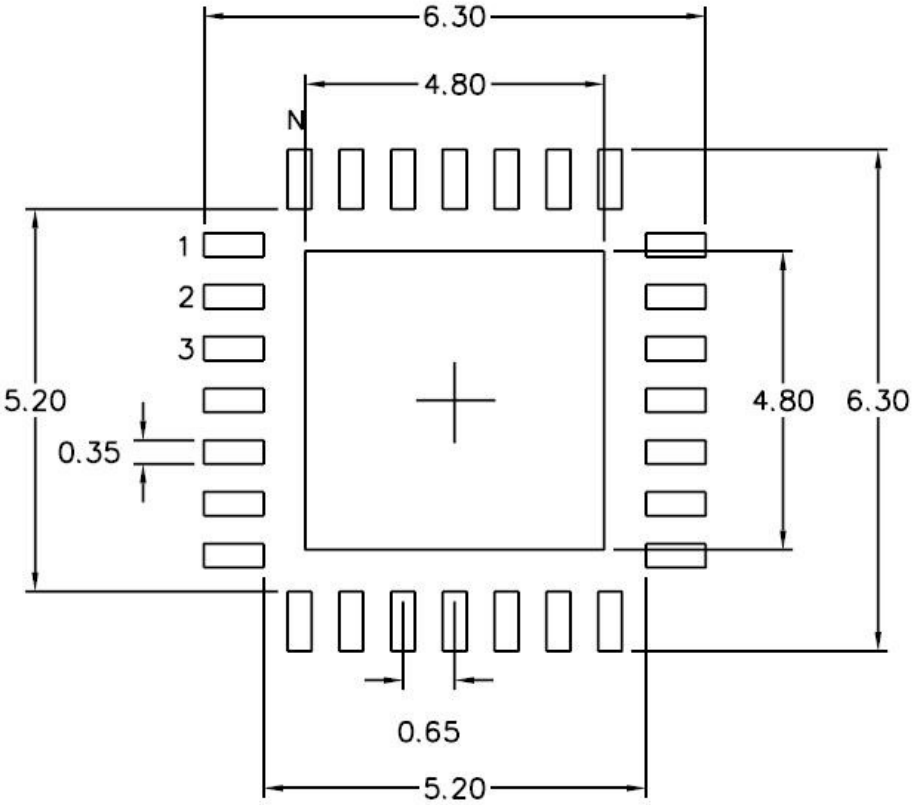
SYMBOL	JEDEC VARIATION BBA			NOTE
	MIN	NOM	MAX	
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	9.00 BSC			4
D1	7.00 BSC			5,2
E	9.00 BSC			4
E1	7.00 BSC			5,2
N	32			
e	.80 BSC			
b	.30	.37	.45	7
b1	.30	.35	.40	
ccc	–	–	.10	
ddd	–	–	.20	

RECOMMENDED LANDING PATTERN, 32-pin TQFP



	MIN	MAX
P	9.80	10.00
P1	6.80	7.00
P2	5.60 BSC	
X	.40	.60
e	.80 BSC	
N	32	

RECOMMENDED LANDING PATTERN, 28-pin VFQFPN



NL 28 pin

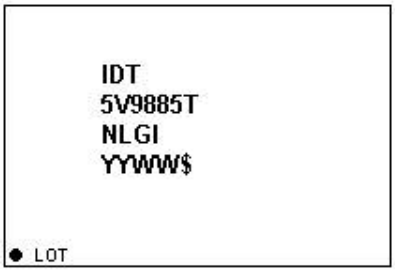
NOTE: All dimensions are in millimeters.

ORDERING INFORMATION

Part Number	Shipping Packaging	Package	Temperature
5V9885TPFGI	Tubes	32-pin TQFP	-40 to +85°C
5V9885TPFGI8	Tape and Reel	32-pin TQFP	-40 to +85°C
5V9885TNLGI	Tubes	28-pin VFQFPN	-40 to +85°C
5V9885TNLGI8	Tape and Reel	28-pin VFQFPN	-40 to +85°C

MARKING DIAGRAM (5V9885TPFGI)

MARKING DIAGRAM (5V9885TNLGI)



NOTES:
1. 'YYWW' is the date code.
2. '$' is the assembly mark code.
3. 'G' denotes RoHS compliant package.
4. 'I' denotes industrial temperature range.
5. Bottom marking: country of origin.

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