



**THE DATASHEET OF
74ABT240CMTCX**



74ABT240

Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The ABT240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

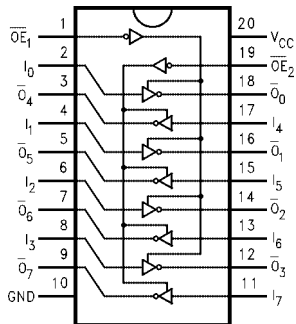
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code:

Order Number	Package Number	Package Description
74ABT240CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ABT240CSJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT240CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ABT240CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
I_0-I_7	Inputs
$\overline{O}_0-\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
\overline{OE}_1	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
\overline{OE}_2	I_n	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

74ABT240 Octal Buffer/Line Driver with 3-STATE Outputs

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current (Across Comm Operating Range)	-150 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.5			V	Min	I _{OH} = -3 mA
		2.0			V	Min	I _{OH} = -32 mA
V _{OL}	Output LOW Voltage		0.55		V	Min	I _{OL} = 64 mA
I _{IH}	Input HIGH Current		1		μA	Max	V _{IN} = 2.7V (Note 3)
			1		μA	Max	V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-1	μA	Max	V _{IN} = 0.5V (Note 3)
				-1	μA	Max	V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current			10	μA	0 - 5.5V	V _{OUT} = 2.7V; $\overline{OE}_n = 2.0V$
I _{OZL}	Output Leakage Current			-10	μA	0 - 5.5V	V _{OUT} = 0.5V; $\overline{OE}_n = 2.0V$
I _{OS}	Output Short-Circuit Current	-100		-275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			50	μA	Max	$\overline{OE}_n = V_{CC}$; All Others at V _{CC} or Ground
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled		1.5	mA	Max	V _I = V _{CC} - 2.1V
		Outputs 3-STATE		1.5	mA		Enable Input V _I = V _{CC} - 2.1V
		Outputs 3-STATE		50	μA		Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or Ground
I _{CCD}	Dynamic I _{CC} (Note 3)	No Load		0.1	mA/ MHz	Max	Outputs Open $\overline{OE}_n = GND$, (Note 4) One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed, but not tested.

Note 4: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

AC Electrical Characteristics

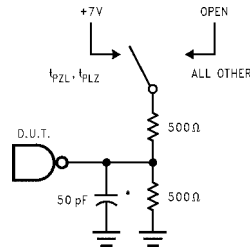
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.0		4.8	0.8	5.5	1.0	4.8	ns
t_{PHL}	Data to Outputs	1.6		4.8	1.0	5.5	1.6	4.8	
t_{PZH}	Output Enable	1.1		6.2	0.8	7.5	1.1	6.2	ns
t_{PZL}	Time	1.1		6.2	0.8	7.7	1.1	6.2	
t_{PHZ}	Output Disable	1.8		6.4	1.0	7.5	1.8	6.4	ns
t_{PLZ}	Time	1.6		5.8	1.0	7.2	1.6	5.8	

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0\text{V}$
C_{OUT} (Note 5)	Output Capacitance	9.0	pF	$V_{CC} = 5.0\text{V}$

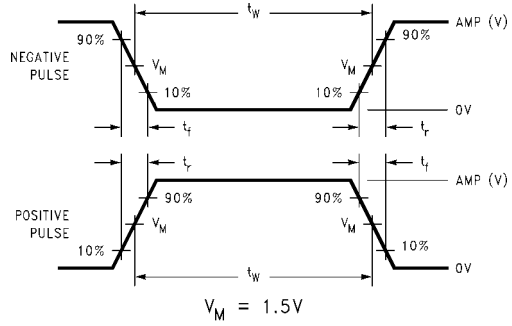
Note 5: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

Standard AC Test Load

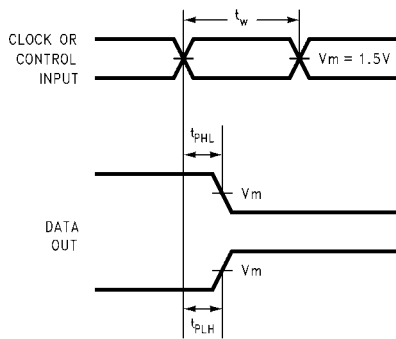


Test Input Signal Levels

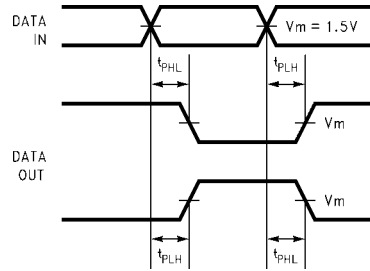
Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

Test Input Signal Requirements

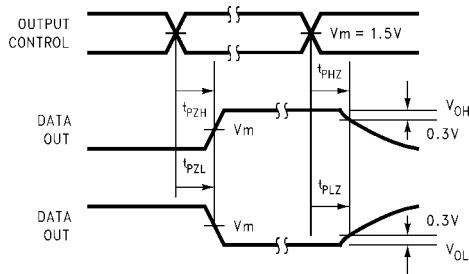
AC Waveforms



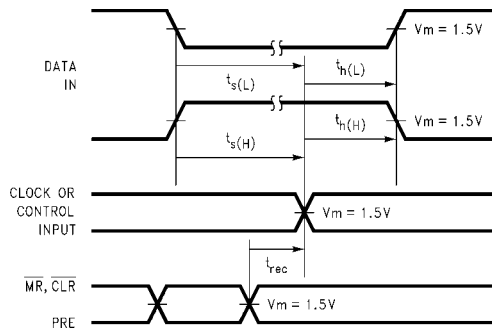
Propagation Delay, Pulse Width Waveforms



Propagation Delay Waveforms for Inverting and Non-Inverting Functions

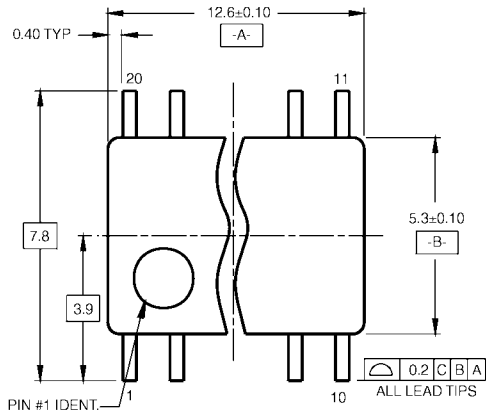


3-STATE Output HIGH and LOW Enable and Disable Times

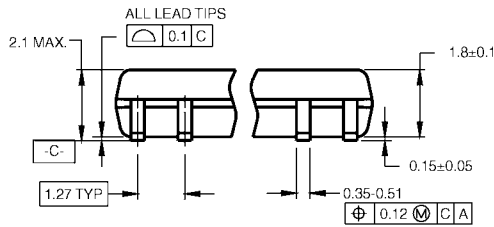


Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



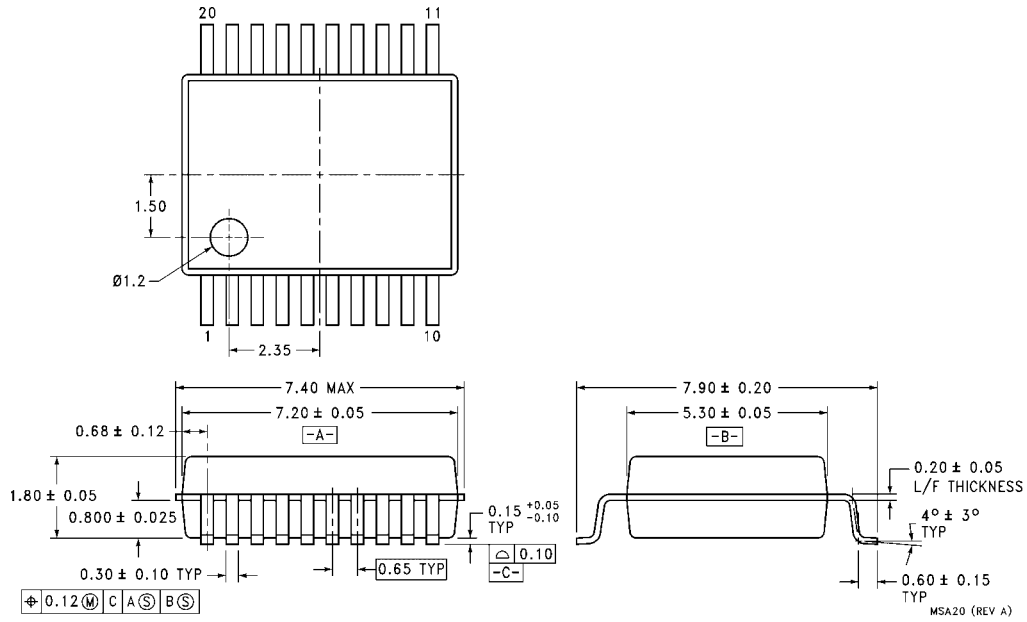
DETAIL A

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

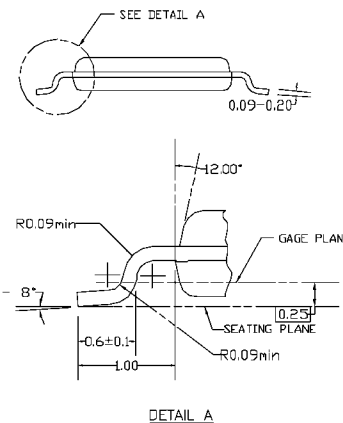
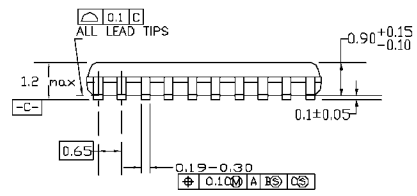
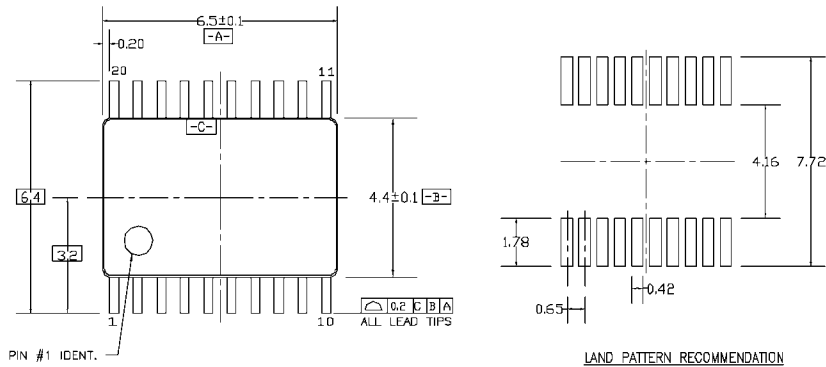
Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
 Package Number MSA20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

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