THE DATASHEET OF

SC2618SKTRT

SC2618
Miniature PWM Controller for Buck Regulator

Description

The SC2618 is a hysteretic mode PWM controller designed for high efficiency, low cost “Point of Load” applications.

The hysteretic control scheme allows the use of ceramic output capacitors without the need for compensation components and difficult calculations.

An internal soft start prevents output voltage from start up overshoot. A “Hiccup” short circuit protection provides protection against output short circuits as well as adverse input supply sequencing.

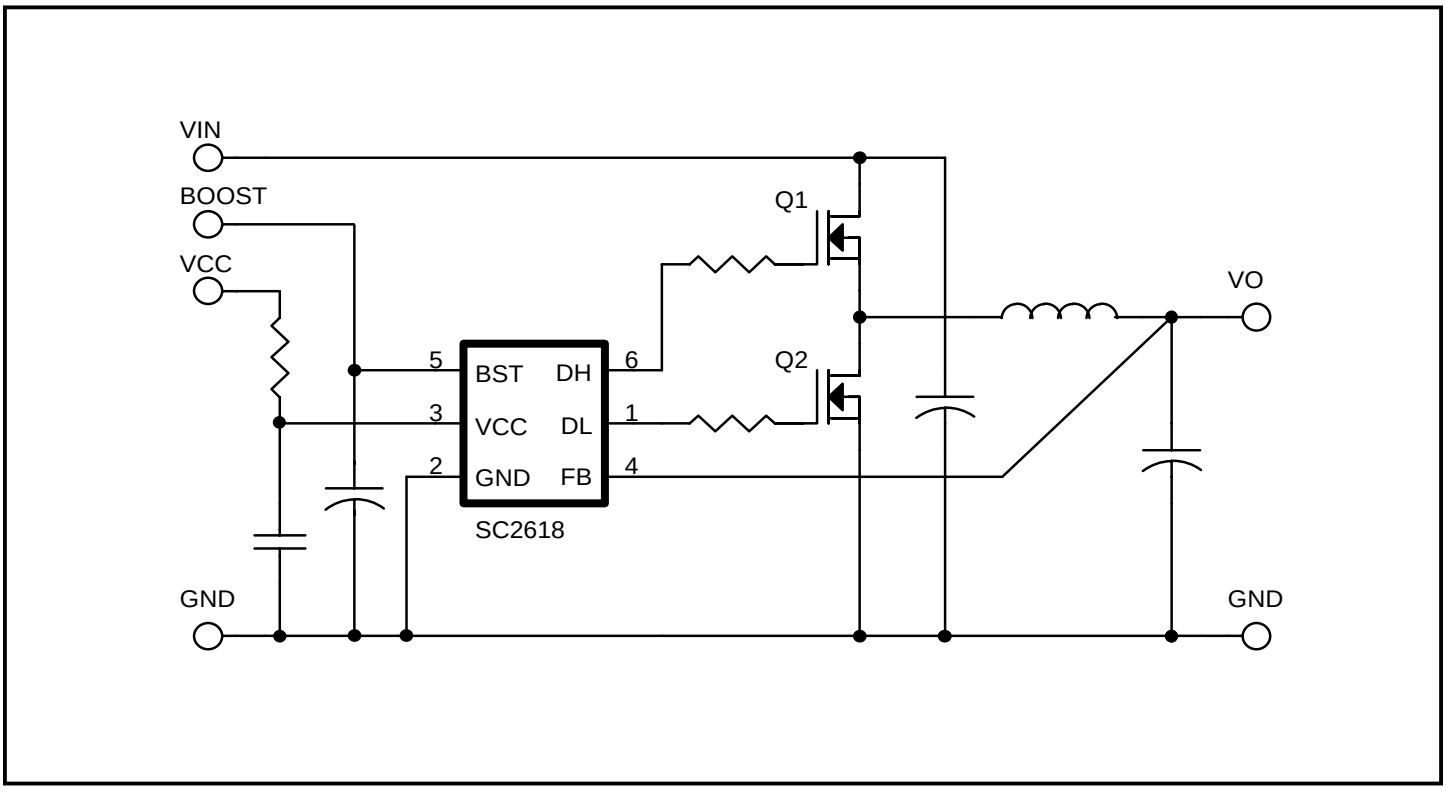
Features

- Operating Frequency up to 500kHz
- Input supply from 5V to 12V
- 0.5A gate drive capability
- Internal soft start
- Internal, trimmed bandgap reference (±1%)
- Hiccup mode short circuit protection
- Input supply sequence protection
- 6 lead SOT23 package

Applications

- Graphics IC Power supplies
- Embedded, low cost, high efficiency converters

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V_{CC}	15	V
Boost Supply Voltage	V_{BST}	30	V
FB Voltage	V_{FB}	8	V
DL to GND	V_{DL}	-1 to V_{CC} +0.3	V
DH to GND	V_{DH}	-1 to V_{BST} +0.3	V
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to 125	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (Soldering) 10s	T_{LEAD}	300	°C
Thermal Resistance Junction to Ambient	θ_{JA}	96 (1)	°C/W
Thermal Resistance Junction to Case	θ_{JC}	62	°C/W
ESD Rating (Human Body Model)	ESD	2	kV

Note: (1) 1 square inch of FR4, double sided, 1oz, minimum copper weight

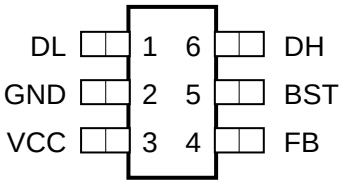
Electrical Characteristics

Unless specified: $V_{CC} = V_{IN}$ = 5V, V_{BST} = 12V, $V_{FB} = V_O$; T_A = 25°C. Values in **bold** are over full operating temperature range.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
VCC Supply Voltage	VCC			4.75		14	V
VCC Quiescent Current	IQVCC	V_{CC} = 5.0V, V_{REF} = 0V, V_{FB} = 100mV			5	10	mA
VCC Under Voltage Lockout	UVVCC			4.0	4.2	4.5	V
Boost Supply Voltage	VBST					29	V
Boost Quiescent Current	I_{QBST}	V_{FB} = 1.200V			3		mA
Soft Start Time	Tss				100		us
Output Voltage	VO	IO = 20mA; $V_{FB} = V_O$		1.237	1.250	1.263	V
				1.225		**1.275**	
Load Regulation		IO = 0.2A to 4A			1		%
Line Regulation					±0.5		%
Short Circuit Trip Voltage	VSCT				1.05		V
Minimum ON/OFF Time	tDEL				1		us
FB bias current	IFB	VFB = 1.25V				-1	uA
Peak DH Sink/Source Current		BST - DH = 4.5V,	DH - GND = 3.5V DH - GND = 1.5V	0.5 50			A mA
Peak DL Sink/Source Current		BST - DL = 4.5V,	DL - GND = 3.5V DL - GND = 1.5V	0.5 50			A mA
DH, DL NonoverlappingTime		C_{LOAD} =1000pF; Measured at DH/DL = 2V		20	50		ns

Pin Configuration

TOP VIEW



(SOT-23 6L)

Ordering Information

Part Numbers	Package
SC2618SKTRT(1)(2)	SOT23-6

Notes:

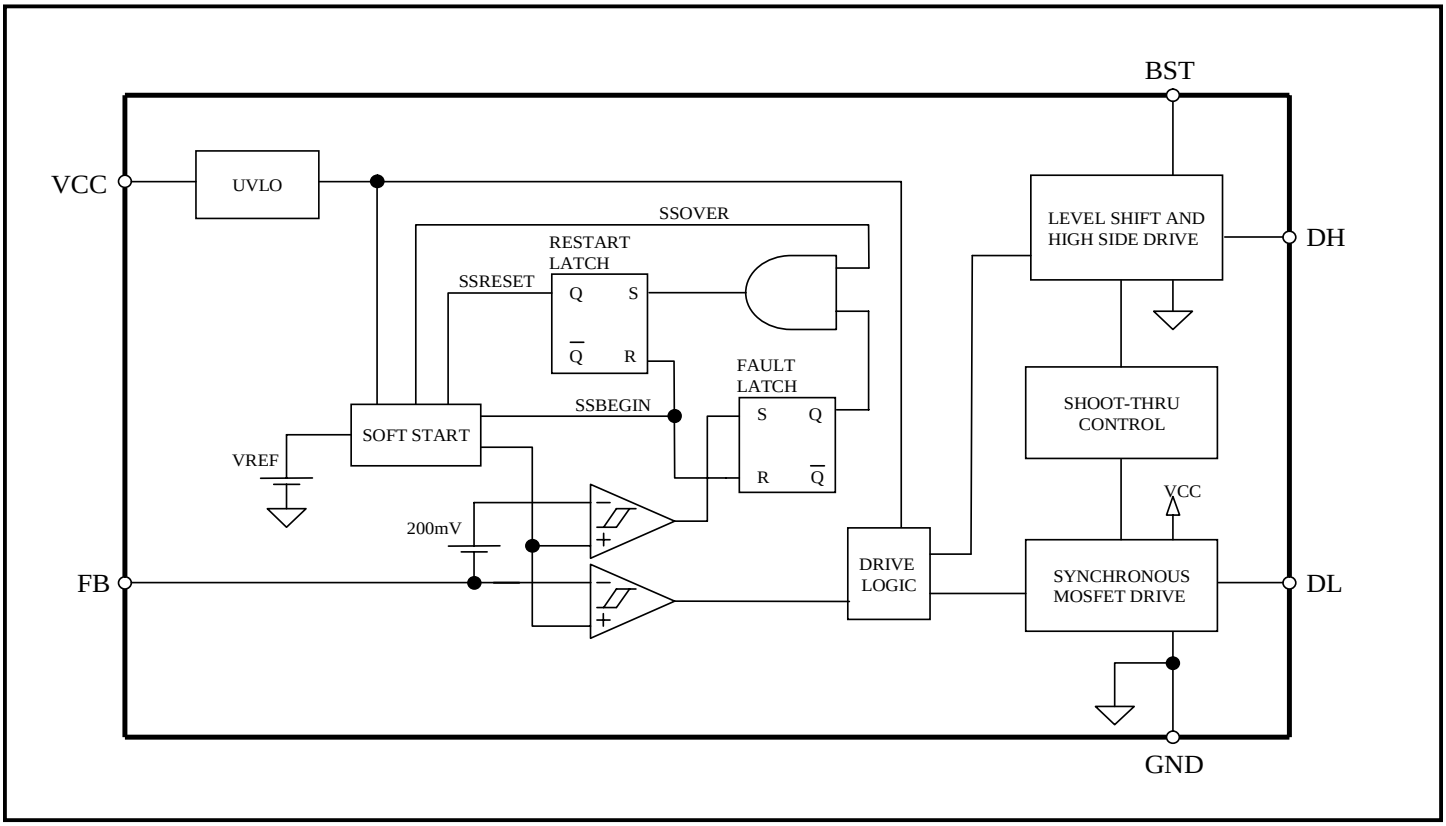
(1) Only available in tape and reel packaging. A reel contains 3000 devices.

(2) SC2618SKTRT is the lead free version. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	DL	Low side FET drive output.
2	GND	Analog and Power Ground, connect directly to ground plane, see layout guidelines.
3	VCC	Chip Supply Input Voltage and Low Side FET drive supply.
4	FB	Feedback input.
5	BST	Supply voltage for high gate driver.
6	DH	High Side FET drive output.

Block Diagram



Theory of Operation

The SC2618 is a hysteretic mode PWM controller. It uses a comparator to generate PWM wave with minimum on time and off time control. As shown in the block diagram, the output voltage is fed back to the comparator negative input and compared to a setting voltage. If the output voltage is below its set point, the top gate drive will turn on and remain on until the minimum on time has expired AND the output voltage has risen above the set point. Similarly, if the output voltage is above its set point, top gate drive will be turned off and bottom gate will turn on and stay on until the minimum off time has expired AND the output is below its set point. Because of this minimum time control scheme, the comparator hysteresis is not required and is internally set to zero.

Switching Frequency vs. Duty Cycle

This control scheme will force a buck converter to operate either at minimum on time, or minimum off time, or both. The SC2618 has minimum time of 1us. Its switching frequency, peaking at 500kHz, can be found in Fig. 1 as long as the voltage ratio of the buck converter has been decided.

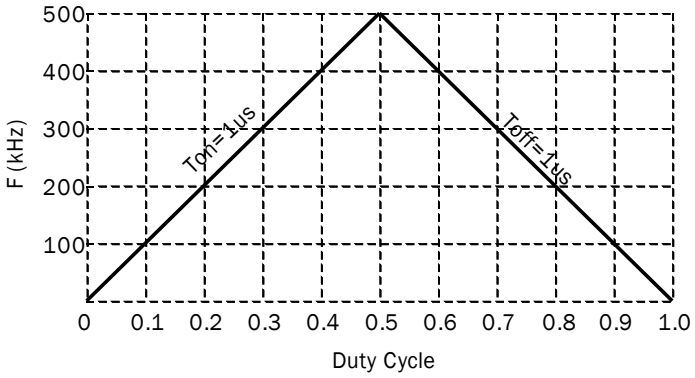


Fig. 1. Switching frequency vs. duty cycle

UVLO, Start up and Shut down

To initiate the SC2618, supply voltages are applied to Vcc and BST pins. The top gate (DH) and bottom gate (DL) are held low until Vcc exceed UVLO threshold, typically 4.5V. At that point, the internal soft start capacitor begins to charge, the top gate remains low, and the bottom gate is pulled high to turn on the bottom FET. When the voltage at soft start cap reaches a setting level, the top and bottom gates of PWM controller begin to switch. The switching regulator output is slowly ramping up for a soft turn on. If, however, one or more supply voltage rails are late or absent, the output voltage will not rise and the part will behave as if there was a short circuit at the output, that is, it will go into hiccup mode. It will remain in this mode until all the necessary voltage rails are present, at which time normal operation will start.

If the supply voltage Vcc falls below UVLO threshold during normal operation, the soft start capacitor begins to discharge. When the voltage reaches the setting level, the PWM controller control the switching regulator output to ramp down slowly for a soft turn off.

Hiccup Mode Short Circuit Protection

Short circuit protection is implemented by comparing the feedback node with the soft start and reference voltage. If the FB voltage falls more than about 200mV below it's correct voltage the short circuit latch is set which immediately disables the top drive. If the short circuit occurred during soft start, the soft start capacitor continues to charge to it's full voltage before discharging towards zero. If the short occurred during steady state operation, the internal soft start capacitor begins to discharge immediately, at the same rate as it charged, towards zero. Once the soft start capacitor reaches its minimum voltage, the latches are cleared and a normal soft start is attempted, if the short circuit condition has not been cleared, the fault latch will again be set once the soft start voltage reaches about 200mV and the cycle will repeat until the short is cleared.

It is also possible, with large output capacitor values, that the output voltage will be unable to rise fast enough to accurately follow the soft start voltage and a short circuit trip may result. During soft start the bottom gate drive is disabled to prevent discharging the output capacitor and so the output capacitor will retain the voltage achieved before the trip and will charge to a higher voltage during the next hiccup cycle. In this way the output voltage will achieve the set point value but may take several hiccup cycles to do so.

Component Selection

General design guideline of switching power supplies can be applied to the component selection for SC2618.

Output Filter Components

The purpose of soft start is to control inductor current during start up, this in turn controls the amount of excess charge the output capacitor will receive and therefore the output voltage overshoot that will occur at the end of soft start.

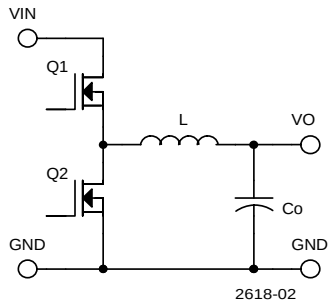


Fig. 2. Output filter components

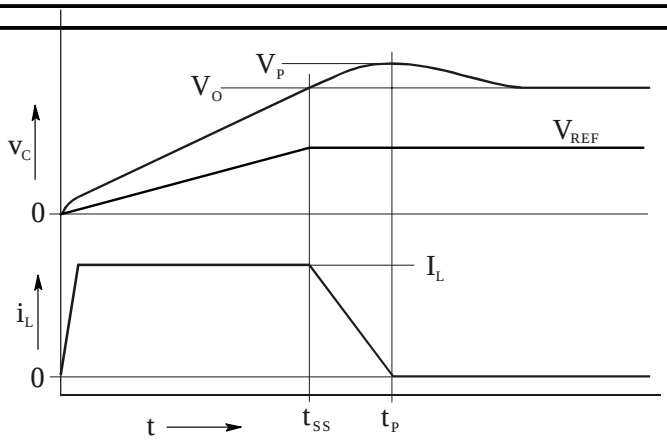


Fig. 3. Soft start, inductor current and overshoot

Normally, controllers with an external soft start capacitor, have soft start set so long that overshoot is undetectable. Since the soft start for the SC2618 is internal, it is necessarily limited and the maximum values of L and Co should meet the constraints of:

$$L \cdot C_O = \frac{t_{SS}^2 \cdot X_S}{50}$$

where tss is soft start time, 100us typically, and Xs is the percentage overshoot allowable.

Inductor and MOSFETs

The selection of inductor and MOSFETs should meet thermal requirement because they are power loss dominant components. Pick an inductor with as high inductance as possible if without adding extra cost and size. Higher inductance, lower ripple current, smaller core loss and higher efficiency. However, too high inductance slows down output transient response. It is recommended to choose the inductance that gives the inductor ripple current to be approximate 20% of maximum load current. So choose inductor value from:

$$L = \frac{5}{I_O \cdot f_{osc}} \cdot V_O \cdot (1 - \frac{V_O}{V_{IN}})$$

The MOSFETs are selected from their Rdson, gate charge, and package. The SC2618 provides 0.5A gate drive current. To drive a 25nC gate charge MOSFET gives 25nC/0.5A=50ns switching time. The switching time ts contributes to the top MOSFET switching loss:

$$P_S = I_O \cdot V_{IN} \cdot t_S \cdot f_{OSC}$$

There is no switching loss for the bottom MOSFET because of its zero voltage switching. The conduction losses of the top and bottom MOSFETs are given by:

$$P_{C\_TOP} = I_O^2 \cdot R_{dson} \cdot D$$

$$P_{C\_BOT} = I_O^2 \cdot R_{dson} \cdot (1 - D)$$

If the requirement of total power losses for each MOSFET is given, the above equations can be used to calculate the values of Rdson and gate charge can be calculated using above equations, then the devices can be determined accordingly. The solution should ensure the MOSFET is within its maximum junction temperature at highest ambient temperature.

Output Capacitor(s)

The output capacitors should be selected to meet both output ripple and transient response criteria. The output capacitor ESR causes output ripple VRIPPLE during the inductor ripple current flowing in. To meet output ripple criteria, the ESR value should be:

$$R_{ESR} < \frac{L \cdot f_{OSC} \cdot V_{RIPPLE}}{V_O \cdot (1 - \frac{V_O}{V_{IN}})}$$

Component Selection (Cont.)

The output capacitor ESR also causes output voltage transient V_T during a transient load current I_T flowing in. To meet output transient criteria, the ESR value should be:

$$R_{ESR} < \frac{V_T}{I_T}$$

To meet both criteria, the smaller one of above two ESRs is required.

The output capacitor value also contributes to load transient response. Based on a worst case where the inductor energy 100% dumps to the output capacitor during the load transient, the capacitance then can be calculated by:

$$C > L \cdot \frac{I_T^2}{V_T^2}$$

Input Capacitor

The input capacitor should be chosen to handle the RMS ripple current of a synchronous buck converter. This value is given by:

$$I_{RMS} = \sqrt{(1-D) \cdot I_{IN}^2 + D \cdot (I_o - I_{IN})^2}$$

where I_O is the load current, I_{IN} is the input average current, and D is the duty cycle. Choosing low ESR input capacitors will help maximize ripple rating for a given size.

Bootstrap Circuit

The SC2618 uses an external bootstrap circuit to provide a voltage at BST pin for the top MOSFET drive. This voltage is held up by a bootstrap capacitor. Typically, it is recommended to use a 1uF ceramic capacitor with 25V rating and a commonly available diode IN4148 for the bootstrap circuit.

Filter for Vcc Supply Power

For the pin of Vcc, it is recommended to use a 1uF/25V ceramic capacitor for decoupling. In addition, place a small resistor (10 ohm) in between Vcc pin and the supply power for noise reduction.

Divider Ratio

The top resistor of the voltage divider can be chosen from 5k to 15k. Then the bottom resistor is found from

$$R_{bot} = \frac{1.25V}{V_O - 1.25V} \cdot R_{top}$$

where 1.25V is the internal reference voltage of the SC2618.

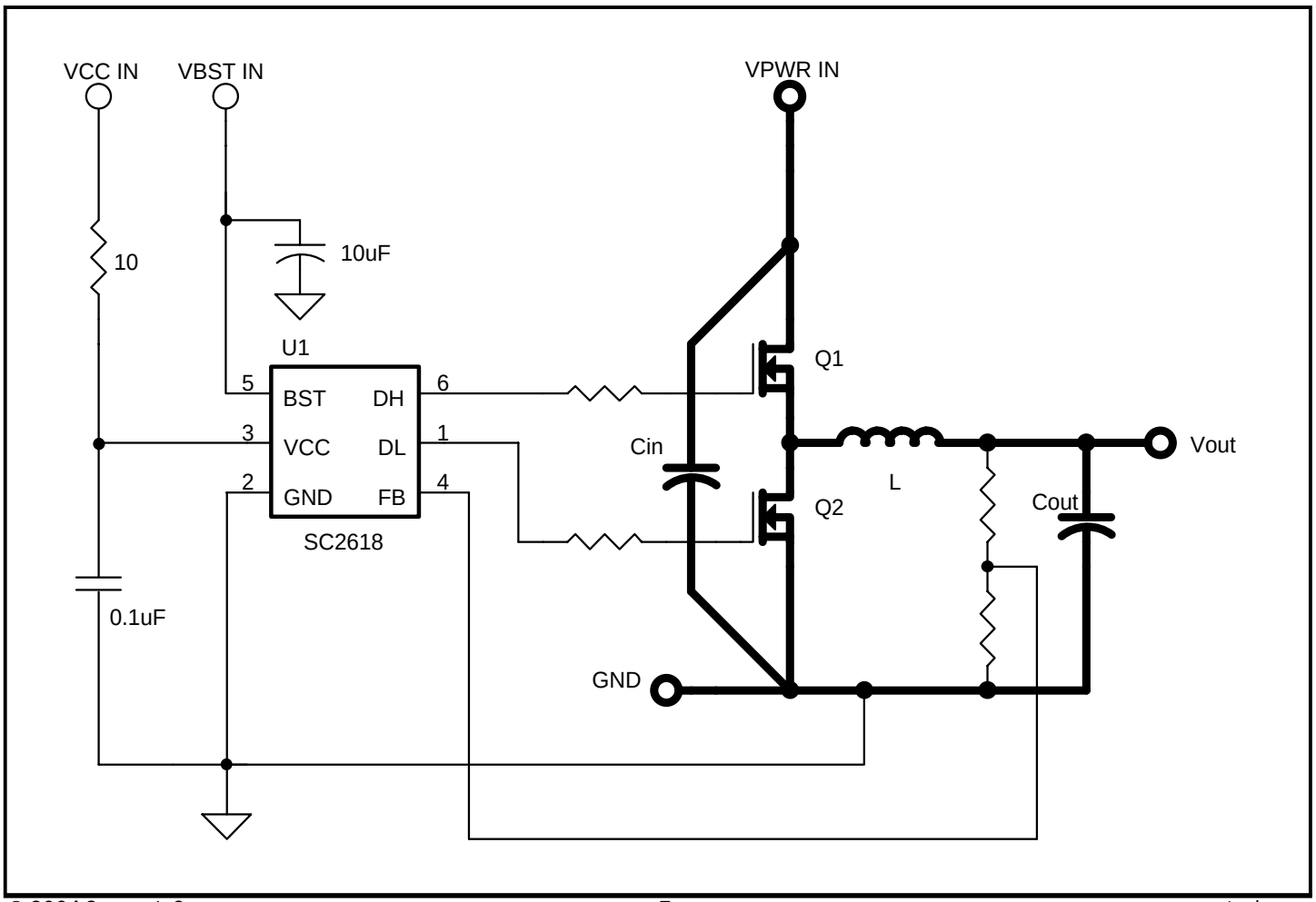
Layout Guidelines

Careful attention to layout requirements are necessary for successful implementation of the SC2618 controller. High currents switching at up to 500kHz are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

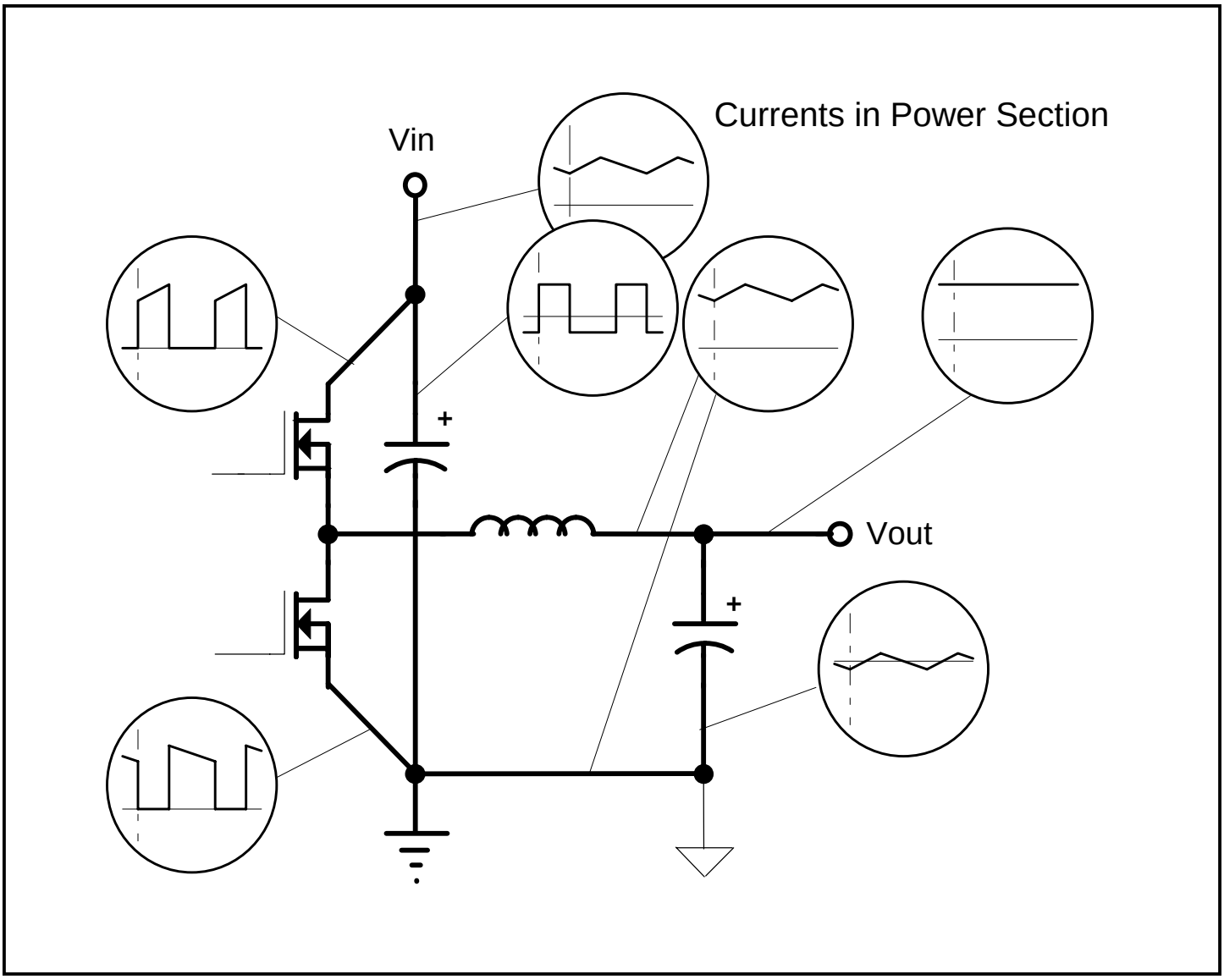
1). The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and bottom FET ground.

2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (Q1) and the Bottom FET (Q2) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals. Cin should consist of the bulk input capacitors and must be supplemented with one or more ceramic decoupling capacitors as close as possible to the FETs

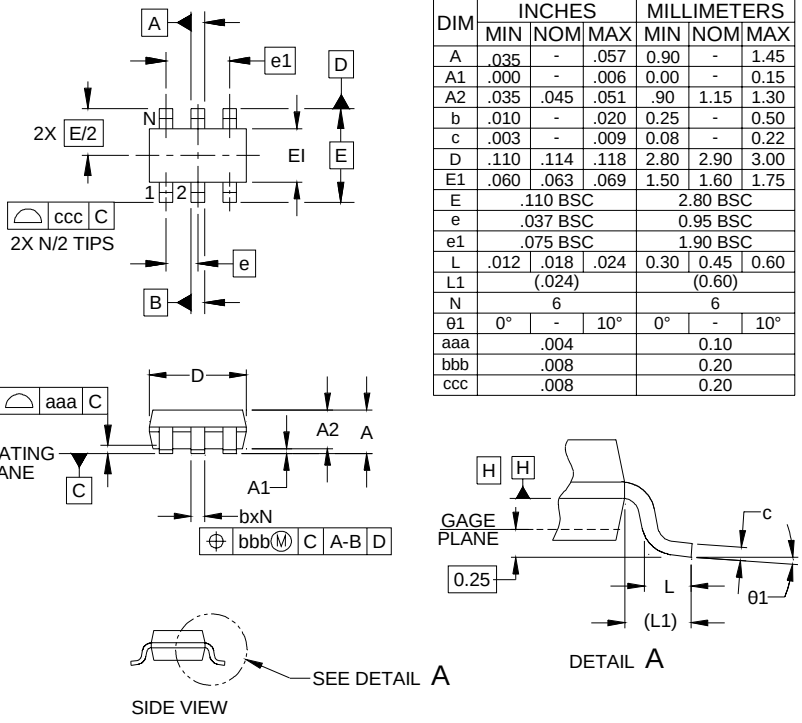
3). The connection between the junction of Q1, Q2 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. The connection between the output inductor and the output capacitors should be a wide trace or copper area, there are no fast voltage or current transitions in this connection and length is not so important, however adding unnecessary impedance will reduce efficiency.



Layout Guidelines (Cont.)



Outline Drawing - SOT23-6

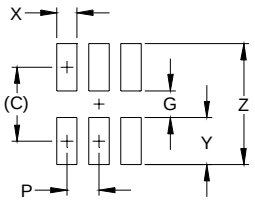


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.035	-	.057	0.90	-	1.45
A1	.000	-	.006	0.00	-	0.15
A2	.035	.045	.051	.90	1.15	1.30
b	.010	-	.020	0.25	-	0.50
c	.003	-	.009	0.08	-	0.22
D	.110	.114	.118	2.80	2.90	3.00
E1	.060	.063	.069	1.50	1.60	1.75
E	.110 BSC			2.80 BSC		
e	.037 BSC			0.95 BSC		
e1	.075 BSC			1.90 BSC		
L	.012	.018	.024	0.30	0.45	0.60
L1	(.024)			(0.60)		
N	6			6		
θ1	0°	-	10°	0°	-	10°
aaa	.004			0.10		
bbb	.008			0.20		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Minimum Land Pattern - SOT23-6



DIM	INCHES	MILLIMETERS
C	(.098)	(2.50)
G	.055	1.40
P	.037	0.95
X	.024	0.60
Y	.043	1.10
Z	.141	3.60

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804

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