THE DATASHEET OF

SC4624SETRT

SC4624

Low Input Voltage, High Efficiency, 4A Integrated FET Synchronous Step down DC/DC Regulator

POWER MANAGEMENT

Description

The SC4624 is a highly integrated synchronous step-down DC/DC regulator designed for low input voltage range of 2.3V to 5.5 Volts. It can deliver 4A continuous output current with the output voltage as low as 0.5 Volts. The internal low $R_{DS(ON)}$ synchronous power switches eliminate the need for external Schottky diode while delivering overall converter efficiency up to 95%.

A power good pin is available to monitor the output voltage status. Operating frequency is adjustable from 200 kHz to 2MHz with a single resistor and it can be synchronized to an external clock.

The SC4624 offers adjustable current limit, soft start and over temperature protection to safeguard the device under extreme operating conditions. The soft start provides a controlled output voltage ramp up at startup. When a logic low is applied to the Enable pin, the SC4624 enters the shutdown mode and it consumes less than 1.5µA of current.

The SC4624 is available in 4x4 MLPQ-20 and SOIC-16EDP packages.

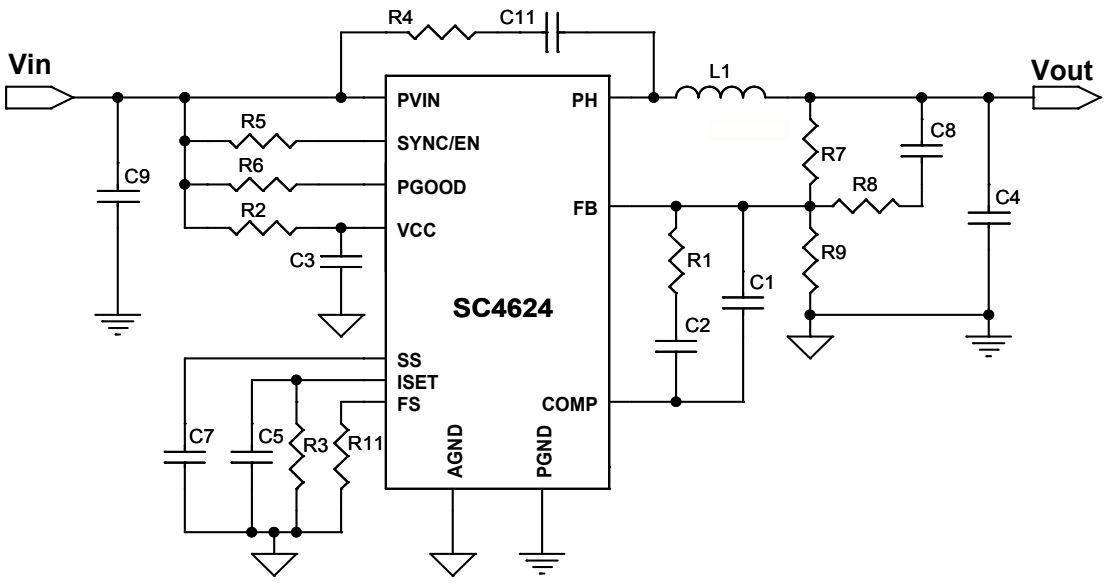
Features

- VIN Range: 2.3 – 5.5V
- 4A Continuous Output Current
- Adjustable Output Voltage 0.5V to Vin
- Low $R_{DS(ON)}$ integrated FETs: 74mΩ and 47mΩ
- Up to 95% Efficiency
- Synchronizable and Programmable Frequency: 200kHz – 2MHz
- Power Good Monitor
- <1.5µA of Shutdown Current
- Programmable Soft Start
- Programmable Current Limit
- Over Temperature protection
- Starts into pre-biased output
- 4x4mm MLPQ-20 and SOIC-16EDP packages- WEEE and RoHS Compliant

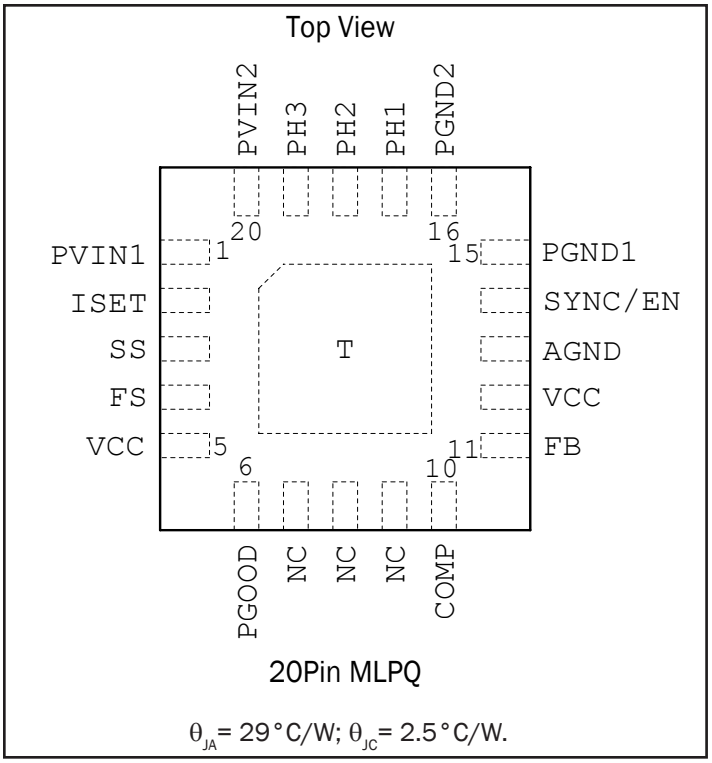
Applications

- Low Voltage Distributed DC-DC Converters
- Telecommunication Power Supplies
- Portable Equipment
- xDSL

Typical Application Circuit

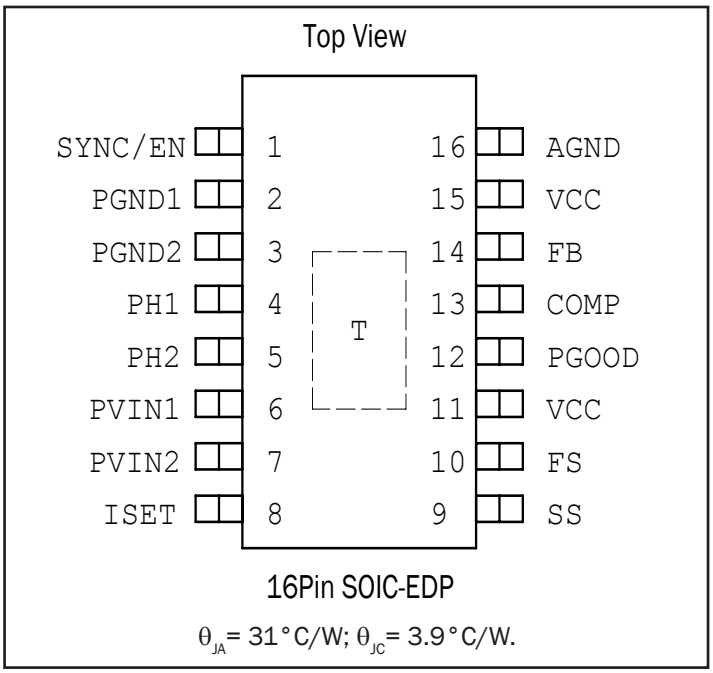


Pin Configuration



20Pin MLPQ

θ_{JA}= 29°C/W; θ_{JC}= 2.5°C/W.



16Pin SOIC-EDP

θ_{JA}= 31°C/W; θ_{JC}= 3.9°C/W.

Ordering Information

Device	Top Mark	Package
SC4624MLTRT (1) (2)	SC 4624	MLPQ-20
SC4624SETRT (1) (2)	SC4624	SO-16 EDP
SC4624EVB-MLPQ	Evaluation Board	
SC4624EVB-SO		

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices for MLPQ-20 package and 2,500 devices for SO-16 package.
(2) Available in lead-free package only. Device is WEEE and RoHS compliant.

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage	PV_{IN}, V_{CC}	-0.3 to 6	V
PVIN to VCC		+/- 0.3	V
FB, COMP, ISET, SYNC/EN, FS, SS, PGOOD to AGND		-0.3 to VCC+ 0.3	V
PGND to AGND		+/- 0.3	V
PHASE Voltage to PGND	V_{PHASE}	-0.3 to PVIN+ 0.3	V
PHASE Pulse Voltage to PGND Tpulse < 50ns	V_{PHASE}	-3 to PVIN+ 2	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Junction Temperature	T_J	150	°C
Junction Temperature (Operating)		-40 to 125	°C
IR Reflow Temperature	T_P	260	°C
Lead Temperature (Soldering) 10 sec for SO Package Only	T_{LEAD}	300	°C
ESD Protection Level(1)	V_{ESD}	2	kV

Note:
1) Tested in accordance to JEDEC standard JESD22-A114B.

Recommended Operating Conditions

The Performance is not guarantied if exceeding the specifications below.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Input Voltage Operating Range	V_{IN}		2.3		5.5	V
Max. Output Current	I_{OUTMAX}		0		4	A

Electrical Characteristics

Unless otherwise specified, V_{IN} = V_{CC}=SYNC/EN=3.3V, R_{OSC}=51.1KΩ, R_{ISET}=27.4KΩ, T_J = -40°C to 125°C

Parameter	Symbol	Conditions	Min	Typ		Units
Power Supply						
Start Threshold Voltage, UVLO	V_{IUV}	V_{IN} Rising		2	2.25	V
Hysteresis Voltage, UVLO	V_{IUVHY}			120		mV
Supply Current, Shutdown	I_{SD}	V_{SYNC} = 0V		0.2	1.5	µA

Electrical Characteristics (Cont.)

Unless otherwise specified, V_{IN}= V_{CC}=SYNC/EN=3.3V, R_{OSC}=51.1KΩ, R_{ISET}=27.4KΩ, T_J = -40°C to 125°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply (Cont.)						
Supply Current, Operating	$I_{Qswitching}$	FB = COMP, No Load		**7**	**10**	mA
	I_{QL}	FB = 0.6V, No Load		**3.5**	**7**	mA
Thermal Shutdown						
Thermal Shutdown Trip Point	T_{OTP}	Temperature Rising		160		°C
Thermal Shutdown Hysteresis	T_{OTP_HYS}			10		°C
Synchronization, Enable Input						
SYNC/EN Threshold	V_{ENL}	Logic Low			0.8	V
	V_{ENH}	Logic High	2.0			V
Frequency Range, SYNC	F_{SYNC}	20% Higher than F_{OSC}	200		2000	kHz
Oscillator						
Osciilator Frequency Range	F_{OSC}		200		2000	kHz
Osciilator Frequency Accuracy		R_{OSC}= 51.1KΩ	415	500	600	kHz
		R_{OSC}=51.1KΩ, T_A=T_J=25°C	435	500	565	kHz
Ramp Peak to Valley(1)	V_{PV}			1.0		V
Ramp Peak Voltage(1)	V_P			1.25		V
Ramp Valley Voltage(1)	V_V			0.25		V
Soft Start, Current Limit						
Soft-Start Charge Current	I_{SS}			4		µA
ISET Bias Voltage	V_{ISET}	R_{ISET} = 27.4KΩ	0.45	0.55	0.62	V
Over Current Trip	I_{IST}	R_{ISIT} = 57.6KΩ	1.9	2.55	3.1	A
Output UVLO	V_{OUV}	VFB drop		0.3		V
Hiccup period(1)	T_{OCHP}			131072		clks
Error Amplifier						
Error Amplifier Open Loop Voltage Gain (1)				100		dB
Error Amplifier Unity Gain Bandwidth(1)				10		MHz
Output Voltage Slew Rate, COMP(1)				4		V/µs

Electrical Characteristics (Cont.)

Unless otherwise specified, V_{IN} = V_{CC}=SYNC/EN=3.3V, R_{OSC}=51.1KΩ, R_{ISET}=27.4KΩ, T_J = -40°C to 125°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Error Amplifier (Cont.)						
Source Output Current, COMP		FB = 0.4V		20		mA
Sink Output Current, COMP		FB = 0.6V		25		mA
Output Voltage High, COMP		FB = 0.4V, I_{COMP} = -1mA		2.5		V
Output Voltage Low, COMP		FB = 0.6V, I_{COMP} = 1mA		0.1	0.25	V
Feedback Voltage	V_{FB}		0.4925	0.5	0.5075	V
		Vcc = 2.3V to 5.5V	-2	±1	+2	%
Input Bias Current(1)	I_{FB}	FB=V_{REF}			300	nA
Power Switches						
High-Side P-MOSFET	$R_{DSH(on)}$	V_{IN}=V_{CC}=5V, I_{SOURCE} = 1A, T_A=T_J=25 °C		74	100	mΩ
Low Side N-MOSFET	$R_{DSL(on)}$	V_{IN}=V_{CC}=5V, I_{SINK} = 1A, T_A=T_J=25 °C		47	85	mΩ
Power Good						
PGood Voltage Low	V_{PGL}	I_{PGOOD} = 1mA		0.2		V
PGood Leakage Current	I_{PGOOD}	PGOOD = 5V			1	µA
PGood Delay Time(1)	T_D	Vout rising or Vout falling		1024		clks
PGood High Window		With respect to nominal output, T_A=T_J=25 °C	±8	±10	±15	%

Note:
(1) Guaranteed by design.

Typical Performance Characteristics

Circuit condition: Application circuit#1, $5V_{IN}$, $1V_{OUT}$

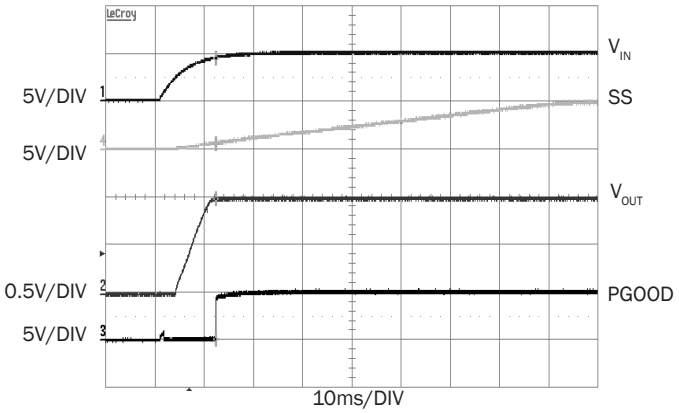


Figure 1. Start Up by V_{IN}@0A

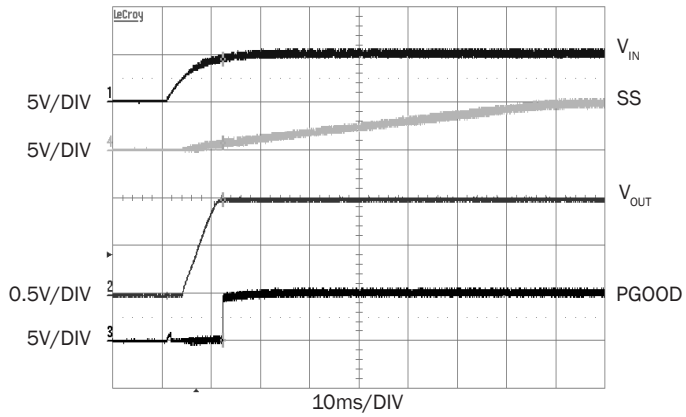


Figure 2. Start Up by V_{IN}@4A

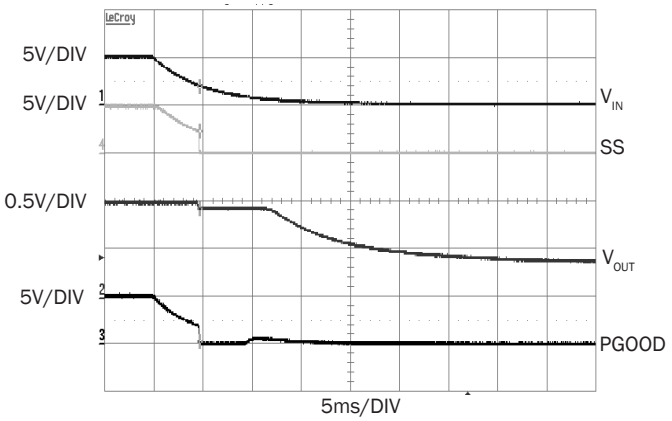


Figure 3. Shutdown by V_{IN}@0A

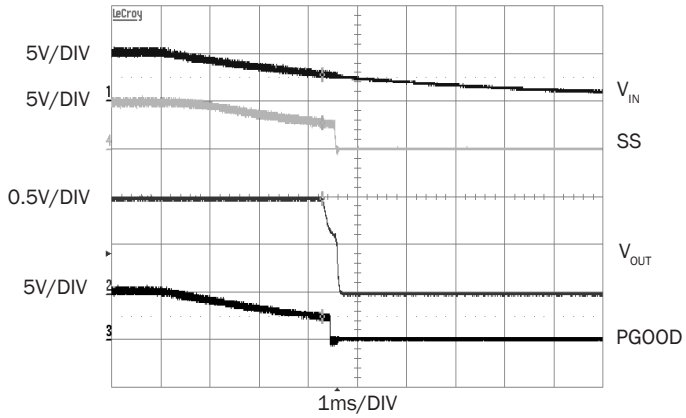


Figure 4. Shutdown by V_{IN}@4A

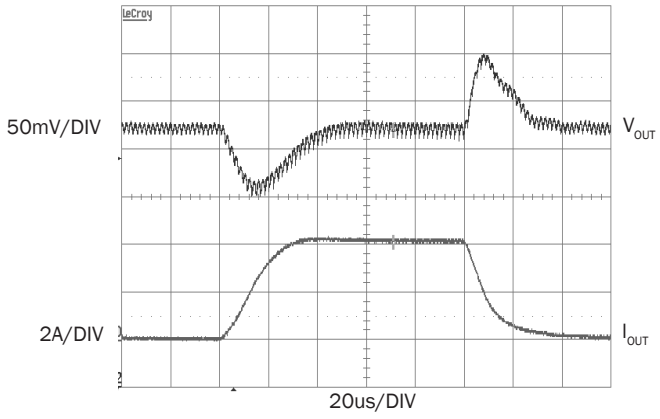


Figure 5. Transient Response@ 0 to 4A

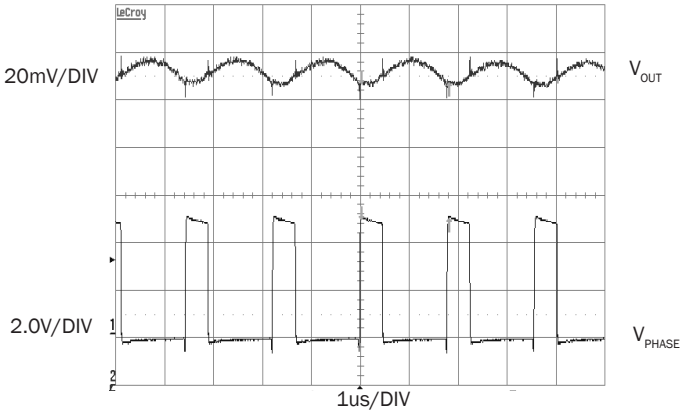


Figure 6. Ripple and Stability@4A

Typical Performance Characteristics (Cont.)

Circuit condition: Application circuit#1, $5V_{IN}$, $1V_{OUT}$

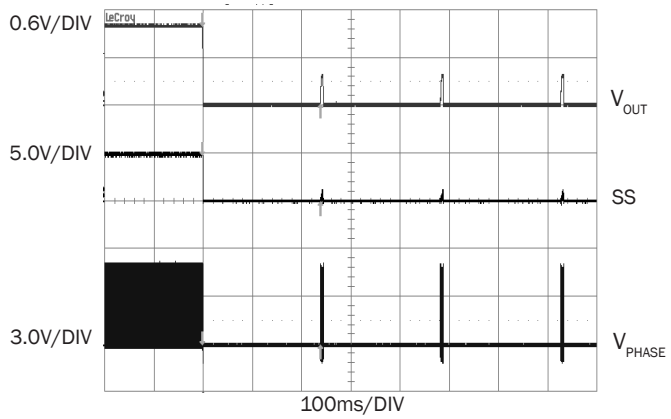


Figure 7. Over Load Hiccup

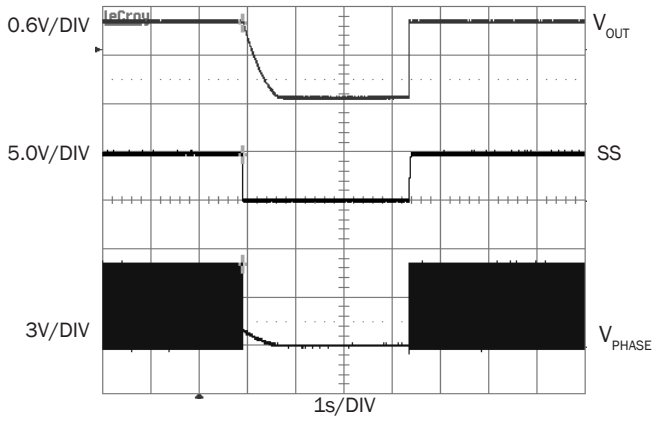


Figure 8. Thermal Shutdown Protection@0A

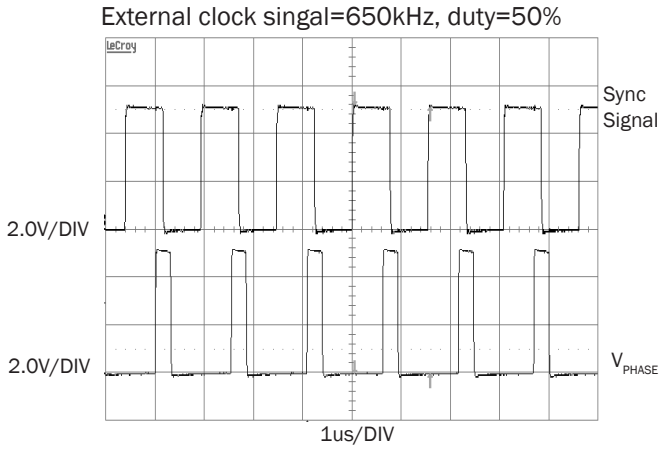


Figure 9. Synchronization

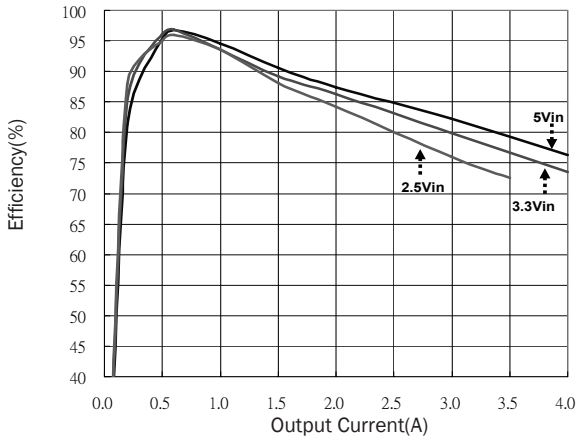


Figure 10. Efficiency(V_{IN})

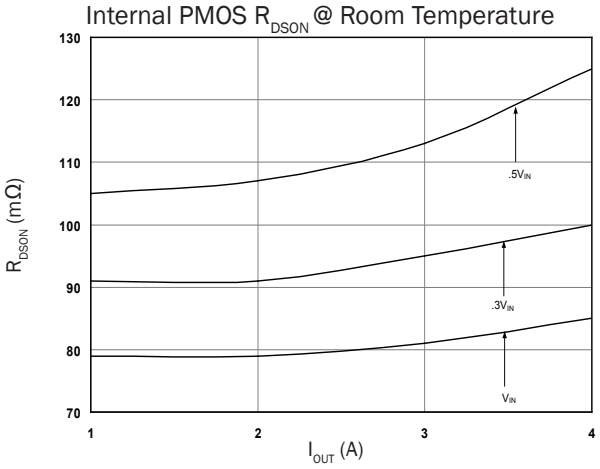


Figure 11. High-Side P-MOSFET

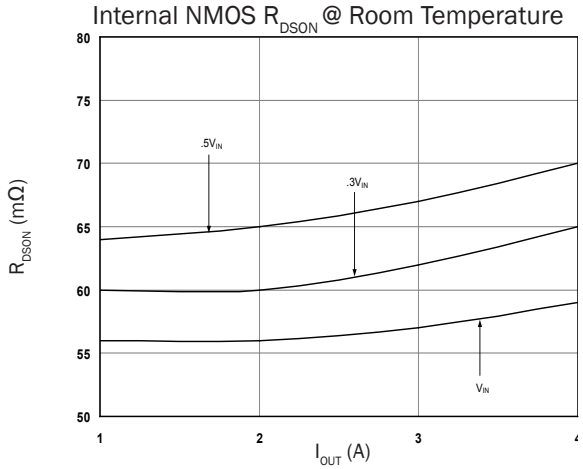


Figure 12. Low-Side N-MOSFET

Typical Performance Characteristics (Cont.)

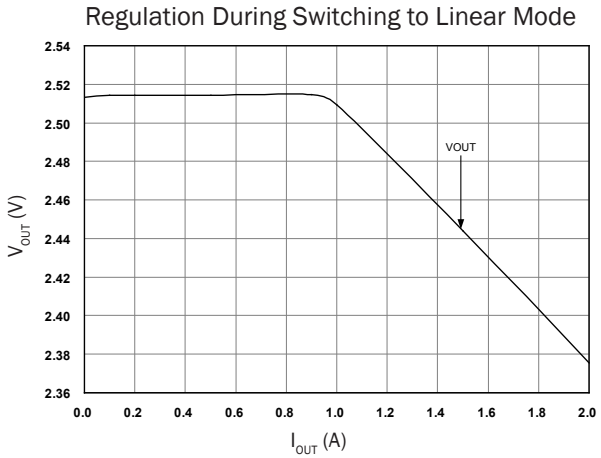


Figure 13. Loading Regulation

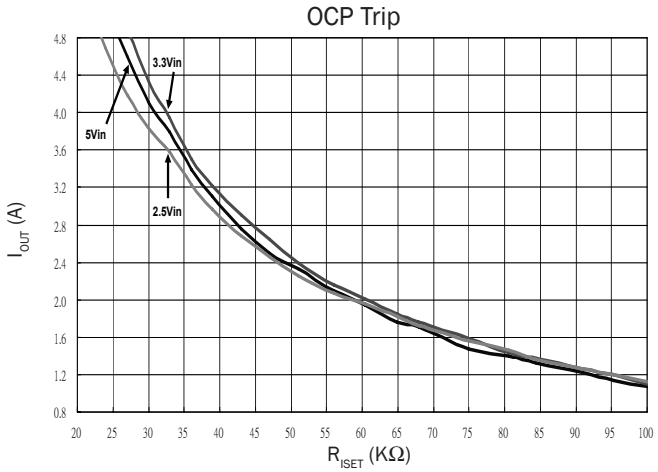
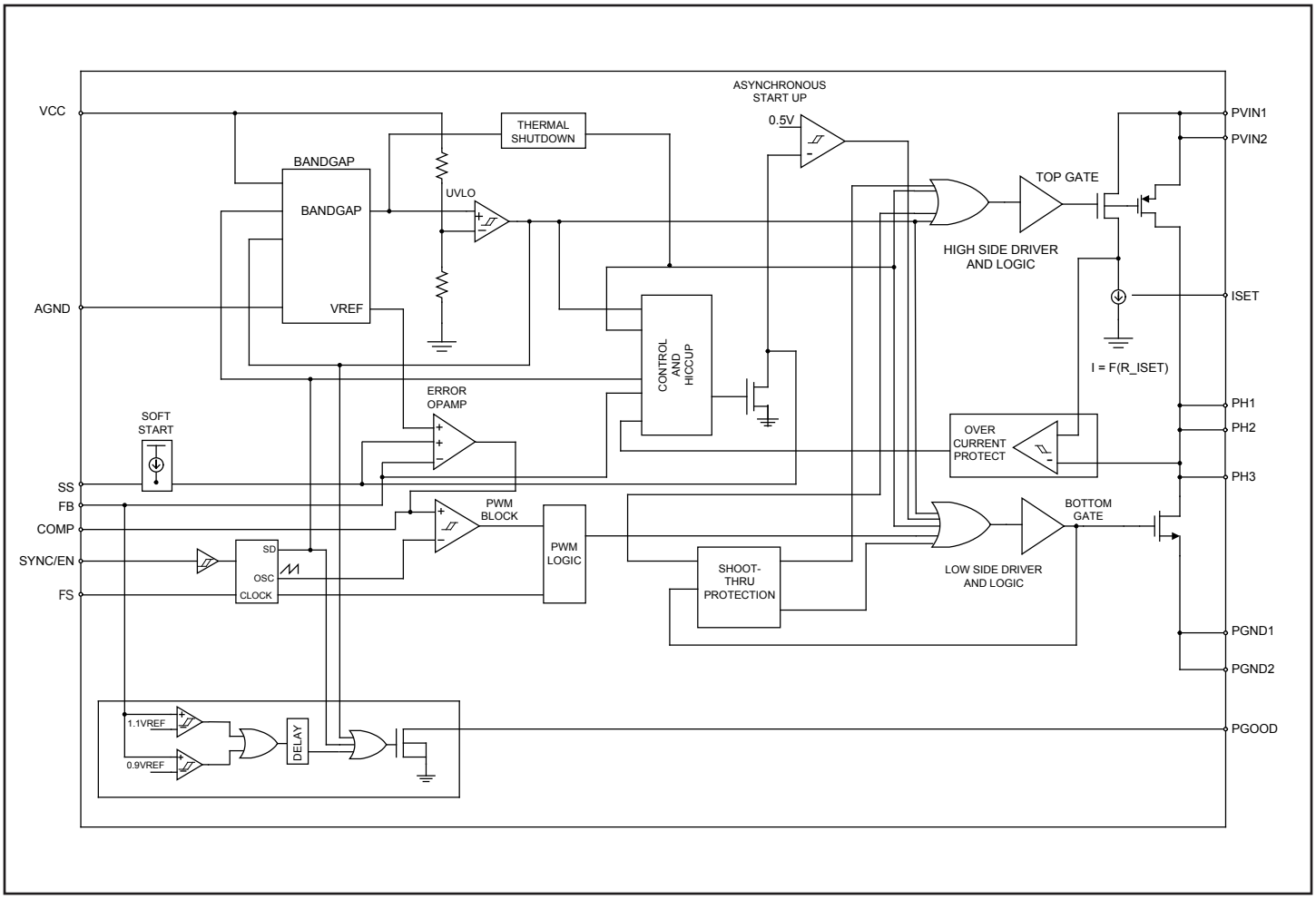


Figure 14. Over Current Setting versus R_{ISET}

Pin Descriptions

Pin SO-16	Pin MLPQ-20	Pin Name	Pin Functions
6	1	PVIN1	Power supply voltage for high side MOSFETs.
8	2	ISET	Current limit setting pin. A resistor connected between ISET and AGND sets the over current protection threshold. A ceramic decoupling between ISET pin to AGND have to be reserved to prevent from noise influence.
9	3	SS	Soft start time setting pin. A cap connected from this pin to GND sets the soft start up time.
10	4	FS	Oscillator frequency setting pin. An external resistor connected from this pin to GND sets the oscillator frequency.
11,15	5,12	VCC	Power supply voltage for the analog section of the controller.
12	6	PGOOD	Power good indicator. It is an open drain output. Low when the output is below the power good threshold level.
	7,8,9	NC	No connection.
13	10	COMP	This is the output of the error amplifier. The voltage at this point is connected to the inverting input of the PWM comparator. A compensation network is required in order to optimize the dynamic performance of the voltage mode control loop.
14	11	FB	The inverting input of the error amplifier. It serves as the output voltage feedback point for the buck controller. It senses the output voltage through an external divider.
16	13	AGND	Analog signal gound.
1	14	SYNC/EN	The oscillator frequency of the SC4624 is set by FS when SYNC/EN is pulled and held above 2V. Its synchronous mode is activated as SYNC/EN is driven by an external clock. Its shutdown mode is invoked if SYNC/EN is pulled and held below 0.8V.
2	15	PGND1	Power ground.
3	16	PGND2	Power ground.
4	17	PH1	Switching nodes
5	18	PH2	Switching nodes
	19	PH3	Switching nodes
7	20	PVIN2	Power supply voltage for high side MOSFETs.
		THERMAL PAD	Pad for heatsinking purposes only. Connect to ground plane using multiple vias. Not electrically connected internally.

Block Diagram



Application Information

Overview

The SC4624 is a programmable high switching frequency, integrated 4A MOSFET, synchronous step down regulator. This reduces external component count and makes it effective for applications which are low in cost and sized small. A non-overlap protection is provided for the gate drive signals to prevent shoot through of the internal MOSFET pair.

The SC4624 is capable of producing an output voltage as low as 0.5V and Its operation frequency is programmable up to 2MHz by an external resistor. It features lossless current sensing of the voltage drop across the internal drain to source resistance of the high side MOSFET during its conduction period.

The quiescent supply current in shutdown mode is typically lower than 1μA. An external soft start is provided to prevent output voltage overshoot during start-up. Over Temperature Protection, Power Good Indicator, External Clock Synchronization are some of the internal added features.

Enable

The SC4624 is enabled by applying a voltage greater than 2V (typical) to the V_{CC} and SYNC/EN pin. The voltage on the V_{CC} pin determines the operation of the SC4624. As V_{CC} increases during start up, the UVLO block senses V_{CC} and keeps the high side and low side MOSFETs off and the internal soft start voltage low until V_{CC} reaches 2V. If no faults are present, the SC4624 will initiate a soft start when V_{CC} exceeds 2V. A typical 120mV hysteresis in the UVLO comparator provides noise immunity during its start up. (refer to Figure 1 to 2).

Shutdown

The SC4624 is disabled when V_{CC} falls below 1.88V (typical) or shutdown mode operation is invoked by clamping the SYNC/EN pin to a voltage below 0.8V. During the shutdown mode, A typical 0.2μA current draw through the V_{CC} pin, the internal soft start voltage is held low and the internal MOSFETs are turned off. (refer to Figure 3 to 4).

Soft Start

The soft start function is required for step down controllers to prevent excess in-rush current through the DC bus during start up. An external capacitor is necessary for the soft start function and is connected from SS pin to AGND.

During start up or restart, A typical 4μA sourcing current charges the capacitor and then the voltage of capacitor ramp up the error amp reference slowly. The closed loop creates narrow width driver pulses while the output voltage is low and allows these pulses to increase to their steady state duty cycle as the output voltage reaches its regulated value. The duration of the soft start in the SC4624 is controlled by an external capacitor.

The SC4624 starts up in asynchronous mode before SS voltage reaches to 0.5V, and the bottom FET diode is used for circulating current during the top FET off time. Ths SS voltage level is clamped at V_{CC} finally.

Pre-biased Output

The SC4624 is able to start into pre-biased output by adding external RC circuit, where R(10KΩ) is between V_{CC} pin and EN pin, C(0.1uF) is between EN pin and AGND. If there is a pre-biased load on the output of SC4624 during start-up, the internal low-side MOSFET of SC4624 is always disabled before SS reach to 0.5V, the output voltage is maintained. The great feature avoids negative voltage spikes or short circuit on the output, which could cause damage to the down-stream IC during start-up.

Timing between V_{CC} and EN is very important for pre-biased output. V_{CC} must lead EN. When V_{CC} and EN voltage rise at same time(tied together), the pre-biased output voltage is pull low before V_{CC} reach to the voltage of UVLO. If this isn't desirable, RC(10KΩ and 0.1uF) must be added at EN to prevent this from happening.

Oscillator

The FS pin is used to set the PWM oscillator frequency through an external resistor that is connected from the FS pin to the AGND. The internal ramp is a triangle at the PWM frequency with a peak voltage of 1.25V and a valley voltage of 0.25V. The approximate operating frequency is determined by the value of an external resistor as shown in Figure 15.

Application Information (Cont.)

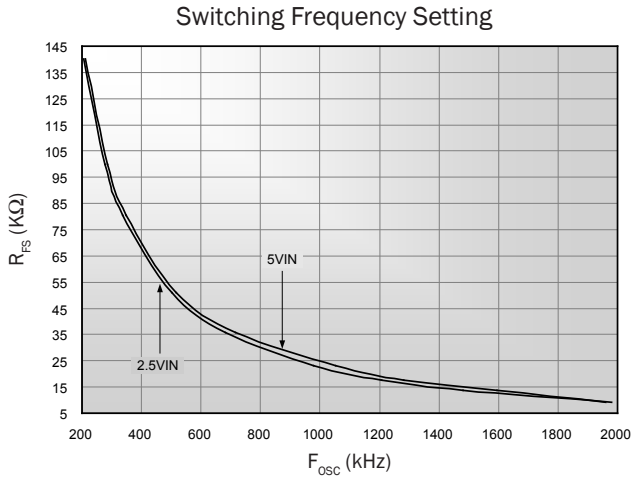


Figure 15. Switching Frequency vs. R_{FS}

The operation frequency can be programmed up to 2MHz, but there is a minimum on-time limitation which is around 110ns. Users should take care of minimum limitation on the operating duty cycle under high frequency application.

Synchronization Frequency

Synchronization operation mode is invoked by using an external clock signal and is activated when the SYNC/EN is pulled and held above 2V and held below 0.8V. The range of synchronization frequency is from 200kHz to 2MHz.

A jitter happens when sync pulse clock edge is less than 120ns before the phase switches. It is caused by the ground bounce of synchronization pulse coupled to PWM comparator. Users try to avoid this application. (refer to Figure 9).

Power Good Indicator

The PGOOD pin is an open-drain and incorporated window comparators output. It's is necessary that a pull-up resistor from the PGOOD pin to the input supply for setting the logic high level of the PGOOD signal. When FB voltage is within ±10% setting output voltages typical, the output of power good comparator becomes high impedance after delay time. The PGOOD signal delay time is around 1024/ F_{OSC}. In shutdown mode the power good output is actively pulled low.

For example, 1MHz switching frequency applications, the PGOOD delay time is around 1ms.

Thermal Shutdown

When the junction temperature rises up around 160°C, the internal soft start voltage is held low, the internal high side and low side MOSFETs are turned off and the output voltage will fall to zero. Once the junction temperature goes below hysteresis temperature around 10°C, the regulator will restart. (refer to Figure 8).

Linear Mode Operation (100% duty)

The SC4624 can allows 100% duty cycle operation. The Vout is,

$$V_{OUT} = V_{IN} - (R_L + R_{DSH}) \times I_{OUT}$$

where

R_L : Output inductor DC resistance.
R_{DSH} : Internal high side P-MOSFET resistance. (refer to Figure11).

As Vin drops gradually and close to Vout, the buck regulator will go into 100% duty cycle ratio. A matter needing attention is internal high side PMOS has minimum off time limitation and is related to duty cycle rate. This condition makes the working duty cycle perform at randon with the output ripple increasing and a poor transient response. Above phenomenon can be improved by larger output capacitor and smaller output inductor. Users need to verify whether above application condition has opposite influence on entire circuit.

Over Current Protection

A over current setting is programmed by an external resistor (R_{ISET}). It goes through internal sense resistor and generates a voltage.

$$V2 = V_{cc} - I \times R_{Onsense}$$

where

I : The current is generated by R_{ISET}, and it is amplified by internal current amplifier.
$R_{ONSENSE}$: Internal sense resistor.

Output inductor current goes through internal high side P-MOSFET and generate a voltage.

$$V1 = V_{IN} - I_L \times R_{DSH(ON)}$$

where

I_L : Output inductor current.
$R_{DSH(ON)}$: High side P-MOSFET conduction resistance.

Application information (Cont.)

After the high side PMOS turn on around 30ns, the OCP comparator will compare between V2 and V1. When the converter detects an over current condition (V2 > V1) as shown in Figure 16, the SC4624 proceeds into the cycle by cycle protection mode (Point B to Point C), which responds to minor over current cases and the output voltage is monitored.

If the over current and low output voltage (set at 60% of nominal output voltage) occur at the same time, the SS pin is pull low by an internal switch and the comp pin is pulled low and the devices stops switching. Assume start from FB = 0V, FB and SS voltage rise forward 0.5V. Once SS voltage exceeds 0.4V, the hiccup comparator becomes enabled. The hiccup period is around $2^{17}/F_{OSC}$. (Point C to Point D).

For example, with a switching frequency application of 550kHz, the hiccup period is around 238ms. (refer to Figure 7).

A poor layout will make OCP trip point shift and is not easily to calculate by R_{ISET}. This is because it is affected by ground bounce, spiker voltage between Vin pin and PH pin, and internal parameter tolerance. Users can refer to Figure 14, it shows how to set maximum output current by R_{ISET}.

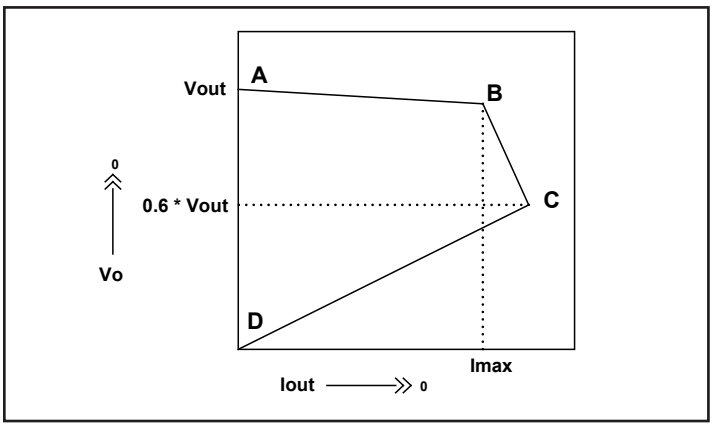


Figure 16. Over Current Protection Characteristic

Inductor Selection

For a typical SC4624 application, the inductor selection is mainly based on its value, saturation current and DC resistance. The inductor should be able to handle the peak current without saturating and its copper resistance in the winding should be as low as possible to minimize its resistive power loss.

The inductor value can be determined according to its operating point and the switching frequency as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_s \times \Delta I \times I_{OMAX}}$$

where

fs = switching frequency.

ΔI = ratio of the peak to peak inductor current to the maximum output load current.

The peak to peak inductor current is:

$$I_{P-P} = \Delta I \times I_{OMAX}$$

After the required inductor value is selected, the proper selection of the core material is based on the peak inductor current and efficiency requirements. The core must be able to handle the peak inductor current I_{PEAK} without saturation and produce low core loss during the high frequency operation and is given as follows:

$$I_{PEAK} = I_{IOMAX} + \frac{I_{P-P}}{2}$$

The power loss for the inductor includes its core loss and copper loss. If possible, the winding resistance should be minimized to reduce any copper loss of the inductor, (the core loss can be found in the manufacturer's datasheet).

The inductor's copper loss can be estimated as follows:

$$P_{COOPER} = I^2_{LRMS} \times R_{WINDING}$$

where

I_{LRMS} is the RMS current in the inductor.

This current can be calculated as follows:

$$I_{LRMS} = I_{OMAX} \times \sqrt{1 + \frac{1}{3} \times \Delta I^2}$$

Output Capacitor Selection

Basically there are two major factors to consider in selecting the type and quantity of the output capacitors. The first one is the required ESR (Equivalent Series Resistance) which should be low enough to reduce the voltage deviation from its nominal one during its load changes. The second one is the required capacitance, which should be high enough to hold up the output voltage. Before the

Application Information (Cont.)

SC4624 regulates the inductor current to a new value during a load transient, the output capacitor delivers all the additional current needed by the load.

The ESR and ESL of the output capacitor, the loop parasitic inductance between the output capacitor and the load combined with inductor ripple current are all major contributors to the output voltage ripple.

Input Capacitor Selection

The input capacitor selection is based on its ripple current level, required capacitance and voltage rating. This capacitor must be able to provide the ripple current by the switching actions. For the continuous conduction mode, the RMS value of the input capacitor can be calculated from:

$$I_{CIN(RMS)} = I_{OMAX} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}^2}}$$

This current gives the capacitor's power loss as follows:

$$P_{CIN} = I^2_{CIN(RMS)} \times R_{CIN(ESR)}$$

This capacitor's RMS loss can be a significant part of the total loss in the converter and reduces the overall converter efficiency. The input ripple voltage mainly depends on the input capacitor's ESR and its capacitance for a given load, input voltage and output voltage. Assuming that the input current of the converter is constant, the required input capacitance for a given voltage ripple can be calculated by:

$$C_{IN} = I_{OMAX} \times \frac{D \times (1 - D)}{f_S \times (\Delta V_I - I_{OMAX} \times R_{CIN(ESR)})}$$

where

$D = V_O/V_I$, duty ratio.

ΔV_I = the given input voltage ripple.

Loop Compensation Design

For a DC/DC converter, it is usually required that the converter has a loop gain of a high cross-over frequency for fast load response, high DC and low frequency gain for low steady state error, and enough phase margin for its operating stability. Often one can not have all these properties at the same time. The purpose of the loop compensation is to arrange the poles and zeros of the compensation network to meet the requirements for a specific application.

The SC4624 has an internal error amplifier and requires the compensation network to connect among the COMP pin and FB pin, GND, and the output as shown in Figure 17. The compensation network includes C1, C2, R1, R7, R8 and C8. R9 is used to program the output voltage according to:

$$V_o = 0.5 \times (1 + \frac{R_7}{R_9})$$

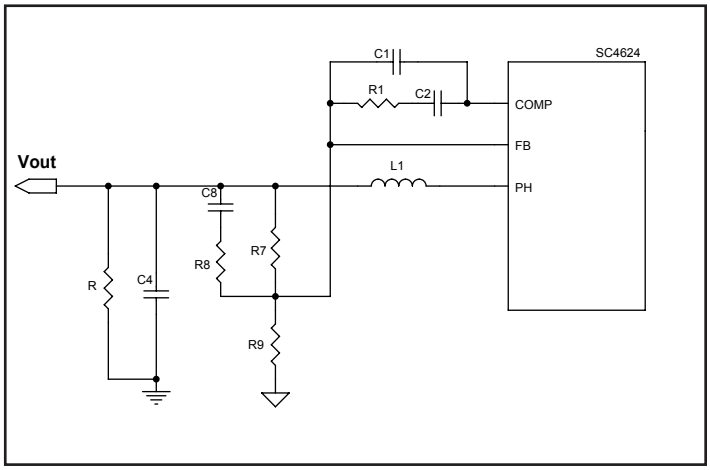


Figure 17. Compensation Network Provides 3 Poles and 2 Zeros

For voltage mode step down applications as shown in Figure 17, the power stage transfer function is:

$$G_{VD}(s) = V_I \frac{1 + \frac{s}{\frac{1}{R_C \cdot C_4}}}{1 + s\frac{L_1}{R} + s^2 L_1 C_4}$$

where

R = load resistance

R_C = C4's ESR.

The compensation network will have these characteristics:

$$G_{COMP}(s) = \frac{\omega_I}{s} \cdot \frac{1 + \frac{s}{\omega_{Z1}}}{1 + \frac{s}{\omega_{P1}}} \cdot \frac{1 + \frac{s}{\omega_{Z2}}}{\cdot 1 + \frac{s}{\omega_{P2}}}$$

Application Information (Cont.)

where

$$\omega_I = \frac{1}{R_7 \cdot (C_1 + C_2)}$$

$$\omega_{Z1} = \frac{1}{R_1 \cdot C_2}$$

$$\omega_{Z2} = \frac{1}{(R_7 + R_8) \cdot C_8}$$

$$\omega_{P1} = \frac{C_1 + C_2}{R_1 \cdot C_1 \cdot C_2}$$

$$\omega_{P2} = \frac{1}{R_8 \cdot C_8}$$

After the compensation, the converter will have the following loop gain:

$$T(s) = G_{PWM} \cdot G_{COMP}(s) \cdot G_{VD}(s)$$

$$= \frac{\frac{1}{V_M} \cdot \omega_I \cdot V_I}{s} \cdot \frac{1 + \frac{s}{\omega_{Z1}}}{1 + \frac{s}{\omega_{P1}}} \cdot \frac{1 + \frac{s}{\omega_{Z2}}}{\cdot 1 + \frac{s}{\omega_{P2}}} \cdot \frac{1 + \frac{s}{\frac{1}{R_C \cdot C_4}}}{1 + s\frac{L_1}{R} + s^2 L_1 C}$$

where

G_{PWM} = PWM gain.

V_M = 1.0V, ramp peak to valley voltage of SC4624.

The design guidelines for the SC4624 applications are as follows:

1. Set the loop gain crossover corner frequency ω_C for given switching corner frequency $\omega_S = 2\pi fs$,
2. Place an integrator at the origin to increase DC and low frequency gains.
3. Select ω_{Z1} and ω_{Z2} such that they are placed near ω_0 to damp the peaking and the loop gain has a -20dB/dec rate to go across the 0dB line for obtaining a wide bandwidth.
4. Cancel the zero from C4's ESR by a compensator pole ω_{P1} ($\omega_{P1} = \omega_{ESR} = 1/(R_C C_4)$).
5. Place a high frequency compensator pole ω_{P2} ($\omega_{P2} = \pi fs$) to get the maximum attenuation of the switching ripple and high frequency noise with the adequate phase lag at ω_C.

The compensated loop gain will be as given as show in Figure 18.

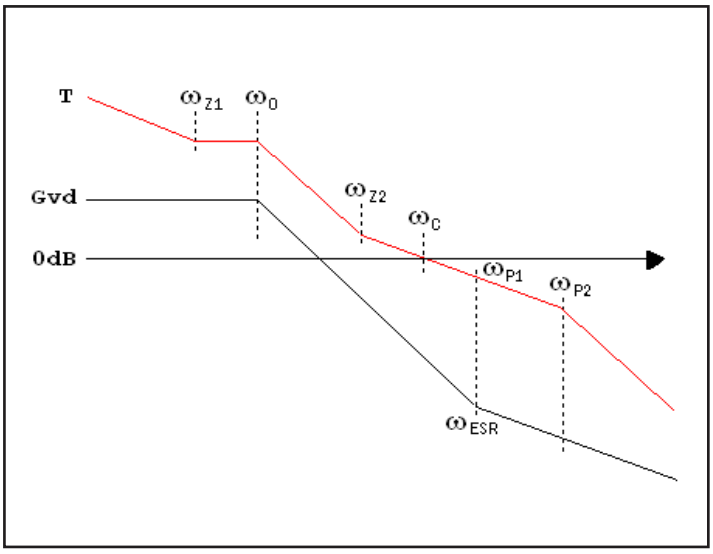


Figure 18. Asymptotic Diagrams of Power Stage and Loop Gain

Application Information (Cont.)

Layout Guidelines

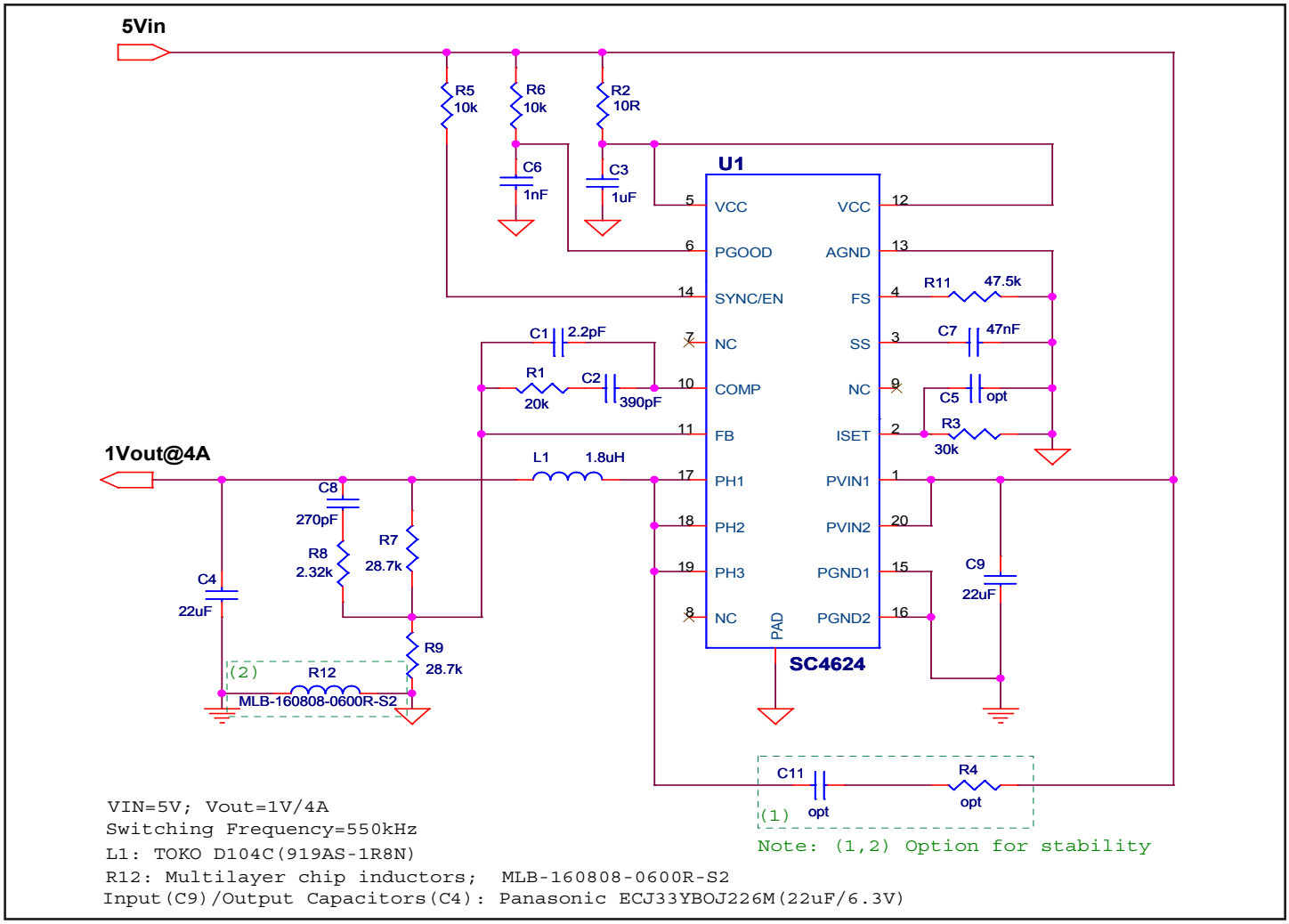
In order to achieve optimal thermal and noise immunity for high frequency converters, special attention must be paid to the PCB layout. The goal of layout optimization is to minimize the high di/dt loops and reduce ground bounce.

Output voltage setting, line regulation, stability , switching frequency and OCP trip point shifted are affected by a poor layout. The following guidelines should be used to ensure proper functions of the converters.

1. Both Power ground (PGND) and signal ground (AGND) are separated.
2. A ground plane is recommended to minimize noise and copper losses, and maximize heat dissipation.
3. Start the PCB layout by placing the power components first. Arrange the power circuit to achieve a clean power flow route.
4. Minimize all high di/dt loops. These loops pass high di/dt current. Make sure the trace width is wide enough to reduce copper losses in this loop. Ground bounce happen to magnetic flux changed and it is proportional to a magnetic filed which goes through high di/dt loops.
5. The input ceramic capacitor (C_{IN}) should be close to PV_{IN} pins and PGND pins.
6. Both input ceramic capacitor gnd and output ceramic capacitor gnd are at same port.
7. A RC snubber circuit between PV_{IN} and PH pins is helpful for stability operation. Be careful with power derating of snubber circuit.
8. The V_{CC} bypass capacitor should be placed next to the V_{CC} and AGND pins.
9. The OCP setting resistor (R_{ISET}) and filter capacitor (C_{ISET}) should be placed next to the ISET and AGND pins.
10. Feedback divider connects to output connector by Kelvin connection and far away from the noise sources such as switching node and switching components.
11. A multilayer chip beads between AGND and PGND will reduce the ground bounce injected to the “quiet” circuit. It’s helpful for stability operation.
12. A large copper area underneath the SC4624 IC is necessary for heat sinking purpose. And multiple layers of large copper area connected through vias can be used for better thermal performance. The size of the vias as the connection between multiple layers should not be too large or solder may seep through the big vias to the bottom layer during the re-flow process .

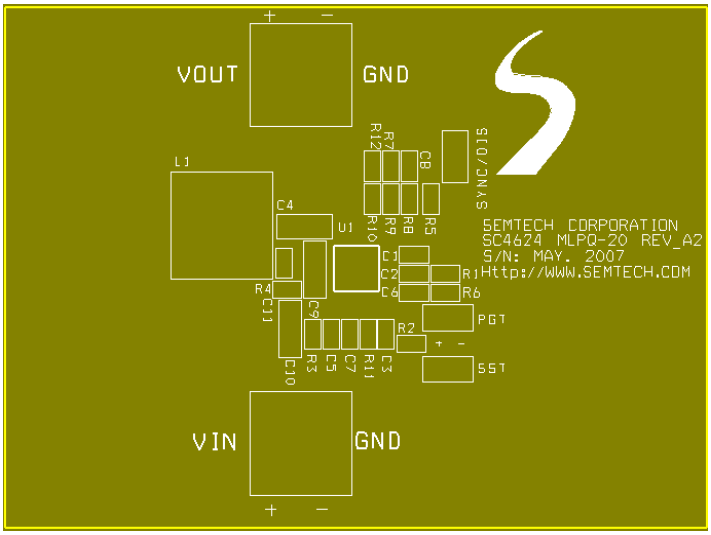
Application Information (Cont.)

$5V_{IN}$, $1V_{OUT}$, 4A, all ceramic capacitors (application circuit#1)

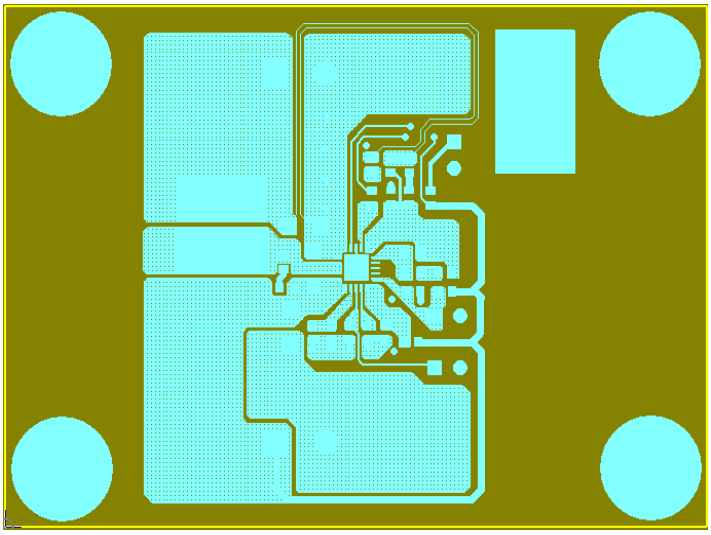


PCB Layout

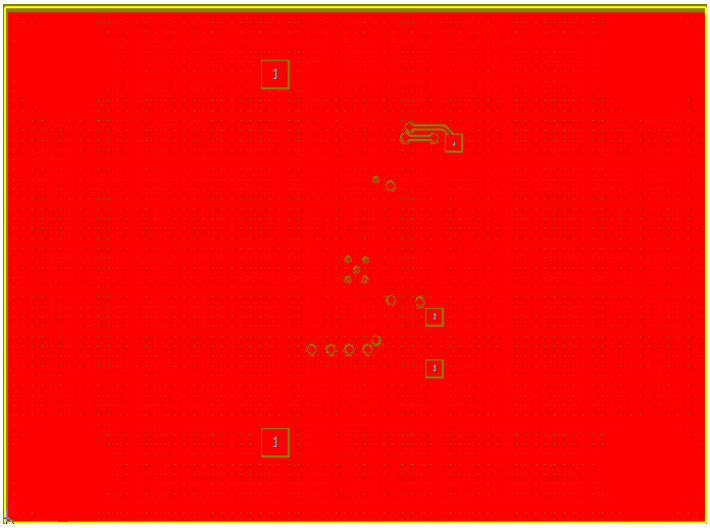
Component Side (TOP)



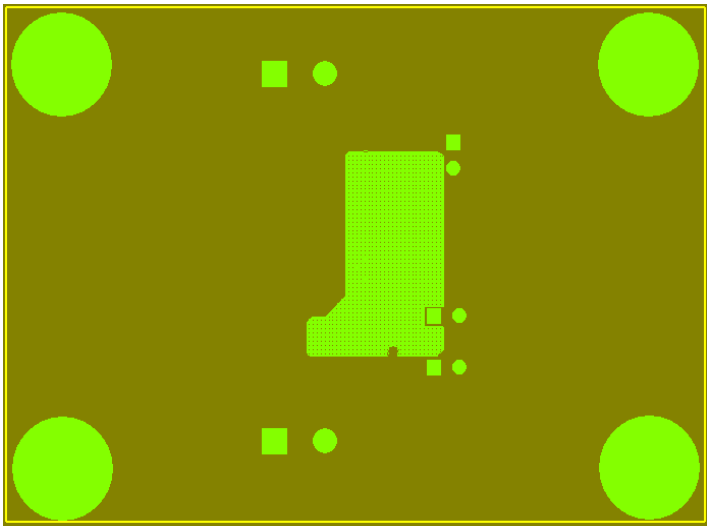
(TOP layer)



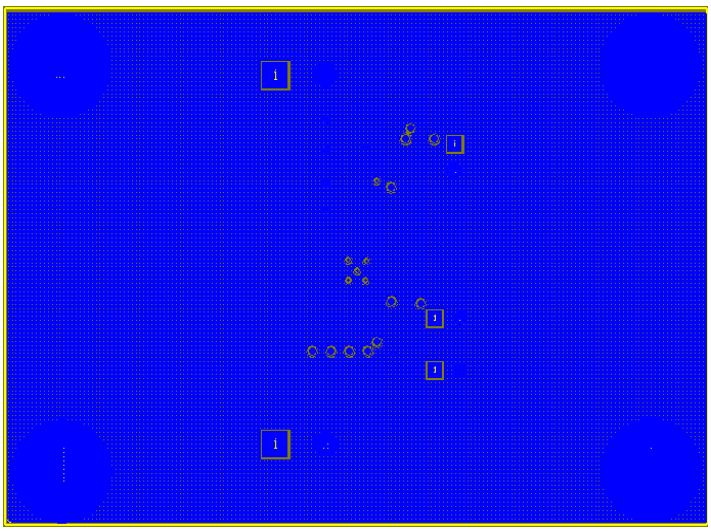
(Bottom layer)



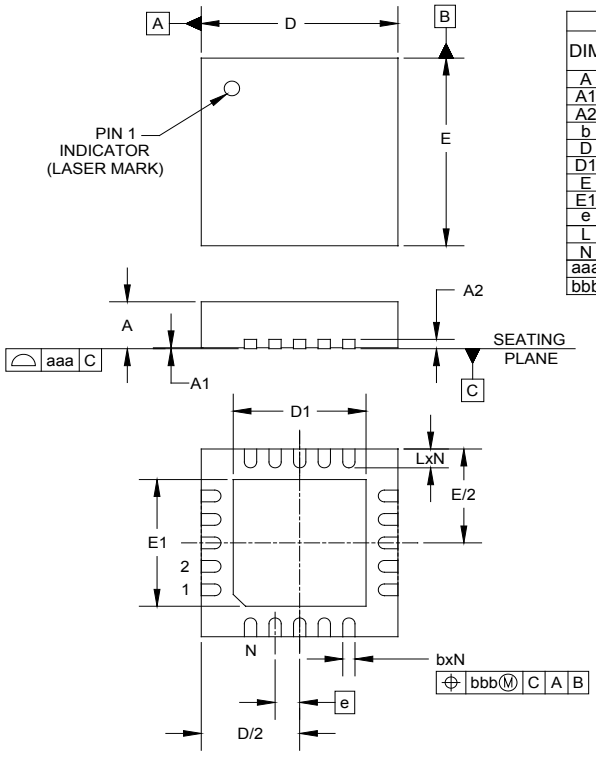
(IN1 layer)



(IN2 layer)



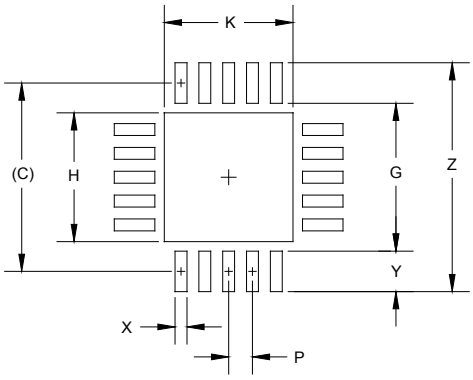
Outline Drawing - MLPQ - 20



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.039	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.154	.157	.161	3.90	4.00	4.10
D1	.100	.106	.110	2.55	2.70	2.80
E	.154	.157	.161	3.90	4.00	4.10
E1	.100	.106	.110	2.55	2.70	2.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	20			20		
aaa	.004			0.10		
bbb	.004			0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

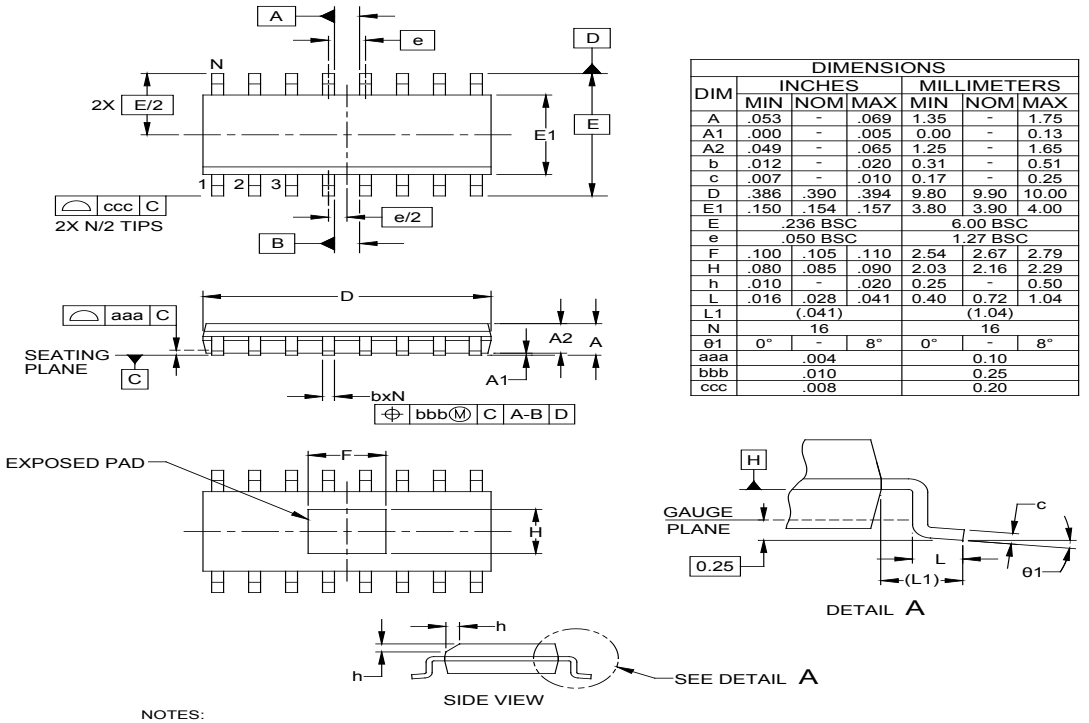
Land Pattern - MLPQ - 20



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.020	0.50
X	.010	0.25
Y	.033	0.85
Z	.189	4.80

NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

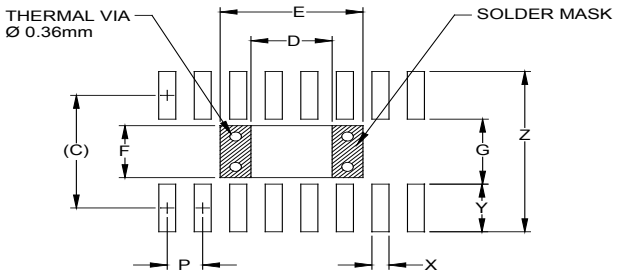
Outline Drawing - SO-16 EDP



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.000	-	.005	0.00	-	0.13
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.386	.390	.394	9.80	9.90	10.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
F	.100	.105	.110	2.54	2.67	2.79
H	.080	.085	.090	2.03	2.16	2.29
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	16			16		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AC.

Land Pattern - SO-16 EDP



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
D	.114	2.90
E	.201	5.10
F	.094	2.40
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

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Contact Information

Semtech Corporation
Power Mangement Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

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