



# THE DATASHEET OF 74AC646SPC



## 74AC646 • 74ACT646

### Octal Transceiver/Register with 3-STATE Outputs

#### General Description

The AC/ACT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in Figures 1, 2, 3, and Figure 4.

#### Features

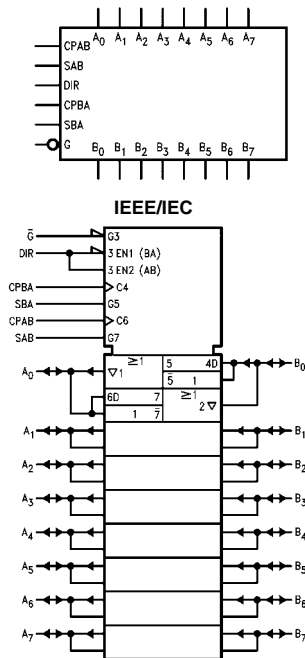
- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- 3-STATE outputs
- 300 mil dual-in-line package
- Outputs source/sink 24 mA
- ACT646 has TTL compatible inputs

#### Ordering Code:

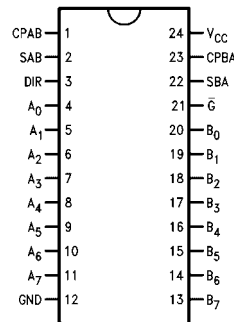
Order Number	Package Number	Package Description
74AC646SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74AC646SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74ACT646SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACT646SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Logic Symbols



#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
A <sub>0</sub> -A <sub>7</sub>	Data Register A Inputs
	Data Register A Outputs
B <sub>0</sub> -B <sub>7</sub>	Data Register B Inputs
	Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\bar{G}$	Output Enable Input
DIR	Direction Control Input

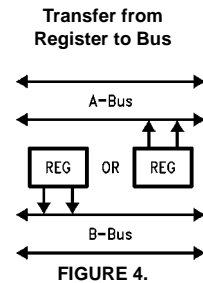
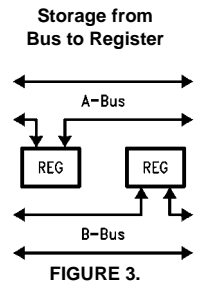
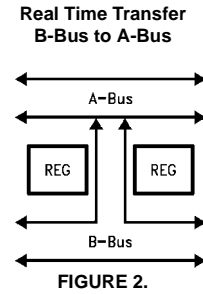
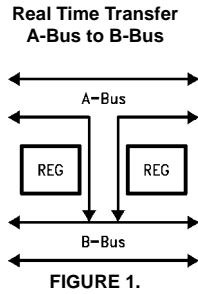
FACT™ is a trademark of Fairchild Semiconductor Corporation.

**Function Table**

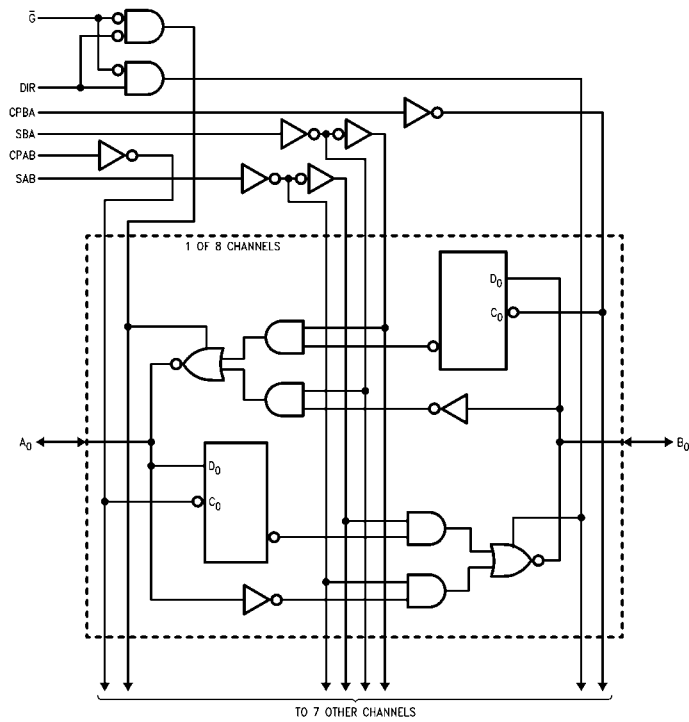
Inputs						Data I/O (Note 1)		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>0</sub> -A <sub>7</sub>	B <sub>0</sub> -B <sub>7</sub>	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↘	X	X	X			Clock A <sub>n</sub> Data into A Register
H	X	X	↘	X	X			Clock B <sub>n</sub> Data into B Register
L	H	X	X	L	X	Input	Output	A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode)
L	H	↘	X	L	X			Clock A <sub>n</sub> Data into A Register
L	H	H or L	X	H	X			A Register to B <sub>n</sub> (Stored Mode)
L	H	↘	X	H	X			Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	L	X	X	X	L	Output	Input	B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode)
L	L	X	↘	X	L			Clock B <sub>n</sub> Data into B Register
L	L	X	H or L	X	H			B Register to A <sub>n</sub> (Stored Mode)
L	L	X	↘	X	H			Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub>

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↘ = LOW-to-HIGH Transition

**Note 1:** The data output functions may be enabled or disabled by various signals at the  $\overline{G}$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.



**Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
PDIP	140°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
AC Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-  
out exception, to ensure that the system design is reliable over its power  
supply, temperature, and output/input loading variables. Fairchild does not  
recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics for AC**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits	Typ	Guaranteed Limits		
$V_{IH}$	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
$V_{IL}$	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
$V_{OH}$	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 3)	
		4.5		3.86	3.76			
		5.5		4.86	4.76			
$V_{OL}$	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = 12$ mA $I_{OL} = 24$ mA $I_{OH} = 24$ mA (Note 3)	
		4.5		0.36	0.44			
		5.5		0.36	0.44			
$I_{IN}$ (Note 5)	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, GND$	
$I_{OLD}$	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max	
$I_{OHD}$	Output Current (Note 4)	5.5			-75	mA	$V_{OHD} = 3.85V$ Min	
$I_{CC}$ (Note 5)	Maximum Quiescent Supply Current	5.5		8.0	80.0	$\mu A$	$V_{IN} = V_{CC}$ or GND	
$I_{OZT}$	Maximum I/O Leakage Current	5.5		$\pm 0.6$	$\pm 6.0$	$\mu A$	$V_I$ (OE) = $V_{IL}, V_{IH}$ $V_I = V_{CC}, GND$ $V_O = V_{CC}, GND$	

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:**  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

## DC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I <sub>OUT</sub> = -50 μA
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA (Note 6)
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I <sub>OUT</sub> = 50 μA
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA (Note 6)
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current (Note 7)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>OZT</sub>	Maximum I/O Leakage Current	5.5		±0.6	±6.0	μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND

**Note 6:** All outputs loaded; thresholds on input associated with output under test.

**Note 7:** Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V) (Note 8)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	3.3	4.0	10.5	16.5	3.0	18.5	ns
	Clock to Bus	5.0	2.5	7.5	12.0	2.0	13.0	
t <sub>PHL</sub>	Propagation Delay	3.3	3.0	9.5	14.5	2.5	16.0	ns
	Clock to Bus	5.0	2.0	6.5	10.5	1.5	11.5	
t <sub>PLH</sub>	Propagation Delay	3.3	2.5	7.5	12.0	2.0	13.5	ns
	Bus to Bus	5.0	1.5	5.0	8.0	1.0	9.0	
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	7.5	12.5	1.5	13.5	ns
	Bus to Bus	5.0	1.5	5.0	9.0	1.0	9.5	
t <sub>PLH</sub>	Propagation Delay	3.3	2.0	8.5	13.5	1.5	15.5	ns
	SBA or SAB to A <sub>n</sub> or B <sub>n</sub> (w/ A <sub>n</sub> or B <sub>n</sub> HIGH or LOW)	5.0	1.5	6.0	10.0	1.5	11.0	
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	8.5	13.5	1.5	15.0	ns
	SBA or SAB to A <sub>n</sub> or B <sub>n</sub> (w/ A <sub>n</sub> or B <sub>n</sub> HIGH or LOW)	5.0	1.5	6.0	10.0	1.5	11.0	
t <sub>PZH</sub>	Enable Time	3.3	2.5	7.0	11.5	2.0	12.5	ns
	$\overline{G}$ to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	5.0	8.5	1.5	9.0	
t <sub>PZL</sub>	Enable Time	3.3	2.5	7.5	12.5	2.0	14.0	ns
	$\overline{G}$ to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	5.5	9.0	1.5	10.0	
t <sub>PHZ</sub>	Disable Time	3.3	3.0	8.0	12.5	2.5	13.5	ns
	$\overline{G}$ to A <sub>n</sub> or B <sub>n</sub>	5.0	2.0	6.5	10.0	2.0	11.0	
t <sub>PLZ</sub>	Disable Time	3.3	2.0	7.5	12.0	2.0	13.5	ns
	$\overline{G}$ to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	6.0	9.5	1.5	10.5	
t <sub>PZH</sub>	Enable Time	3.3	2.0	6.5	11.0	1.5	12.0	ns
	DIR to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	5.0	7.5	1.0	8.5	
t <sub>PZL</sub>	Enable Time	3.3	2.5	7.0	11.5	2.0	13.0	ns
	DIR to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	5.0	8.0	1.0	9.0	
t <sub>PHZ</sub>	Disable Time	3.3	2.5	7.5	11.5	1.5	12.5	ns
	DIR to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	5.5	9.5	1.5	10.0	
t <sub>PLZ</sub>	Disable Time	3.3	1.5	7.5	12.0	1.5	13.5	ns
	DIR to A <sub>n</sub> or B <sub>n</sub>	5.0	1.5	5.5	9.5	1.5	10.5	

Note 8: Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements for AC

Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Typ	Guaranteed Minimum			
t <sub>S</sub>	Setup Time, HIGH or LOW	3.3	2.0	5.0	5.5		ns
	Bus to Clock	5.0	1.5	4.0	4.5		
t <sub>H</sub>	Hold Time, HIGH or LOW	3.3	-1.5	0	0		ns
	Bus to Clock	5.0	-0.5	0.5	1.0		
t <sub>W</sub>	Clock Pulse Width	3.3	2.0	3.5	4.5		ns
	HIGH or LOW	5.0	2.0	3.5	3.5		

Note 9: Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT								
Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Clock to Bus	5.0	3.5	12.0	14.5	3.0	16.0	ns
t <sub>PHL</sub>	Propagation Delay Clock to Bus	5.0	4.0	12.0	14.5	3.5	16.0	ns
t <sub>PLH</sub>	Propagation Delay Bus to Bus	5.0	3.0	8.5	10.5	2.5	11.5	ns
t <sub>PHL</sub>	Propagation Delay Bus to Bus	5.0	2.5	8.5	10.5	2.0	11.5	ns
t <sub>PLH</sub>	Propagation Delay SBA or SAB to A <sub>n</sub> to B <sub>n</sub> (w/A <sub>n</sub> or B <sub>n</sub> , HIGH or LOW)	5.0	3.0	9.5	11.5	2.5	12.5	ns
t <sub>PHL</sub>	Propagation Delay SBA or SAB to A <sub>n</sub> to B <sub>n</sub> (w/A <sub>n</sub> or B <sub>n</sub> , HIGH or LOW)	5.0	3.0	9.5	11.5	2.5	12.5	ns
t <sub>PZH</sub>	Enable Time $\overline{G}$ to A <sub>n</sub> or B <sub>n</sub>	5.0	2.0	9.0	11.0	1.5	12.0	ns
t <sub>PZL</sub>	Enable Time $\overline{G}$ to A <sub>n</sub> or B <sub>n</sub>	5.0	3.5	9.0	11.0	3.0	12.0	ns
t <sub>PHZ</sub>	Disable Time $\overline{G}$ to A <sub>n</sub> or B <sub>n</sub>	5.0	5.0	10.5	13.0	4.5	14.5	ns
t <sub>PLZ</sub>	Disable Time $\overline{G}$ to A <sub>n</sub> or B <sub>n</sub>	5.0	3.5	10.0	12.5	3.0	14.0	ns
t <sub>PZH</sub>	Enable Time DIR to A <sub>n</sub> or B <sub>n</sub>	5.0	2.0	6.5	10.5	1.5	11.5	ns
t <sub>PZL</sub>	Enable Time DIR to A <sub>n</sub> or B <sub>n</sub>	5.0	3.5	6.5	10.5	3.0	11.5	ns
t <sub>PHZ</sub>	Disable Time DIR to A <sub>n</sub> or B <sub>n</sub>	5.0	5.0	8.5	12.5	4.5	13.5	ns
t <sub>PLZ</sub>	Disable Time DIR to A <sub>n</sub> or B <sub>n</sub>	5.0	3.5	8.5	12.5	3.0	13.5	ns

**Note 10:** Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for ACT						
Symbol	Parameter	V <sub>CC</sub> (V) (Note 11)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	Units
			Typ	Guaranteed Minimum		
t <sub>S</sub>	Setup Time, HIGH or LOW BUS to Clock	5.0	2.5	7.0	8.0	ns
t <sub>H</sub>	Hold Time, HIGH or LOW Bus to Clock	5.0	0	2.5	2.5	ns
t <sub>W</sub>	Clock Pulse Width HIGH or LOW	5.0	4.5	7.0	8.0	ns

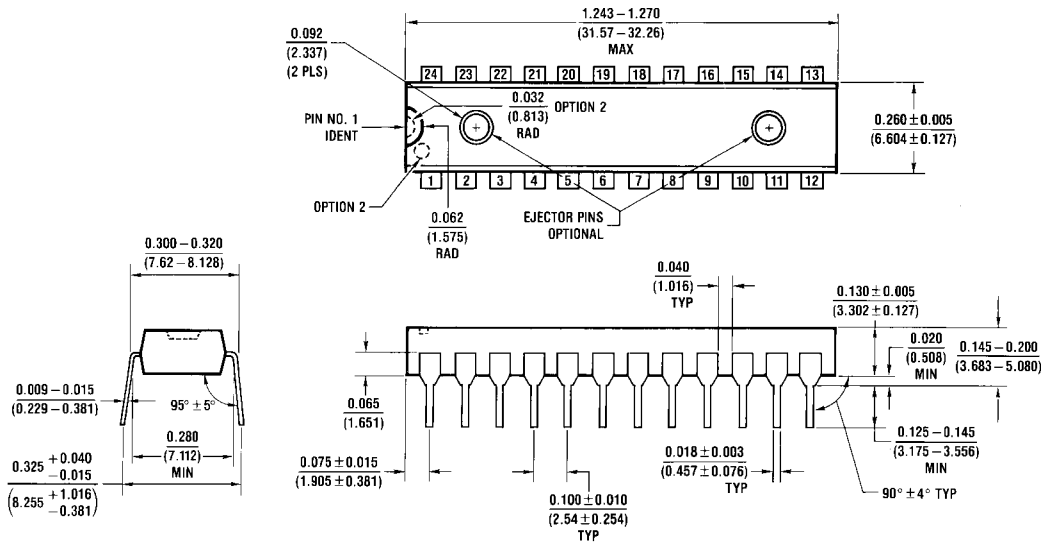
**Note 11:** Voltage Range 5.0 is 5.0V ± 0.5V

### Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>I/O</sub>	Input/Output Capacitance	15.0	pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance	60.0	pF	V <sub>CC</sub> = 5.0V



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N24C**

N24C (REV F)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View 74AC646SPC on WIN SOURCE](#)
- ⊖ [Fairchild/ON Semiconductor Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management