



# THE DATASHEET OF 74F652SPC



## 74F652 Transceivers/Registers

### General Description

These devices consist of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

### Features

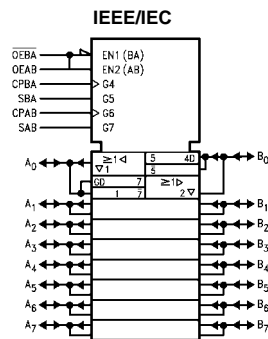
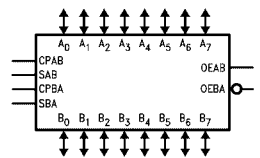
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 74F652 non-inverting data path

### Ordering Code:

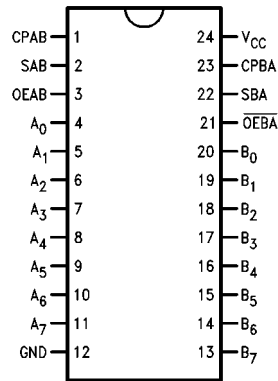
Order Number	Package Number	Package Description
74F652SC (Note 1)	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F652SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

**Note 1:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



## Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0$ – $A_7$ , $B_0$ – $B_7$	A and B Inputs/ 3-STATE Outputs	1.0/1.0 600/106.6 (80)	20 $\mu$ A/–0.6 mA –12 mA/64 mA (48 mA)
CPAB, CPBA	Clock Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
SAB, SBA	Select Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
OEAB, OEBA	Output Enable Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA

## Function Table

Inputs						Inputs/Outputs (Note 2)		Operating Mode
OEAB	OEBA	CPAB	CPBA	SAB	SBA	$A_0$ thru $A_7$	$B_0$ thru $B_7$	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	$\curvearrowright$	$\curvearrowright$	X	X			Store A and B Data
X	H	$\curvearrowright$	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	$\curvearrowright$	$\curvearrowright$	X	X	Input	Output	Store A in Both Registers
L	X	H or L	$\curvearrowright$	X	X	Not Specified	Input	Hold A, Store B
L	L	$\curvearrowright$	$\curvearrowright$	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level      X = Immaterial  
L = LOW Voltage Level       $\curvearrowright$  = LOW-to-HIGH Clock Transition

**Note 2:** The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

## Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW-to-HIGH transitions at the appropriate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

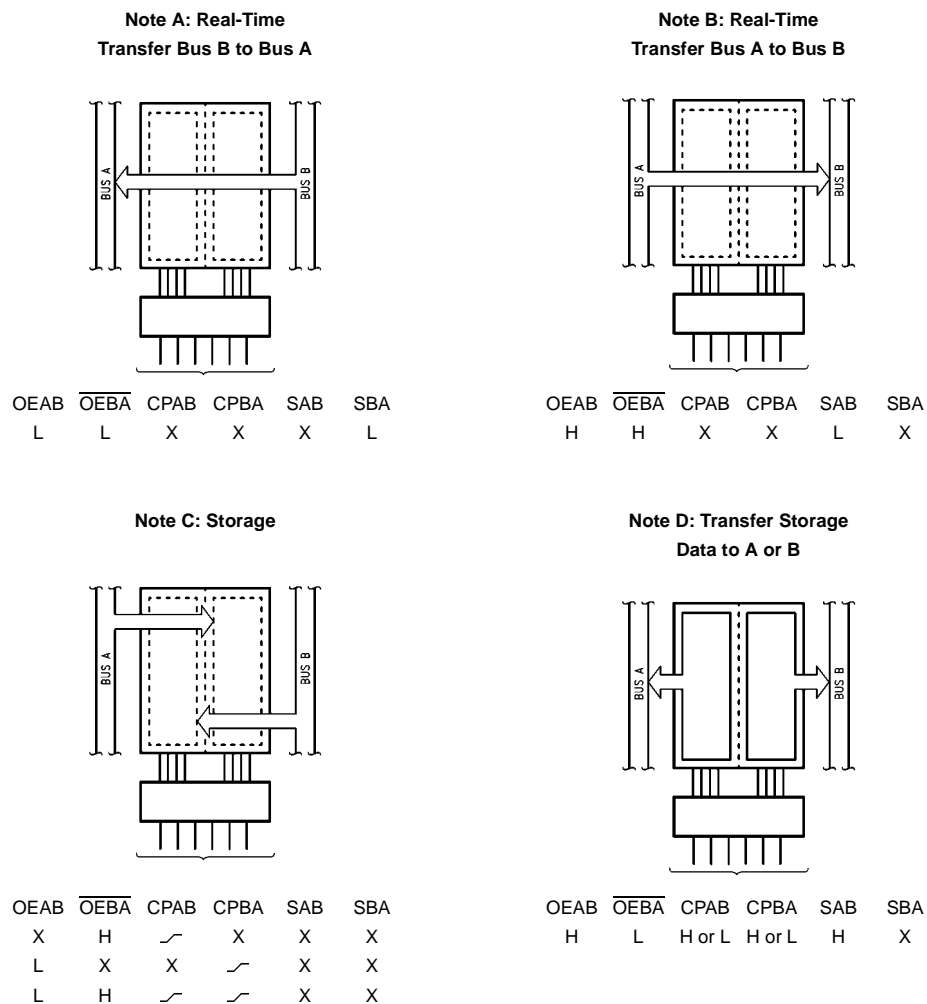
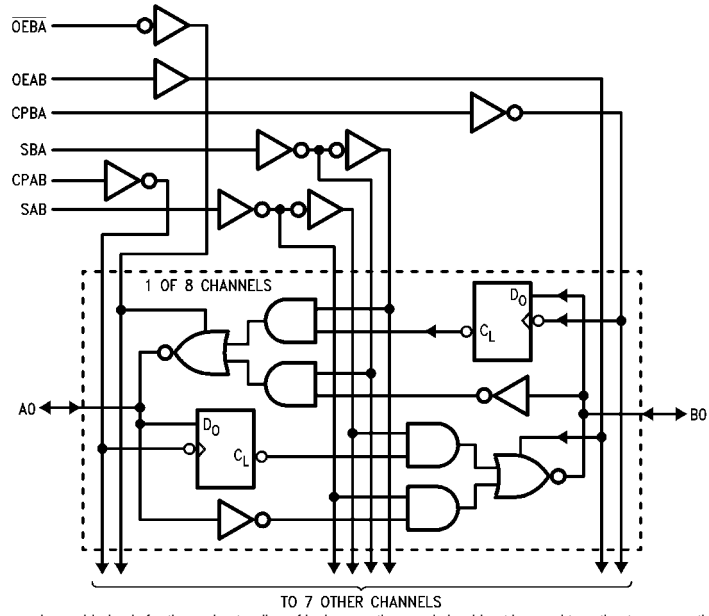


FIGURE 1.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 3)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 4)	-0.5V to +7.0V
Input Current (Note 4)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 3:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

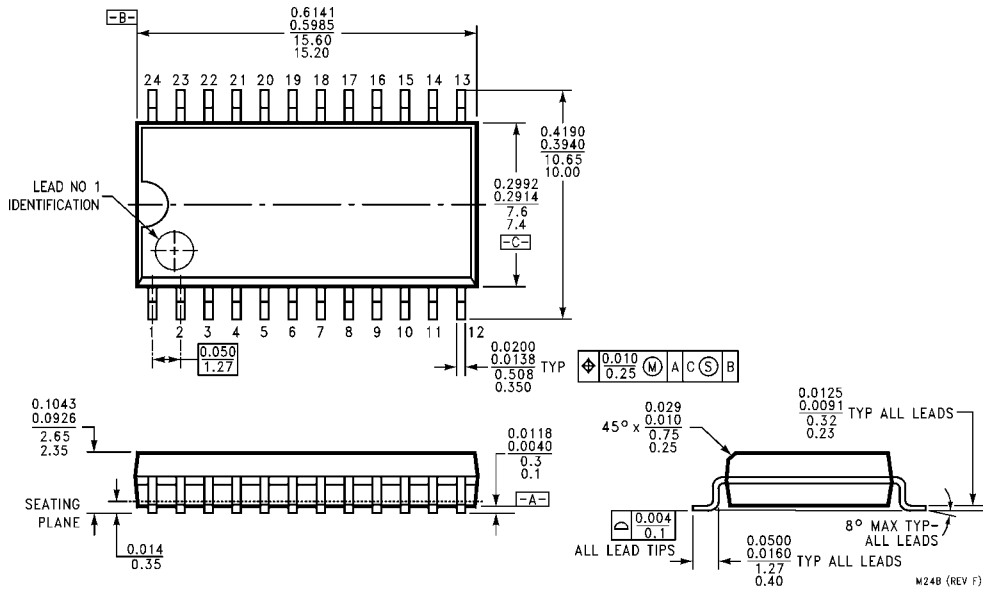
**Note 4:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	2.0		V	Min	I <sub>OH</sub> = -15 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V (Non I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>I<sub>OD</sub></sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		105	135	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		118	150	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		115	150	mA	Max	V <sub>O</sub> = HIGH Z

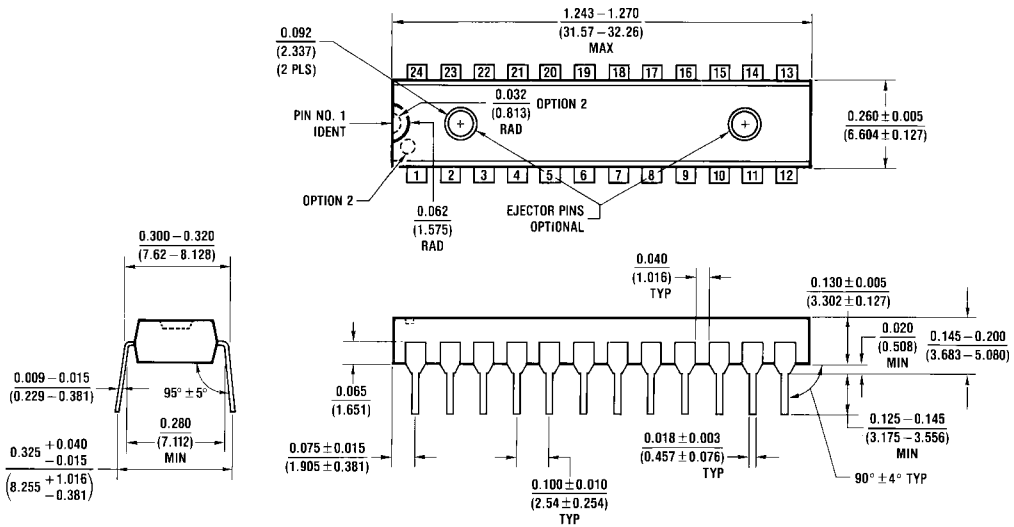
AC Electrical Characteristics								
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Max	Min	Max	Min	Max	
$f_{MAX}$	Max. Clock Frequency	90		75		90		MHz
$t_{PLH}$	Propagation Delay	2.0	7.0	2.0	8.5	2.0	8.0	ns
$t_{PHL}$	Clock to Bus	2.0	8.0	2.0	9.5	2.0	9.0	
$t_{PLH}$	Propagation Delay	1.0	7.0	1.0	8.0	1.0	7.5	ns
$t_{PHL}$	Bus to Bus	1.0	6.5	1.0	8.0	1.0	7.0	
$t_{PLH}$	Propagation Delay	2.0	8.5	2.0	11.0	2.0	9.5	ns
$t_{PHL}$	SBA or SAB to A or B	2.0	8.0	2.0	10.0	2.0	9.0	
AC Operating Requirements								
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		Units
		Min	Max	Min	Max	Min	Max	
$t_{PZH}$	Enable Time	2.0	9.5	2.0	10.0	2.0	10.0	ns
$t_{PZL}$	*OEBA to A	2.0	12.0	2.0	10.0	2.0	12.5	
$t_{PHZ}$	Disable Time	1.0	7.5	1.0	9.0	1.0	8.0	
$t_{PLZ}$	*OEBA to A	2.0	8.5	1.0	9.0	2.0	9.0	
$t_{PZH}$	Enable Time	2.0	9.5	2.0	10.0	2.0	10.0	ns
$t_{PZL}$	OEAB to B	3.0	13.0	2.0	12.0	3.0	14.0	
$t_{PHZ}$	Disable Time	2.0	9.0	1.0	9.0	2.0	10.0	ns
$t_{PLZ}$	OEAB to B	2.0	10.5	1.0	12.0	2.0	11.0	
$t_S(H)$	Setup Time, HIGH or	5.0		5.0		5.0		ns
$t_S(L)$	LOW, Bus to Clock	5.0		5.0		5.0		
$t_H(H)$	Hold Time, HIGH or	2.0		2.5		2.0		ns
$t_H(L)$	LOW, Bus to Clock	2.0		2.5		2.0		
$t_W(H)$	Clock Pulse Width	5.0		5.0		5.0		ns
$t_W(L)$	HIGH or LOW	5.0		5.0		5.0		

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M24B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



N24C (REV F)

**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N24C**

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