



**THE DATASHEET OF  
74F827SPC**



## 74F827 • 74F828 10-Bit Buffers/Line Drivers

### General Description

The 74F827 and 74F828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

The 74F828 is an inverting version of the 74F827.

### Features

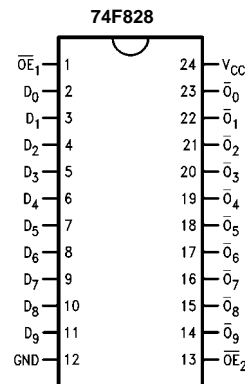
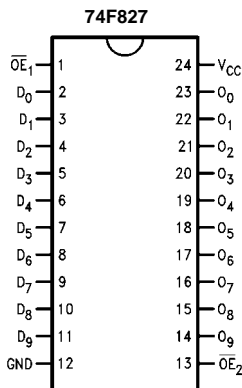
- 3-STATE output
- 74F828 is inverting

### Ordering Code:

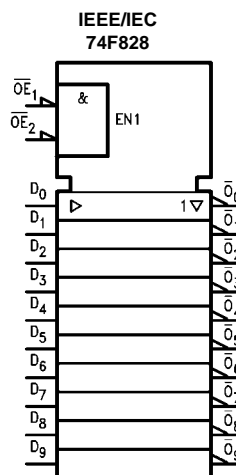
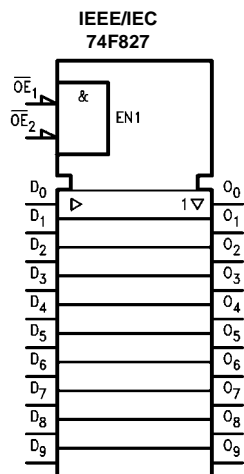
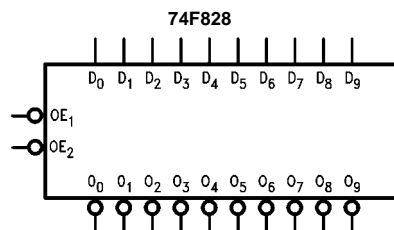
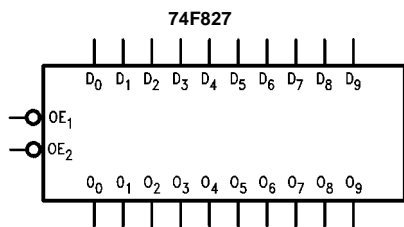
Order Number	Package Number	Package Description
74F827SC (Note 1)	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F827SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74F828SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F828SPC (Note 1)	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

**Note 1:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagrams



### Logic Symbols



### Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input	1.0/1.0	20 $\mu$ A/-0.6 mA
$D_0$ - $D_7$	Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$O_0$ - $O_7$	Data Outputs, 3-STATE	600/106.6 (80)	-12 mA/64 mA (48 mA)

### Functional Description

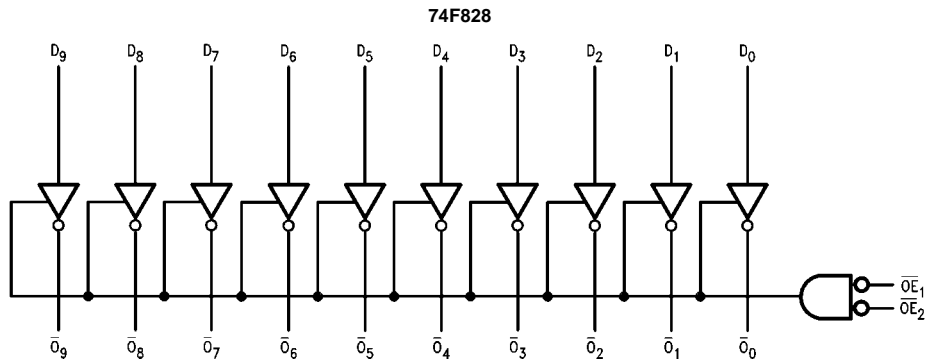
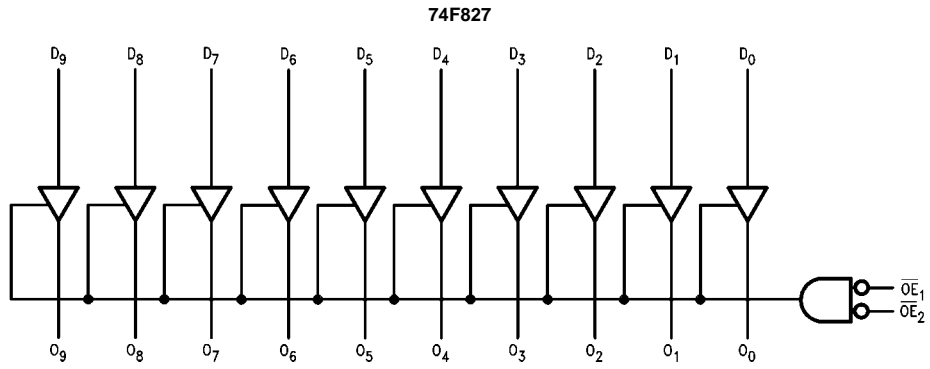
The 74F827 and 74F828 are line drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density. The devices have 3-STATE outputs controlled by the Output Enable ( $\overline{OE}$ ) pins. The outputs can sink 64 mA and source 15 mA. Input clamp diodes limit high-speed termination effects.

### Function Table

Inputs		Outputs		Function
$\overline{OE}$	$D_n$	$O_n$		
		74F827	74F828	
L	H	H	L	Transparent
L	L	L	H	Transparent
H	X	Z	Z	High Z

H = HIGH Voltage level  
 L = LOW Voltage Level  
 Z = High Impedance  
 X = Immaterial

Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

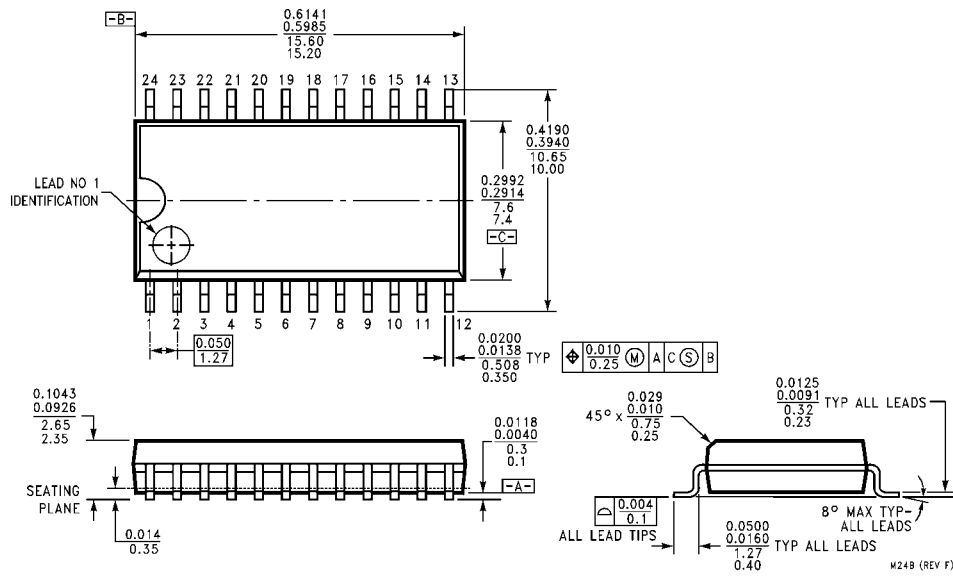
**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA
		10% V <sub>CC</sub>	2.0		V	Min	I <sub>OH</sub> = -15 mA
		5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current (74F827)		30	45	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current (74F827)		60	90	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current (74F827)		40	60	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current (74F828)		14	20	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current (74F828)		56	85	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current (74F828)		35	50	mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics

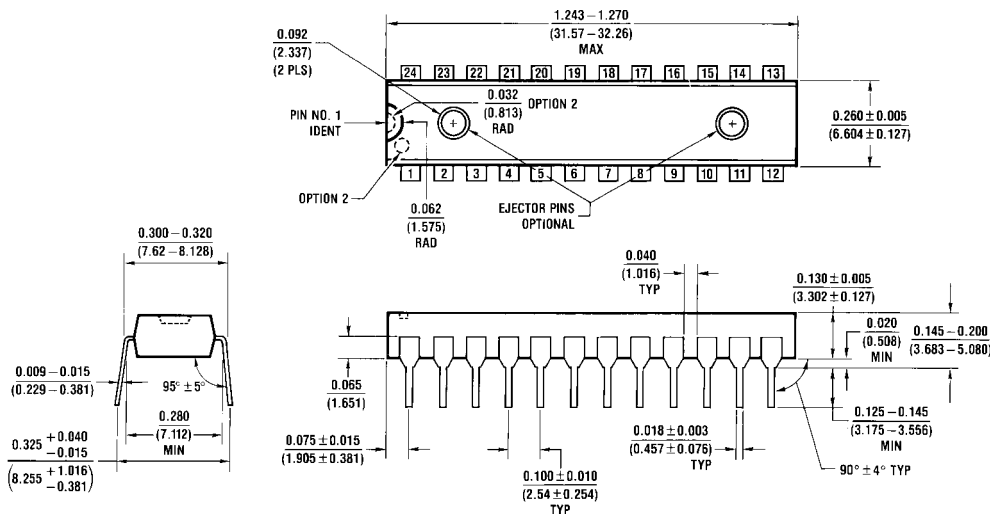
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay	1.0	3.0	5.5	1.0	7.5	1.0	6.5	ns
$t_{PHL}$	Data to Output (74F827)	1.5	3.3	5.5	1.5	7.0	1.5	6.0	
$t_{PLH}$	Propagation Delay	1.0	3.0	5.0			1.0	5.5	ns
$t_{PHL}$	Data to Output (74F828)	1.0	2.0	4.0			1.0	4.0	
$t_{PZH}$	Output Enable Time	3.0	5.7	9.0	2.5	10.0	2.5	9.5	ns
$t_{PZL}$	$\overline{OE}$ to $O_n$	3.5	6.8	11.5	3.0	12.5	3.0	12.0	
$t_{PHZ}$	Output Disable Time	1.5	3.3	8.0	1.5	9.0	1.5	8.5	ns
$t_{PLZ}$	$\overline{OE}$ to $O_n$	1.0	3.5	8.0	1.0	9.0	1.0	8.5	

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M24B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N24C**

N24C (REV F)

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