THE DATASHEET OF

SN65LVDS049PWR

www.win-source.net 0086-755-83957316

SN65LVDS049 Dual-LVDS Differential Drivers and Receivers

1 Features

- DS90LV049 Compatible
- Up to 400-Mbps Signaling Rates
- Flow-Through Pinout
- 50-ps Driver Channel-to-Channel Skew (Typical)
- 50-ps Receiver Channel-to-Channel Skew (Typical)
- 3.3-V Power Supply
- High-Impedance Disable for All Outputs
- Internal Fail-safe Biasing of Receiver Inputs
- 1.4-ns Driver Propagation Delay (Typical)
- 1.9-ns Receiver Propagation Delay (Typical)
- High-Impedance Bus Pins on Power Down
- ANSI TIA/EIA-644-A Compliant
- Receiver Input and Driver Output ESD Exceeds 10 kV
- 16-Pin TSSOP Package

2 Applications

- Full-Duplex LVDS Communications of Clock and Data
- Printers

3 Description

The SN65LVDS049 device is a dual flow-through differential line driver-receiver pair that uses low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The driver and receiver electrical interfaces are compliant to the TIA/EIA-644-A standard.

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.

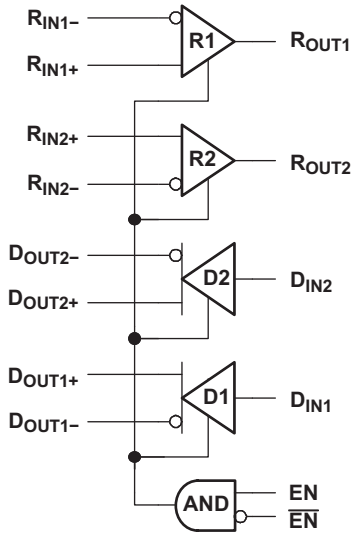
The SN65LVDS049 is characterized for operation from –40°C to 85°C

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS049	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Device Electrical Characteristics ... 5
6.6 Switching Characteristics ... 6
6.7 Dissipation Rating ... 6
6.8 Typical Characteristics ... 7
7 Parameter Measurement Information ... 8
8 Detailed Description ... 11
8.1 Overview ... 11
8.2 Functional Block Diagram ... 11
8.3 Feature Description ... 11
8.4 Device Functional Modes ... 12
9 Application and Implementation ... 14
9.1 Application Information ... 14
9.2 Typical Applications ... 14
10 Power Supply Recommendations ... 19
11 Layout ... 20
11.1 Layout Guidelines ... 20
11.2 Layout Example ... 23
12 Device and Documentation Support ... 25
12.1 Device Support ... 25
12.2 Documentation Support ... 25
12.3 Community Resources ... 25
12.4 Trademarks ... 25
12.5 Electrostatic Discharge Caution ... 25
12.6 Glossary ... 25
13 Mechanical, Packaging, and Orderable Information ... 25

4 Revision History

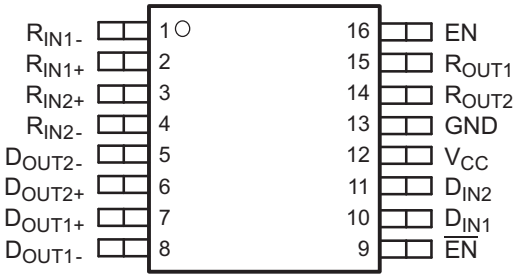
Changes from Original (August 2003) to Revision A **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Copyright © 2003–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

PW Package (Marked as LVDS049)
16-Pin TSSOP
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	13	–	Ground
D_{IN1}	10	I	LVTTL input signals
D_{IN2}	11		
D_{OUT1+}	7	O	Differential (LVDS) noninverting output
D_{OUT2+}	6		
$D_{OUT1–}$	8	O	Differential (LVDS) inverting output
$D_{OUT2–}$	5		
EN	16	I	Driver and receiver enable
$\overline{EN}$	9	I	Driver and receiver inverse-enable
R_{IN1+}	2	I	Differential (LVDS) noninverting input
R_{IN2+}	3		
$R_{IN1–}$	1	I	Differential (LVDS) inverting input
$R_{IN2–}$	4		
R_{OUT1}	15	O	LVTTL output signals
R_{OUT2}	14		
V_{CC}	12	–	Supply voltage

Copyright © 2003–2015, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage(2), V_{CC}		–0.3	4	V
Voltage	D_{IN}, R_{OUT}, EN, or $\overline{EN}$	–0.3	(V_{CC} + 0.3 V)	V
	R_{IN+} or R_{IN-}	–0.3	4	
	D_{OUT+} or D_{OUT-}	–0.3	3.9	
LVDS output short circuit duration (DOUT+, DOUT-)		Continuous		
Continuous power dissipation		See *Dissipation Rating*		
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds			260	°C
Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	R_{IN+}, R_{IN-}, D_{OUT+}, and D_{OUT-}	±10000	V
			All pins	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Receiver input voltage	GND			V
Common-mode input voltage, V_{IC}	$2.4 - \frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V
			V_{CC} - 0.8	V
Operating free-air temperature, T_A	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN65LVDS049 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	10.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2003–2015, Texas Instruments Incorporated

6.5 Device Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
INPUT DC SPECIFICATIONS (D_{IN}, EN, $\overline{EN}$)						
V_{IH}	Input high voltage		2		V_{CC}	V
V_{IL}	Input low voltage		GND		0.8	V
I_{IH}	Input high current	$V_{IN} = V_{CC}$	–10	3	10	µA
I_{IL}	Input low current	V_{IN} = GND	–10	1	10	µA
V_{CL}	Input clamp voltage	I_{CL} = -18 mA	–1.5	–0.8		V
LVDS OUTPUT DC SPECIFICATIONS (D_{OUT+}, D_{OUT-})						
$\|V_{OD}\|$	Differential output voltage	R_L = 100 Ω, See Figure 3	250	350	450	V
$\Delta\|V_{OD}\|$	Change in magnitude of V_{OD} for complementary output states		–35	1	35	mV
V_{OS}	Offset voltage		1.125	1.2	1.375	V
ΔV_{OS}	Change in magnitude of V_{OS} for complementary output states		–25	1	25	mV
I_{OS}	Output short-circuit current	Enabled $D_{IN} = V_{CC}$ and D_{OUT+} = 0 V, or D_{IN} = GND and D_{OUT-} = 0 V		-4.5	-9	mA
I_{OSD}	Differential output short-circuit current(2)	Enabled, V_{OD} = 0 V		–3.6	-9	mA
I_{OFF}	Power-off leakage	V_{CC} = 0 V or Open; VO = 0 or 3.6 V	–20	0	20	µA
I_{OZ}	Output high-impedance current	EN = 0 V and $\overline{EN} = V_{CC}$, V_O = 0 or V_{CC}	–10	0	10	µA
LVDS INPUT DC SPECIFICATIONS (R_{IN+}, R_{IN-})						
V_{IT+}	Differential input high threshold	V_{CM} = 1.2 V, 0.05 V, 2.35 V			100	mV
V_{IT-}	Differential input low threshold	V_{CM} = 1.2 V, 0.05 V, 2.35 V	–100			mV
V_{CMR}	Common-mode voltage range	V_{ID} = ± 100 mV	0.05		2.35	V
I_{IN}	Input current	V_{CC} = 3.6 V, V_{IN} = 0 V or 2.8 V	–20		20	µA
		V_{CC}= 0 V, V_{IN} = 0 V, 2.8 V, or 3.6 V	–20		20	
OUTPUTS DC SPECIFICATIONS (R_{OUT})						
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{ID} = 200 mV	2.7	3.3		V
V_{OL}	Output low voltage	I_{OL} = 2 mA, V_{ID} = –200 mV		0.05	0.25	V
I_{OZ}	Output high-impedance current	Disabled, V_{OUT} = 0 V or V_{CC}	–10	0	10	µA
DEVICE DC SPECIFICATIONS						
I_{CC}	Power supply current (LVDS loaded, enabled)	EN = 3.3 V, $D_{IN} = V_{CC}$ or Gnd, 100-Ω differential LVDS loads		17	35	mA
I_{CCZ}	High-impedance supply current (disabled)	No loads, EN = 0 V		1	25	mA

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) Output short-circuit current (IOS) is specified as magnitude only; the minus sign indicates direction only

Copyright © 2003–2015, Texas Instruments Incorporated

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
LVDS OUTPUTS (D_{OUT+}, D_{OUT-})						
t_{PLHD}	Differential propagation delay low to high	R_L = 100 Ω, C_L = 15 pF distributed, See Figure 4		1.3	2	ns
t_{PHLD}	Differential propagation delay high to low			1.4	2	ns
$t_{sk(p)}$	Differential pulse skew ($\|t_{PHL} - t_{PLH}\|$)		0	0.15	0.4	ns
$t_{sk(o)}$	Differential channel-to-channel skew(2)		0	0.05	0.5	ns
$t_{sk(pp)}$	Differential part-to-part skew(3)		0		1	ns
t_r	Differential rise time		0.2	0.5	1	ns
t_f	Differential fall time		0.2	0.5	1	ns
t_{PHZ}	Disable time, high level to high impedance	R_L = 100 Ω, C_L = 15 pF distributed, See Figure 5		2.7	4	ns
t_{PLZ}	Disable time, low level to high impedance			2.7	4	ns
t_{PZH}	Enable time, high impedance to high level		1	5	8	ns
t_{PZL}	Enable time, high impedance to low level		1	5	8	ns
f_{MAX}	Maximum operating frequency(4)			250		MHz
LVCMOS OUTPUTS (R_{OUT})						
t_{PLH}	Propagation delay low to high	V_{ID}= 200 mV, C_L = 15 pF distributed, See Figure 6	0.5	1.9	3.5	ns
t_{PHL}	Propagation delay high to low		0.5	1.7	3.5	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)		0	0.2	0.4	ns
$t_{sk(o)}$	Channel-to-channel skew(5)		0	0.05	0.5	ns
$t_{sk(pp)}$	Part-to-part skew(6)		0		1	ns
t_r	Rise time		0.3	0.5	1.4	ns
t_f	Fall time		0.3	0.5	1.4	ns
t_{PHZ}	Disable time, high level to high impedance	C_L = 15 pF distributed, See Figure 7	3	7.2	9	ns
t_{PLZ}	Disable time, low level to high impedance		2.5	4	8	ns
t_{PZH}	Enable time, high impedance to high level		2.5	4.2	7	ns
t_{PZL}	Enable time, high impedance to low level		2	3.3	7	ns
f_{MAX}	Maximum operating frequency(7)		200	250		MHz

(1) All typical values are at 25°C and with a 3.3 V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) $f_{(MAX)}$ generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output Criteria: duty cycle = 45% to 55%, V_{OD} > 250 mV, all channels switching.
(5) $t_{sk(lim)}$ is the maximum delay time difference between drivers over temperature, V_{CC}, and process.
(6) tsk(pp) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate wf(MAX) generaith the same supply voltages, at the same temperature, and have identical packages and test circuits
(7) $f_{(MAX)}$ generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, V_{ID} = 200 mV, V_{CM} = 1.2 V. Output criteria: duty cycle = 45% to 55%, V_{OH} > 2.7 V, V_{OL} < 0.25 V, all channels switching.

6.7 Dissipation Rating

PACKAGE	CIRCUIT BOARD MODEL	T_A ≤25°C POWER RATING	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING
PW	Low-K(2)	774 mW	6.2 mW/°C	402 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

Copyright © 2003–2015, Texas Instruments Incorporated

6.8 Typical Characteristics

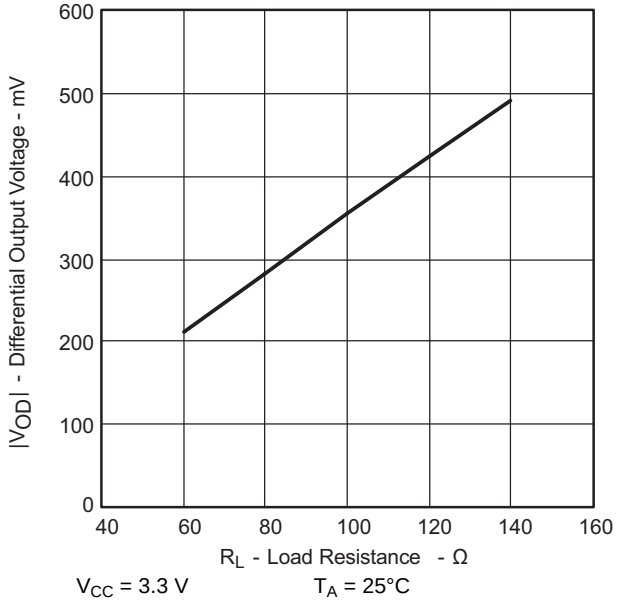


Figure 1. V_{OD} vs. Load Resistance

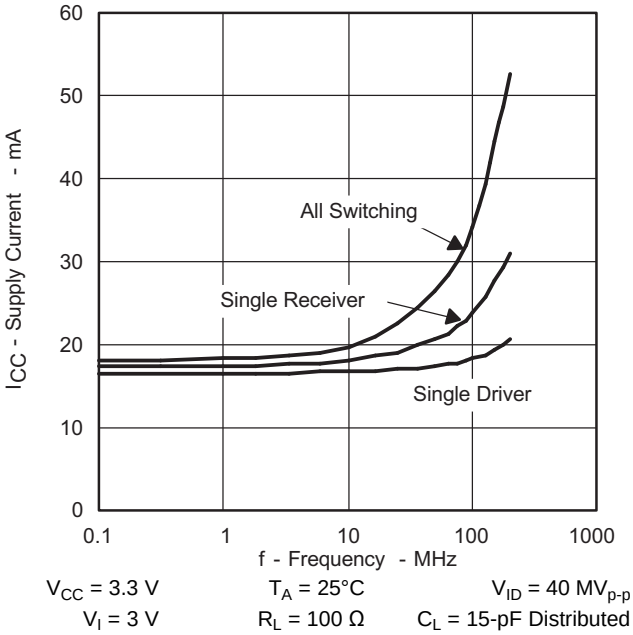


Figure 2. Power Supply Current vs. Frequency

7 Parameter Measurement Information

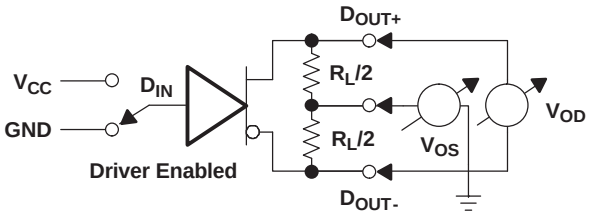


Figure 3. Driver V_{OD} and V_{OS} Test Circuit

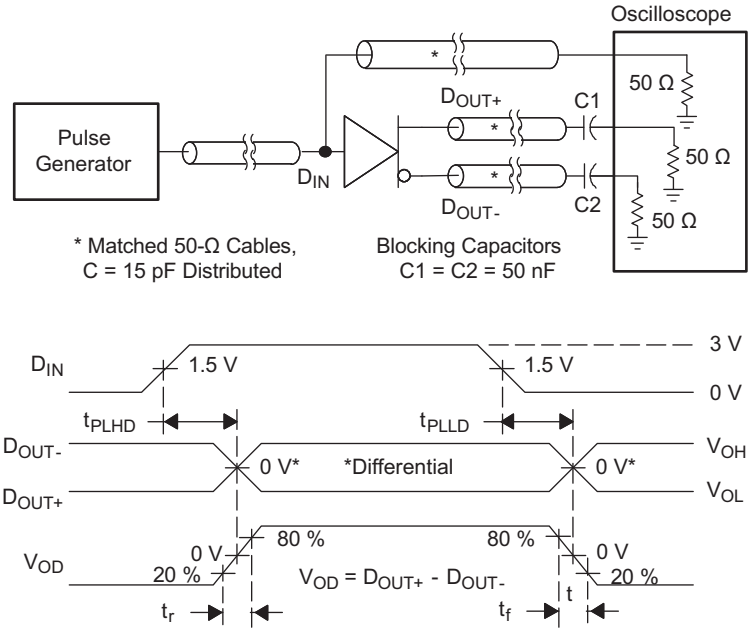


Figure 4. Driver Propagation Delay and Rise and Fall Time Test Circuit and Waveforms

Copyright © 2003–2015, Texas Instruments Incorporated

Parameter Measurement Information (continued)

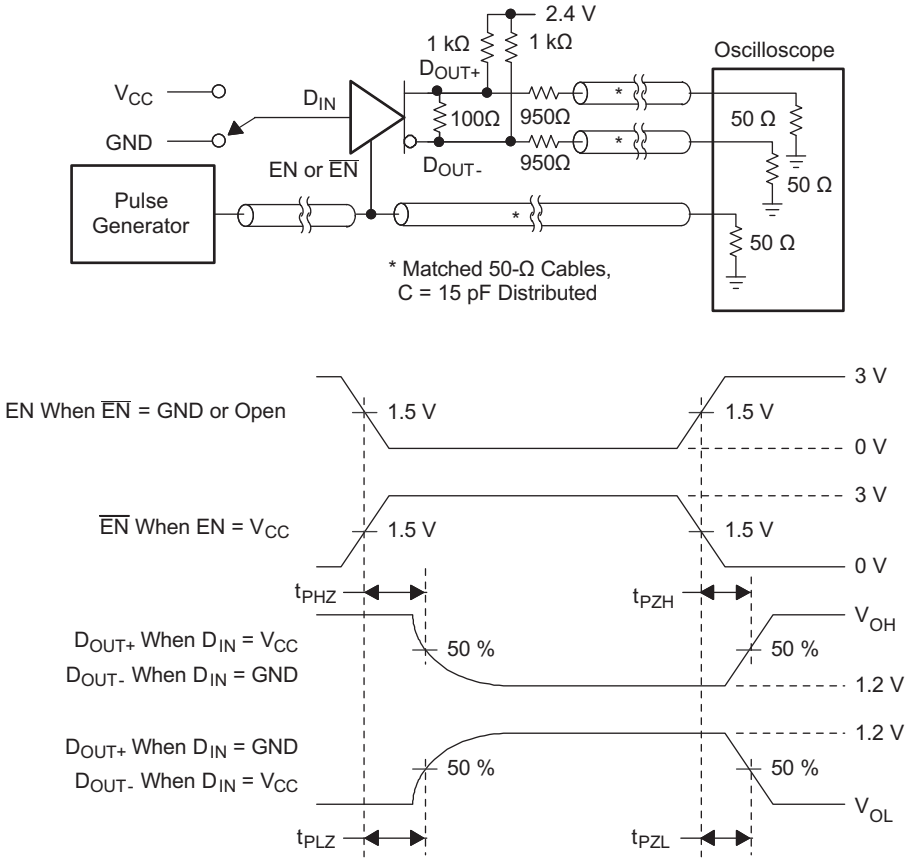


Figure 5. Driver High-Impedance State Delay Test Circuit and Waveforms

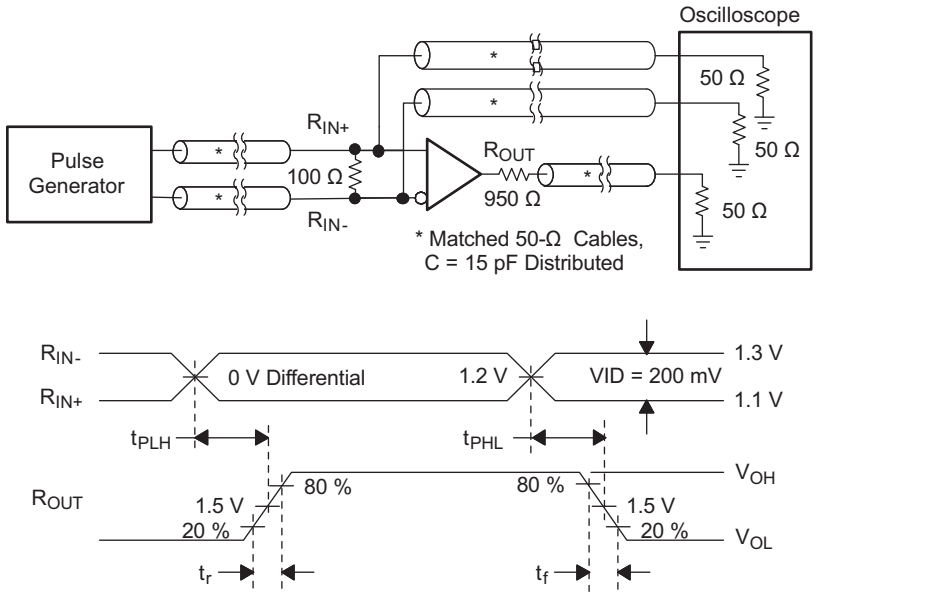


Figure 6. Receiver Propagation Delay and Rise and Fall Test Circuit and Waveforms

Copyright © 2003–2015, Texas Instruments Incorporated

Parameter Measurement Information (continued)

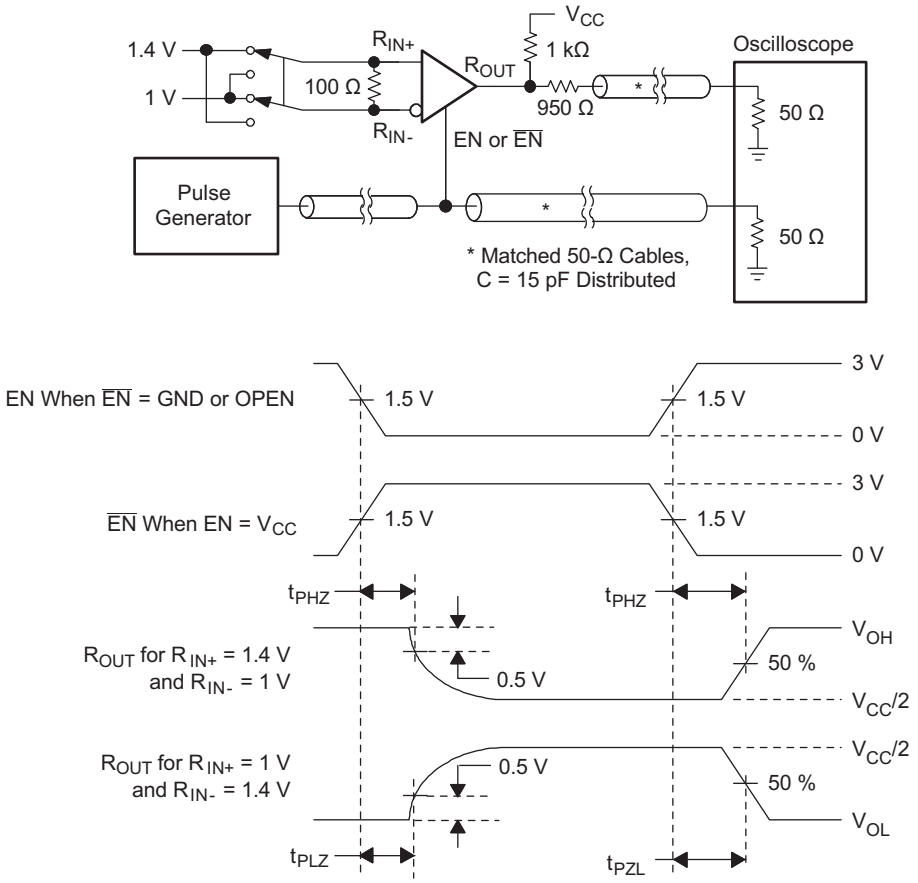


Figure 7. Receiver High-Impedance State Delay Test Circuit and Waveforms (V_{CC} = 3.3 V)

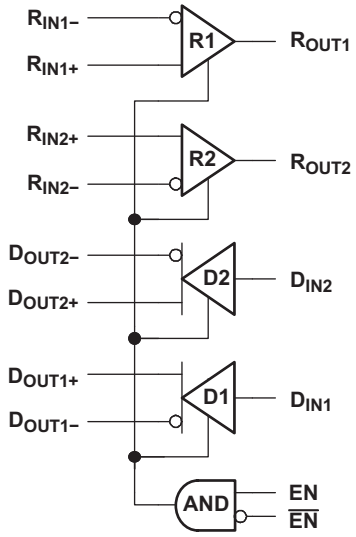
Copyright © 2003–2015, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The SN65LVDS049 device is a dual flow-through differential line driver-receiver pair that uses low-voltage differential signaling (LVDS) to achieve signaling rates of up to 400 Mbps. The device operates from a single supply that is nominally 3.3 V, but can be as low as 3.0 V and as high as 3.6 V. The TIA/EIA-644-A standard compliant electrical interface provides a minimum differential output voltage magnitude of 250 mV into a 100-Ω load and receipt of signals with up to 1 V of ground potential difference between a transmitter and receiver. The LVDS receivers have internal fail-safe biasing that places the outputs into a known high state for unconnected differential inputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Driver Offset

An LVDS-compliant driver is required to maintain the common-mode output voltage at 1.2 V. The SN65LVDS049 incorporates sense circuitry and a control loop to source common-mode current and keep the output signal within specified values. Further, the device maintains the output common-mode voltage at this set point over the full 3 V to 3.6 V supply range.

8.3.2 Receiver Open Circuit Fail-Safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers in that its output logic state can be indeterminate when the differential input voltage is in the range from –100 mV to 100 mV and within its recommended input common-mode voltage range. However, the TI LVDS receiver is different in how it handles the open-input circuit situation.

Open circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal to VCC through 300-kΩ resistors as shown in Figure 8. The fail-safe feature uses an AND gate to detect this condition and force the output to a high level.

Copyright © 2003–2015, Texas Instruments Incorporated

Feature Description (continued)

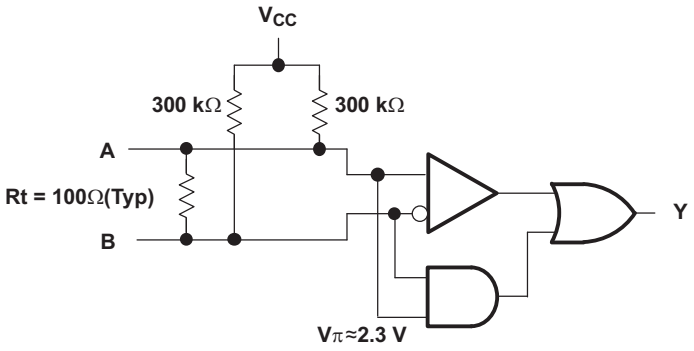


Figure 8. Open-Circuit Fail-Safe of the LVDS Receiver

Only under these conditions is the output of the receiver valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in Figure 8. Other termination circuits may allow a DC to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

8.3.3 Receiver Common-Mode Range

For all supply voltages, the valid input signal is from ground to 0.9 V below the supply rail. Hence, if the device is operating with a 3.3-V supply, and a minimum differential voltage of 100 mV, common-mode values in the range of 0.05 V to 2.35 V are supported.

8.4 Device Functional Modes

Table 1. Driver Truth Table

INPUT	ENABLES		OUTPUTS(1)	
DIN	EN	$\overline{EN}$	D_{OUT+}	D_{OUT-}
L	H	L or OPEN	L	H
H			H	L
X	All other conditions		Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

Table 2. Receiver Truth Table

DIFFERENTIAL INPUT	ENABLES		OUTPUT(1)
$R_{IN-} - R_{IN+}$	EN	$\overline{EN}$	R_{OUT}
$V_{ID} \geq 100$ mV	H	L or OPEN	H
$V_{ID} \leq -100$ mV			L
Open/short or terminated			H
X	All other conditions		Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

Copyright © 2003–2015, Texas Instruments Incorporated

Table 3. Enable Function Table

ENABLES		OUTPUTS	
EN	$\overline{EN}$	LVDS Out	LVCMOS Out
L or Open	L or Open	Disabled	Disabled
H	L or Open	Enabled	Enabled
L or Open	H	Disabled	Disabled
H	H	Disabled	Disabled

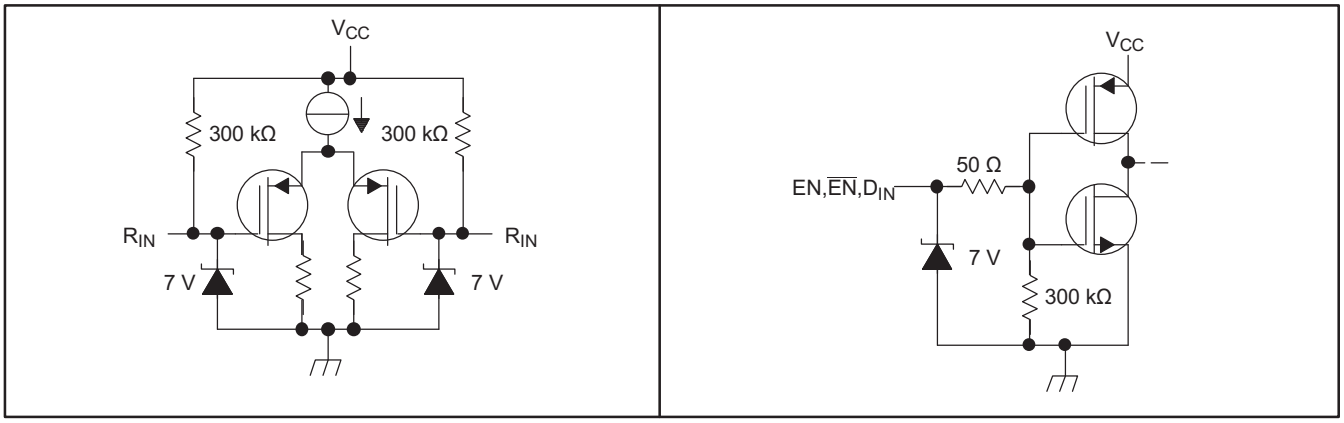


Figure 9. Equivalent Input and Output Schematic Diagrams

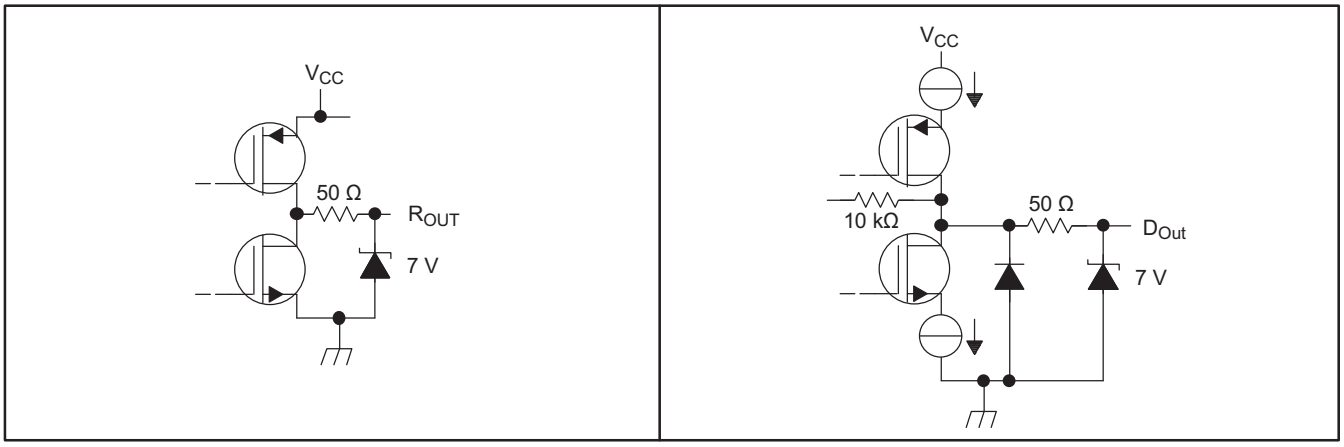


Figure 10. Equivalent Input and Output Schematic Diagrams

Copyright © 2003–2015, Texas Instruments Incorporated

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN65LVDS049 is a dual LVDS driver-receiver pair. The functionality of these devices is simple, yet extremely flexible, leading to their use in designs ranging from wireless base stations to desktop computers. The varied class of potential applications share features and applications discussed in the paragraphs below.

9.2 Typical Applications

9.2.1 Point-to-Point Communications

The most basic application for LVDS buffers, as found in this data sheet, is for point-to-point communications of digital data, as shown in Figure 11.

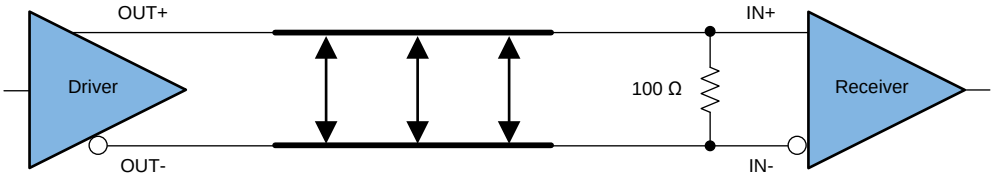


Figure 11. Point-to-Point Topology

A point-to-point communications channel has a single transmitter (driver) and a single receiver. This communications topology is often referred to as simplex. In Figure 11 the driver receives a single-ended input signal and the receiver outputs a single-ended recovered signal. The LVDS driver converts the single-ended input to a differential signal for transmission over a balanced interconnecting media of 100-Ω characteristic impedance. The conversion from a single-ended signal to an LVDS signal retains the digital data payload while translating to a signal whose features are more appropriate for communication over extended distances or in a noisy environment.

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 4.

Table 4. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Driver supply voltage (V_{CCD})	3 to 3.6 V
Driver input voltage	0.8 to V_{CCD} V
Driver signaling rate	DC to 400 Mbps
Interconnect characteristic impedance	100 Ω
Termination resistance	100 Ω
Receiver supply voltage (V_{CCR})	3 to 3.6 V
Number of receiver nodes	1
Receiver input voltage	0 to V_{CCR} – 0.8 V
Ground shift between driver and receiver	±1 V

Copyright © 2003–2015, Texas Instruments Incorporated

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. At low frequencies, power supply offers very low-impedance paths between the terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 µF to 1000 µF) at the board level do a good job into the kHz range. Due to their size and length of their leads, large capacitors tend to have large inductance values at the switching frequencies. To solve this problem, smaller capacitors should be (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance of approximately 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson, equations 8.18 to 8.21. A conservative rise time of 4 ns and a worst-case change in supply current of 100 mA covers the whole range of LVDS devices offered by TI. In this example, the maximum power supply noise tolerated is 100 mV; however, this figure varies depending on the noise budget available in your design. (1)

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \quad (1)$$

$$C_{LVDS} = \left(\frac{100\ \text{mA}}{0.1\ \text{V}} \right) \times 4\ \text{ns} = 0.004\ \mu\text{F} \quad (2)$$

The following example, Figure 12, lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found in Equation 2 (0.004 µF). You should place the smallest value of capacitance as close as possible to the chip.

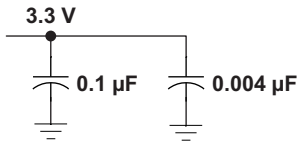


Figure 12. Recommended LVDS Bypass Capacitor Layout

9.2.1.2.2 Driver Supply Voltage

The device can support operation with a supply as low as 3 V and as high as 3.6 V. As shown in *Device Electrical Characteristics*, the differential output voltage is nominally 350 mV over the complete output range. The minimum output voltage stays within the specified LVDS limits (247 mV to 454 mV) for a 3.3-V supply.

9.2.1.2.3 Driver Input Voltage

The driver will operate with a decision threshold of approximately 1.4 V for LVTTL input signals.

9.2.1.2.4 Driver Output Voltage

The SN65LVDS049 driver output is a 1.2-V common-mode voltage, with a nominal differential output signal of 350 mV. This 350 mV is the absolute value of the differential swing (VOD = $|V^+ - V^-|$). The peak-to-peak differential voltage is twice this value, or 700 mV.

9.2.1.2.5 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the LVDS standard. This media may be a twisted-pair, twinax, flat ribbon cable, or PCB traces.

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

Copyright © 2003–2015, Texas Instruments Incorporated

The nominal characteristic impedance of the interconnect should be from 100 Ω to 120 Ω with variation no more than 10% (90 Ω to 132 Ω).

9.2.1.2.6 PCB Transmission Lines

As per SNLA187, Figure 13 depicts several transmission line structures commonly used in PCBs. Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed near one another, they form a pair of coupled transmission lines. Figure 13 shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, if S is less than 2×W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

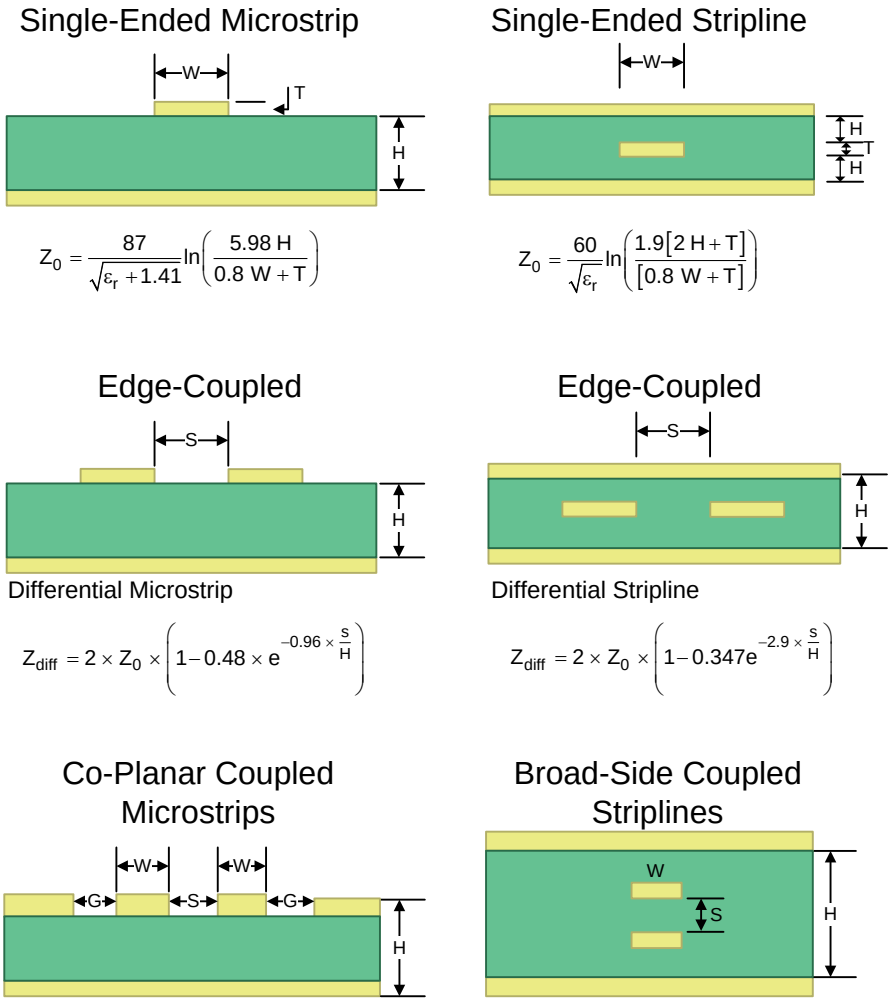


Figure 13. Controlled-Impedance Transmission Lines

Copyright © 2003–2015, Texas Instruments Incorporated

9.2.1.2.7 Termination Resistor

As shown earlier in Figure 11, an LVDS communication channel employs a current source driving a transmission line which is terminated with a resistive load. This load serves to convert the transmitted current into a voltage at the receiver input. To ensure good signal integrity, the termination resistance should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistance is within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistance should be from 90 Ω to 110 Ω.

The line termination resistance should be located as close as possible to the receiver, thereby minimizing the stub length from the resistor to the receiver.

When a multidrop topology is used, line termination resistors are typically placed at the end (or ends) of the transmission line.

9.2.1.2.8 Receiver Supply Voltage

The receiver can support operation with a supply as low as 3 V and as high as 3.6 V.

9.2.1.2.9 Receiver Input Common-Mode Range

Receiver supports common-mode values in the range of 0.05 V to 2.35 V. This is assuming 100 mV differential signal and a 3.3 V supply.

The driver has an output common-mode range of 1.2 V. Using the receiver discussed here, we see that valid operation of the communication link will occur when the ground difference between transmitter and receiver is within approximately ±1 V. The use of differential signaling in LVDS allows operation in an environment where the combination of ground difference and common-mode noise result in a common-mode difference between transmitter and receiver of 1 V. This 1-V potential difference hints at the intended application of LVDS circuits.

Standards such as RS-485 support potential differences of almost 10 V, allowing for communication over distances of greater than 1 km. The intended application of LVDS devices is more moderate distances, such as those from chip to chip on a board, board to board in a rack, or from rack to nearby rack. When the 1 V potential difference is not adequate, yet the high-speed and low-voltage features of LVDS are still needed, the designer can choose from either M-LVDS devices available from TI, or from LVDS devices with extended common-mode ranges, such as the SN65LVDS33.

9.2.1.2.10 Receiver Input Signal

The LVDS receivers herein comply with the LVDS standard and correctly determine the bus state when the differential input voltage is greater than 100 mV (HI output) or less than –100 mV (LO output).

9.2.1.2.11 Receiver Output Signal

Receiver outputs comply with LVTTL output voltage standards when the supply voltage is within the range of 3 V to 3.6 V.

Copyright © 2003–2015, Texas Instruments Incorporated

9.2.1.3 Application Curve

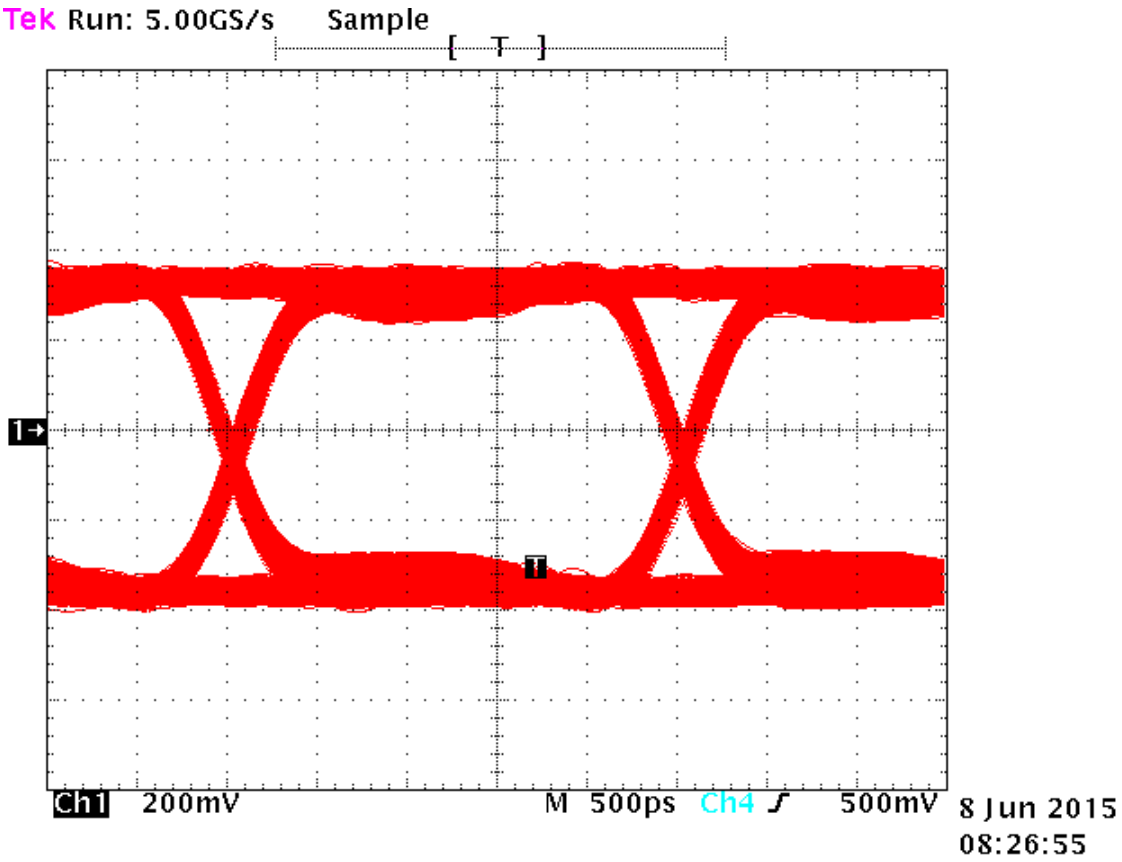


Figure 14. Typical Driver Output Eye Pattern in Point-to-Point System

9.2.2 Multidrop Communications

A second common application of LVDS buffers is a multidrop topology. In a multidrop configuration, a single driver and a shared bus are present, along with two or more receivers (with a maximum permissible number of 32 receivers). Figure 15 below shows an example of a multidrop system.

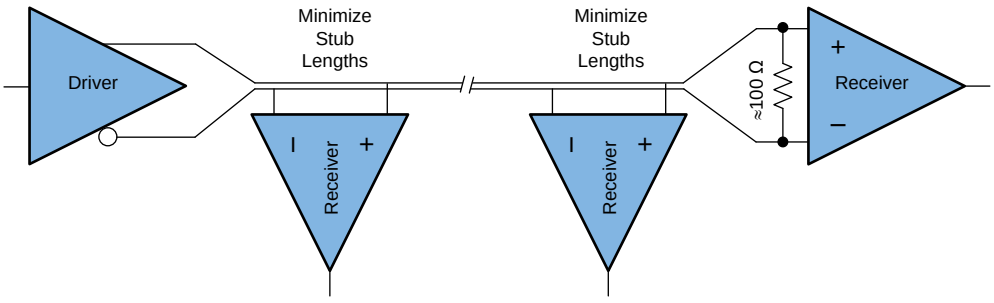


Figure 15. Multidrop Topology

Copyright © 2003–2015, Texas Instruments Incorporated

9.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 5.

Table 5. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3 to 3.6 V
Driver Input Voltage	0.8 to V_{CCD} V
Driver Signaling Rate	DC to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	2 to 32
Receiver Supply Voltage (V_{CCR})	3 to 3.6 V
Receiver Input Voltage	0 to V_{CCR} – 0.8 V
Receiver Signaling Rate	DC to 400 Mbps
Ground shift between driver and receiver	±1 V

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Interconnecting Media

The interconnect in a multidrop system differs considerably from a point-to-point system. While point-to-point interconnects are straightforward, and well understood, the bus type architecture encountered with multidrop systems requires more careful attention. We will use Figure 15 to explore these details.

The most basic multidrop system would include a single driver, located at a bus origin, with multiple receiver nodes branching off the main line, and a final receiver at the end of the transmission line, co-located with a bus termination resistor. While this would be the most basic multidrop system, it has several considerations not yet explored.

The location of the transmitter at one bus end allows the design concerns to be simplified, but this comes at the cost of flexibility. With a transmitter located at the origin, a single bus termination at the far-end is required. The far-end termination absorbs the incident traveling wave. The flexibility lost with this arrangement is thus: if the single transmitter needed to be relocated on the bus, at any location other than the origin, we would be faced with a bus with one open-circuited end, and one properly terminated end. Locating the transmitter say in the middle of the bus may be desired to reduce (by ½) the maximum flight time from the transmitter to receiver.

Another new feature in Figure 15 is clear in that every node branching off the main line results in stubs. The stubs should be minimized in any case, but have the unintended effect of locally changing the loaded impedance of the bus.

To a good approximation, the characteristic transmission line impedance of an unloaded multipoint or multidrop bus is defined by $\sqrt{L/C}$, where L is the inductance per unit length and C is the capacitance per unit length. As capacitance is added to the bus in the form of devices and interconnections, the bus characteristic impedance is lowered. This may result in signal reflections from the impedance mismatch between the unloaded and loaded segments of the bus.

If the number of loads is constant and can be distributed evenly along the line, reflections can be reduced by changing the bus termination resistors to match the loaded characteristic impedance. Normally, the number of loads are not constant or distributed evenly and the reflections resulting from any mismatching must be accounted for in the noise budget.

10 Power Supply Recommendations

The SN65LVDS049 is designed to operate from a single power supply in the range of 3 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than ±1 V. Board level and local device level bypass capacitance should be used and are covered in *Bypass Capacitance*.

Copyright © 2003–2015, Texas Instruments Incorporated

11 Layout

11.1 Layout Guidelines

11.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, PCBs usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 16.

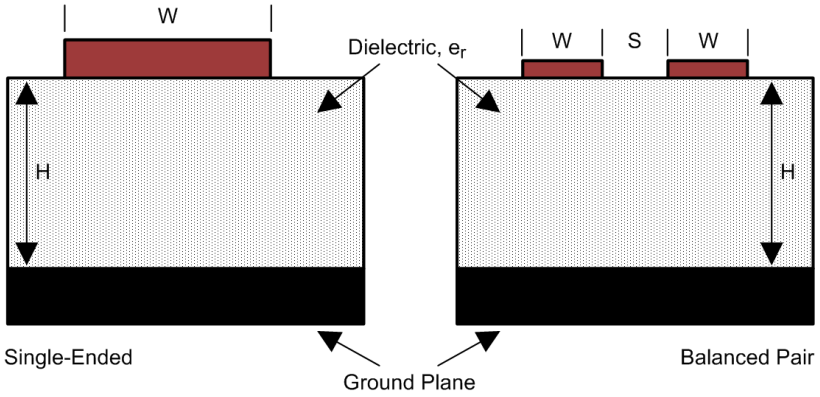


Figure 16. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1, 2, and 3 provide formulas for Z_O and t_{PD} for differential and single-ended traces. (1) (2) (3)

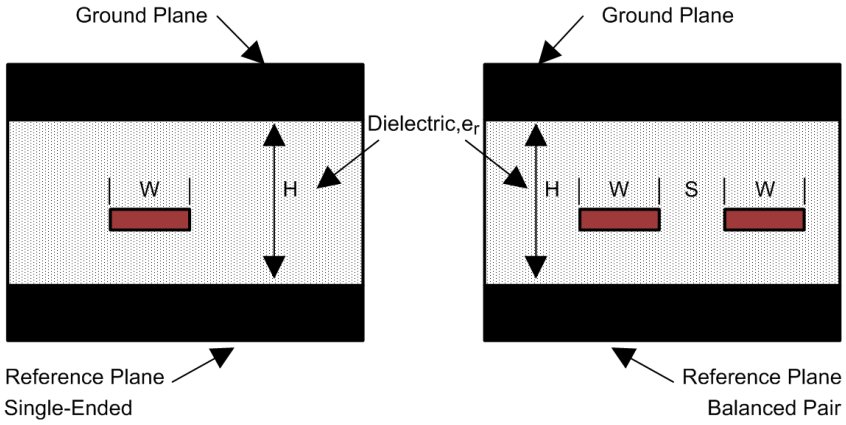


Figure 17. Stripline Topology

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(2) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(3) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

Copyright © 2003–2015, Texas Instruments Incorporated

Layout Guidelines (continued)

11.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

11.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 18.

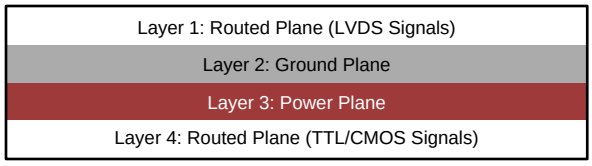


Figure 18. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 µm (0.005 inch). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the 6-layer board, as shown in Figure 19.

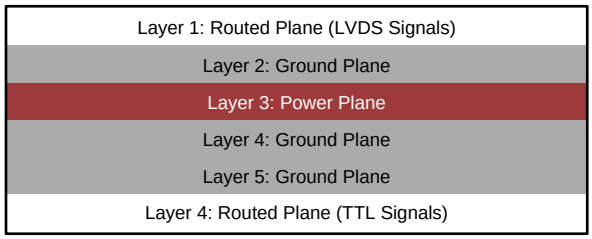


Figure 19. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

11.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

Copyright © 2003–2015, Texas Instruments Incorporated

Layout Guidelines (continued)

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

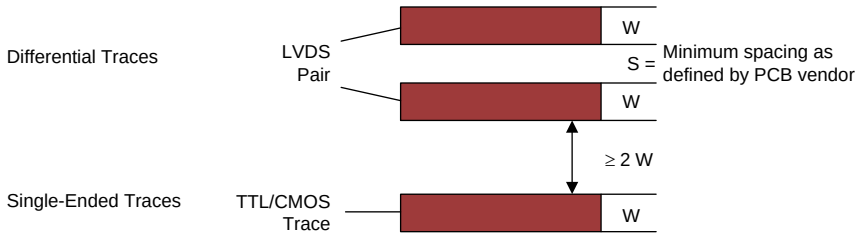


Figure 20. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

11.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

11.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low-inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

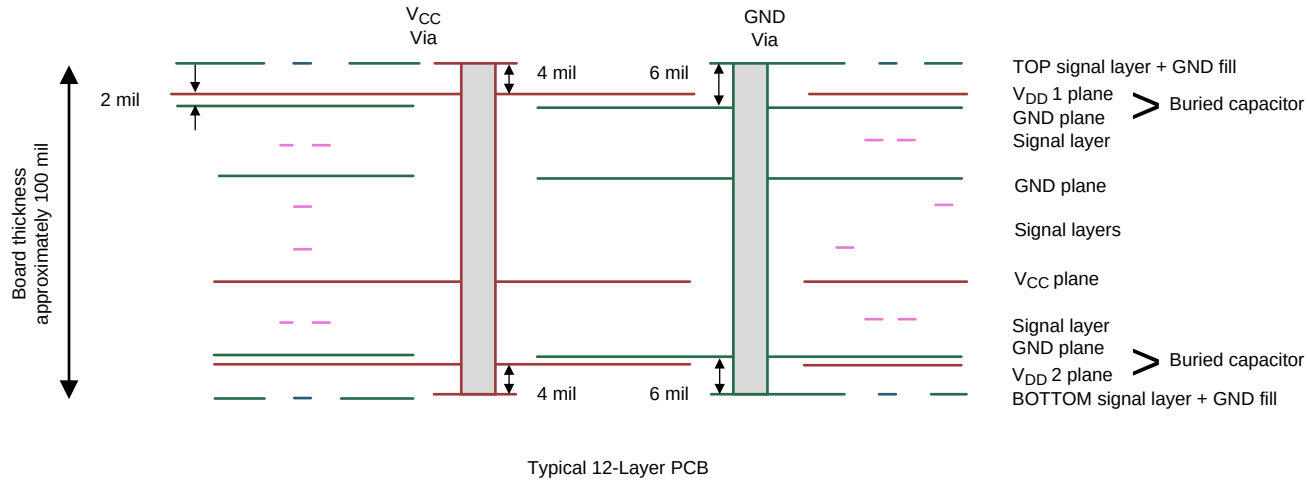


Figure 21. Low Inductance, High-Capacitance Power Connection

Copyright © 2003–2015, Texas Instruments Incorporated

Layout Guidelines (continued)

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402, 0201 or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 22(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 µF, and 0.1 µF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center pad must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the pad connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in Figure 13) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND pad that is so important for heat dissipation makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-pad spacing as shown in Figure 22(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.

Figure 22. Typical Decoupling Capacitor Layouts

11.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 23.

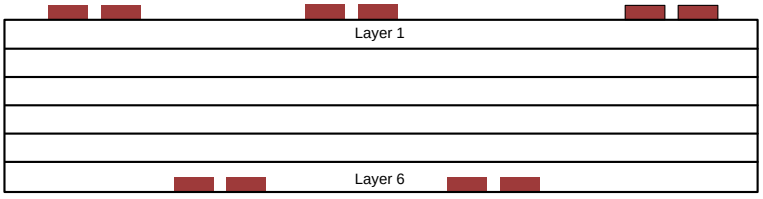


Figure 23. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 24. Vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

Copyright © 2003–2015, Texas Instruments Incorporated

Layout Example (continued)

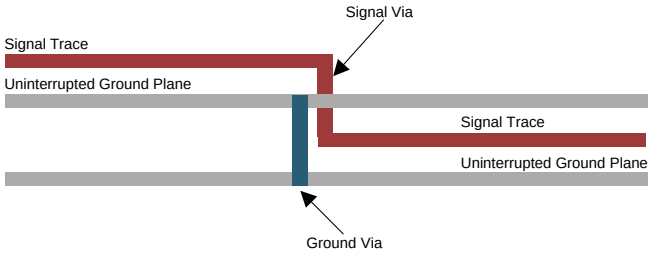


Figure 24. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

Copyright © 2003–2015, Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For the IBIS model, see the SN65LVDS049 product folder, www.ti.com/product/SN65LVDS049.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *Control-Impedance Transmission Lines* (SNLA187)
- *Microstrip vs Stripline Topologies* (SLLD009)

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
Rogers is a trademark of Rogers Corporation.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2003–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS049PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS049	Samples
SN65LVDS049PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS049	Samples
SN65LVDS049PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS049	Samples
SN65LVDS049PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS049	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

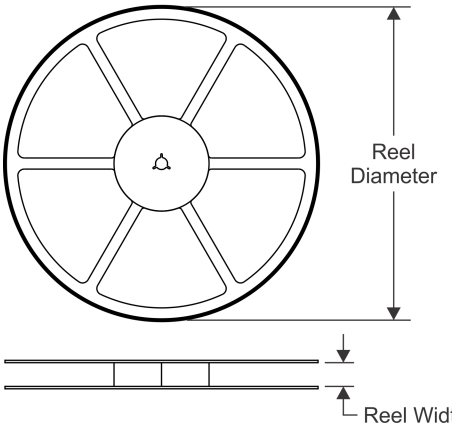
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

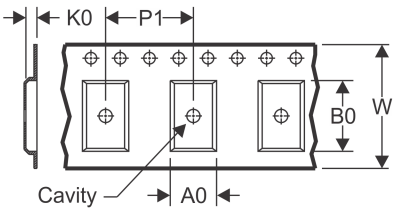
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

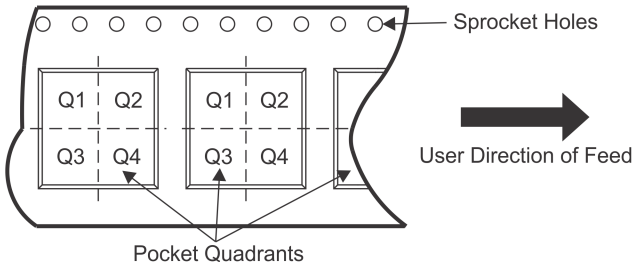


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

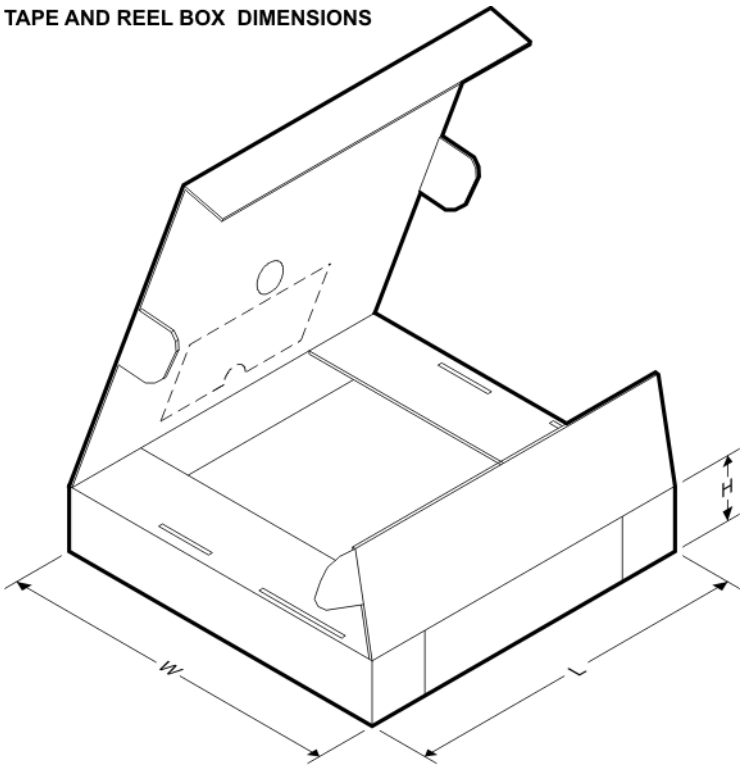
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS049PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

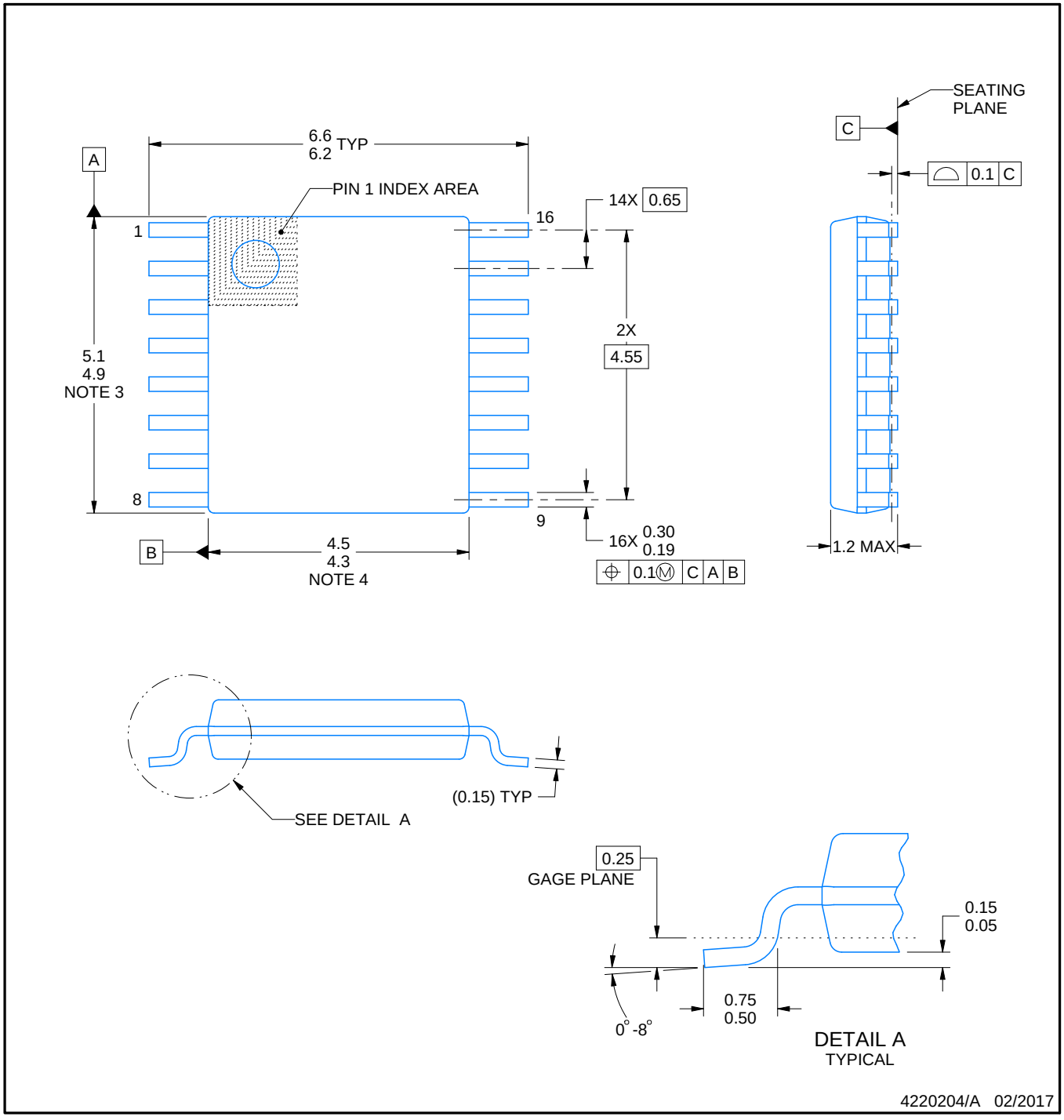
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS049PWR	TSSOP	PW	16	2000	350.0	350.0	43.0

PACKAGE OUTLINE

PW0016A

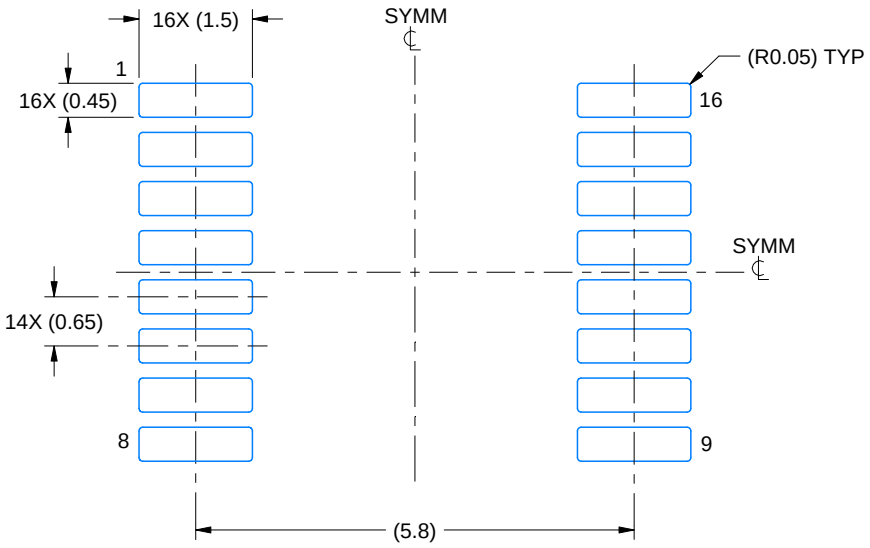
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



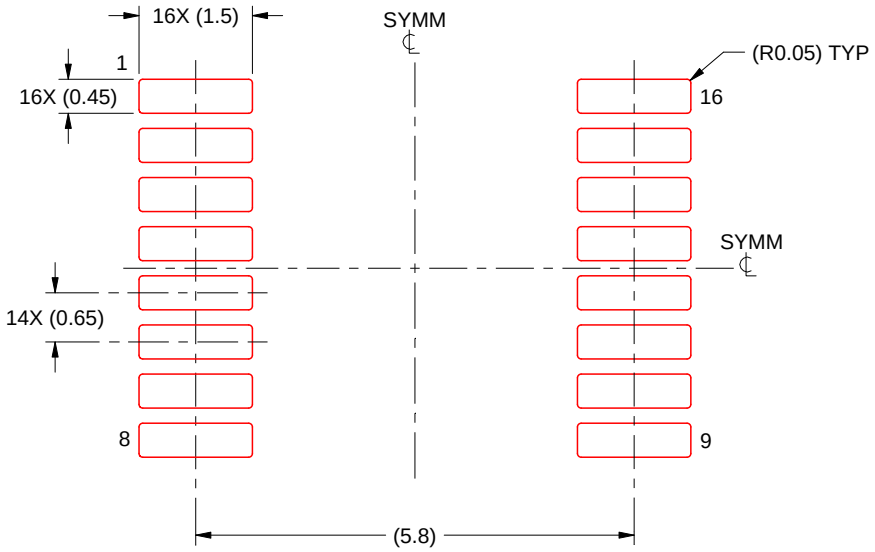
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View SN65LVDS049PWR on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management