THE DATASHEET OF

SN65MLVD047APWR

SN65MLVD047A Multipoint-LVDS Quad Differential Line Driver

1 Features

- Differential line drivers for 30Ω to 55Ω loads and data rates[1] up to 200Mbps, clock frequencies up to 100MHz
- Supports multipoint bus architectures
- Operates from a single 3.3V supply
- Characterized for operation from –40°C to 85°C
- 16-pin SOIC (JEDEC MS-012) and 16-pin TSSOP (JEDEC MS-153) packaging

2 Applications

- AdvancedTCA™ (ATCA™) Clock Bus Driver
- Clock distribution
- Backplane or cabled multipoint data transmission in telecommunications, automotive, industrial, and other computer systems
- Cellular base stations
- Central-office and PBX switching
- Bridges and routers
- Low-power high-speed short-reach alternative to TIA/EIA-485

3 Description

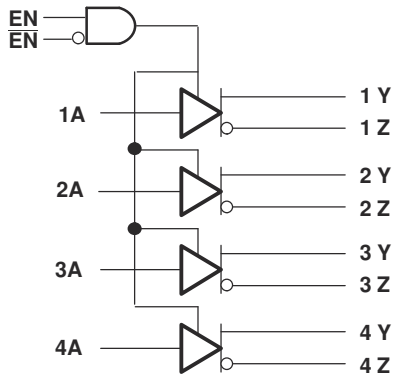
The SN65MLVD047A is a quadruple line driver that complies with the TIA/EIA-899 standard, Electrical Characteristics of Multipoint-Low-Voltage Differential Signaling (M−LVDS). The output current of this M−LVDS device has been increased, in comparison to standard LVDS compliant devices, in order to support doubly terminated transmission lines and heavily loaded backplane bus applications. Backplane applications generally require impedance matching termination resistors at both ends of the bus. The effective impedance of a doubly terminated bus can be as low as 30Ω due to the bus terminations, as well as the capacitive load of bus interface devices. SN65MLVD047A drivers allow for operation with loads as low as 30Ω. The SN65MLVD047A devices allow for multiple drivers to be present on a single bus. SN65MLVD047A drivers are high impedance when disabled or unpowered. Driver edge rate control is incorporated to support operation. The M−LVDS standard allows up to 32 nodes (drivers and/or receivers) to be connected to the same media in a backplane when multiple bus stubs are expected from the main transmission line to interface devices. The SN65MLVD047A provides 9kV ESD protection on all bus pins.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN65MLVD047A	PW (TSSOP, 16)	5mm × 6.4mm
	D (SOIC, 16)	9.9mm × 6mm

(1) For more information, Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

LOGIC DIAGRAM (POSITIVE LOGIC)



[1] The data rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

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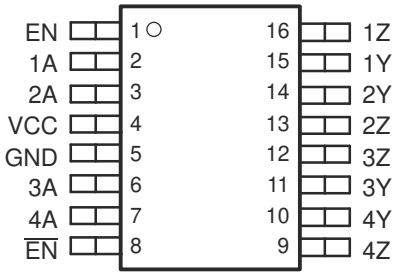
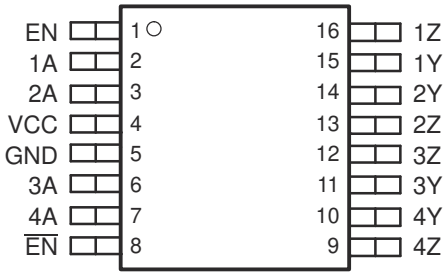
4 Pin Configuration

D PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

			MIN	MAX	UNITS
V_{CC}	Supply voltage range(2)		–0.5	4	V
V_I	Input voltage range	A, EN, $\overline{EN}$	–0.5	4	V
V_O	Output voltage range	Y, Z	–1.8	4	V
T_J	Junction temperature			140	°C
P_D	Device power dissipation	EN = V_{CC}, $\overline{EN}$ = GND, R_L = 50Ω, Input 100MHz 50 % duty cycle square wave to 1A:4A, T_A = 85°C		288.5	mW
T_{stg}	Storage Temperature		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to the circuit ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Y and Z	±9000	V
			All pins	±4000	
		Charged device model (CDM), per AEC Q100-011(2)	All pins	±1500	
		Machine Model	All pins	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

see Figure 6-1

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
	Voltage at any bus terminal (separate or common mode) V_Y or V_Z	–1.4		3.8	V
R_L	Differential load resistance	30		55	Ω
$1/t_{UI}$	Signaling rate			200	Mbps
	Clock frequency			100	MHz
T_J	Junction temperature	–40		125	°C

5.4 Package Dissipation Ratings

PACKAGE	PCB JEDEC STANDARD	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C(1)	T_A = 85°C POWER RATING
D(16)	Low-K(2)	898mW	7.81mW/°C	429mW
PW(16)	Low-K(2)	592mW	5.15mW/°C	283mw
	High-K(3)	945mW	8.22mW/°C	452mw

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

5.5 Thermal Information

PARAMETER		TEST CONDITIONS		VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	Low-K board(1), no airflow	D	128	°C/W
		Low-K board(1), no airflow	PW	194.2	
		Low-K board(1), 150 LFM		146.8	
		Low-K board(1), 250 LFM		133.1	
		High-K board(2), no airflow		121.6	
θ_{JB}	Junction-to-board thermal resistance	High-K board(2)	D	51.1	°C/W
			PW	85.3	
θ_{JC}	Junction-to-case thermal resistance		D	45.4	°C/W
			PW	34.7	

(1) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(2) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

5.6 Device Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	Driver enabled	EN = V_{CC}, $\overline{EN}$ = GND, R_L = 50Ω, All inputs = V_{CC} or GND		59	70	mA
		Driver disabled	EN = GND, $\overline{EN}$ = V_{CC}, R_L = No load, All inputs = V_{CC} or GND		2	4	

(1) All typical values are at 25°C and with a 3.3V supply voltage.

5.7 Device Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
LVTTL (EN, $\overline{EN}$, 1A:4A)						
$\lvert I_{IH}\rvert$	High-level input current	V_{IH} = 2 V or V_{CC}	0		10	µA
$\lvert I_{IL}\rvert$	Low-level input current	V_{IL} = GND or 0.8 V	0		10	µA
C_i	Input capacitance	V_I = 0.4 sin(30E6πt) + 0.5 V(3)		5		pF
M-LVDS (1Y/1Z:4Y/4Z)						
$\lvert V_{YZ}\rvert$	Differential output voltage magnitude	See Figure 6-2	480		650	mV
$\Delta\lvert V_{YZ}\rvert$	Change in differential output voltage magnitude between logic states		–50		50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	See Figure 6-3	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage				150	mV
$V_{Y(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 6-7	0		2.4	V
$V_{Z(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	See Figure 6-5			1.2 V_{SS}	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output		–0.2 V_{SS}			V
$\lvert I_{OS}\rvert$	Differential short-circuit output current magnitude	See Figure 6-4			24	mA
I_{OZ}	High-impedance state output current	–1.4 V ≤ (V_Y or V_Z) ≤ 3.8 V, Other output = 1.2 V	–15		10	µA
$I_{O(OFF)}$	Power-off output current	–1.4 V ≤ (V_Y or V_Z) ≤ 3.8 V, Other output = 1.2 V, V_{CC} = 0 V	–10		10	µA
C_Y or C_Z	Output capacitance	V_Y or V_Z = 0.4 sin(30E6πt) + 0.5 V,(3) Other input at 1.2 V, driver disabled		3		pF
C_{YZ}	Differential output capacitance	V_{YZ} = 0.4 sin(30E6πt) V,(3) Driver disabled			2.5	pF
$C_{Y/Z}$	Output capacitance balance, (C_Y/C_Z)		0.99	1.01		

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) All typical values are at 25°C and with a 3.3-V supply voltage.
(3) HP4194A impedance analyzer (or equivalent)

5.8 Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 6-5	1	1.5	2.4	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	1.5	2.4	ns
t_r	Differential output signal rise time		1		1.9	ns
t_f	Differential output signal fall time		1		1.9	ns
$t_{sk(o)}$	Output skew(2)				100	ps
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)			22	100	ps
$t_{sk(pp)}$	Part-to-part skew(3)				600	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(4)	All inputs 100 MHz clock input		0.2	1	ps
$t_{jit(c-c)}$	Cycle-to-cycle jitter(4)	All inputs 100 MHz clock input		5	36	ps
$t_{jit(pp)}$	Peak-to-peak jitter(4) (5)	All inputs 200 Mbps 2^{15}-1 PRBS input		46	158	ps
t_{PZH}	Enable time, high-impedance-to-high-level output	See Figure 6-6			9	ns
t_{PZL}	Enable time, high-impedance-to-low-level output				9	ns
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 6-6			10	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output				10	ns

(1) All typical values are at 25°C and with a 3.3V supply voltage.
(2) $t_{sk(o)}$, output skew is the magnitude of the time difference in propagation delay times between any specified terminals of a device.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Stimulus jitter has been subtracted from the measurements.
(5) Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).

5.9 Typical Characteristics

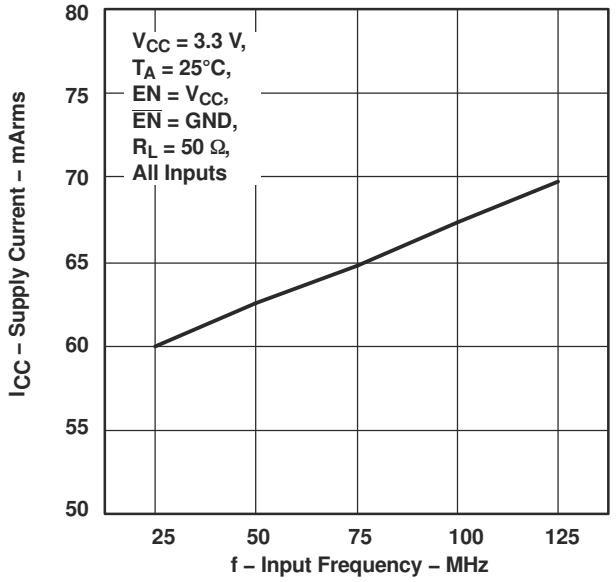


Figure 5-1. RMS Supply Current vs Input Frequency

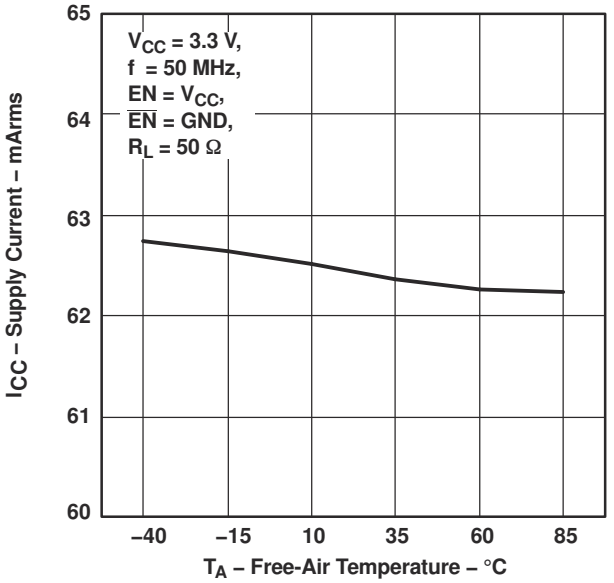


Figure 5-2. RMS Supply Current vs Free-Air Temperature

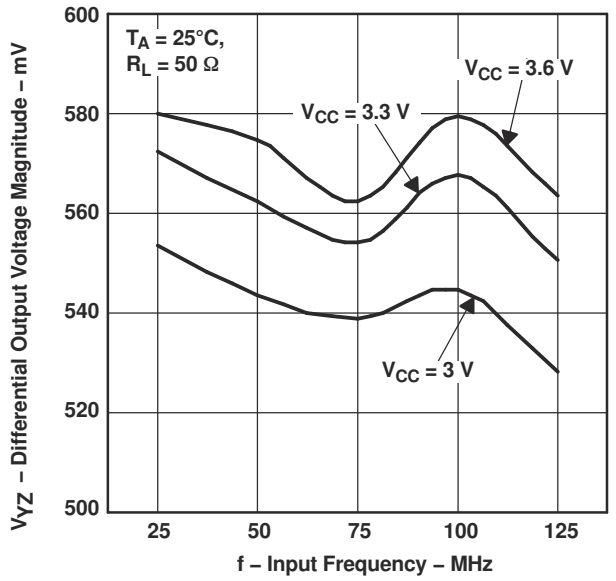


Figure 5-3. Differential Output Voltage Magnitude vs Input Frequency

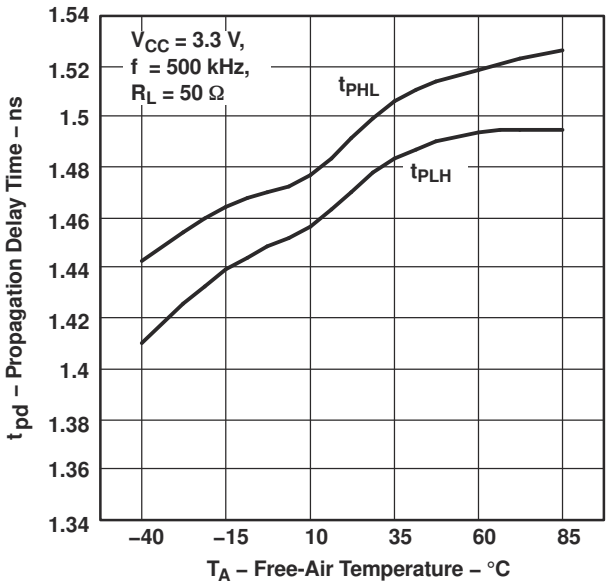


Figure 5-4. Driver Propagation Delay Time vs Free-Air Temperature

5.9 Typical Characteristics (continued)

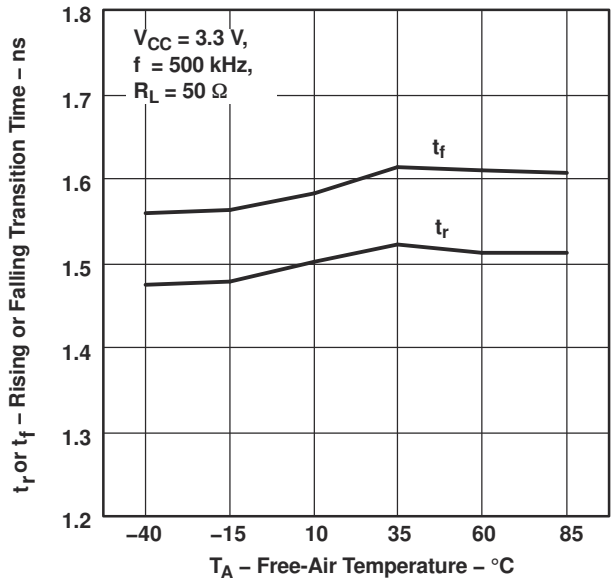


Figure 5-5. Driver Transition Time vs Free-Air Temperature

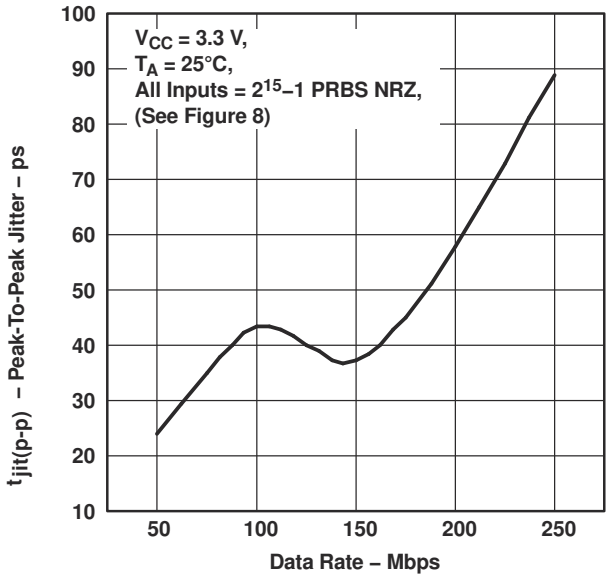


Figure 5-6. Peak-to-Peak Jitter vs Data Rate

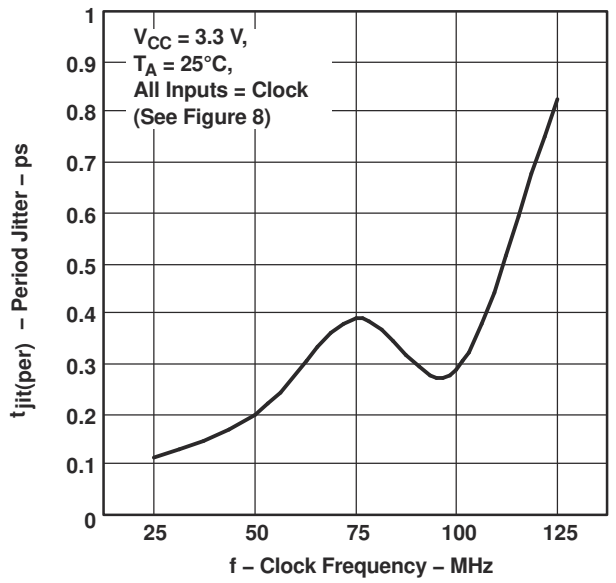


Figure 5-7. Period Jitter vs Clock Frequency

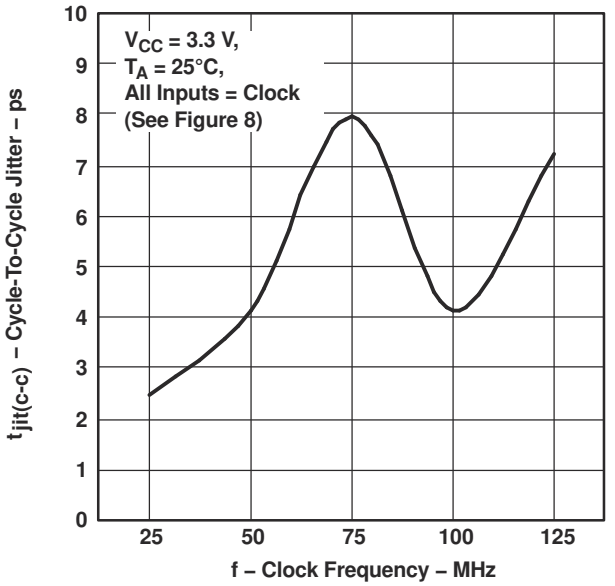


Figure 5-8. Cycle-to-Cycle Jitter vs Clock Frequency

6 Parameter Measurement Information

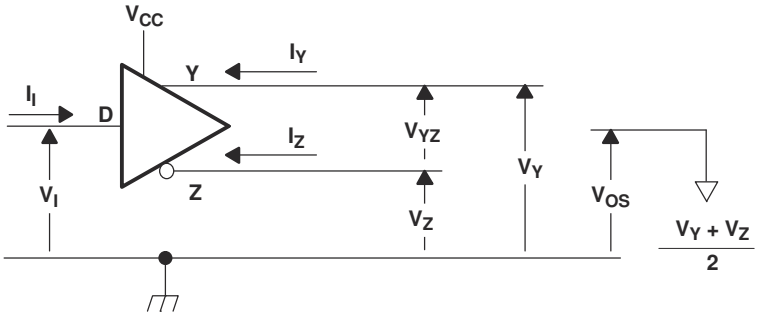
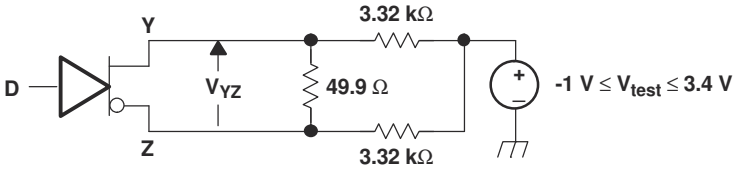
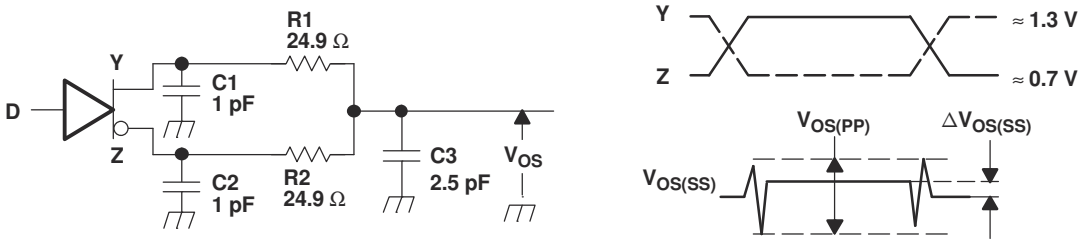


Figure 6-1. Driver Voltage and Current Definitions



All resistors are 1% tolerance.

Figure 6-2. Differential Output Voltage Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1ns, pulse frequency = 500kHz, duty cycle = 50 ± 5%.
B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 and R2 are metal film, surface mount, ±1%, and located within 2 cm of the D.U.T.
D. The measurement of $V_{OS(PP)}$ is made on test equipment with a –3dB bandwidth of at least 1 GHz.

Figure 6-3. Test Circuit and Definitions for the Common-Mode Output Voltage

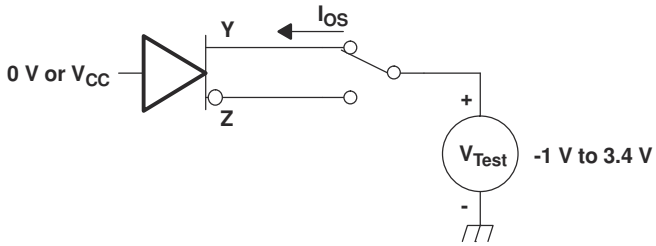
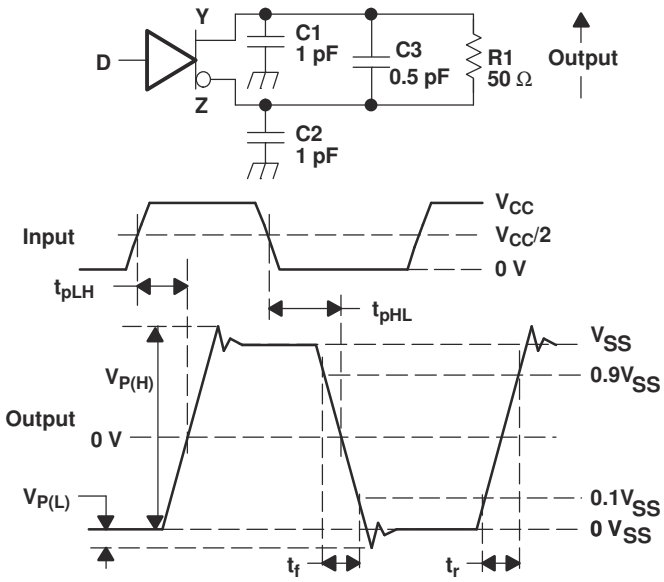
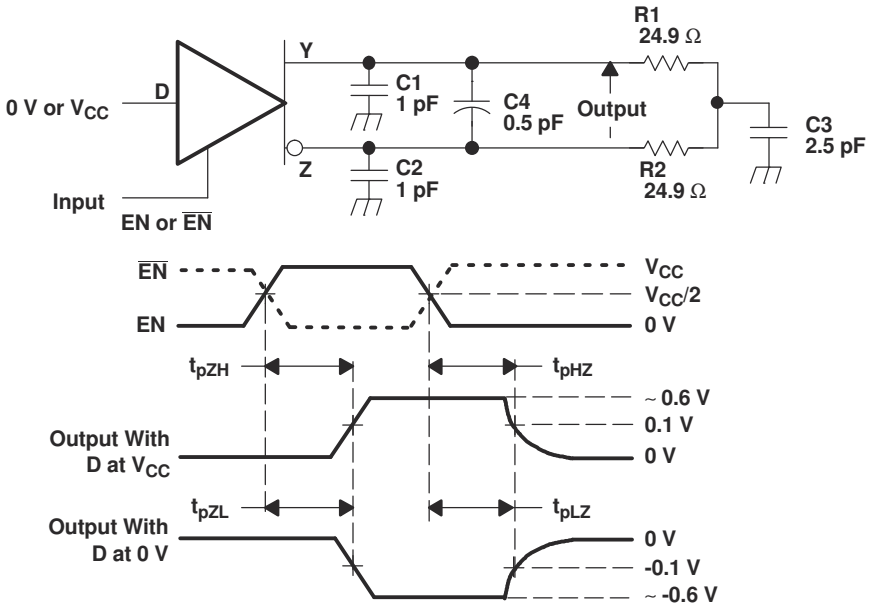


Figure 6-4. Short-Circuit Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1ns, frequency = 500kHz, duty cycle = 50 ± 5%.
B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
D. The measurement is made on test equipment with a –3dB bandwidth of at least 1 GHz.

Figure 6-5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1ns, frequency = 500kHz, duty cycle = 50 ± 5%.
B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
D. The measurement is made on test equipment with a –3dB bandwidth of at least 1GHz.

Figure 6-6. Driver Enable and Disable Time Circuit and Definitions

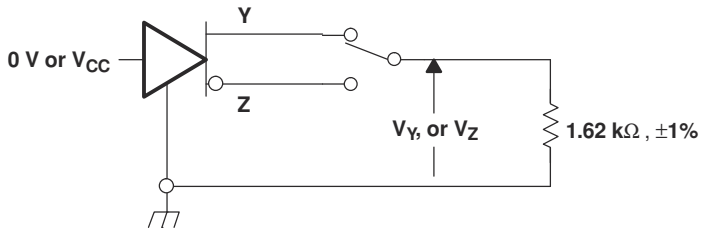
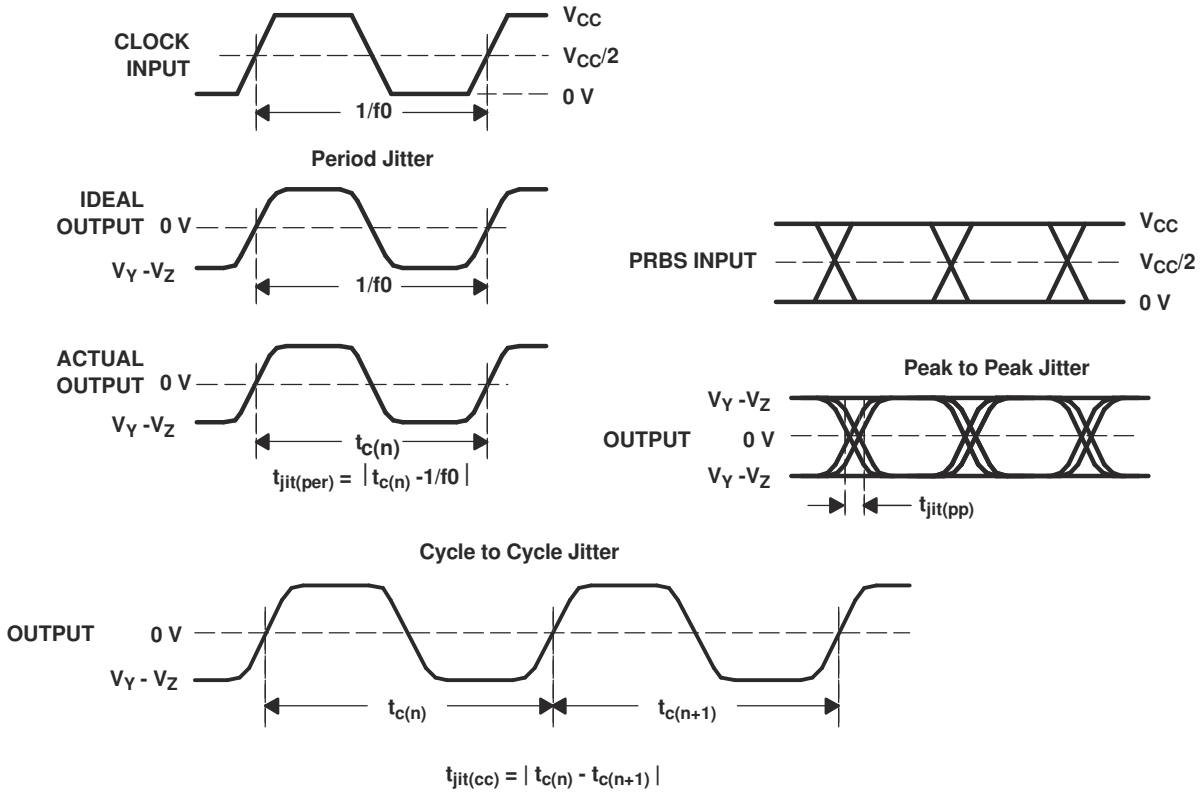


Figure 6-7. Driver Maximum Steady State Output Voltage



A. All input pulses are supplied by an Agilent 8304A Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter and cycle-to-cycle jitter are measured using a 100MHz 50 ±1% duty cycle clock input.
D. Peak-to-peak jitter is measured using a 200Mbps 2^{15} – 1PRBS input.

Figure 6-8. Driver Jitter Measurement Waveforms

7 Device Functional Modes

Table 7-1. Device Function Table

INPUTS(1)			OUTPUTS(1)	
D	EN	$\overline{EN}$	Y	Z
L	H	L	L	H
H	H	L	H	L
OPEN	H	L	L	H
X	L or OPEN	X	Z	Z
X	X	H or OPEN	Z	Z

(1) H = high level, L = low level, Z = high impedance, X = Don't Care

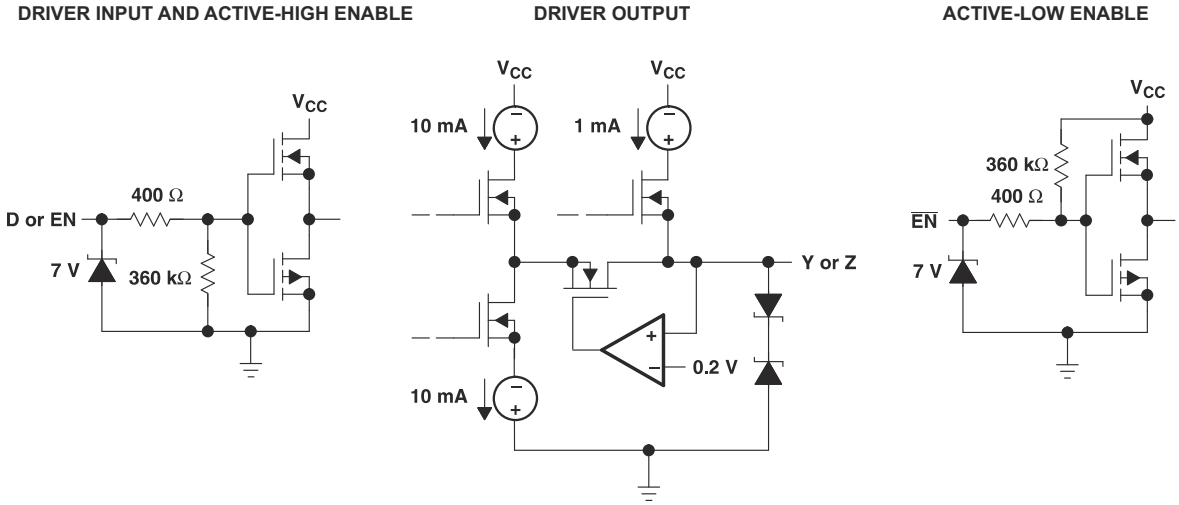


Figure 7-1. Equivalent Input and Output Schematic Diagrams

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Synchroization Clock in AdvancedTCA

Advanced Telecommunications Computing Architecture, also known as AdvancedTCA, is an open architecture to meet the needs of the rapidly changing communications network infrastructure. M−LVDS bused clocking is recommended by the ATCA.

The ATCA specification includes requirements for three redundant clock signals. An 8KHz and a 19.44MHz clock signal as well as an user-defined clock signal are included in the specification. The SN65MLVD047A quad driver supports distribution of these three ATCA clock signals, supporting operation beyond 100MHz, which is the highest clock frequency included in the ATCA specification. A pair of SN65MLVD047A devices can be used to support the ATCA redundancy requirements.

8.1.2 Multipoint Configuration

The SN65MLVD047A is designed to meet or exceed the requirement of the TIA/EIA−899 (M−LVDS) standard, which allows multipoint communication on a shared bus.

Multipoint is a bus configuration with multiple drivers and receivers present. An example is shown in Figure 8-1. The figure shows transceivers interfacing to the bus, but a combination of drivers, receivers, and transceivers is also possible. Termination resistors need to be placed on each end of the bus, with the termination resistor value matched to the loaded bus impedance.

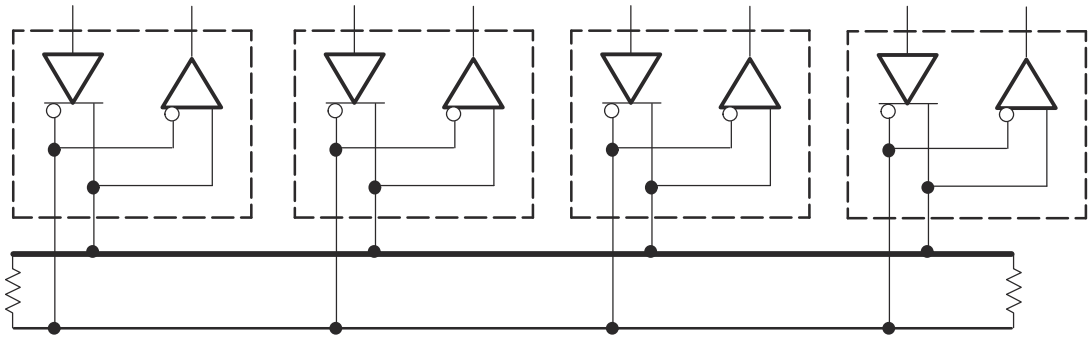


Figure 8-1. Multipoint Architecture

8.1.3 Multidrop Configuration

Multidrop configuration is similar to multipoint configuration, but only one driver is present on the bus. A multidrop system can be configured with the driver at one end of the bus, or in the middle of the bus. When a driver is located at one end, a single termination resistor is located at the far end, close to the last receiver on the bus. Alternatively, the driver can be located in the middle of the bus, to reduce the maximum flight time. With a centrally located driver, termination resistors are located at each end of the bus. In both cases, the termination resistor value should be matched to the loaded bus impedance. Figure 8-2 shows examples of both cases.

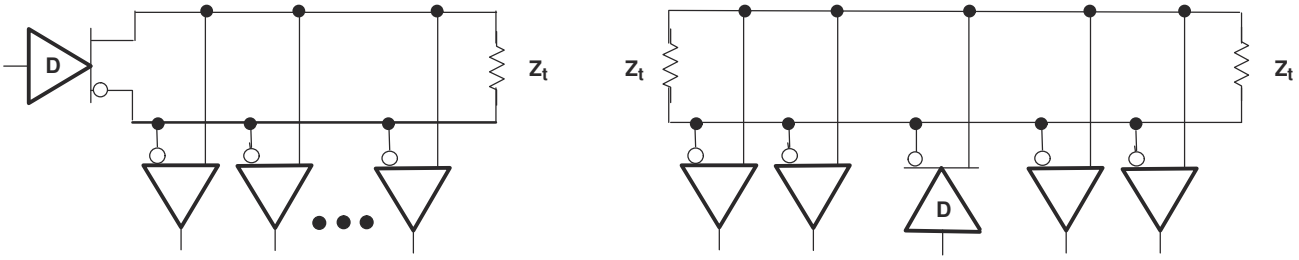


Figure 8-2. Multidrop Architectures With Different Driver Locations

8.1.4 Unused Channel

A 360kΩ pull-down resistor is built in every LVTTL input. The unused driver inputs should be left floating or connected to ground. The low-level output of an unused enabled driver can oscillate if left floating, and should be connected to ground. If the input is floating or connected to ground, the unused Y (non-inverting) output of an enabled driver should be connected to ground. The unused Z (inverting) should be left floating

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2005) to Revision B (February 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65MLVD047AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD047A	Samples
SN65MLVD047ADG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD047A	Samples
SN65MLVD047ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD047A	Samples
SN65MLVD047APW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BUL	Samples
SN65MLVD047APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BUL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

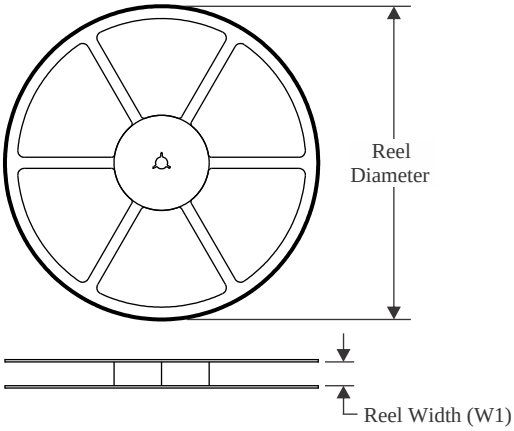
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

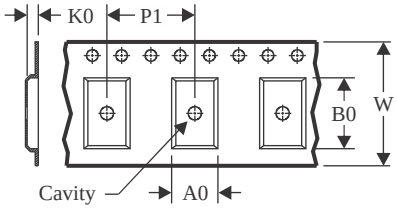
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

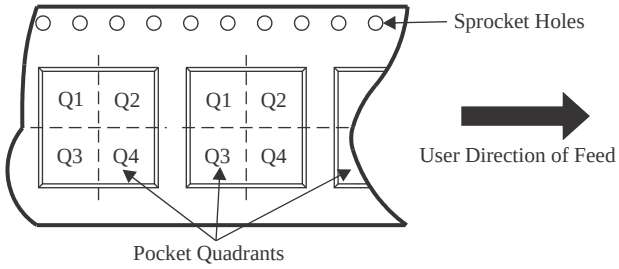


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

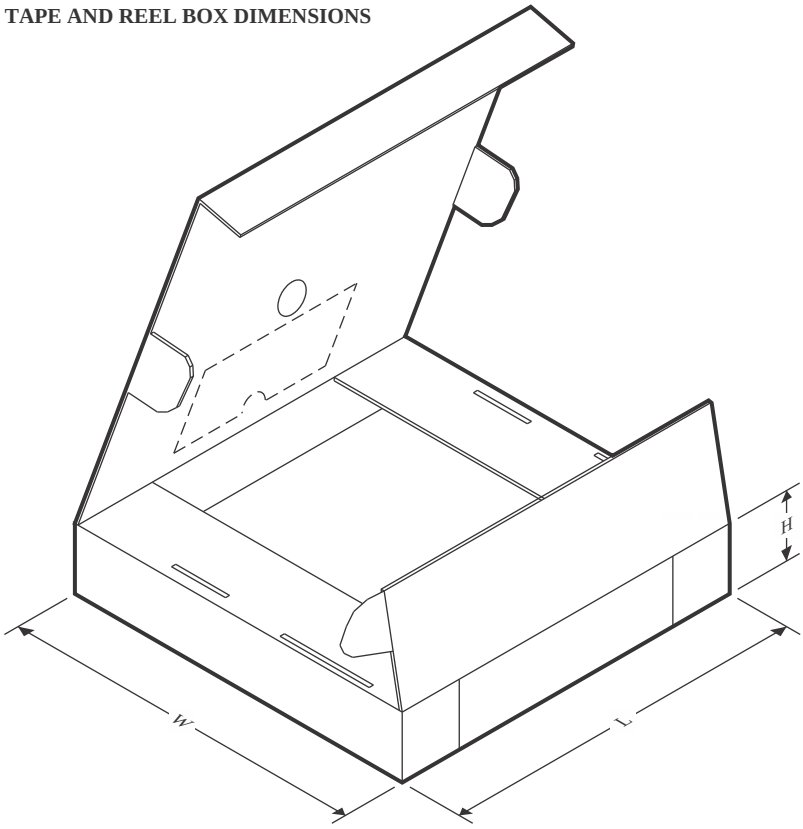
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD047ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65MLVD047APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

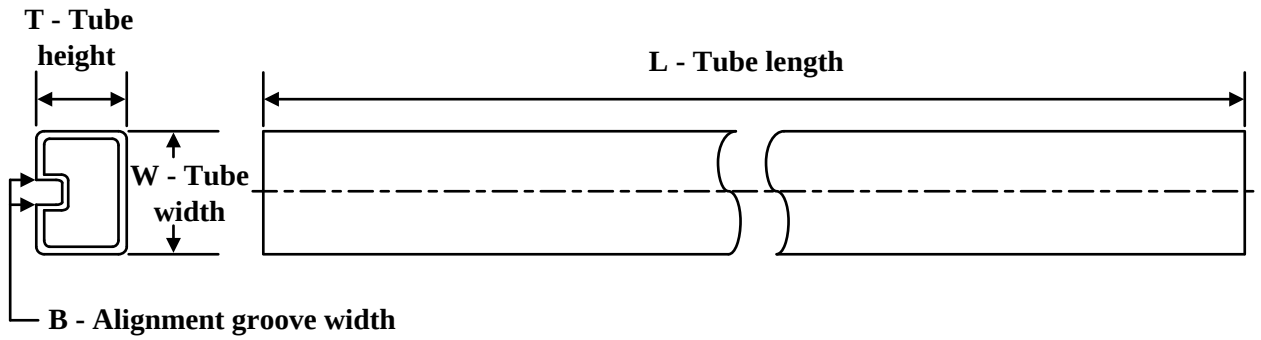
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD047ADR	SOIC	D	16	2500	350.0	350.0	43.0
SN65MLVD047APWR	TSSOP	PW	16	2000	350.0	350.0	43.0

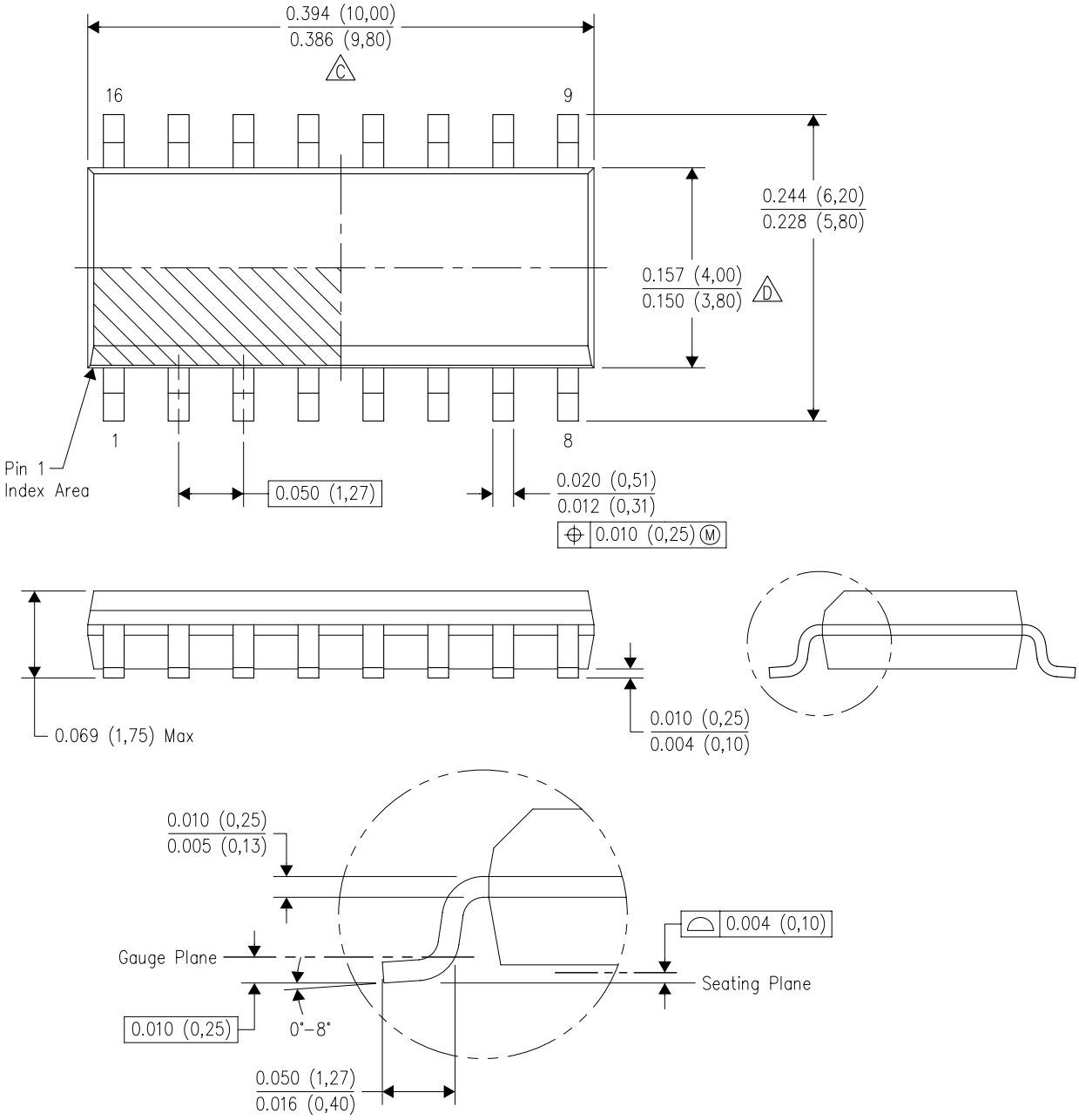
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65MLVD047AD	D	SOIC	16	40	505.46	6.76	3810	4
SN65MLVD047ADG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65MLVD047APW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



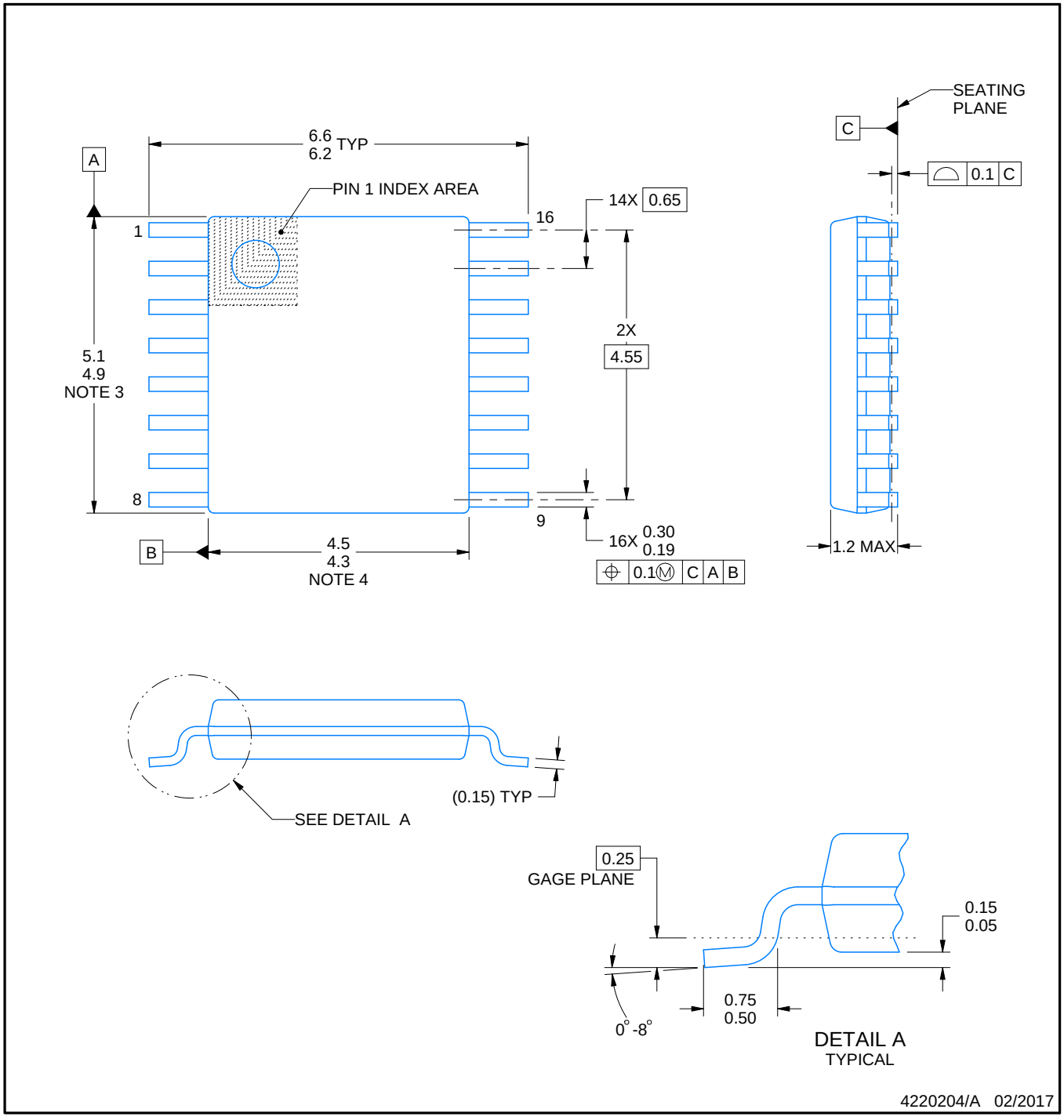
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

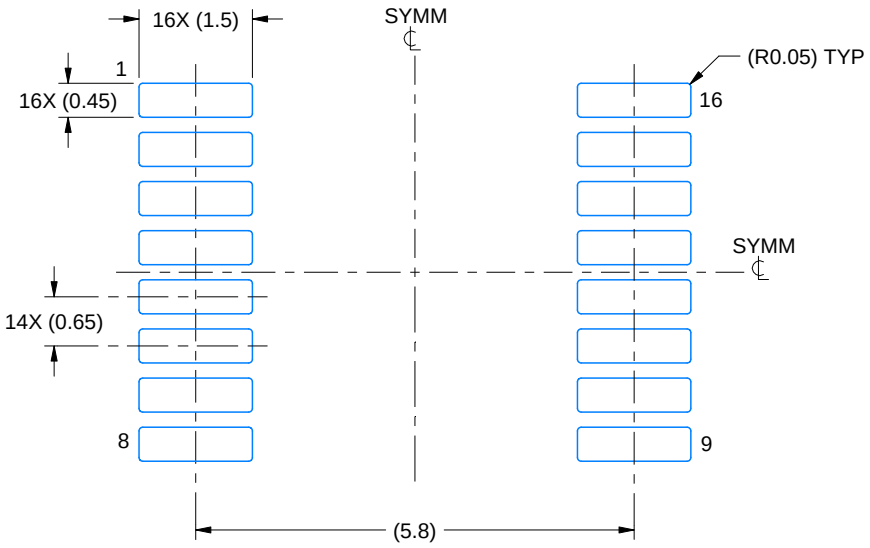
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

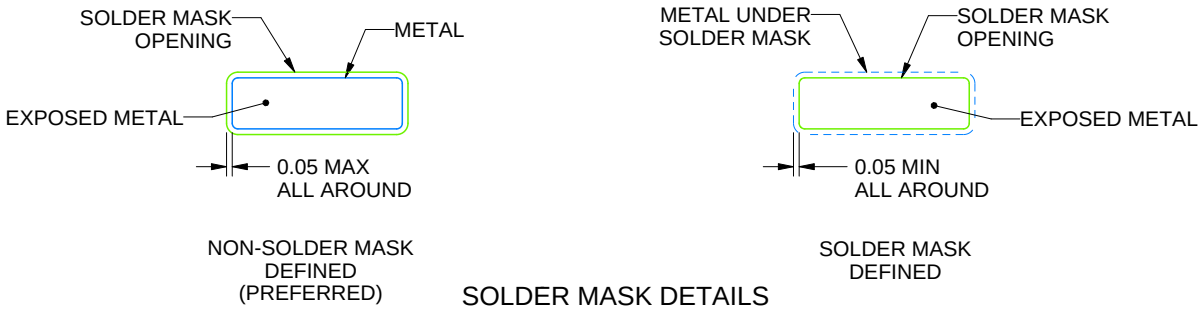


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

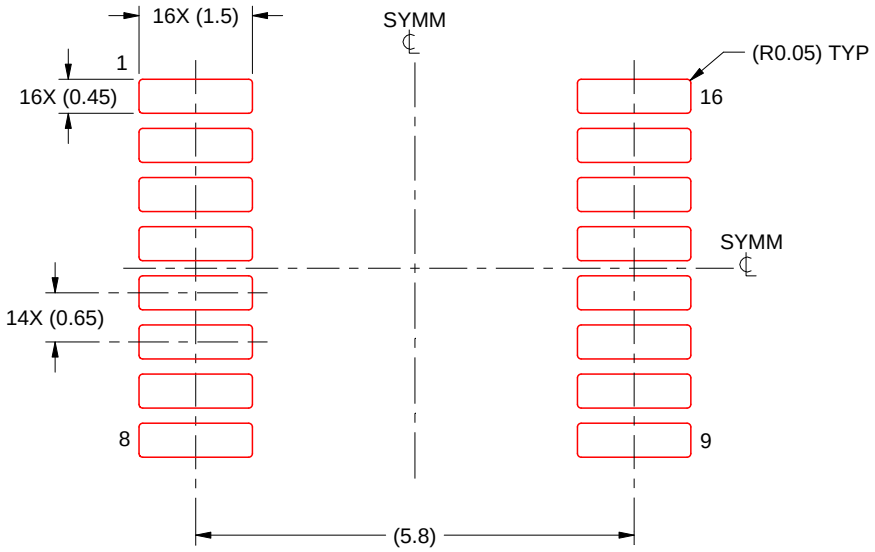


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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