



**THE DATASHEET OF  
SN74CBT3306DR**



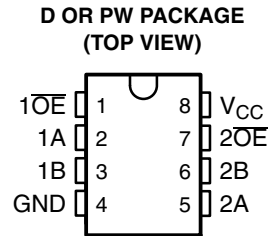
# SN74CBT3306 DUAL FET BUS SWITCH

SCDS016H – MAY 1995 – REVISED JANUARY 2004

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

## description/ordering information

The SN74CBT3306 dual FET bus switch features independent line switches. Each switch is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.



## ORDERING INFORMATION

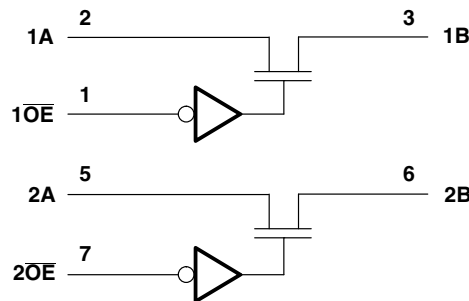
| T <sub>A</sub> | PACKAGE†   |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 85°C  | SOIC – D   | Tube          | SN74CBT3306D          | CU306            |
|                |            | Tape and reel | SN74CBT3306DR         |                  |
|                | TSSOP – PW | Tube          | SN74CBT3306PW         | CU306            |
|                |            | Tape and reel | SN74CBT3306PWR        |                  |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (each bus switch)

| INPUT $\overline{OE}$ | FUNCTION        |
|-----------------------|-----------------|
| L                     | A port = B port |
| H                     | Disconnect      |

## logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN74CBT3306 DUAL FET BUS SWITCH

SCDS016H – MAY 1995 – REVISED JANUARY 2004

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|  |                |
|--|----------------|
| Supply voltage range, $V_{CC}$                                   | -0.5 V to 7 V  |
| Input voltage range, $V_I$ (see Note 1)                          | -0.5 V to 7 V  |
| Continuous channel current                                       | 128 mA         |
| Input clamp current, $I_K$ ( $V_{I/O} < 0$ )                     | -50 mA         |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package | 97°C/W         |
| PW package   | 149°C/W        |
| Storage temperature range, $T_{stg}$                             | -65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

|   | MIN | MAX | UNIT |
|---|-----|-----|------|
| $V_{CC}$ Supply voltage                   | 4   | 5.5 | V    |
| $V_{IH}$ High-level control input voltage | 2   |     | V    |
| $V_{IL}$ Low-level control input voltage  |     | 0.8 | V    |
| $T_A$ Operating free-air temperature      | -40 | 85  | °C   |

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                    | TEST CONDITIONS                          |   | MIN           | TYP <sup>‡</sup> | MAX  | UNIT |
|------------------------------|--|---|---------------|------------------|------|------|
| $V_{IK}$                     | $V_{CC} = 4.5$ V,                        | $I_I = -18$ mA  |               |                  | -1.2 | V    |
| $I_I$                        | $V_{CC} = 5.5$ V,                        | $V_I = 5.5$ V or GND  |               |                  | ±1   | μA   |
| $I_{CC}$                     | $V_{CC} = 5.5$ V,                        | $I_O = 0$ , $V_I = V_{CC}$ or GND                                     |               |                  | 3    | μA   |
| $\Delta I_{CC}$ <sup>§</sup> | Control inputs                           | $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND |               |                  | 2.5  | mA   |
| $C_i$                        | Control inputs                           | $V_I = 3$ V or 0  |               |                  | 3    | pF   |
| $C_{i(OFF)}$                 | $V_O = 3$ V or 0,                        | $\overline{OE} = V_{CC}$  |               |                  | 4    | pF   |
| $r_{on}$ <sup>¶</sup>        | $V_{CC} = 4$ V,<br>TYP at $V_{CC} = 4$ V | $V_I = 2.4$ V,  | $I_I = 15$ mA | 14               | 20   | Ω    |
|                              |  | $V_I = 0$   | $I_I = 64$ mA | 5                | 7    |      |
|                              | $V_{CC} = 4.5$ V                         | $V_I = 0$   | $I_I = 30$ mA | 5                | 7    |      |
|                              |  | $V_I = 2.4$ V,  | $I_I = 15$ mA | 10               | 15   |      |

<sup>‡</sup> All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

<sup>¶</sup> Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

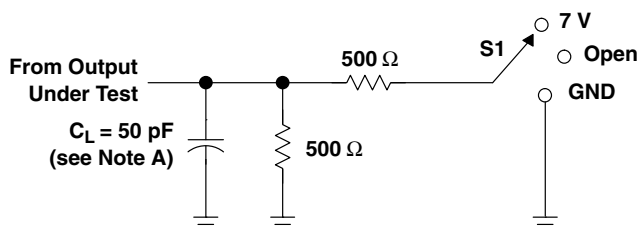


switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT)    | TO (OUTPUT) | $V_{CC} = 4$ V |     | $V_{CC} = 5$ V<br>$\pm 0.5$ V |     | UNIT |
|------------------|-----------------|-------------|----------------|-----|-------------------------------|-----|------|
|                  |                 |             | MIN            | MAX | MIN                           | MAX |      |
| $t_{pd}^\dagger$ | A or B          | B or A      | 0.35           |     | 0.25                          |     | ns   |
| $t_{en}$         | $\overline{OE}$ | A or B      | 5.6            |     | 1.8                           | 5   | ns   |
| $t_{dis}$        | $\overline{OE}$ | A or B      | 4.6            |     | 1                             | 4.3 | ns   |

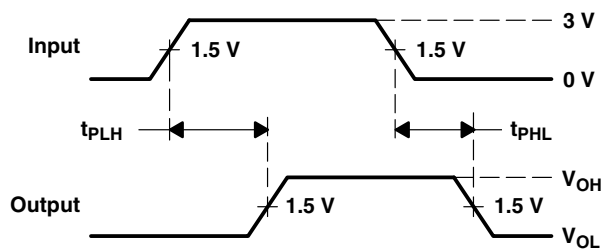
<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

### PARAMETER MEASUREMENT INFORMATION

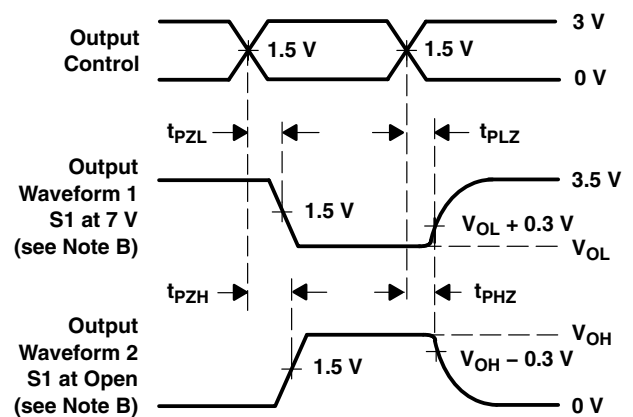


LOAD CIRCUIT

| TEST              | S1   |
|-------------------|------|
| $t_{pd}$          | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74CBT3306D     | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CU306                   | <a href="#">Samples</a> |
| SN74CBT3306DR    | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CU306                   | <a href="#">Samples</a> |
| SN74CBT3306PW    | ACTIVE        | TSSOP        | PW              | 8    | 150         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CU306                   | <a href="#">Samples</a> |
| SN74CBT3306PWR   | ACTIVE        | TSSOP        | PW              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU   CU SN       | Level-1-260C-UNLIM   | -40 to 85    | CU306                   | <a href="#">Samples</a> |
| SN74CBT3306PWRE4 | ACTIVE        | TSSOP        | PW              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CU306                   | <a href="#">Samples</a> |
| SN74CBT3306PWRG4 | ACTIVE        | TSSOP        | PW              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CU306                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

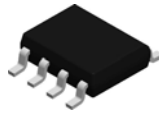

\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBT3306DR    | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN74CBT3306DR    | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN74CBT3306PWR   | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBT3306PWR   | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBT3306PWRG4 | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBT3306DR    | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| SN74CBT3306DR    | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| SN74CBT3306PWR   | TSSOP        | PW              | 8    | 2000 | 367.0       | 367.0      | 35.0        |
| SN74CBT3306PWR   | TSSOP        | PW              | 8    | 2000 | 364.0       | 364.0      | 27.0        |
| SN74CBT3306PWRG4 | TSSOP        | PW              | 8    | 2000 | 367.0       | 367.0      | 35.0        |

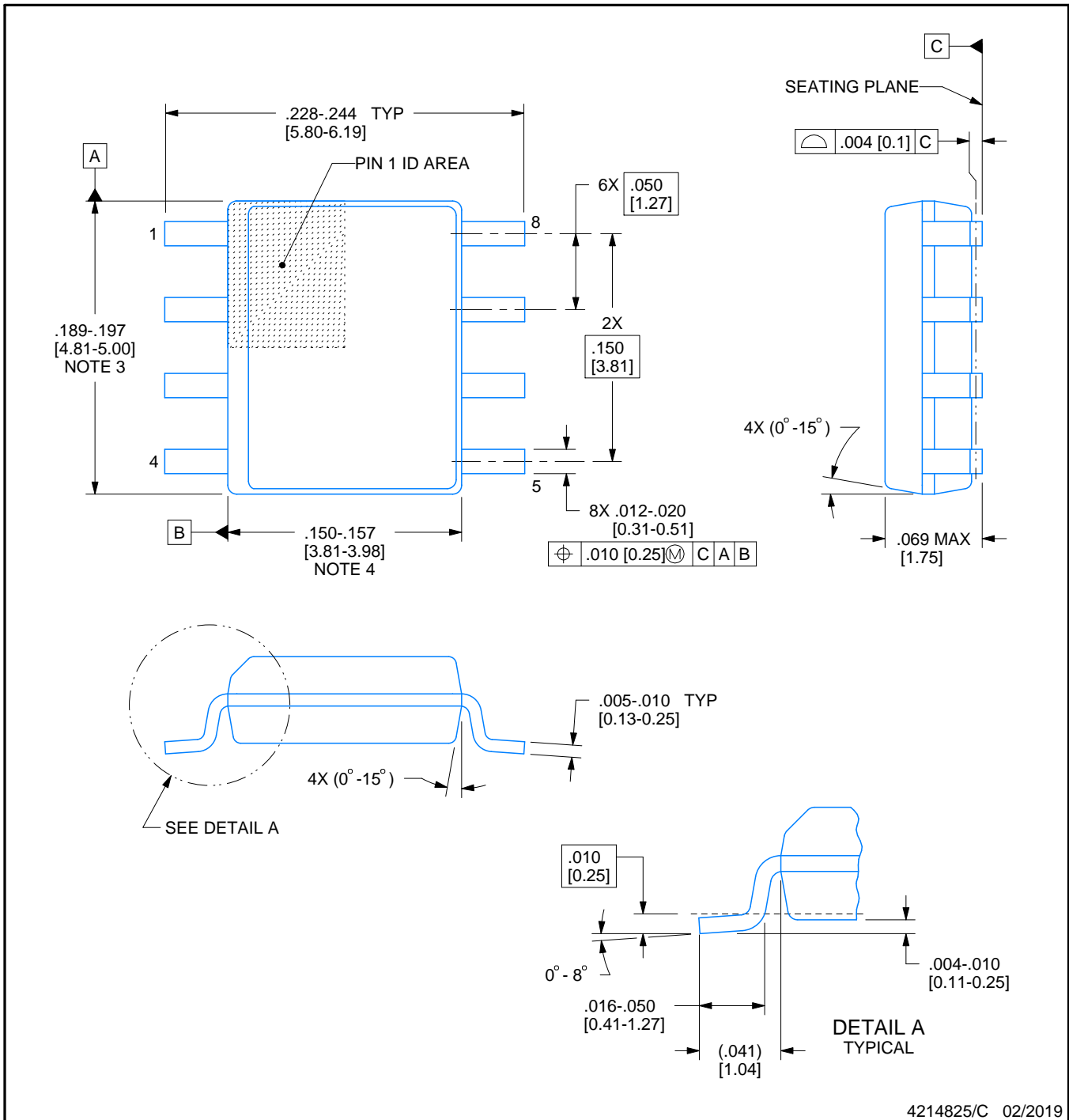


D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

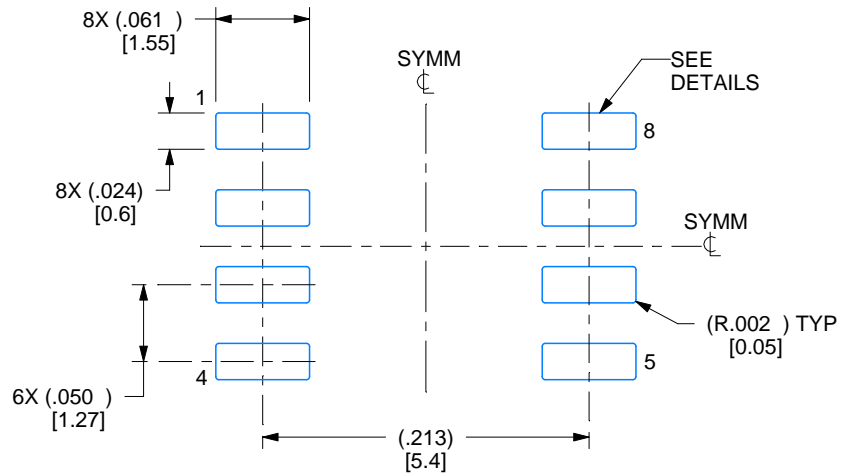
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

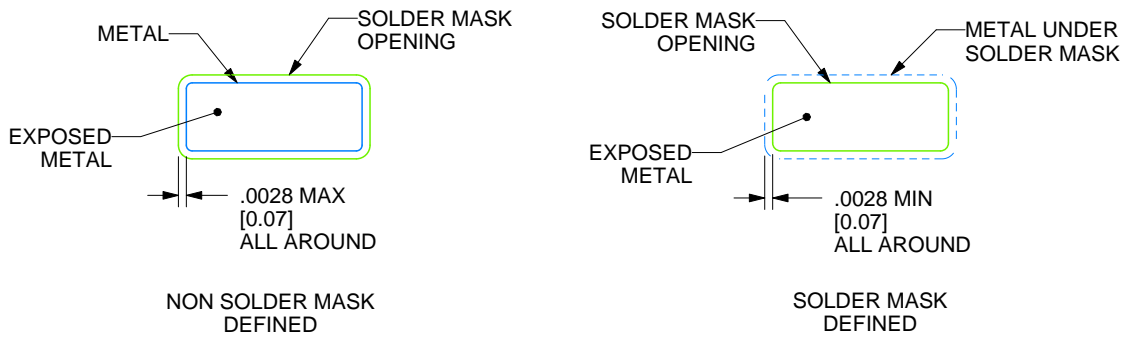
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

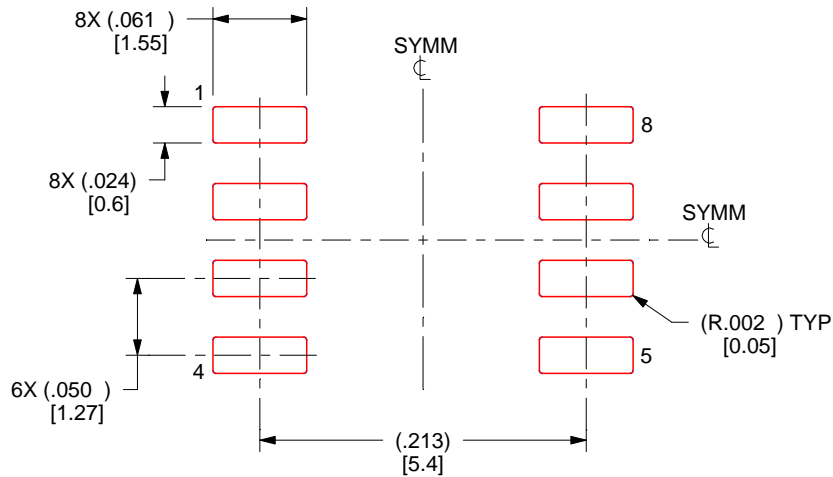
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

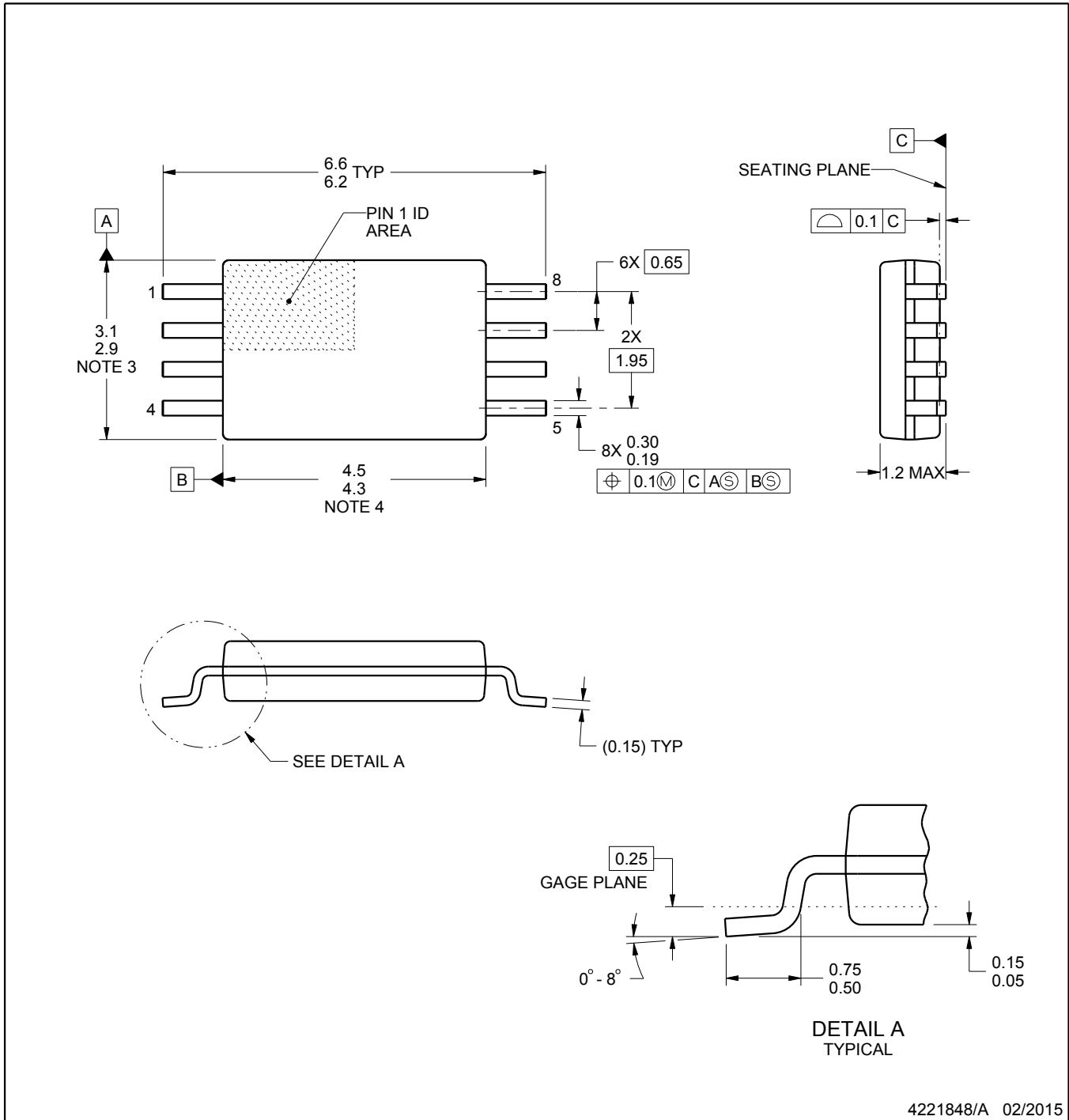
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

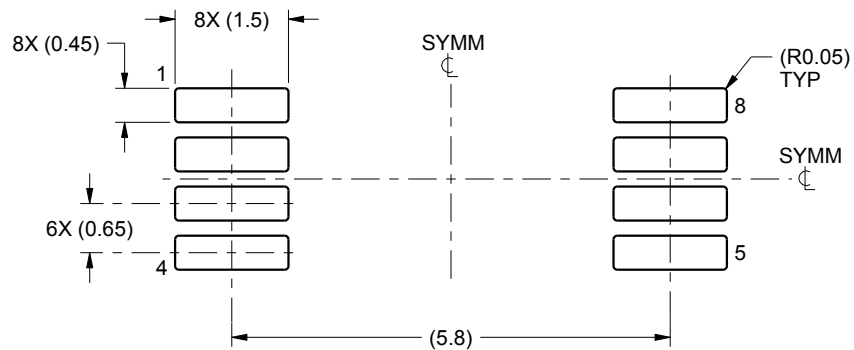
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

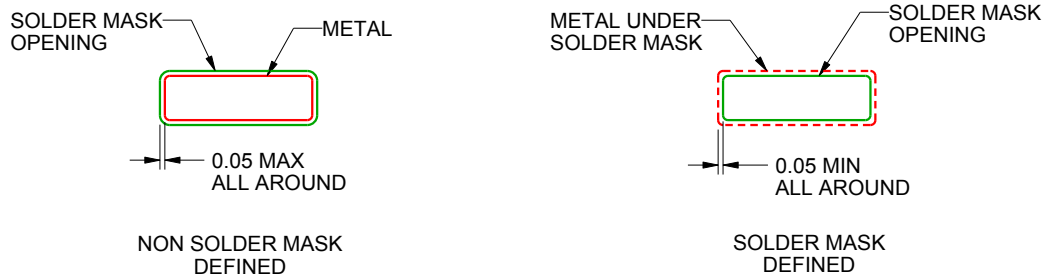
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

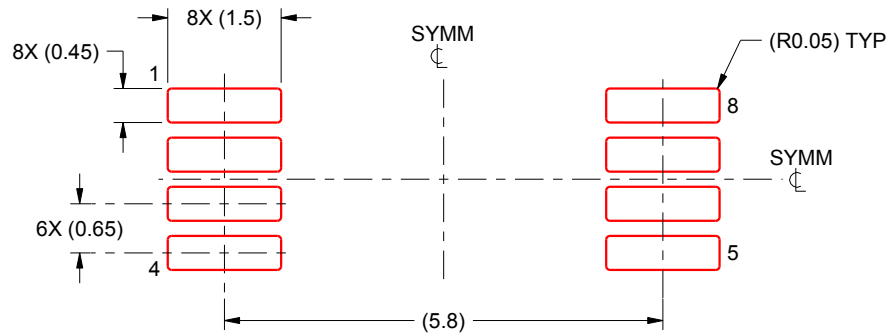
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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