



**THE DATASHEET OF
SN75C1406DW**

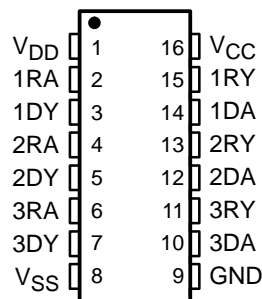


SN65C1406, SN75C1406 TRIPLE LOW-POWER DRIVERS/RECEIVERS

SLLS148E – MAY 1990 – REVISED OCTOBER 2001

- Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28
- Very Low Power Consumption . . . 5 mW Typ
- Wide Driver Supply Voltage Range . . . ± 4.5 V to ± 15 V
- Driver Output Slew Rate Limited to 30 V/ μ s Max
- Receiver Input Hysteresis . . . 1000 mV Typ
- Push-Pull Receiver Outputs
- On-Chip Receiver 1- μ s Noise Filter
- Functionally Interchangeable With Motorola MC145406 and Texas Instruments TL145406
- Package Options Include Plastic Small-Outline (D, DW, NS) Packages and DIPs (N)

SN65C1406 . . . D PACKAGE
SN75C1406 . . . D, DW, N, OR NS PACKAGE
(TOP VIEW)



description

The SN65C1406 and SN75C1406 are low-power BiMOS devices containing three independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices are designed to conform to TIA/EIA-232-F. The drivers and receivers of the SN65C1406 and SN75C1406 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/ μ s, and the receivers have filters that reject input noise pulses shorter than 1 μ s. Both these features eliminate the need for external components.

The SN65C1406 and SN75C1406 are designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C1406 and SN75C1406 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN65C1406 is characterized for operation from -40°C to 85°C . The SN75C1406 is characterized for operation from 0°C to 70°C .

AVAILABLE OPTIONS

| T _A | PACKAGED DEVICES | | | |
|---|-------------------|--------------------|-----------------|----------------------------|
| | SMALL OUTLINE (D) | SMALL OUTLINE (DW) | PLASTIC DIP (N) | PLASTIC SMALL OUTLINE (NS) |
| -40°C to 85°C | SN65C1406D | — | — | — |
| 0°C to 70°C | SN75C1406D | SN75C1406DW | SN75C1406N | SN75C1406NS |

The D, DW, and PW packages are available taped and reeled. Add the suffix R to device type (e.g., SN75C1406DR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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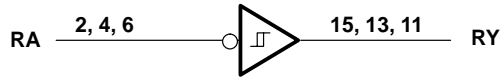
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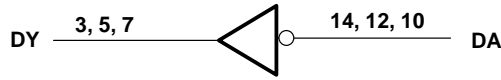
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logic diagram (positive logic)

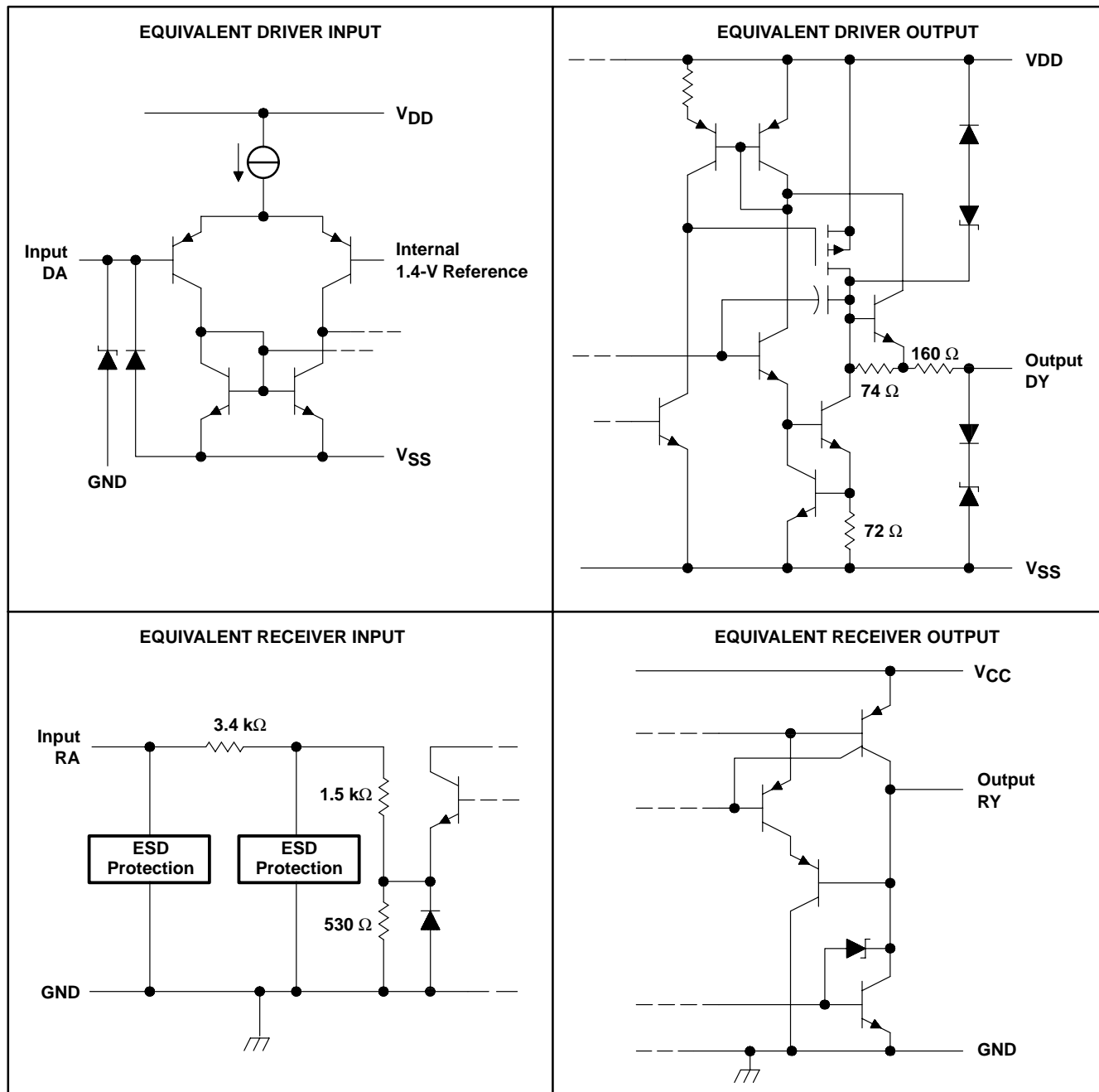
Typical of Each Receiver



Typical of Each Driver



schematics of inputs and outputs



All resistor values shown are nominal.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|--------------------------------------|
| Supply voltage: V_{DD} (see Note 1) | 15 V |
| V_{SS} | -15 V |
| V_{CC} | 7 V |
| Input voltage range, V_I : Driver | V_{SS} to V_{DD} |
| Receiver | -30 V to 30 V |
| Output voltage range, V_O : Driver | $(V_{SS} - 6 V)$ to $(V_{DD} + 6 V)$ |
| Receiver | -0.3 V to $(V_{CC} + 0.3 V)$ |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 73°C/W |
| DW package | 57°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| Storage temperature range, T_{stg} | -65°C to 150 °C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to the network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|----------|--------------------------------|-----------|------------|----------|------|
| V_{DD} | Supply voltage | 4.5 | 12 | 15 | V |
| V_{SS} | Supply voltage | -4.5 | -12 | -15 | V |
| V_{CC} | Supply voltage | 4.5 | 5 | 6 | V |
| V_I | Input voltage | Driver | $V_{SS}+2$ | V_{DD} | V |
| | | Receiver | | ± 25 | |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{OH} | High-level output current | | | -1 | mA |
| I_{OL} | Low-level output current | | | 3.2 | mA |
| T_A | Operating free-air temperature | SN65C1406 | -40 | 85 | °C |
| | | SN75C1406 | 0 | 70 | |



DRIVER SECTION

electrical characteristics over operating free-air temperature range, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|--------------------|--|--|---|------|-------|-------|---------------|
| V _{OH} | High-level output voltage | V _{IH} = 0.8 V, R _L = 3 k Ω , See Figure 1 | V _{DD} = 5 V, V _{SS} = -5 V | 4 | 4.5 | | V |
| | | | V _{DD} = 12 V, V _{SS} = -12 V | 10 | 10.8 | | |
| V _{OL} | Low-level output voltage (see Note 3) | V _{IH} = 2 V, R _L = 3 k Ω , See Figure 1 | V _{DD} = 5 V, V _{SS} = -5 V | | -4.4 | -4 | V |
| | | | V _{DD} = 12 V, V _{SS} = -12 V | | -10.7 | -10 | |
| I _{IH} | High-level input current | V _I = 5 V, See Figure 2 | | | | 1 | μA |
| I _{IL} | Low-level input current | V _I = 0, See Figure 2 | | | | -1 | μA |
| I _{OS(H)} | High-level short-circuit output current‡ | V _I = 0.8 V, V _O = 0 or V _{SS} , See Figure 1 | | -7.5 | -12 | -19.5 | mA |
| I _{OS(L)} | Low-level short-circuit output current‡ | V _I = 2 V, V _O = 0 or V _{DD} , See Figure 1 | | 7.5 | 12 | 19.5 | mA |
| I _{DD} | Supply current from V _{DD} | No load, All inputs at 2 V or 0.8 V | V _{DD} = 5 V, V _{SS} = -5 V | | 115 | 250 | μA |
| | | | V _{DD} = 12 V, V _{SS} = -12 V | | 115 | 250 | |
| I _{SS} | Supply current from V _{SS} | No load, All inputs at 2 V or 0.8 V | V _{DD} = 5 V, V _{SS} = -5 V | | -115 | -250 | μA |
| | | | V _{DD} = 12 V, V _{SS} = -12 V | | -115 | -250 | |
| r _O | Output resistance | V _{DD} = V _{SS} = V _{CC} = 0, See Note 4 | V _O = -2 V to 2 V, | 300 | 400 | | Ω |

† All typical values are at T_A = 25°C.

‡ Not more than one output should be shorted at a time.

NOTES: 3. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.

4. Test conditions are those specified by TIA/EIA-232-F.

switching characteristics at T_A = 25°C, V_{DD} = 12 V, V_{SS} = -12 V, V_{CC} = 5 V \pm 10%

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--|---|--|------|-----|-----|------------------|
| t _{PLH} | Propagation delay time, low- to high-level output§ | R _L = 3 k Ω to 7 k Ω , C _L = 15 pF, See Figure 3 | | | 1.2 | 3 | μs |
| t _{PHL} | Propagation delay time, high- to low-level output§ | R _L = 3 k Ω to 7 k Ω , C _L = 15 pF, See Figure 3 | | | 2.5 | 3.5 | μs |
| t _{TLH} | Transition time, low- to high-level output¶ | R _L = 3 k Ω to 7 k Ω , C _L = 15 pF, See Figure 3 | | 0.53 | 2 | 3.2 | μs |
| t _{THL} | Transition time, high- to low-level output¶ | R _L = 3 k Ω to 7 k Ω , C _L = 15 pF, See Figure 3 | | 0.53 | 2 | 3.2 | μs |
| t _{TLH} | Transition time, low- to high-level output# | R _L = 3 k Ω to 7 k Ω , C _L = 2500 pF, See Figure 3 | | | 1 | 2 | μs |
| t _{THL} | Transition time, high- to low-level output# | R _L = 3 k Ω to 7 k Ω , C _L = 2500 pF, See Figure 3 | | | 1 | 2 | μs |
| SR | Output slew rate | R _L = 3 k Ω to 7 k Ω , C _L = 15 pF, See Figure 3 | | 4 | 10 | 30 | V/ μs |

§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.

¶ Measured between 10% and 90% points of output waveform

Measured between 3-V and -3-V points of output waveform (TIA/EIA-232-F conditions) with all unused inputs tied either high or low

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RECEIVER SECTION

electrical characteristics over operating free-air temperature range, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-------------|--|---|--|-------|------|---------------|
| V_{IT+} | Positive-going input threshold voltage | See Figure 5 | 1.7 | 2 | 2.55 | V |
| V_{IT-} | Negative-going input threshold voltage | See Figure 5 | 0.65 | 1 | 1.25 | V |
| V_{hys} | Input hysteresis voltage ($V_{IT+} - V_{IT-}$) | | 600 | 1000 | | mV |
| V_{OH} | High-level output voltage | $V_I = 0.75\text{ V}$, $I_{OH} = -20\text{ }\mu\text{A}$, See Figure 5 and Note 5 | 3.5 | | | V |
| | | $V_I = 0.75\text{ V}$, $I_{OH} = -1\text{ mA}$, See Figure 5 | $V_{CC} = 4.5\text{ V}$ | 2.8 | 4.4 | |
| | | | $V_{CC} = 5\text{ V}$ | 3.8 | 4.9 | |
| | | $V_{CC} = 5.5\text{ V}$ | 4.3 | 5.4 | | |
| V_{OL} | Low-level output voltage | $V_I = 3\text{ V}$, $I_{OL} = 3.2\text{ mA}$, See Figure 5 | | 0.17 | 0.4 | V |
| I_{IH} | High-level input current | $V_I = 2.5\text{ V}$ | 3.6 | 4.6 | 8.3 | mA |
| | | $V_I = 3\text{ V}$ | 0.43 | 0.55 | 1 | |
| I_{IL} | Low-level input current | $V_I = -2.5\text{ V}$ | -3.6 | -5 | -8.3 | mA |
| | | $V_I = -3\text{ V}$ | -0.43 | -0.55 | -1 | |
| $I_{OS(H)}$ | High-level short-circuit output current | $V_I = 0.75\text{ V}$, $V_O = 0$, See Figure 4 | | -8 | -15 | mA |
| $I_{OS(L)}$ | Low-level short-circuit output current | $V_I = V_{CC}$, $V_O = V_{CC}$, See Figure 4 | | 13 | 25 | mA |
| I_{CC} | Supply current from V_{CC} | No load, All inputs at 0 or 5 V | $V_{DD} = 5\text{ V}$, $V_{SS} = -5\text{ V}$ | 320 | 450 | μA |
| | | | $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$ | 320 | 450 | |

† All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 5: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs remain in the high state.

switching characteristics at $T_A = 25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $V_{CC} = 5\text{ V} \pm 10\%$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|---|--|-----|-----|-----|---------------|
| t_{PLH} | Propagation delay time, low- to high-level output | $C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6 | | 3 | 4 | μs |
| t_{PHL} | Propagation delay time, high- to low-level output | $C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6 | | 3 | 4 | μs |
| t_{TLH} | Transition time, low- to high-level output‡ | $C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6 | | 300 | 450 | ns |
| t_{THL} | Transition time, high- to low-level output‡ | $C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$, See Figure 6 | | 100 | 300 | ns |
| $t_{W(N)}$ | Duration of longest pulse rejected as noise§ | $C_L = 50\text{ pF}$, $R_L = 5\text{ k}\Omega$ | 1 | | 4 | μs |

‡ Measured between 10% and 90% points of output waveform

§ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{W(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{W(N)}$.



PARAMETER MEASUREMENT INFORMATION

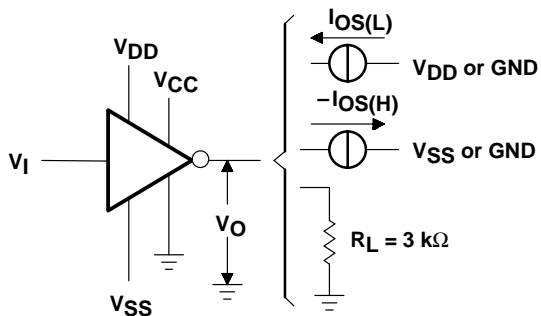


Figure 1. Driver Test Circuit
 V_{OH} , V_{OL} , $I_{OS(L)}$, $I_{OS(H)}$

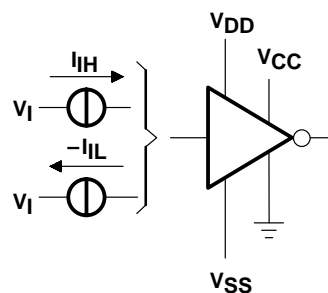
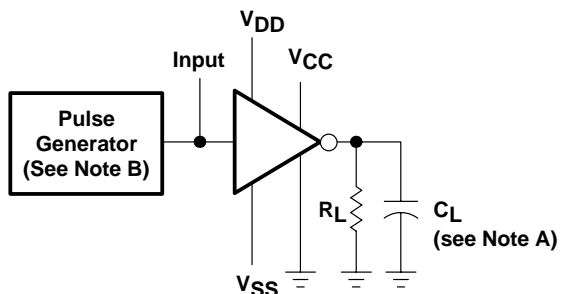
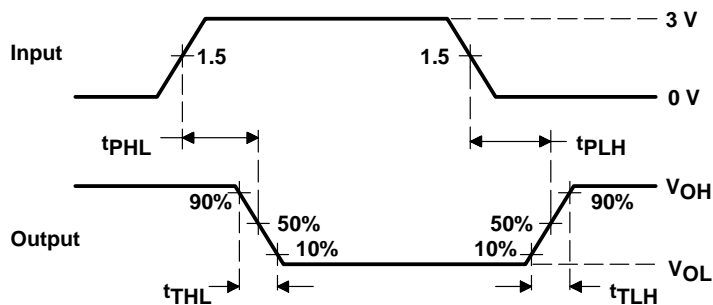


Figure 2. Driver Test Circuit, I_{iL} , I_{iH}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $t_w = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f < 50 \text{ ns}$.

Figure 3. Driver Test Circuit and Voltage Waveforms

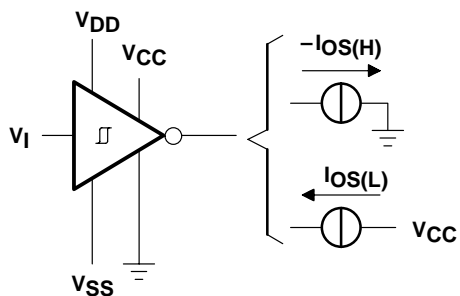


Figure 4. Receiver Test Circuit, $I_{OS(H)}$, $I_{OS(L)}$

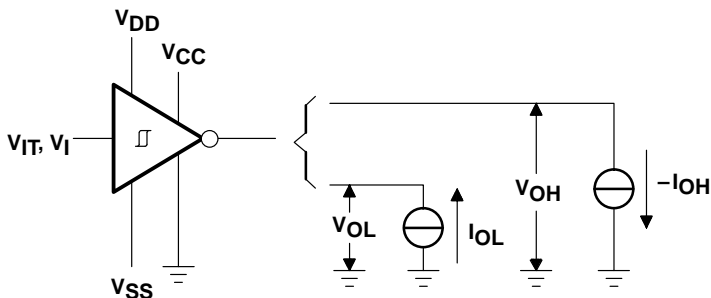
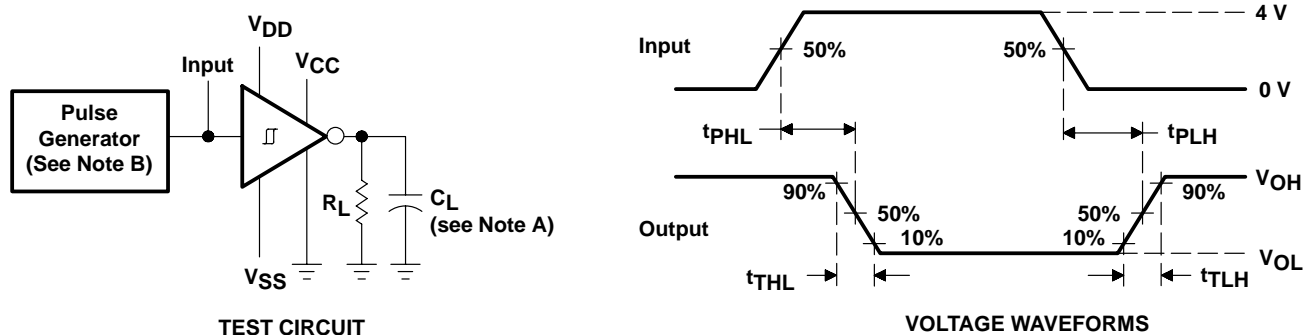


Figure 5. Receiver Test Circuit, V_{IT} , V_{OL} , V_{OH}

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PARAMETER MEASUREMENT INFORMATION



NOTES: C. C_L includes probe and jig capacitance.
D. The pulse generator has the following characteristics: $t_w = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f < 50 \text{ ns}$.

Figure 6. Receiver Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

The TIA/EIA-232-F specification is for data interchange between a host computer and a peripheral at signaling rates up to 20 kbit/s. Many TIA/EIA-232-F devices will operate at higher data rates with lower capacitive loads (short cables). For reliable operation at greater than 20 kbit/s, the designer needs to have control of both ends of the cable. By mixing different types of TIA/EIA-232-F devices and cable lengths, errors can occur at higher frequencies (above 20 kbit/s). When operating within the TIA/EIA-232-F requirements of less than 20 kbit/s and with compliant line circuits, interoperability is assured. For applications operating above 20 kbit/s, the design engineer should consider devices and system designs that meet the TIA/EIA-232-F requirements.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65C1406D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C1406 | Samples |
| SN65C1406DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C1406 | Samples |
| SN65C1406DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65C1406 | Samples |
| SN75C1406D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75C1406 | Samples |
| SN75C1406DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75C1406 | Samples |
| SN75C1406DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75C1406 | Samples |
| SN75C1406DWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75C1406 | Samples |
| SN75C1406DWRE4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75C1406 | Samples |
| SN75C1406N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN75C1406N | Samples |
| SN75C1406NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75C1406 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65C1406DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN75C1406DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN75C1406DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| SN75C1406NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65C1406DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN75C1406DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN75C1406DWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| SN75C1406NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

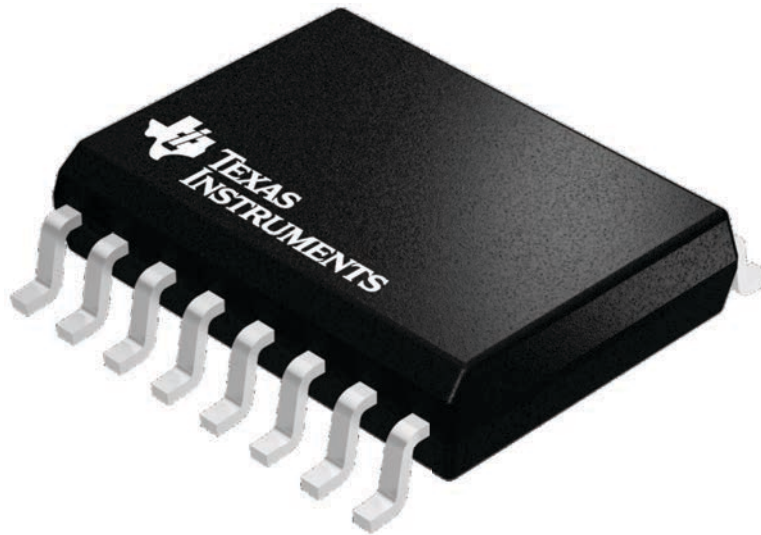
DW 16

SOIC - 2.65 mm max height

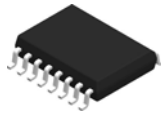
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

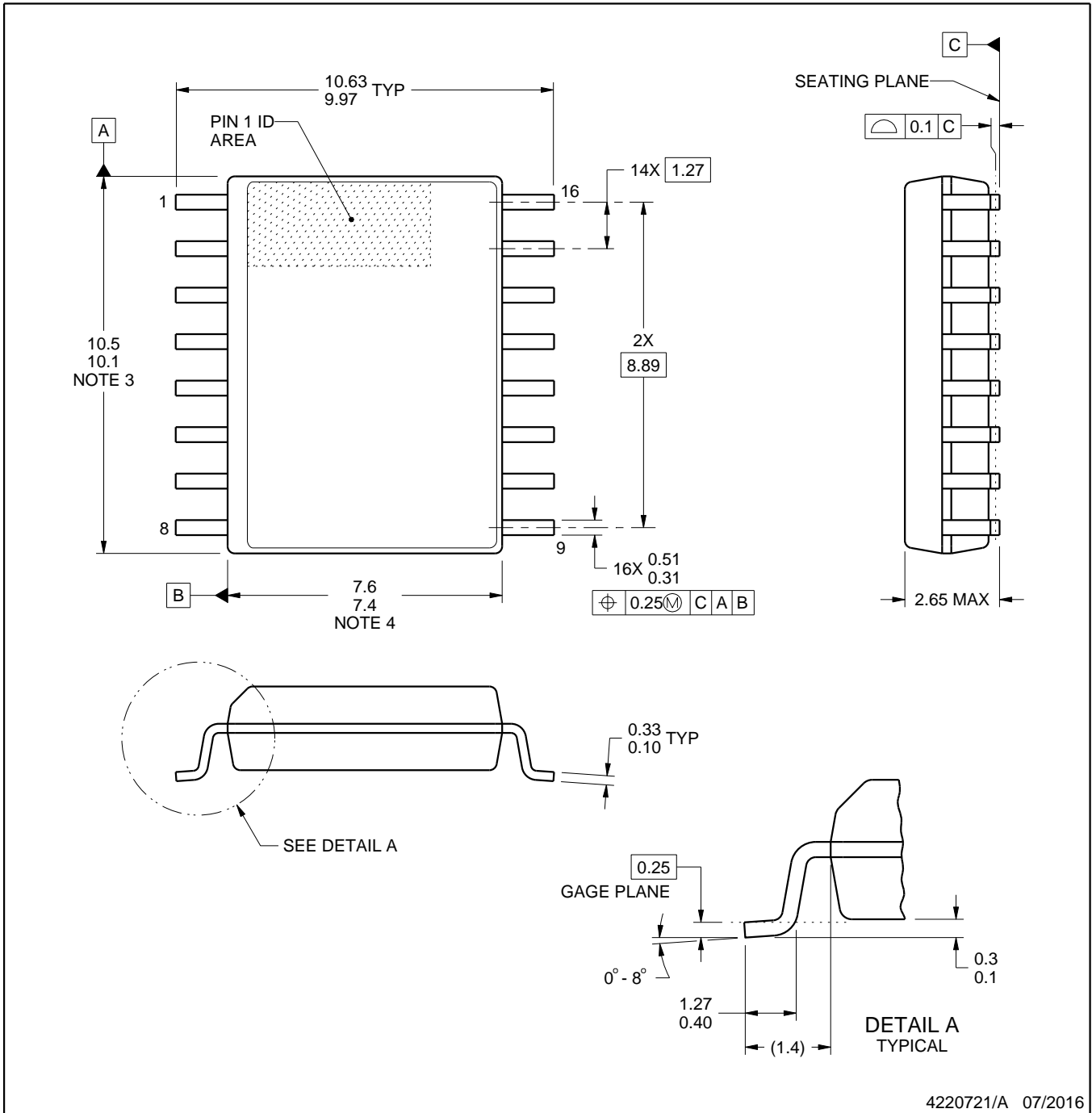


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

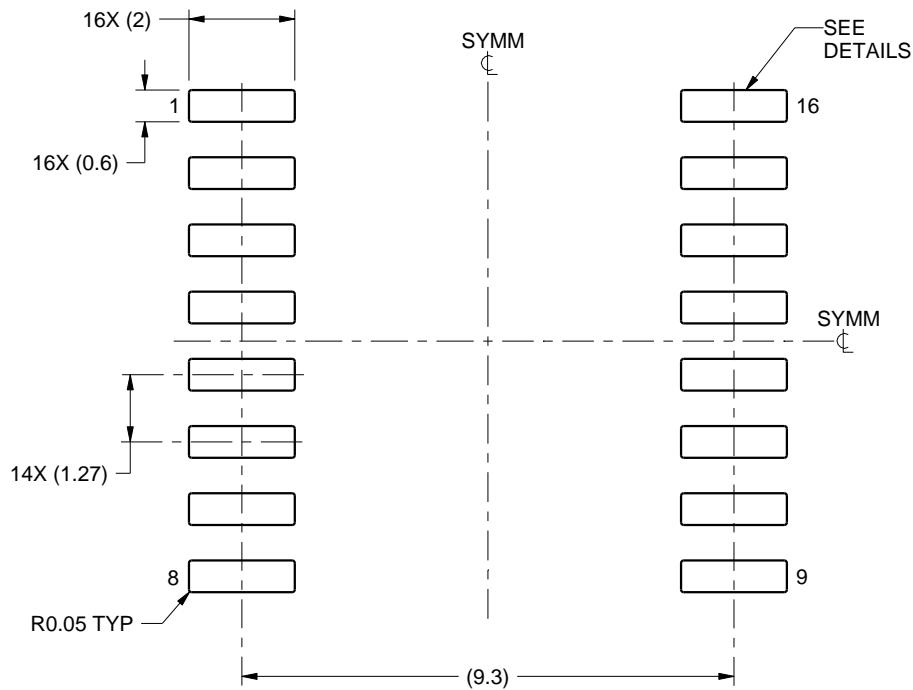
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

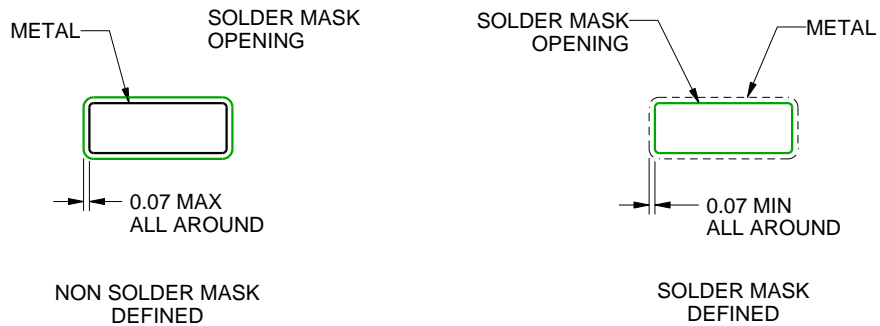
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

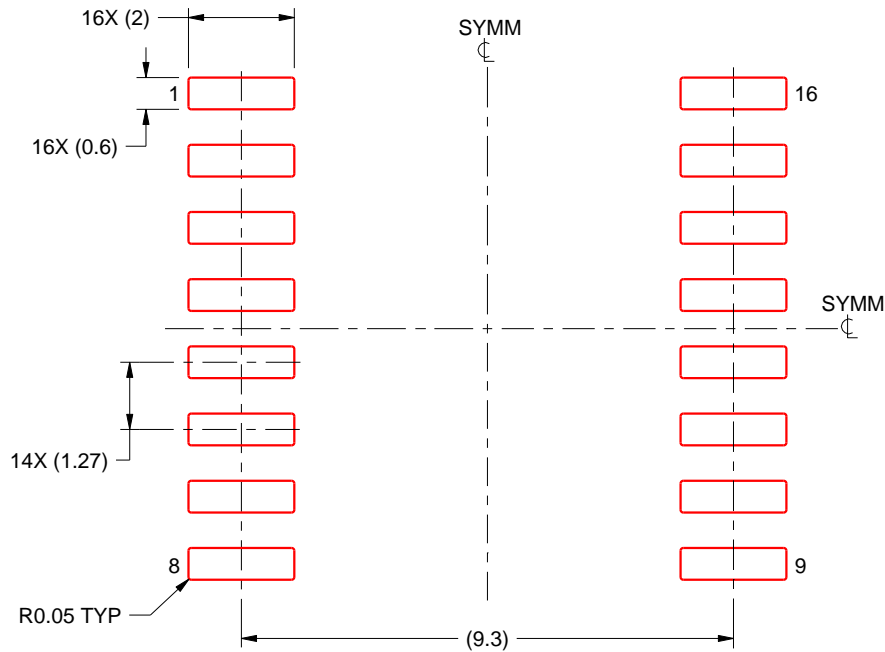
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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