



# THE DATASHEET OF SPA17N80C3



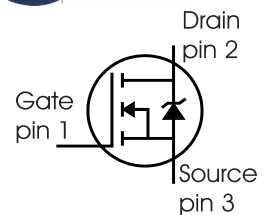
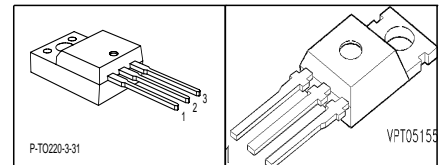
## Cool MOS™ Power Transistor

### Feature

- New revolutionary high voltage technology
- Worldwide best  $R_{DS(on)}$  in TO 220
- Ultra low gate charge
- Periodic avalanche rated
- Extreme  $dv/dt$  rated
- Ultra low effective capacitances
- Improved transconductance
- PG-TO-220-3-31: Fully isolated package (2500 VAC; 1 minute)
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC<sup>0)</sup> for target applications

$V_{DS}$	800	V
$R_{DS(on)}$	0.29	$\Omega$
$I_D$	17	A

PG-TO220-3-31 PG-TO220



Type	Package	Ordering Code	Marking
SPP17N80C3	PG-TO220	Q67040-S4353	17N80C3
SPA17N80C3	PG-TO220-3-31	SP000216353	17N80C3

### Maximum Ratings

Parameter	Symbol	Value		Unit
		SPP	SPA	
Continuous drain current $T_C = 25\text{ }^\circ\text{C}$ $T_C = 100\text{ }^\circ\text{C}$	$I_D$	17 11	17 <sup>1)</sup> 11 <sup>1)</sup>	A
Pulsed drain current, $t_p$ limited by $T_{jmax}$	$I_{D\text{ puls}}$	51	51	A
Avalanche energy, single pulse $I_D=3.4\text{A}$ , $V_{DD}=50\text{V}$	$E_{AS}$	670	670	mJ
Avalanche energy, repetitive $t_{AR}$ limited by $T_{jmax}$ <sup>2)</sup> $I_D=17\text{A}$ , $V_{DD}=50\text{V}$	$E_{AR}$	0.5	0.5	
Avalanche current, repetitive $t_{AR}$ limited by $T_{jmax}$	$I_{AR}$	17	17	A
Gate source voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Gate source voltage AC ( $f > 1\text{Hz}$ )	$V_{GS}$	$\pm 30$	$\pm 30$	
Power dissipation, $T_C = 25\text{ }^\circ\text{C}$	$P_{tot}$	208	42	W
Operating and storage temperature	$T_j, T_{stg}$	-55...+150		$^\circ\text{C}$

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Drain Source voltage slope $V_{DS} = 640 \text{ V}$ , $I_D = 17 \text{ A}$ , $T_j = 125 \text{ }^\circ\text{C}$	$dv/dt$	50	V/ns

**Thermal Characteristics**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.6	K/W
Thermal resistance, junction - case, FullPAK	$R_{thJC \text{ FP}}$	-	-	3.6	
Thermal resistance, junction - ambient, leaded	$R_{thJA}$	-	-	62	
Thermal resistance, junction - ambient, FullPAK	$R_{thJA \text{ FP}}$	-	-	80	
SMD version, device on PCB: @ min. footprint @ 6 cm <sup>2</sup> cooling area <sup>3)</sup>	$R_{thJA}$	-	-	62	
Soldering temperature, wavesoldering 1.6 mm (0.063 in.) from case for 10s <sup>4)</sup>	$T_{sold}$	-	-	260	°C

**Electrical Characteristics, at  $T_j=25^\circ\text{C}$  unless otherwise specified**

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}$ , $I_D=0.25\text{mA}$	800	-	-	V
Drain-Source avalanche breakdown voltage	$V_{(BR)DS}$	$V_{GS}=0\text{V}$ , $I_D=17\text{A}$	-	870	-	
Gate threshold voltage	$V_{GS(th)}$	$I_D=1000\mu\text{A}$ , $V_{GS}=V_D$	2.1	3	3.9	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=800\text{V}$ , $V_{GS}=0\text{V}$ , $T_j=25^\circ\text{C}$ $T_j=150^\circ\text{C}$	-	0.5	25	$\mu\text{A}$
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{V}$ , $V_{DS}=0\text{V}$	-	-	100	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$ , $I_D=11\text{A}$ $T_j=25^\circ\text{C}$ $T_j=150^\circ\text{C}$	-	0.25	0.29	$\Omega$
Gate input resistance	$R_G$	$f=1\text{MHz}$ , open drain	-	0.7	-	

**Electrical Characteristics**

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Transconductance	$g_{fs}$	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$ , $I_D = 11A$	-	15	-	S
Input capacitance	$C_{iss}$	$V_{GS} = 0V$ , $V_{DS} = 25V$ , $f = 1MHz$	-	2320	-	pF
Output capacitance	$C_{oss}$		-	1250	-	
Reverse transfer capacitance	$C_{rss}$		-	60	-	
Effective output capacitance, <sup>5)</sup> energy related	$C_{o(er)}$	$V_{GS} = 0V$ , $V_{DS} = 0V$ to 480V	-	59	-	
Effective output capacitance, <sup>6)</sup> time related	$C_{o(tr)}$		-	124	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 400V$ , $V_{GS} = 0/10V$ , $I_D = 17A$ , $R_G = 4.7\Omega$ , $T_j = 125^\circ C$	-	25	-	ns
Rise time	$t_r$		-	15	-	
Turn-off delay time	$t_{d(off)}$		-	72	82	
Fall time	$t_f$		-	6	9	

**Gate Charge Characteristics**

Gate to source charge	$Q_{gs}$	$V_{DD} = 640V$ , $I_D = 17A$	-	12	-	nC
Gate to drain charge	$Q_{gd}$		-	46	-	
Gate charge total	$Q_g$	$V_{DD} = 640V$ , $I_D = 17A$ , $V_{GS} = 0$ to 10V	-	91	177	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 640V$ , $I_D = 17A$	-	6	-	V

<sup>0</sup>J-STD20 and JESD22

<sup>1</sup>Limited only by maximum temperature

<sup>2</sup>Repetitive avalanche causes additional power losses that can be calculated as  $P_{AV} = E_{AR} \cdot f$ .

<sup>3</sup>Device on 40mm\*40mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air.

<sup>4</sup>Soldering temperature for TO-263: 220°C, reflow

<sup>5</sup> $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

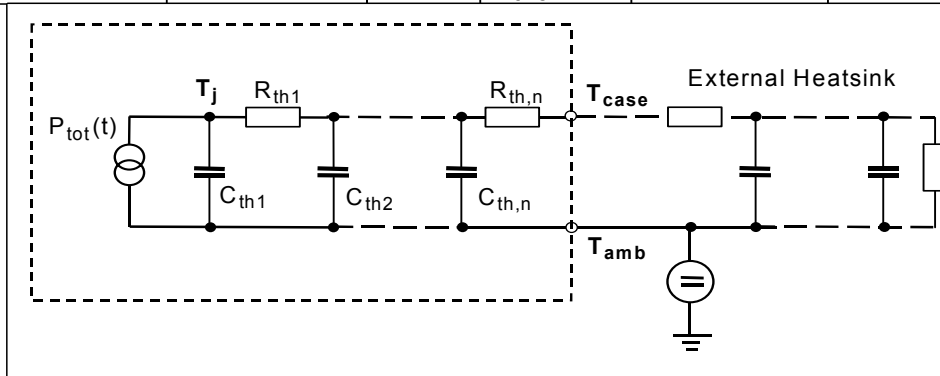
<sup>6</sup> $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Electrical Characteristics**

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Inverse diode continuous forward current	$I_S$	$T_C=25^\circ\text{C}$	-	-	17	A
Inverse diode direct current, pulsed	$I_{SM}$		-	-	51	
Inverse diode forward voltage	$V_{SD}$	$V_{GS}=0\text{V}, I_F=I_S$	-	1	1.2	V
Reverse recovery time	$t_{rr}$	$V_R=400\text{V}, I_F=I_S,$	-	550	-	ns
Reverse recovery charge	$Q_{rr}$	$di_F/dt=100\text{A}/\mu\text{s}$	-	15	-	$\mu\text{C}$
Peak reverse recovery current	$I_{rrm}$		-	51	-	A
Peak rate of fall of reverse recovery current	$di_{rr}/dt$	$T_j=25^\circ\text{C}$	-	1200	-	$\text{A}/\mu\text{s}$

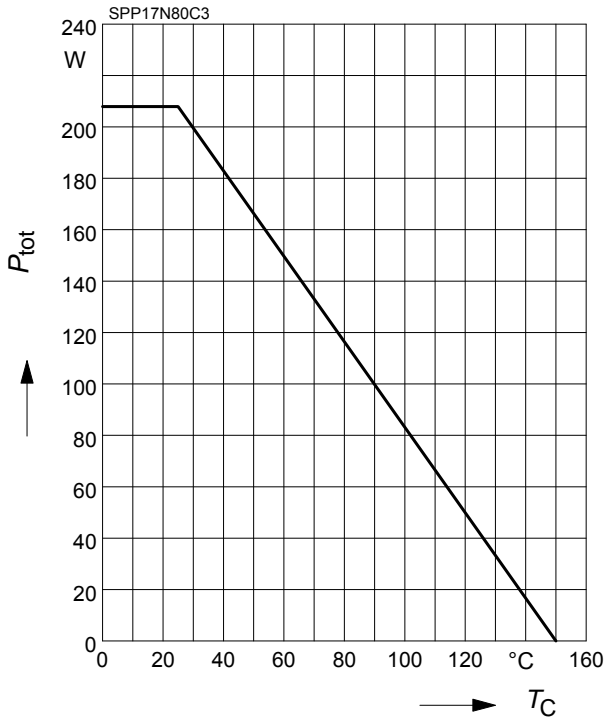
**Typical Transient Thermal Characteristics**

Symbol	Value		Unit	Symbol	Value		Unit
	SPP	SPA			SPP	SPA	
$R_{th1}$	0.00812	0.00812	K/W	$C_{th1}$	0.0003562	0.0003562	Ws/K
$R_{th2}$	0.016	0.016		$C_{th2}$	0.001337	0.001337	
$R_{th3}$	0.031	0.031		$C_{th3}$	0.001831	0.001831	
$R_{th4}$	0.114	0.16		$C_{th4}$	0.005033	0.005033	
$R_{th5}$	0.135	0.324		$C_{th5}$	0.012	0.008657	
$R_{th6}$	0.059	2.522		$C_{th6}$	0.092	0.412	



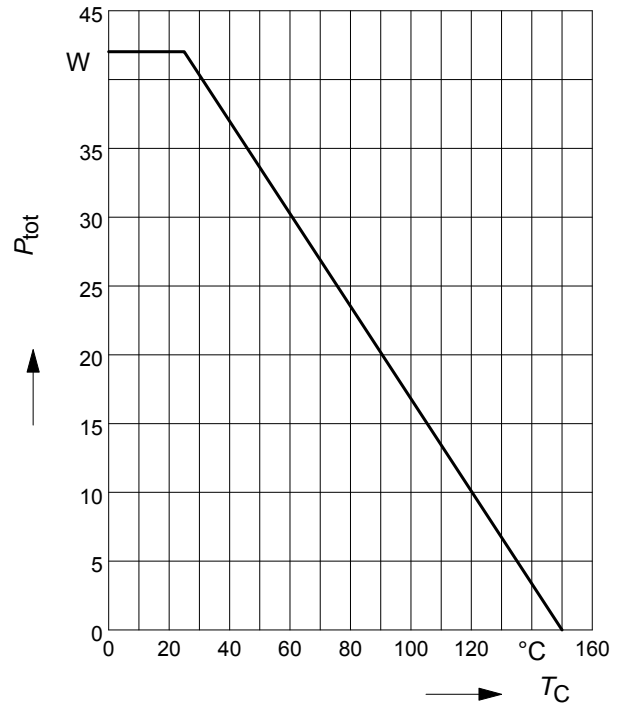
**1 Power dissipation**

$P_{tot} = f(T_C)$



**2 Power dissipation FullPAK**

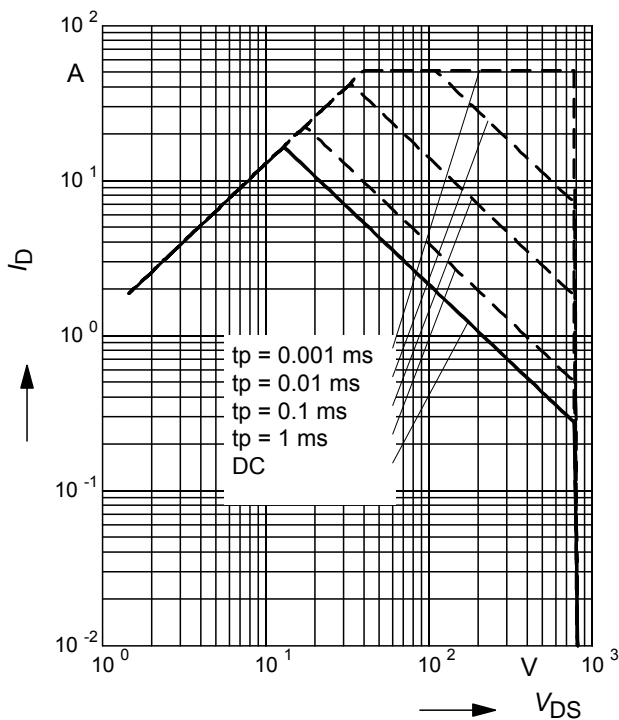
$P_{tot} = f(T_C)$



**3 Safe operating area**

$I_D = f(V_{DS})$

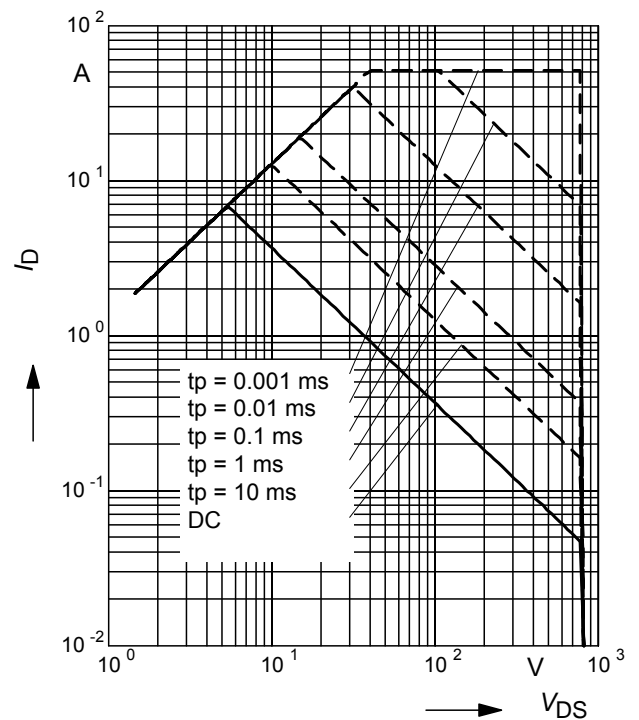
parameter :  $D = 0$  ,  $T_C = 25^\circ\text{C}$



**4 Safe operating area FullPAK**

$I_D = f(V_{DS})$

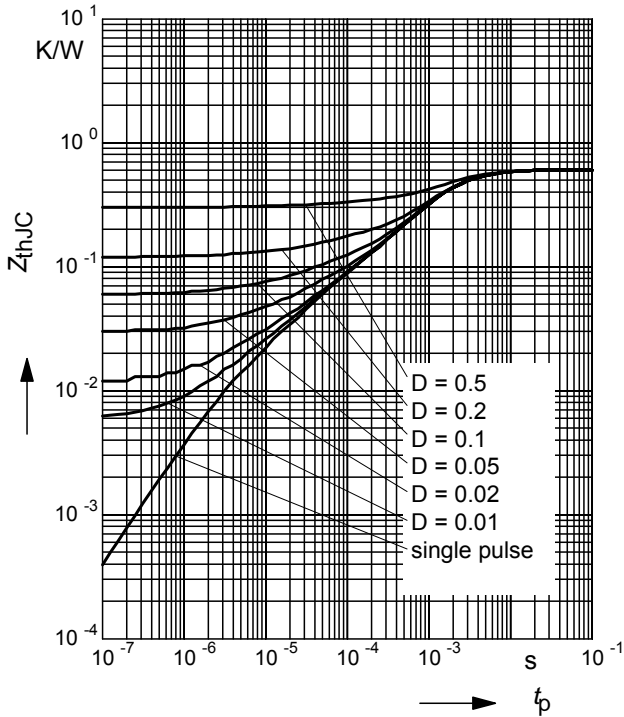
parameter:  $D = 0$  ,  $T_C = 25^\circ\text{C}$



### 5 Transient thermal impedance

$$Z_{thJC} = f(t_p)$$

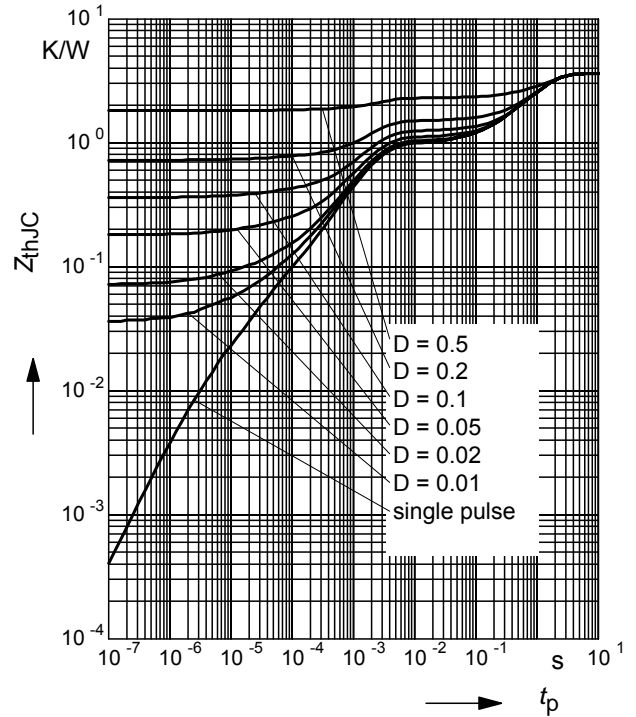
parameter:  $D = t_p/T$



### 6 Transient thermal impedance FullPAK

$$Z_{thJC} = f(t_p)$$

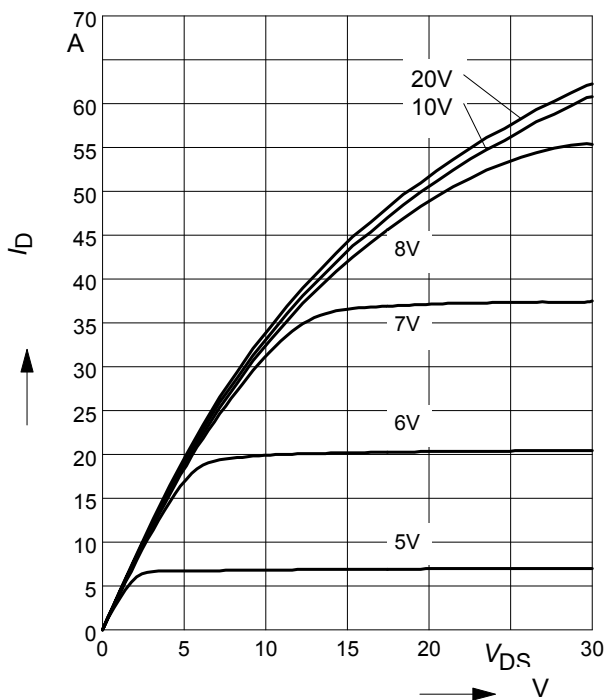
parameter:  $D = t_p/t$



### 7 Typ. output characteristic

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

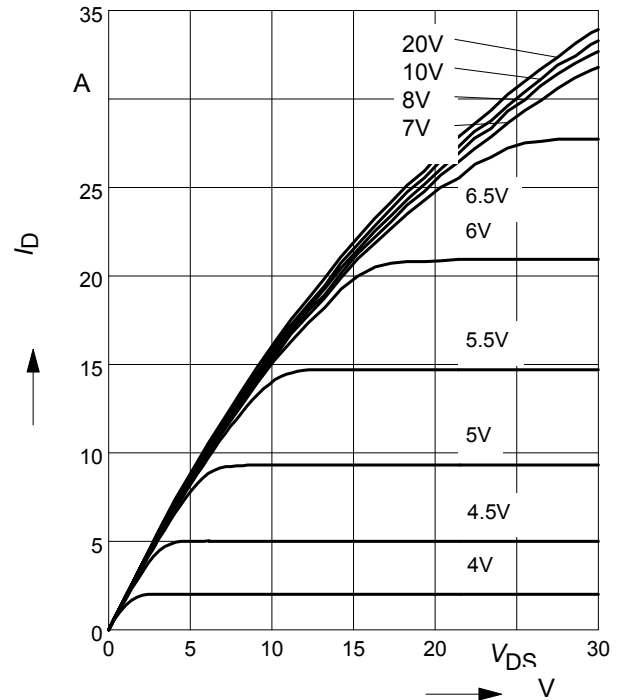
parameter:  $t_p = 10 \mu\text{s}, V_{GS}$



### 8 Typ. output characteristic

$$I_D = f(V_{DS}); T_j = 150^\circ\text{C}$$

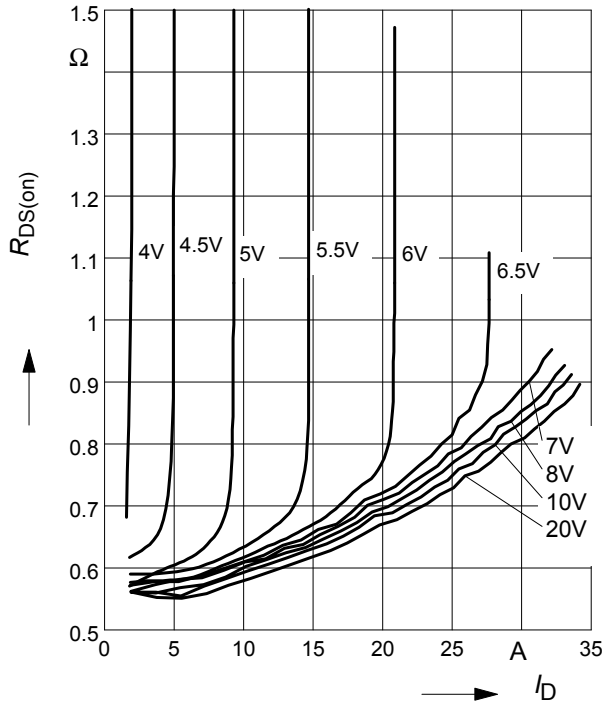
parameter:  $t_p = 10 \mu\text{s}, V_{GS}$



**9 Typ. drain-source on resistance**

$$R_{DS(on)} = f(I_D)$$

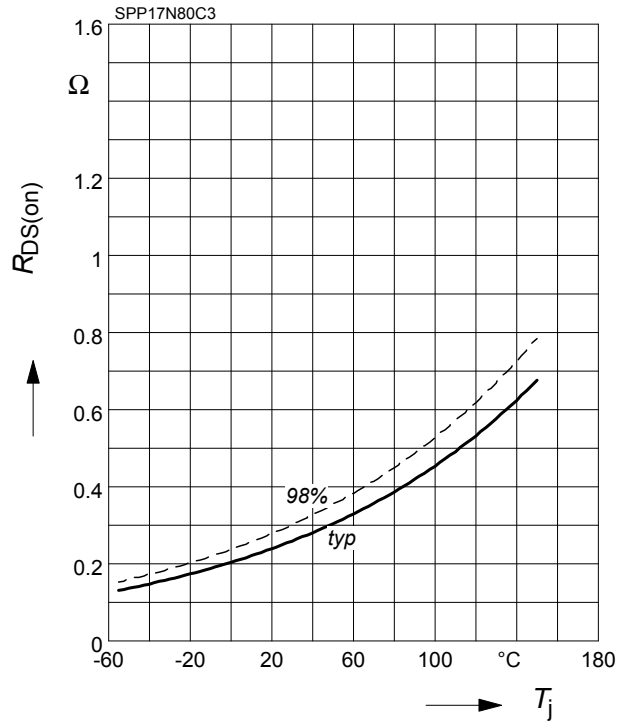
parameter:  $T_j = 150^\circ\text{C}$ ,  $V_{GS}$



**10 Drain-source on-state resistance**

$$R_{DS(on)} = f(T_j)$$

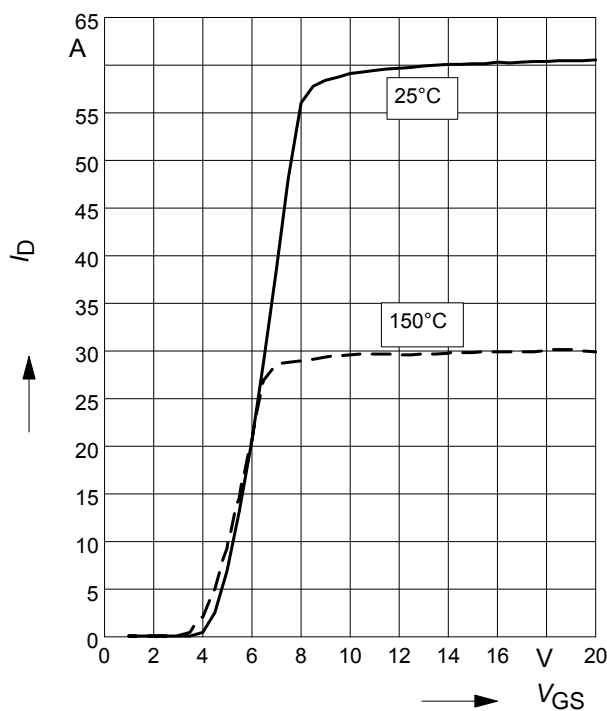
parameter:  $I_D = 11\text{ A}$ ,  $V_{GS} = 10\text{ V}$



**11 Typ. transfer characteristics**

$$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$$

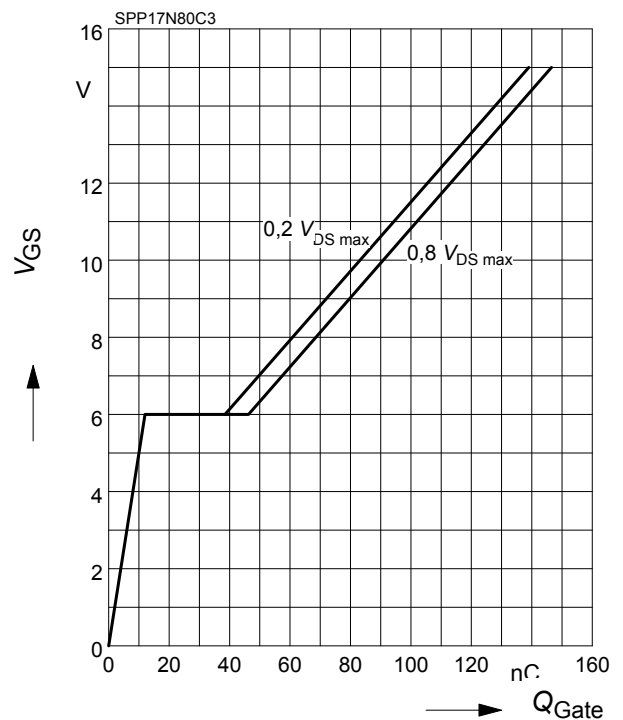
parameter:  $t_p = 10\ \mu\text{s}$



**12 Typ. gate charge**

$$V_{GS} = f(Q_{Gate})$$

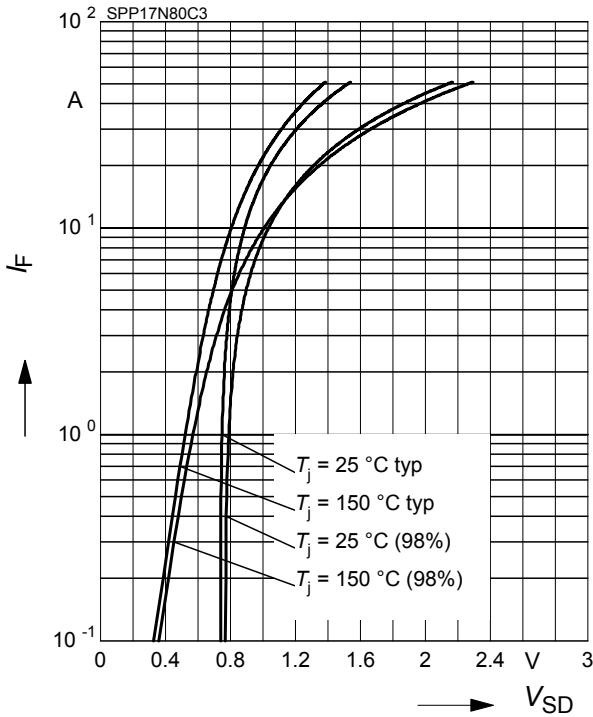
parameter:  $I_D = 17\text{ A pulsed}$



### 13 Forward characteristics of body diode

$$I_F = f(V_{SD})$$

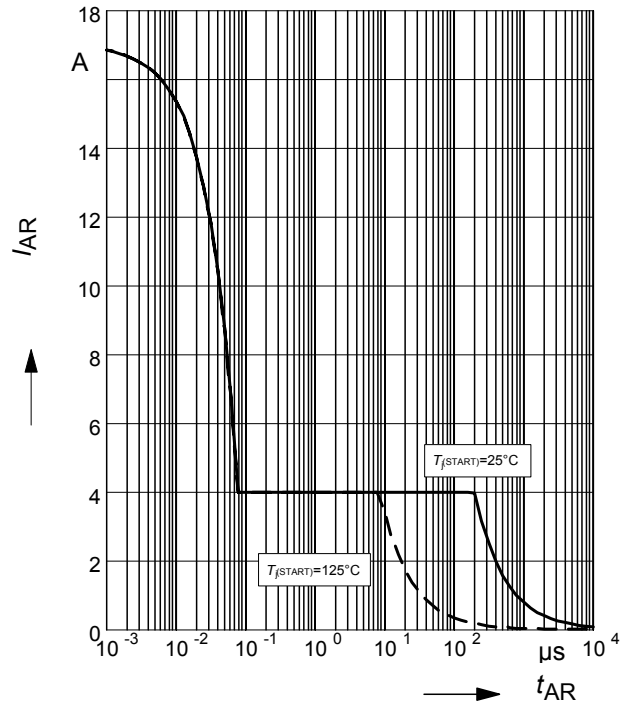
parameter:  $T_j$ ,  $t_p = 10 \mu s$



### 14 Avalanche SOA

$$I_{AR} = f(t_{AR})$$

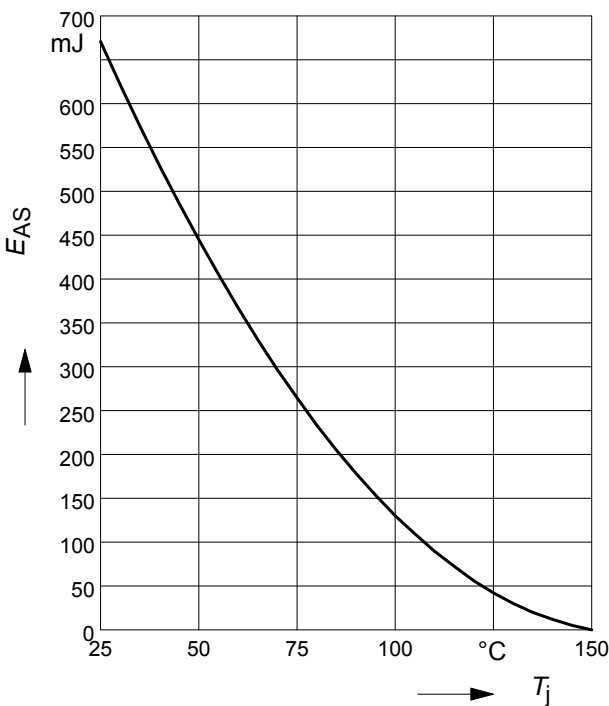
par.:  $T_j \leq 150 \text{ °C}$



### 15 Avalanche energy

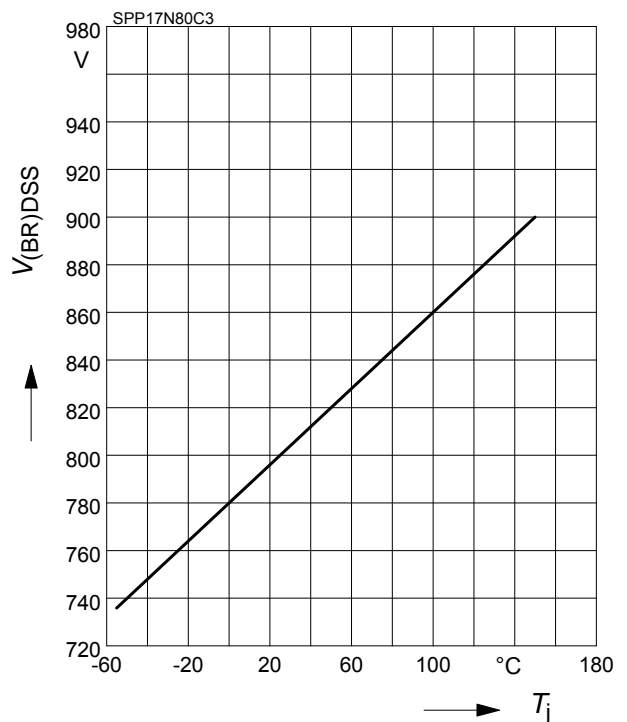
$$E_{AS} = f(T_j)$$

par.:  $I_D = 3.4 \text{ A}$ ,  $V_{DD} = 50 \text{ V}$



### 16 Drain-source breakdown voltage

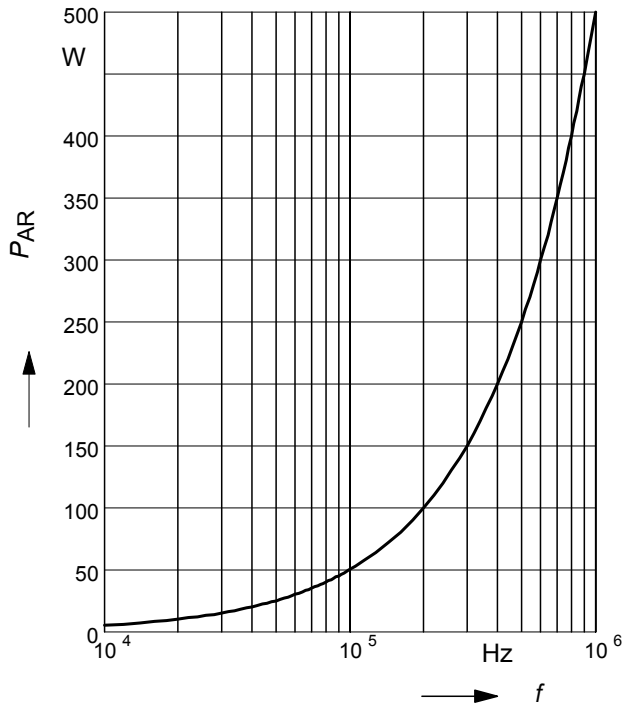
$$V_{(BR)DSS} = f(T_j)$$



**17 Avalanche power losses**

$$P_{AR} = f(f)$$

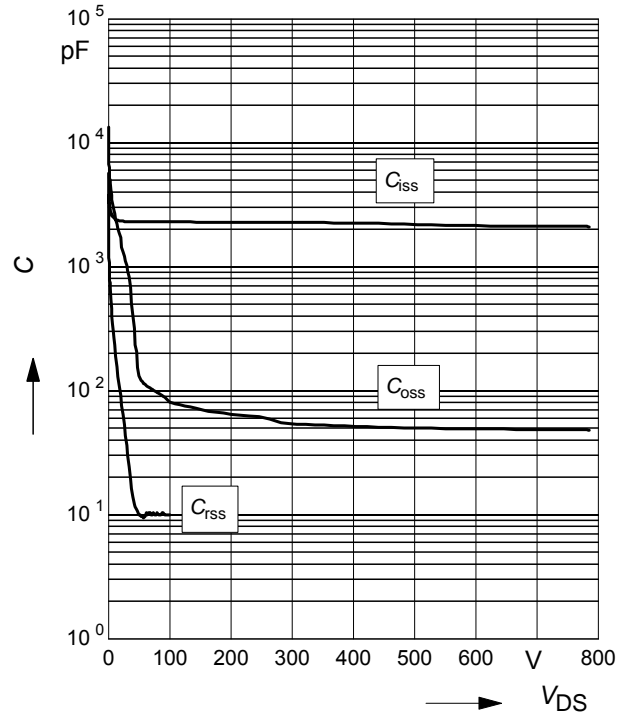
parameter:  $E_{AR}=0.5\text{mJ}$



**18 Typ. capacitances**

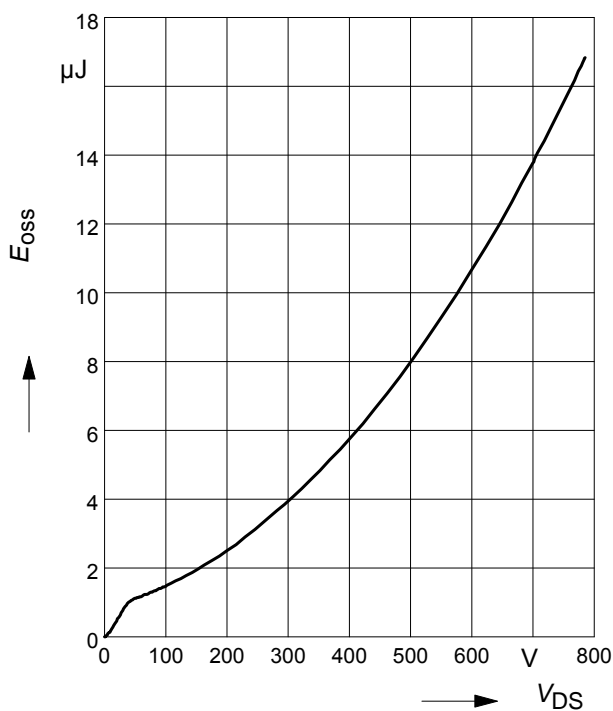
$$C = f(V_{DS})$$

parameter:  $V_{GS}=0\text{V}$ ,  $f=1\text{ MHz}$

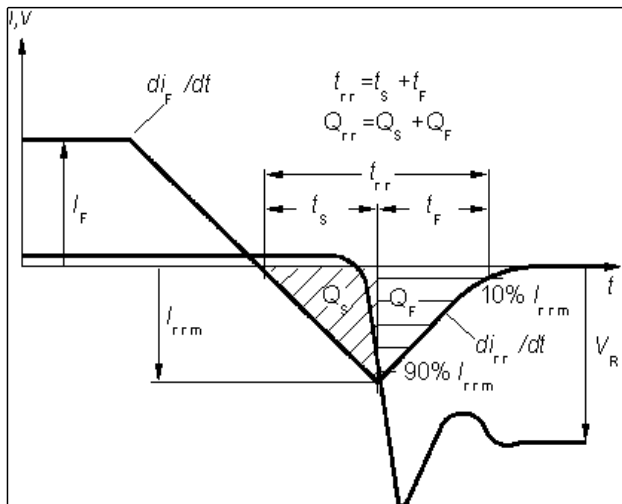


**19 Typ.  $C_{oss}$  stored energy**

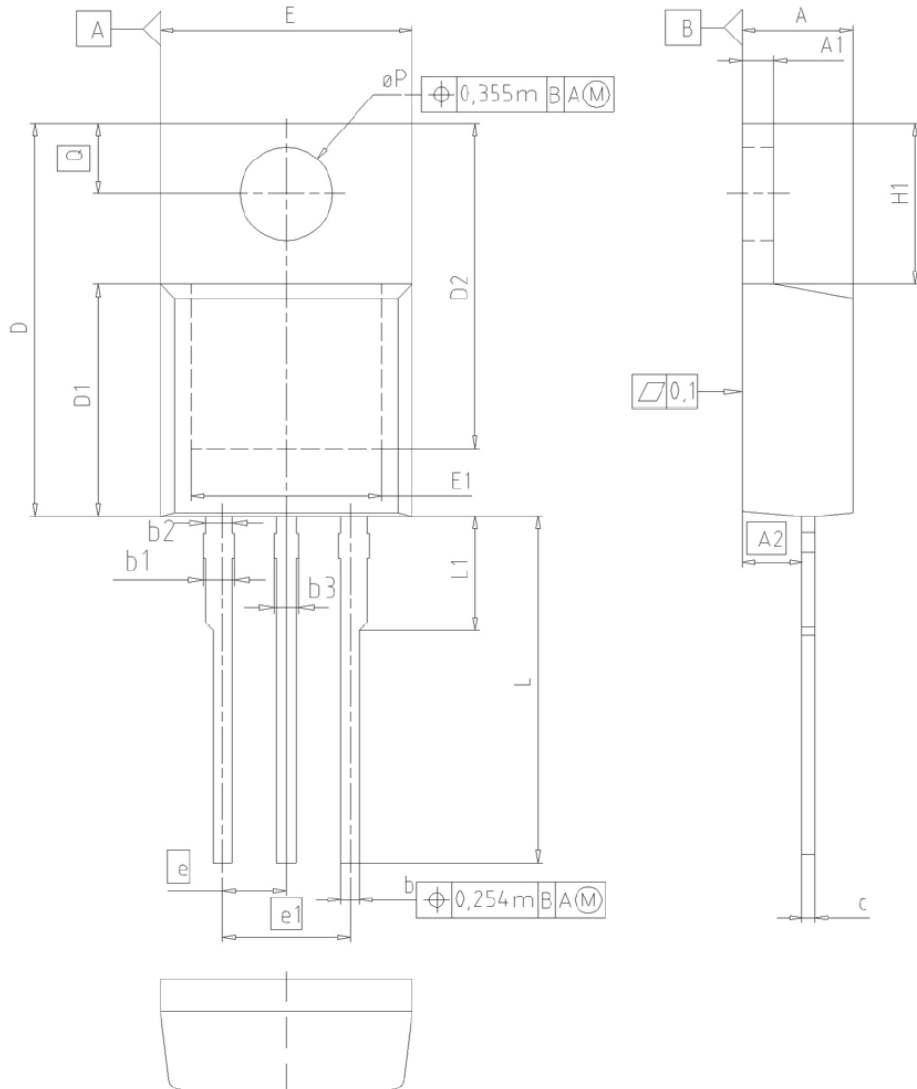
$$E_{oss} = f(V_{DS})$$



Definition of diodes switching characteristics



PG-TO220-3-1, PG-TO220-3-21



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

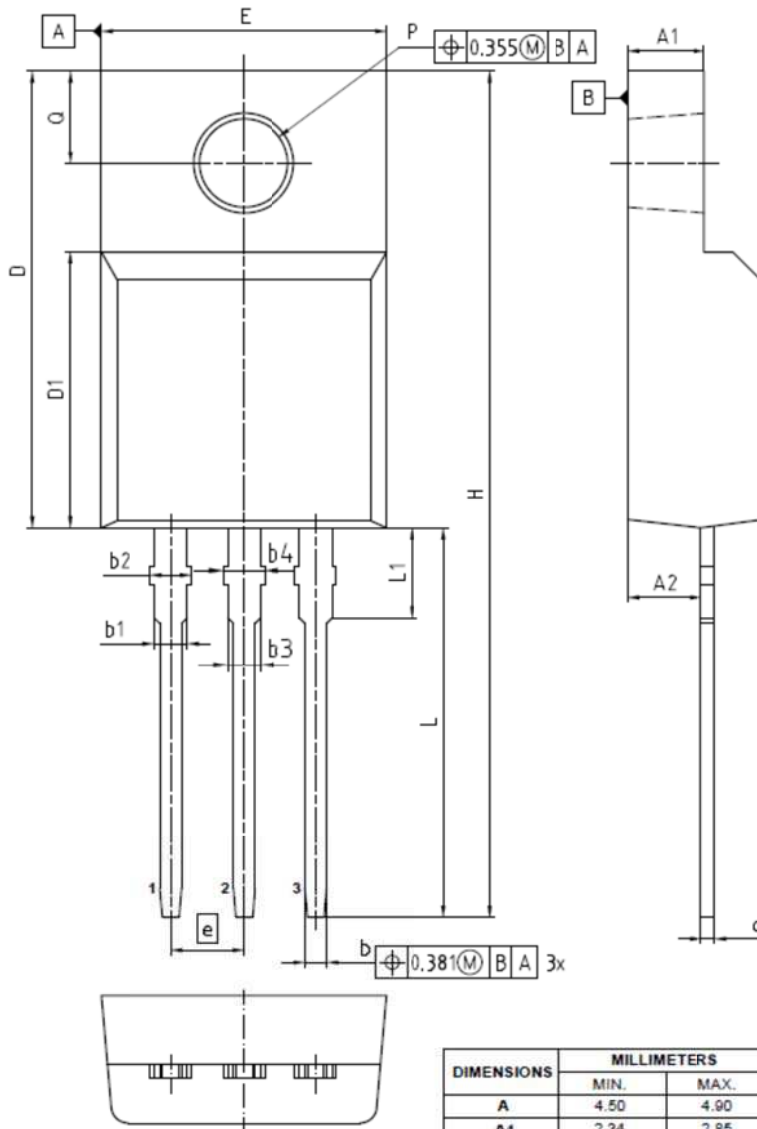
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Z8B00003318

SCALE

EUROPEAN PROJECTION

ISSUE DATE  
23-08-2007

REVISION  
05



NOTES:  
ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281  
AND DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS  
OR GATE BURRS  
GATE BURRS ARE LESS THAN 0.5 nm

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.85
A2	2.42	2.88
b	0.85	0.90
b1	0.95	1.38
b2	0.95	1.51
b3	0.65	1.38
b4	0.65	1.51
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
eP	3.00	3.30
Q	3.15	3.50

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SCALE 5:1 
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ISSUE DATE 27.01.2017

# 800V CoolMOS™ C3 Power Transistor

## SPA17N80C3

### Revision History

SPA17N80C3

**Revision: 2017-07-27, Rev. 2.8**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.8	2017-07-27	Revised package drawing on page 12

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