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# 74LCX540

## Low Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

### Features

- 5V tolerant input and outputs
- 2.3V–3.6V  $V_{CC}$  specifications provided
- 6.5ns  $t_{PD}$  max. ( $V_{CC} = 3.3V$ ), 10 $\mu$ A  $I_{CC}$  max.
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal<sup>(1)</sup>
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds JEDEC 78 conditions
- ESD performance
  - Human body model > 2000V
  - Machine model > 200V
- Leadless DQFN package

### Note:

1. To ensure the high impedance state during power up or down, OE should be tied to  $V_{CC}$  through a pull-up resistor: the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### General Description

The LCX540 is an octal buffer/line driver designed to be employed as a memory and address driver, clock driver and bus oriented transmitter/receiver.

This device is similar in function to the LCX240 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

The LCX540 is designed for low voltage (2.5V or 3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment. The LCX540 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.


### Ordering Information

Order Number	Package Number	Package Description
74LCX540WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX540SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX540BQX <sup>(2)</sup>	MLP20B	20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74LCX540MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LCX540MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

### Note:

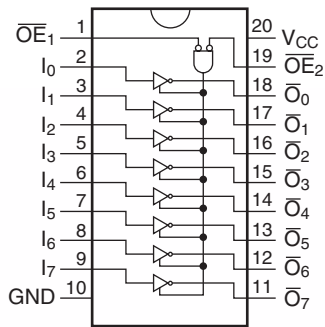
2. DQFN package available in Tape and Reel only.

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

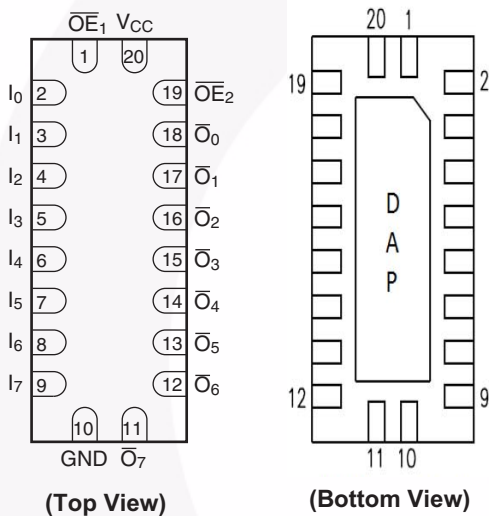
 All packages are lead free per JEDEC: J-STD-020B standard.

## Connection Diagrams

**Pin Assignments for SOIC, SOP, SSOP, TSSOP**



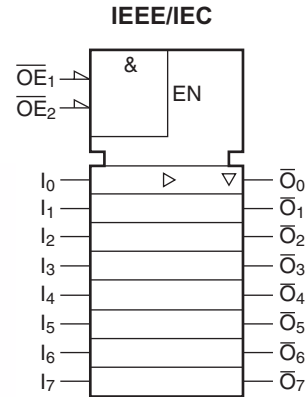
**Pad Assignment for DQFN**



(Top View)

(Bottom View)

## Logic Symbol



## Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	$\overline{O}_n$
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

## Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$\overline{O}_0-\overline{O}_7$	Outputs
DAP	No Connect

Note: DAP (Die Attach Pad)

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Value	Units
$V_{CC}$	Supply Voltage		-0.5 to +7.0	V
$V_I$	DC Input Voltage		-0.5 to +7.0	V
$V_O$	DC Output Voltage	Output in 3-STATE	-0.5 to +7.0	V
		Output in HIGH or LOW State <sup>(3)</sup>	-0.5 to $V_{CC} + 0.5$	
$I_{IK}$	DC Input Diode Current	$V_I < GND$	-50	mA
$I_{OK}$	DC Output Diode Current	$V_O < GND$	-50	mA
		$V_O > V_{CC}$	+50	
$I_O$	DC Output Source/Sink Current		±50	mA
$I_{CC}$	DC Supply Current per Supply Pin		±100	mA
$I_{GND}$	DC Ground Current per Ground Pin		±100	mA
$T_{STG}$	Storage Temperature		-65 to +150	°C

## Recommended Operating Conditions<sup>(4)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Conditions	Min.	Max.	Units
$V_{CC}$	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
$V_I$	Input Voltage		0	5.5	V
$V_O$	Output Voltage	HIGH or LOW State	0	$V_{CC}$	V
		3-STATE	0	5.5	
$I_{OH}/I_{OL}$	Output Current	$V_{CC} = 3.0V - 3.6V$		±24	mA
		$V_{CC} = 2.7V - 3.0V$		±12	
		$V_{CC} = 2.3V - 2.7V$		±8	
$T_A$	Free-Air Operating Temperature		-40	85	°C
$\Delta t/\Delta V$	Input Edge Rate	$V_{IN} = 0.8V - 2.0V, V_{CC} = 3.0V$	0	10	ns/V

### Notes:

- $I_O$  Absolute Maximum Rating must be observed.
- Unused inputs or I/O's must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Max.	
V <sub>IH</sub>	HIGH Level Input Voltage	2.3–2.7		1.7		V
		2.7–3.6		2.0		
V <sub>IL</sub>	LOW Level Input Voltage	2.3–2.7			0.7	V
		2.7–3.6			0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.3–3.6	I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2		V
		2.3	I <sub>OH</sub> = -8mA	1.8		
		2.7	I <sub>OH</sub> = -12mA	2.2		
		3.0	I <sub>OH</sub> = -18mA	2.4		
			I <sub>OH</sub> = -24mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.3–3.6	I <sub>OL</sub> = 100μA		0.2	V
		2.3	I <sub>OL</sub> = 8mA		0.6	
		2.7	I <sub>OL</sub> = 12mA		0.4	
		3.0	I <sub>OL</sub> = 16mA		0.4	
			I <sub>OL</sub> = 24mA		0.55	
I <sub>I</sub>	Input Leakage Current	2.3–3.6	0 ≤ V <sub>I</sub> ≤ 5.5V		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Voltage	2.3–3.6	0 ≤ V <sub>O</sub> ≤ 5.5V, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	0	V <sub>I</sub> or V <sub>O</sub> = 5.5V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.3–3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		10	μA
			3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V <sup>(5)</sup>		±10	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3–3.6	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		500	μA

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V, C <sub>L</sub> = 50pF		V <sub>CC</sub> = 2.7V, C <sub>L</sub> = 50pF		V <sub>CC</sub> = 2.5V ± 0.2V, C <sub>L</sub> = 30pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	1.5	6.5	1.5	7.5	1.5	7.8	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	1.5	7.5	1.5	8.5	1.5	9.0	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew <sup>(6)</sup>		1.0					ns

## Notes:

- Outputs disabled or 3-STATE only.
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

**Dynamic Switching Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C	
				Typical	Units
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	0.8	V
		2.5	C <sub>L</sub> = 30pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	0.6	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	-0.8	V
		2.5	C <sub>L</sub> = 30pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	-0.6	

**Capacitance**

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz	25	pF

### AC Loading and Waveforms (Generic for LCX Family)

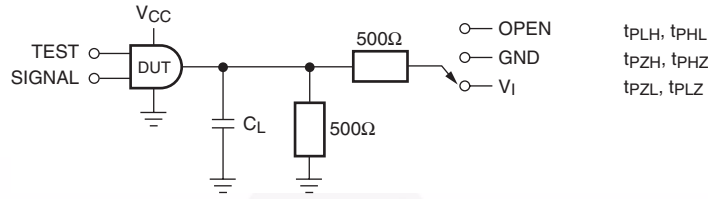
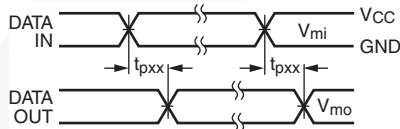
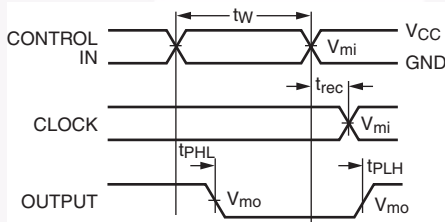


Figure 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)

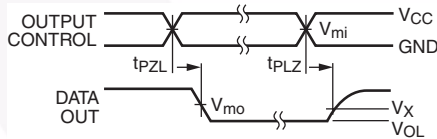
Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}$ , $t_{PHZ}$	GND



Waveform for Inverting and Non-Inverting Functions

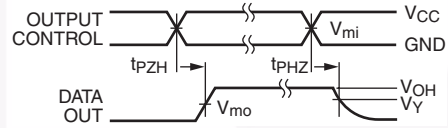


Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms

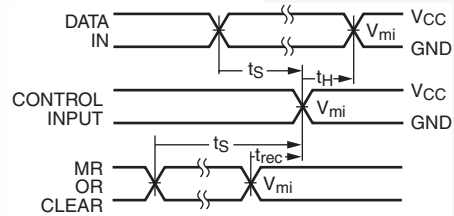


3-STATE Output Low Enable and Disable Times for Logic

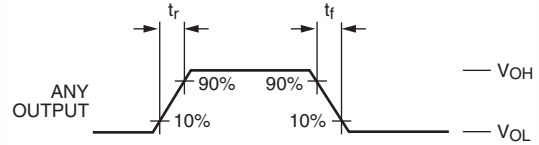
### 3-STATE Output High Enable and



### Disable Times for Logic



### Setup Time, Hold Time and Recovery Time for Logic

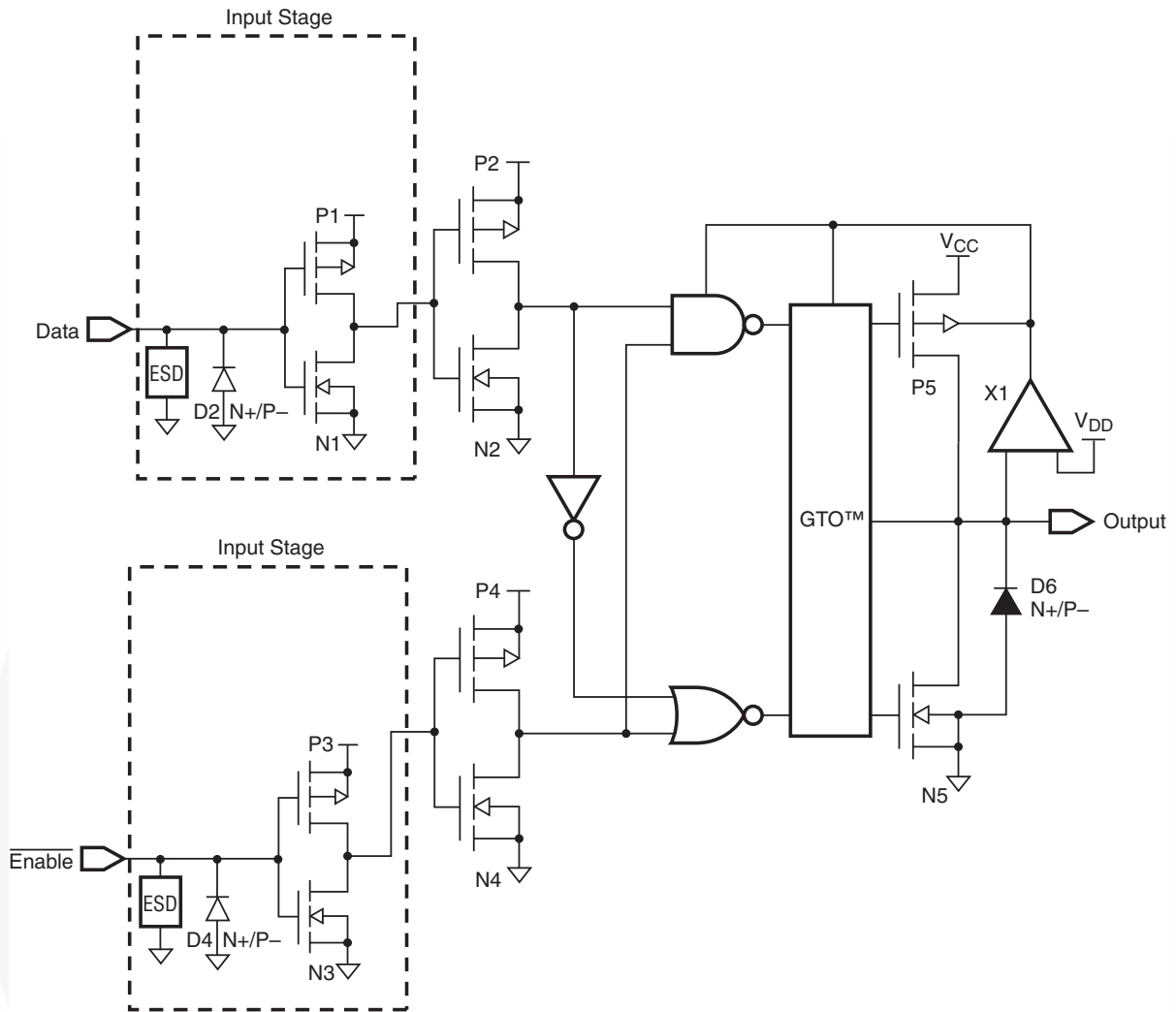


$t_{rise}$  and  $t_{fall}$

Figure 2. Waveforms (Input Characteristics;  $f = 1MHz$ ,  $t_r = t_f = 3ns$ )

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC} / 2$
$V_{mo}$	1.5V	1.5V	$V_{CC} / 2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

**Schematic Diagram** (Generic for LCX Family)

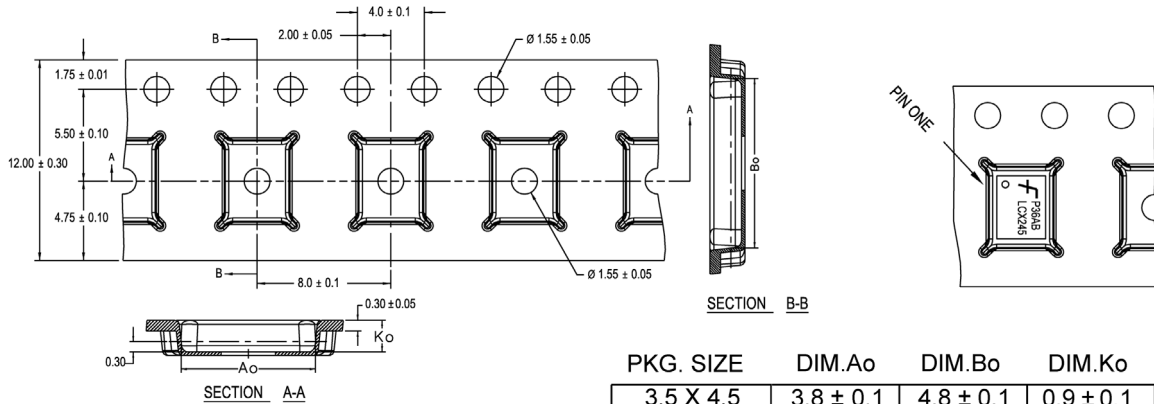


## Tape and Reel Specification

### Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

### Tape Dimensions inches (millimeters)



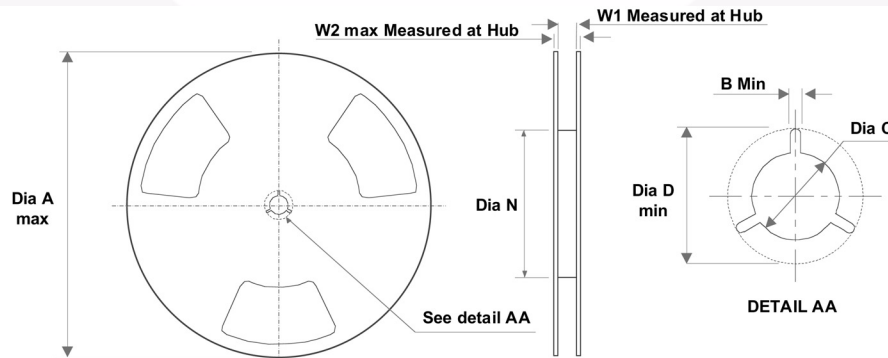
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

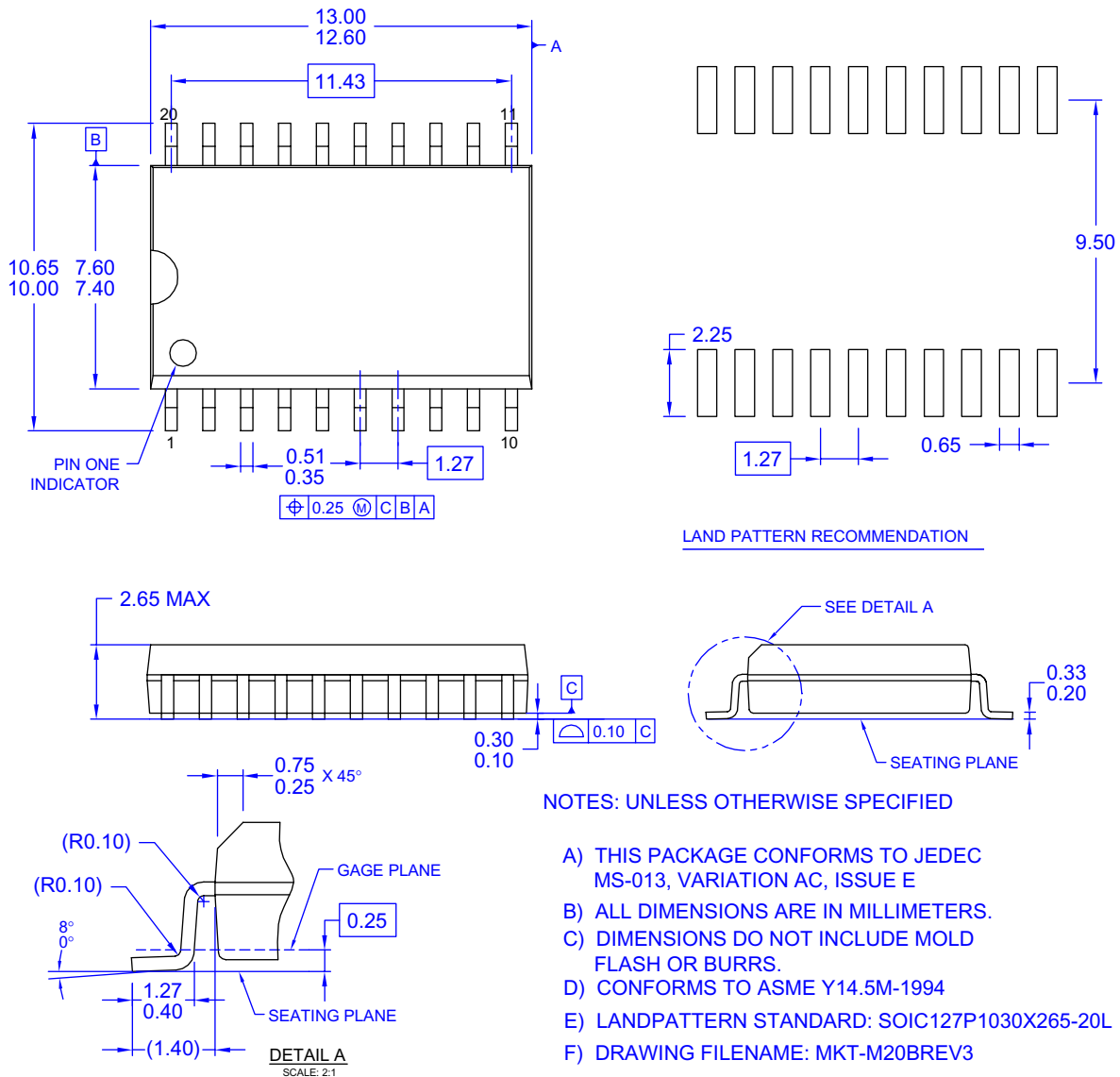
1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is  $\pm 0.002[0.05]$  for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

### Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)

### Physical Dimensions



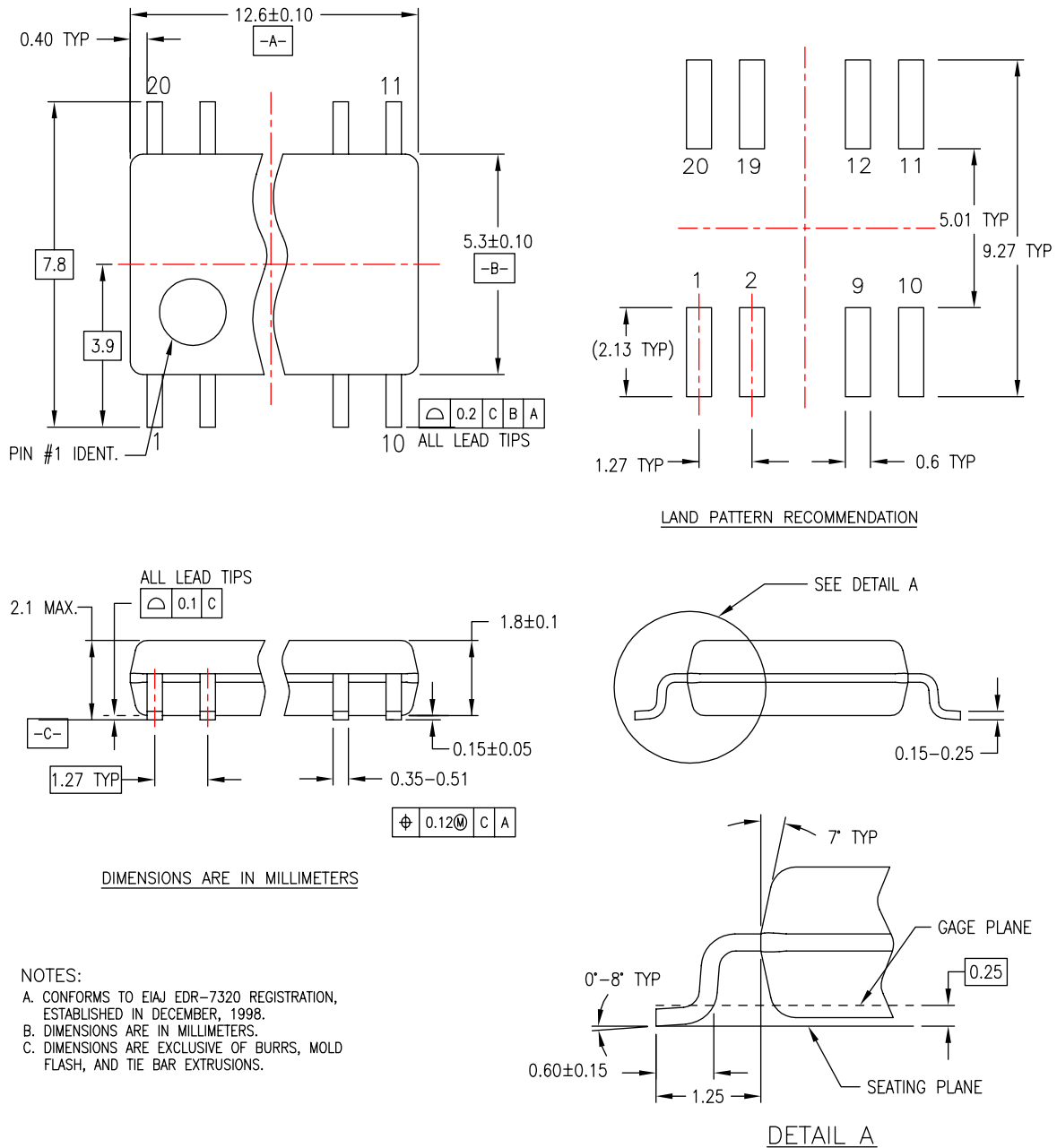
**Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Physical Dimensions (Continued)



- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

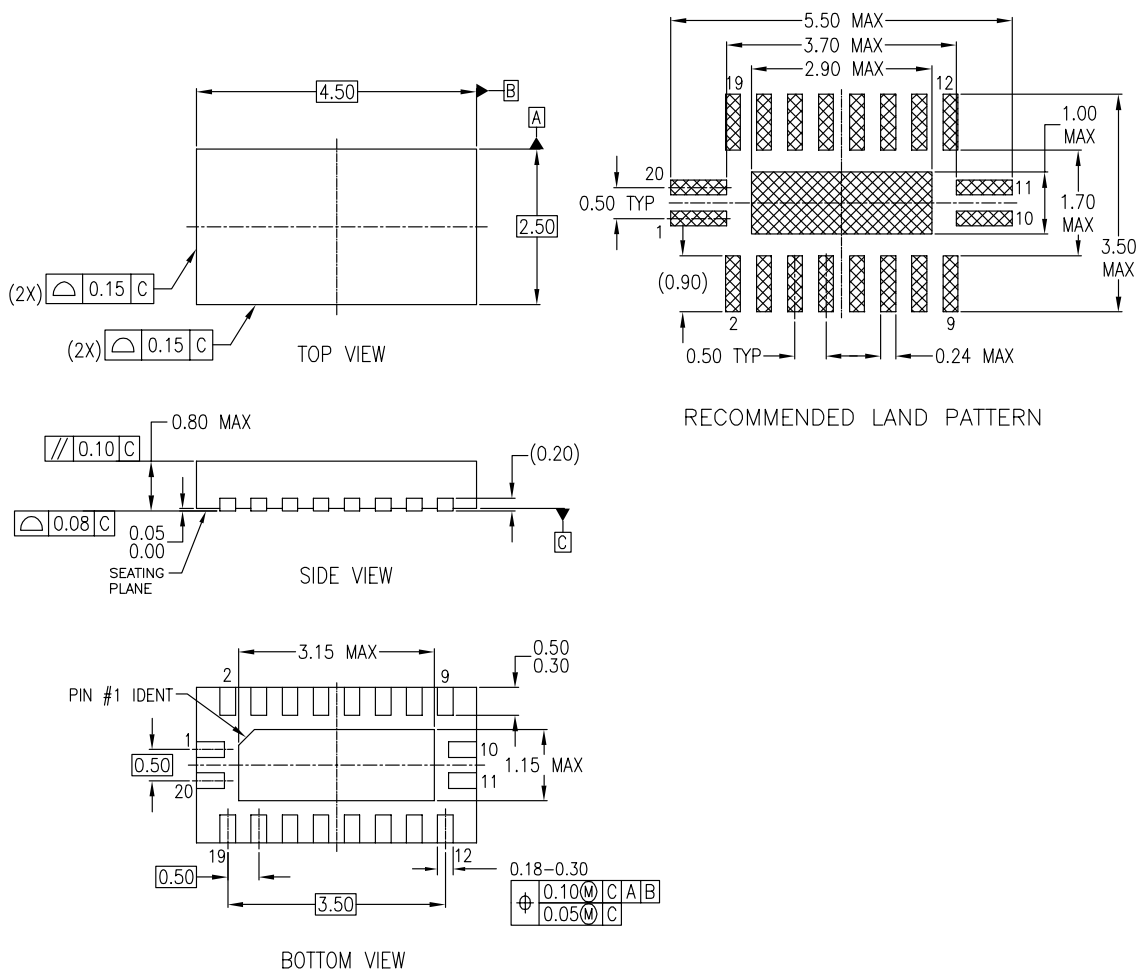
Figure 4. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AC
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP20BrevA

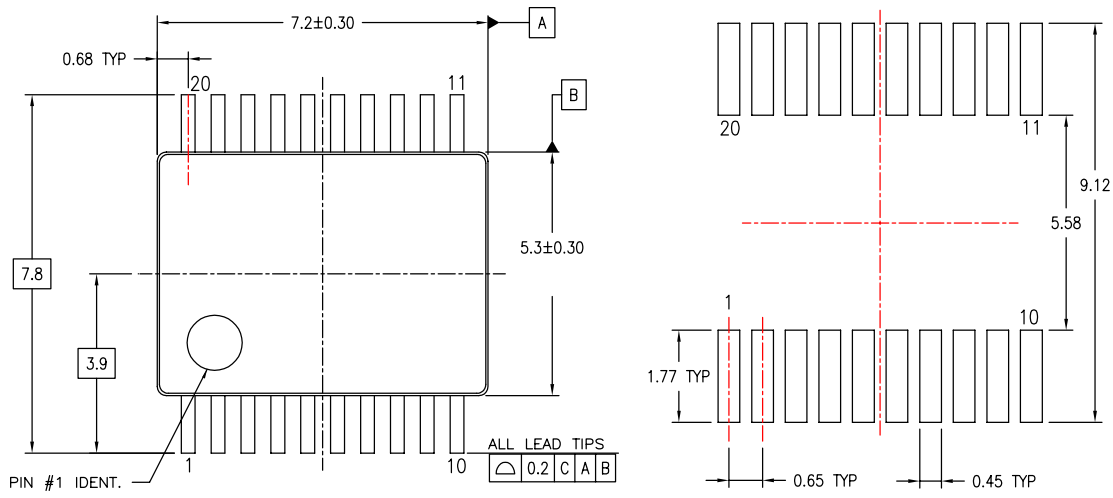
Figure 5. 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm

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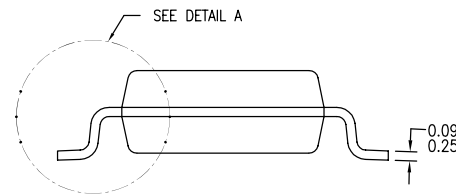
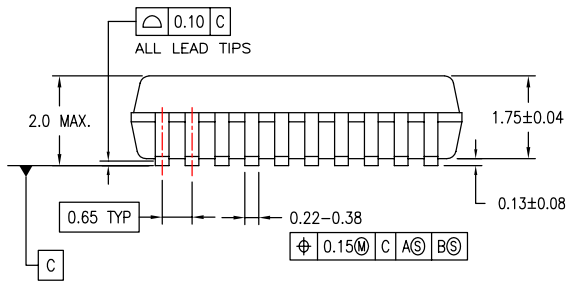
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**Physical Dimensions (Continued)**



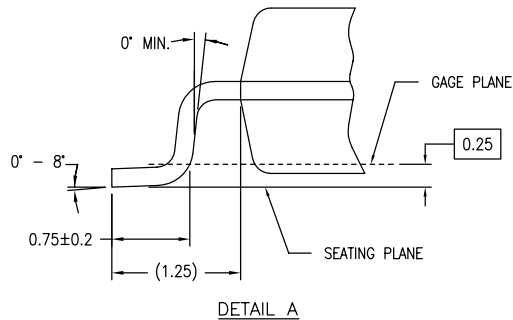
**LAND PATTERN RECOMMENDATIONS**



DIMENSIONS ARE IN MILLIMETERS

**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-150, VARIATION AE, DATE 1/94.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M - 1994.



MSA20REVB

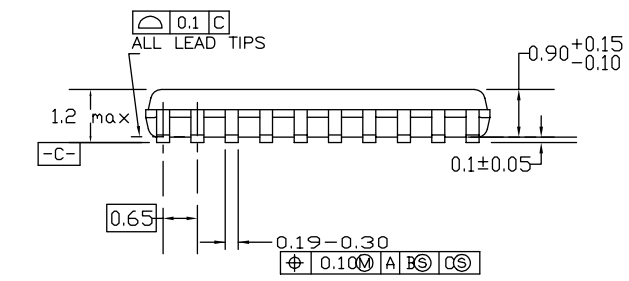
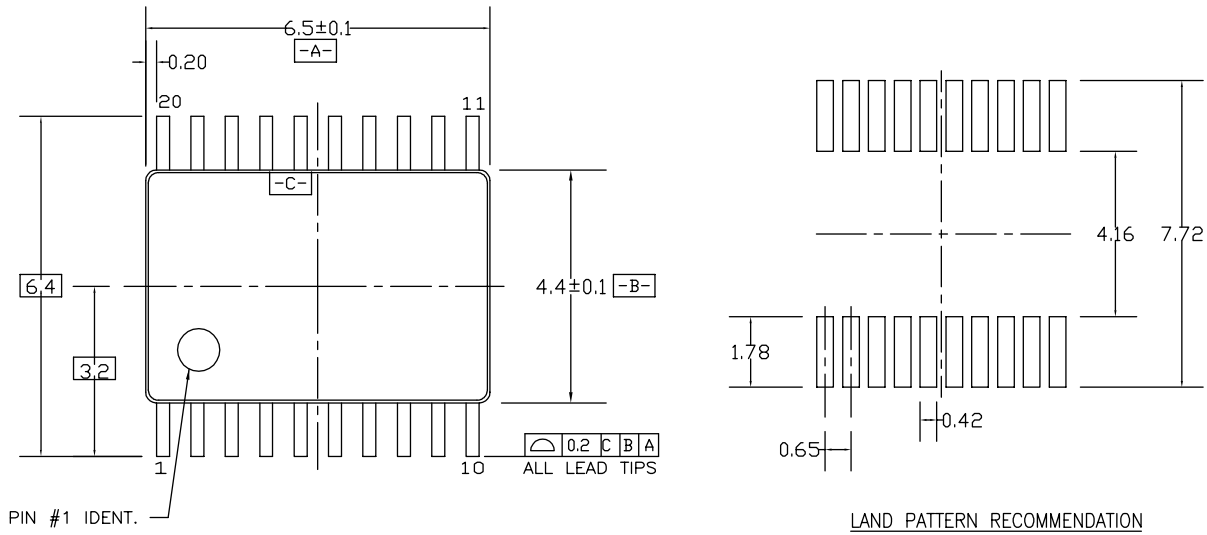
**Figure 6. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide**

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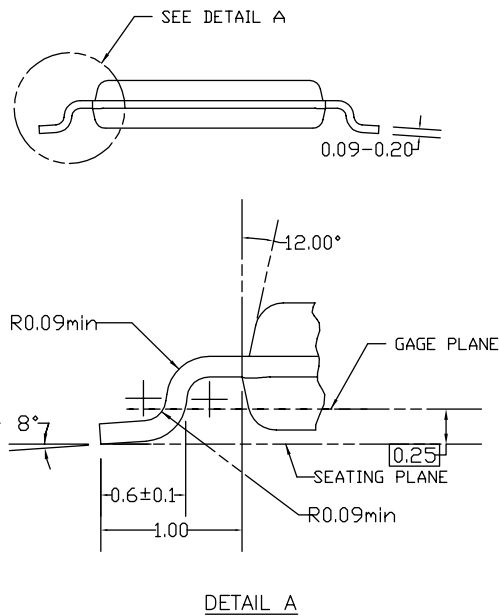
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Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

Figure 7. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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