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## 74LCXZ16244

### Low Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

#### General Description

The LCXZ16244 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

When  $V_{CC}$  is between 0 and 1.5V, the LCXZ16244 is in the high impedance state during power up or power down. This places the outputs in high impedance (Z) state preventing intermittent low impedance loading or glitching in bus oriented applications.

The LCXZ16244 is designed for low voltage (2.7V or 3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

The LCXZ16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### Features

- 5V tolerant inputs and outputs
- Guaranteed power up/down high impedance
- Supports live insertion/withdrawal
- 2.7V–3.6V  $V_{CC}$  specifications provided
- 4.5 ns  $t_{PD}$  max ( $V_{CC} = 3.0V$ ), 20  $\mu A$   $I_{CC}$  max
- $\pm 24$  mA output drive ( $V_{CC} = 3.0V$ )
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

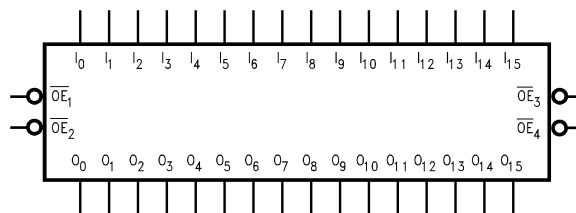
#### Ordering Code:

Order Number	Package Number	Package Description
74LCXZ16244GX (Note 1)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74LCXZ16244MEA (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCXZ16244MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

**Note 1:** BGA package available in Tape and Reel only.

**Note 2:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

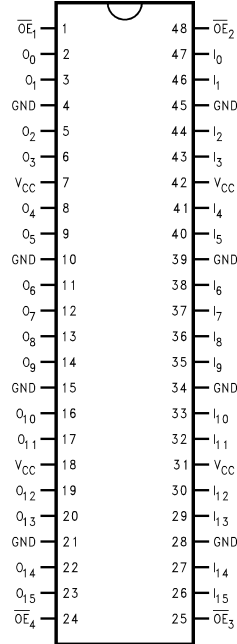
#### Logic Symbol



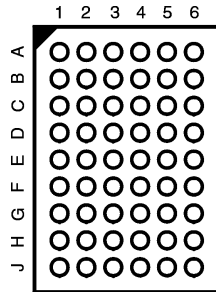
74LCXZ16244 Low Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

### Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$I_0$ - $I_{15}$	Inputs
$O_0$ - $O_{15}$	Outputs
NC	No Connect

### FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	$O_0$	NC	$\overline{OE}_1$	$\overline{OE}_2$	NC	$I_0$
<b>B</b>	$O_2$	$O_1$	NC	NC	$I_1$	$I_2$
<b>C</b>	$O_4$	$O_3$	$V_{CC}$	$V_{CC}$	$I_3$	$I_4$
<b>D</b>	$O_6$	$O_5$	GND	GND	$I_5$	$I_6$
<b>E</b>	$O_8$	$O_7$	GND	GND	$I_7$	$I_8$
<b>F</b>	$O_{10}$	$O_9$	GND	GND	$I_9$	$I_{10}$
<b>G</b>	$O_{12}$	$O_{11}$	$V_{CC}$	$V_{CC}$	$I_{11}$	$I_{12}$
<b>H</b>	$O_{14}$	$O_{13}$	NC	NC	$I_{13}$	$I_{14}$
<b>J</b>	$O_{15}$	NC	$\overline{OE}_4$	$\overline{OE}_3$	NC	$I_{15}$

### Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_0$ - $I_3$	$O_0$ - $O_3$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	$I_4$ - $I_7$	$O_4$ - $O_7$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	$I_8$ - $I_{11}$	$O_8$ - $O_{11}$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}$ - $I_{15}$	$O_{12}$ - $O_{15}$
L	L	L
L	H	H
H	X	Z

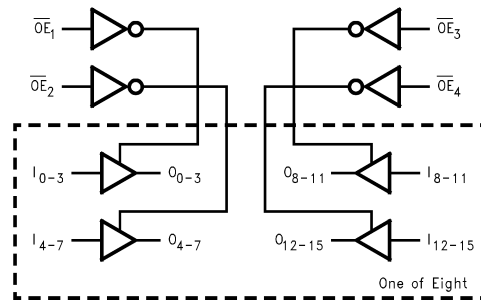
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

## Functional Description

The LCXZ16244 contains sixteen non-inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The

3-STATE outputs are controlled by an Output Enable ( $\overline{OE}_n$ ) input for each nibble. When  $\overline{OE}_n$  is LOW, the outputs are in 2-state mode. When  $\overline{OE}_n$  is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

## Logic Diagram



Absolute Maximum Ratings (Note 3)						
Symbol	Parameter	Value	Conditions	Units		
V <sub>CC</sub>	Supply Voltage	-0.5 to +7.0		V		
V <sub>I</sub>	DC Input Voltage	-0.5 to +7.0		V		
V <sub>O</sub>	DC Output Voltage	-0.5 to +7.0 -0.5 to V <sub>CC</sub> + 0.5	Output in 3-STATE or V <sub>CC</sub> = 0-1.5V Output in HIGH or LOW State (Note 4)	V		
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA		
I <sub>OK</sub>	DC Output Diode Current	-50 +50	V <sub>O</sub> < GND V <sub>O</sub> > V <sub>CC</sub>	mA		
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA		
I <sub>CC</sub>	DC Supply Current per Supply Pin	±100		mA		
I <sub>GND</sub>	DC Ground Current per Ground Pin	±100		mA		
T <sub>STG</sub>	Storage Temperature	-65 to +150		°C		
Recommended Operating Conditions (Note 5)						
Symbol	Parameter	Min	Max	Units		
V <sub>CC</sub>	Supply Voltage	Operating	2.7	3.6	V	
V <sub>I</sub>	Input Voltage	0	5.5	V		
V <sub>O</sub>	Output Voltage	HIGH or LOW State 3-STATE or V <sub>CC</sub> = OFF	0 0	V <sub>CC</sub> 5.5	V	
I <sub>OH</sub> /I <sub>OL</sub>	Output Current	V <sub>CC</sub> = 3.0V - 3.6V V <sub>CC</sub> = 2.7V - 3.0V		±24 ±12	mA	
T <sub>A</sub>	Free-Air Operating Temperature	-40	85	°C		
Δt/ΔV	Input Edge Rate, V <sub>IN</sub> = 0.8V-2.0V, V <sub>CC</sub> = 3.0V	0	10	ns/V		
<p><b>Note 3:</b> The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.</p> <p><b>Note 4:</b> I<sub>O</sub> Absolute Maximum Rating must be observed.</p> <p><b>Note 5:</b> Unused inputs must be held HIGH or LOW. They may not float.</p>						
DC Electrical Characteristics						
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units
				Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage		2.7 - 3.6		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA	2.7 - 3.6	V <sub>CC</sub> - 0.2		V
		I <sub>OH</sub> = -12 mA	2.7	2.2		
		I <sub>OH</sub> = -18 mA	3.0	2.4		
		I <sub>OH</sub> = -24 mA	3.0	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.7 - 3.6		0.2	V
		I <sub>OL</sub> = 12 mA	2.7		0.4	
		I <sub>OL</sub> = 16 mA	3.0		0.4	
		I <sub>OL</sub> = 24 mA	3.0		0.55	
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 5.5V	2.7 - 3.6		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 5.5V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 - 3.6		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>I</sub> or V <sub>O</sub> = 5.5V	0		10	μA
I <sub>PU/PD</sub>	Power Up/Down 3-STATE Output Current	V <sub>O</sub> = 0.5V to V <sub>CC</sub> V <sub>I</sub> = GND or V <sub>CC</sub>	0 - 1.5		±5.0	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.7 - 3.6		225	μA
		3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V (Note 6)	2.7 - 3.6		±225	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.7 - 3.6		500	μA
<p><b>Note 6:</b> Outputs disabled or 3-STATE only.</p>						

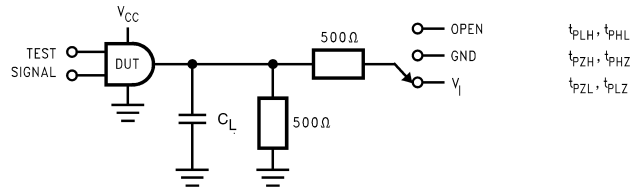
AC Electrical Characteristics						
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, R_L = 500 \Omega$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		$C_L = 50 \text{ pF}$				
		Min	Max	Min	Max	
$t_{PHL}$	Propagation Delay	1.0	4.5	1.0	5.2	ns
$t_{PLH}$	Data to Output	1.0	4.5	1.0	5.2	
$t_{PZL}$	Output Enable Time	1.0	5.5	1.0	6.3	ns
$t_{PZH}$		1.0	5.5	1.0	6.3	
$t_{PLZ}$	Output Disable Time	1.0	5.4	1.0	5.7	ns
$t_{PHZ}$		1.0	5.4	1.0	5.7	
$t_{OSHL}$	Output to Output Skew (Note 7)		1.0			ns
$t_{OSLH}$			1.0			

**Note 7:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.

Dynamic Switching Characteristics					
Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$	Units
				Typical	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	0.8	V
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	-0.8	V

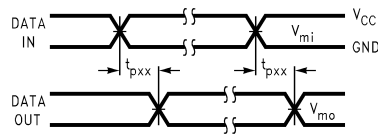
Capacitance				
Symbol	Parameter	Conditions	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0V \text{ or } V_{CC}$	7	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}, f = 10 \text{ MHz}$	20	pF

**AC LOADING and WAVEFORMS** Generic for LCX Family

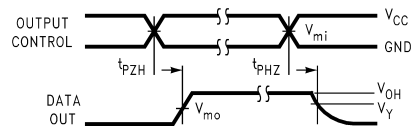


**FIGURE 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)**

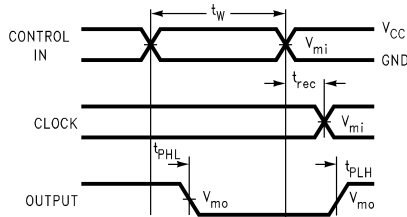
$V_I$	$C_L$
6V for $V_{CC} = 3.3V, 2.7V$	50 pF



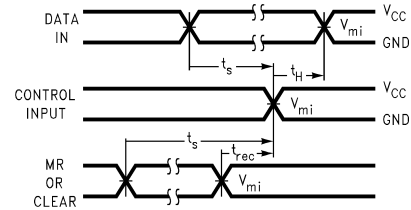
**Waveform for Inverting and Non-Inverting Functions**



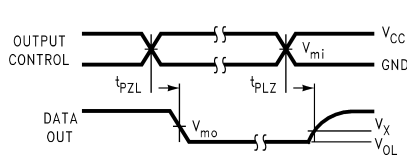
**3-STATE Output High Enable and Disable Times for Logic**



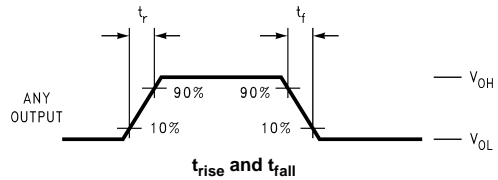
**Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**



**Setup Time, Hold Time and Recovery Time for Logic**



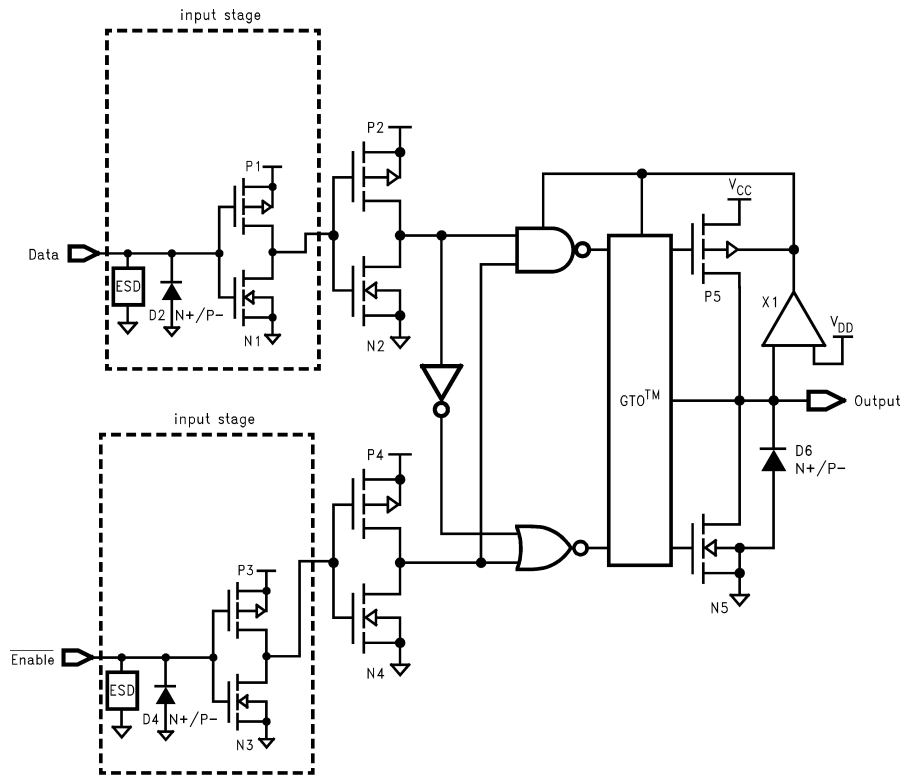
**3-STATE Output Low Enable and Disable Times for Logic**



**FIGURE 2. Waveforms**  
(Input Characteristics;  $f = 1 \text{ MHz}, t_r = t_f = 3 \text{ ns}$ )

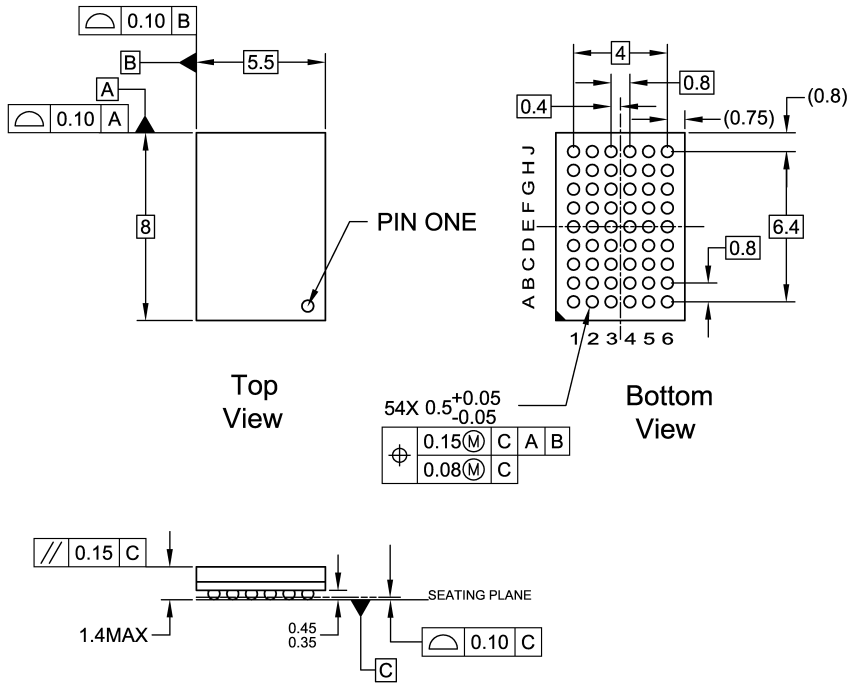
Symbol	$V_{CC}$	
	$3.3V \pm 0.3V$	$2.7V$
$V_{mi}$	1.5V	1.5V
$V_{mo}$	1.5V	1.5V
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$

**Schematic Diagram** Generic for LCX Family



74LCXZ16244

**Physical Dimensions** inches (millimeters) unless otherwise noted



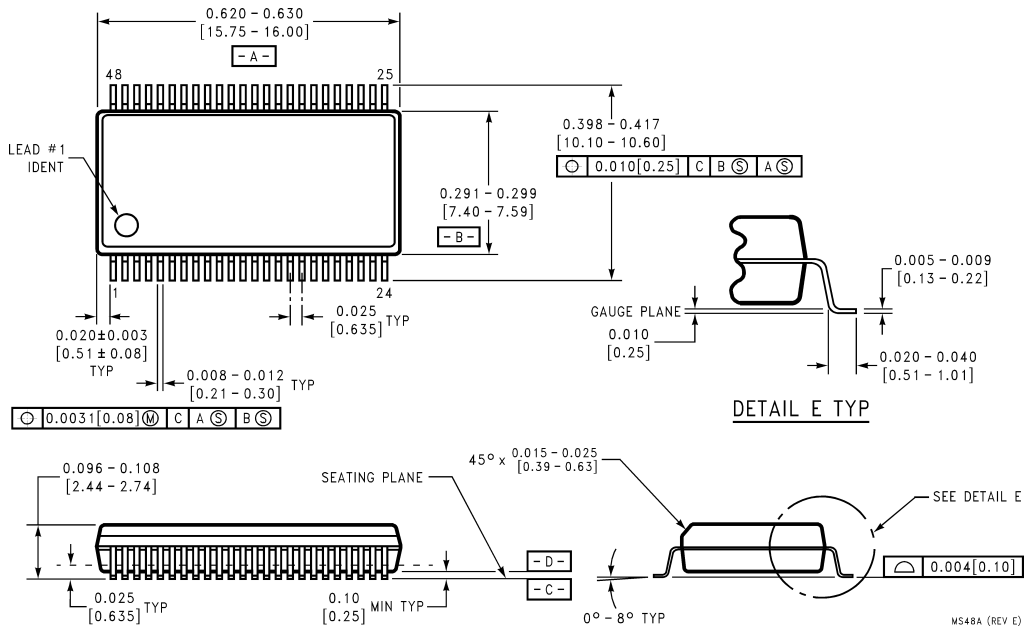
NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

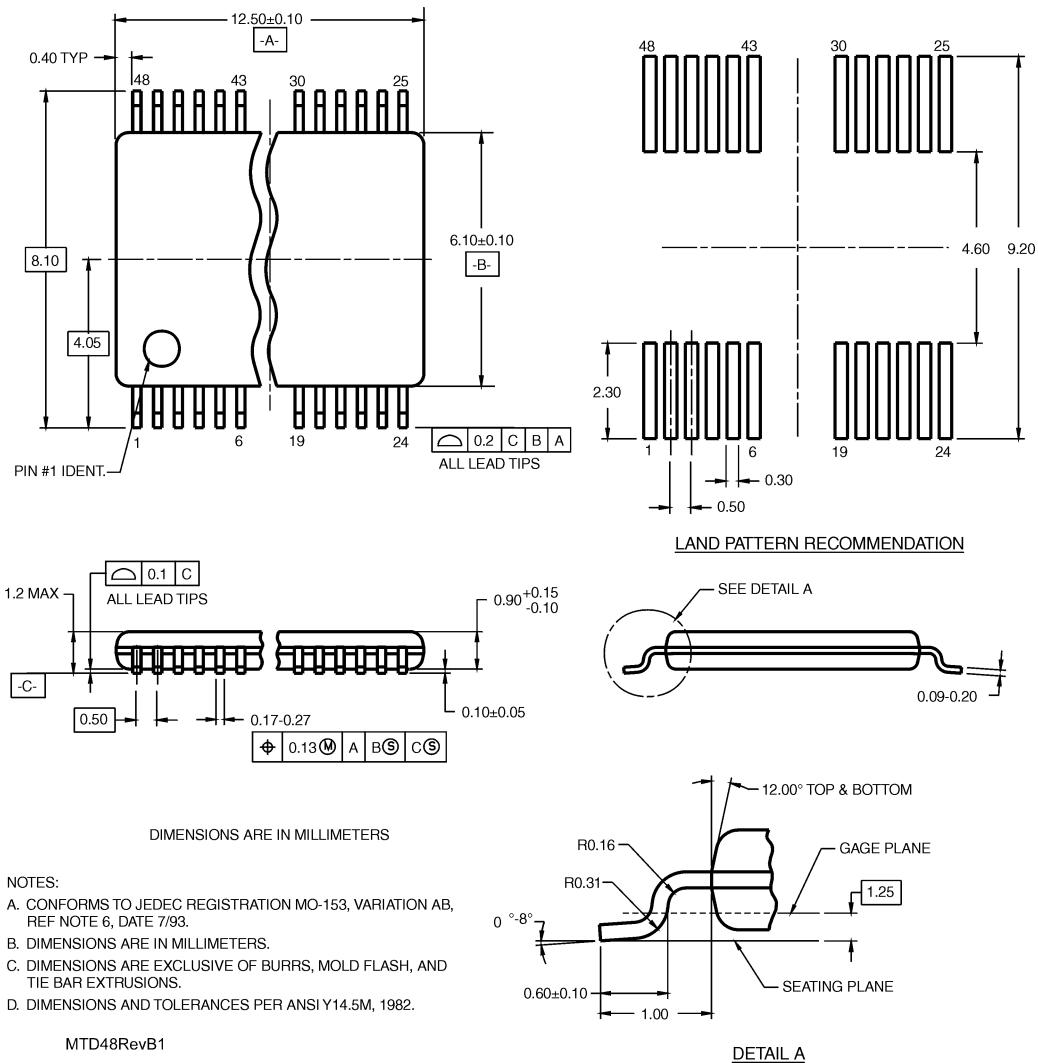
**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide  
Package Number BGA54A  
Preliminary**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



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