



**THE DATASHEET OF
STB14NK60ZT4**



N-channel 600 V, 0.45 Ω typ., 13.5 A SuperMESH™ Power MOSFETs in D²PAK and TO-220FP packages

Datasheet - production data

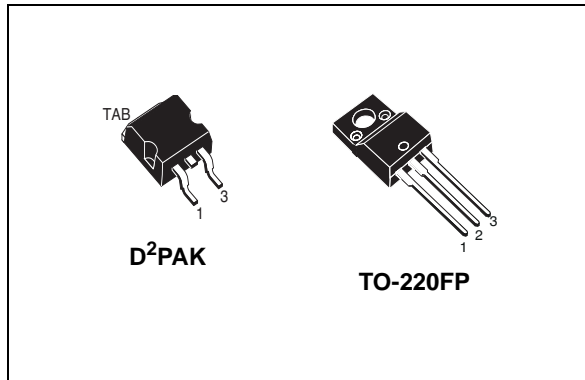
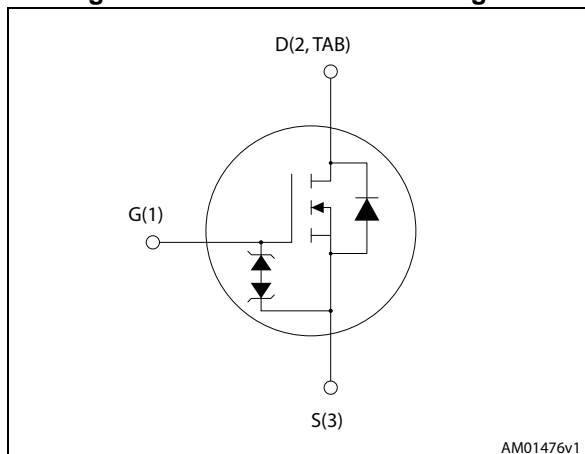


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STB14NK60ZT4	600 V	0.5 Ω	13.5 A	160 W
STP14NK60ZFP				40 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Zener-protected Power MOSFETs developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB14NK60ZT4	B14NK60Z	D ² PAK	Tape and reel
STP14NK60ZFP	P14NK60ZFP	TO-220FP	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK	TO-220FP	
V _{DS}	Drain-source voltage	600		V
V _{DGR}	Drain-gate voltage (R _{GS} = 20 kΩ)	600		V
V _{GS}	Gate-source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25°C	13.5	13.5 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C =100°C	8.5	8.5 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	54	54 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25°C	160	40	W
	Derating factor	1.28	0.32	W/°C
ESD	Gate-source human body model (R= 1.5 kΩ, C= 100pF)	4		kV
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T _C = 25 °C)		2500	V
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

- Limited by maximum junction temperature
- Pulse width limited by safe operating area
- I_{SD} ≤ 13.5A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ T_{JMAX}.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	0.78	3.1	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	62.5	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _{Jmax})	12	A
E _{AS}	Single pulse avalanche energy (starting T _J =25°C, I _D =I _{AR} , V _{dd} =50 V)	300	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600 \text{ V}$			1	μA
		$V_{DS} = 600 \text{ V}, T_C = 125^{\circ}C$			50	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 30 \text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100 \mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}$		0.45	0.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}, f = 1 \text{ MHz}, V_{GS} = 0$	-	2220	-	pF
C_{oss}	Output capacitance		-	240	-	pF
C_{rss}	Reverse transfer capacitance		-	57	-	pF
$C_{oss \text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0 \text{ V to } 480 \text{ V}$	-	122	-	pF
Q_g	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 12 \text{ A}, V_{GS} = 10 \text{ V}$	-	75	-	nC
Q_{gs}	Gate-source charge		-	13.2	-	nC
Q_{gd}	Gate-drain charge		-	38.6	-	nC

1. $C_{oss \text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=300\text{ V}$, $I_D=6\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 17)	-	26	-	ns
t_r	Rise time		-	18	-	ns
$t_{d(off)}$	Turn-off delay time		-	62	-	ns
t_f	Fall time		-	13	-	ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD}=480\text{ V}$, $I_D=12\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 19)	-	12	-	ns
t_f	Fall time		-	9.5	-	ns
t_c	Cross-over time		-	22	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=12\text{ A}$, $V_{GS}=0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD}=12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=50\text{ V}$	-	490		ns
Q_{rr}	Reverse recovery charge		-	4.7		μC
I_{RRM}	Reverse recovery current		-	19.3		A
t_{rr}	Reverse recovery time	$I_{SD}=12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=50\text{ V}$, $T_j=150\text{ }^\circ\text{C}$	-	664		ns
Q_{rr}	Reverse recovery charge		-	6.8		μC
I_{RRM}	Reverse recovery current		-	20.5		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D=0$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK

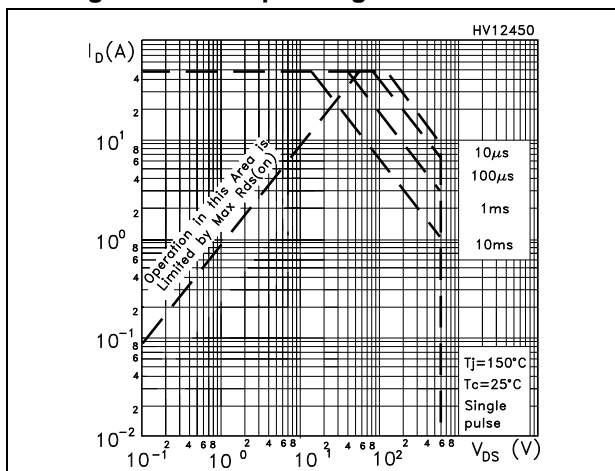


Figure 3. Thermal impedance for D²PAK

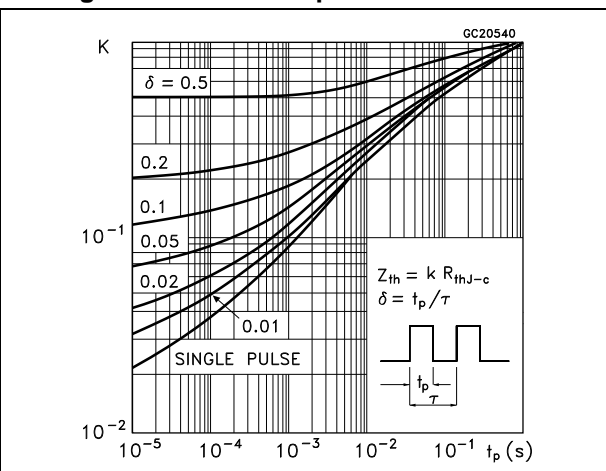


Figure 4. Safe operating area for TO-220FP

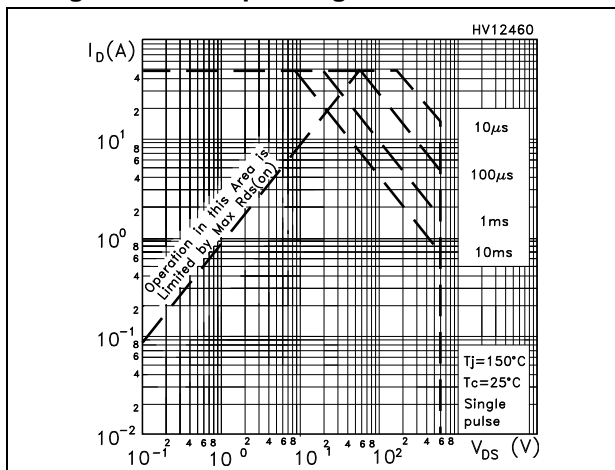


Figure 5. Thermal impedance for TO-220FP

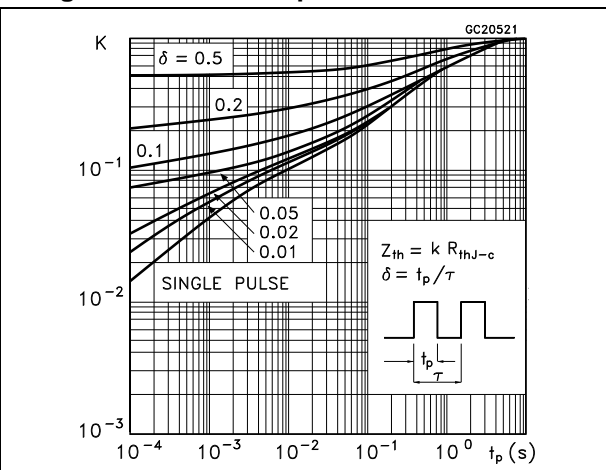


Figure 6. Output characteristics

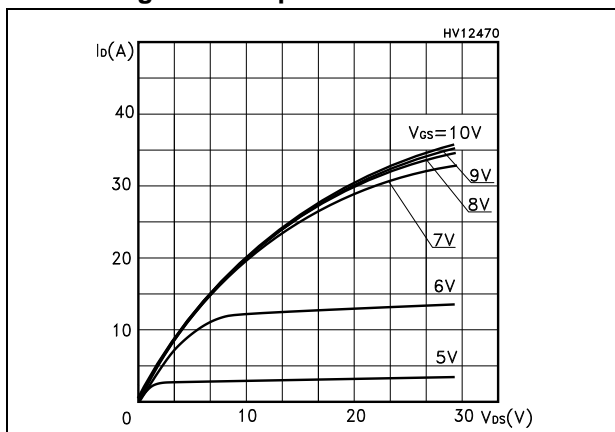


Figure 7. Transfer characteristics

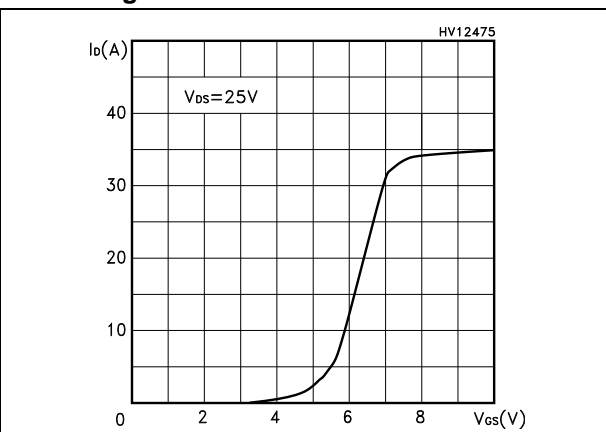


Figure 8. Transconductance

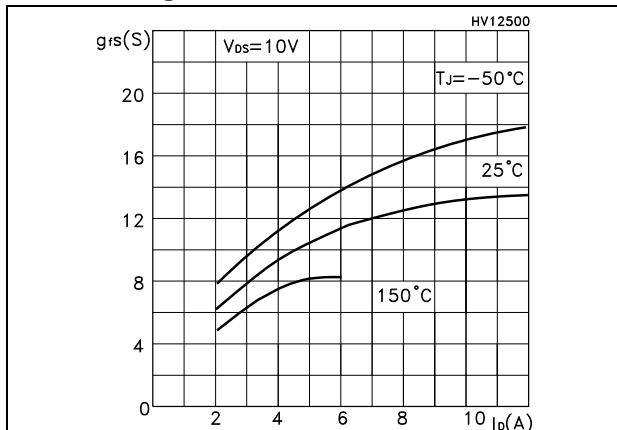


Figure 9. Static drain-source on-resistance

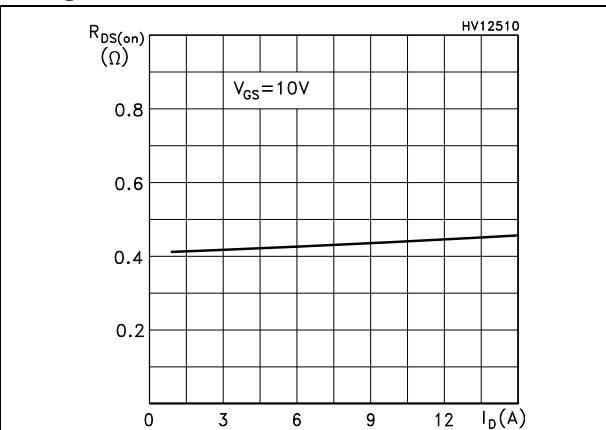


Figure 10. Gate charge vs gate-source voltage

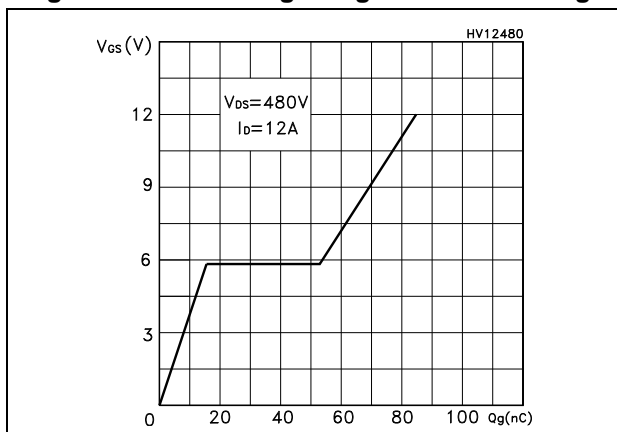


Figure 11. Capacitance variations

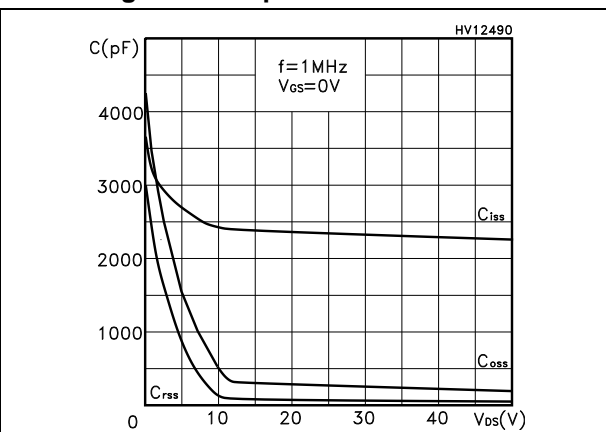


Figure 12. Normalized gate threshold voltage vs temperature

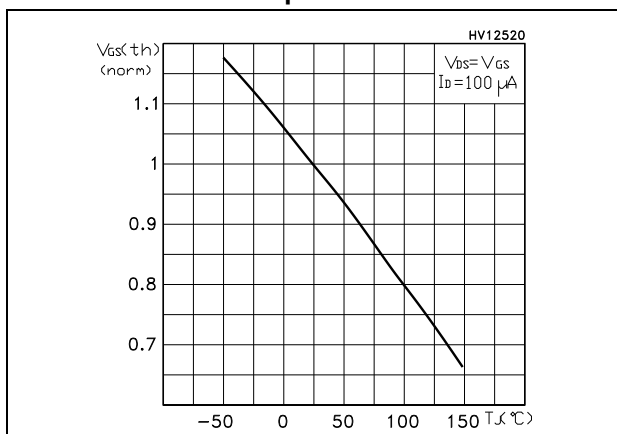


Figure 13. Normalized on-resistance vs temperature

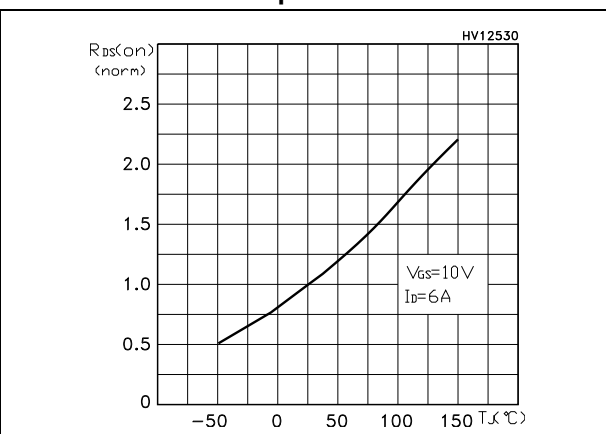


Figure 14. Source-drain diode forward characteristics

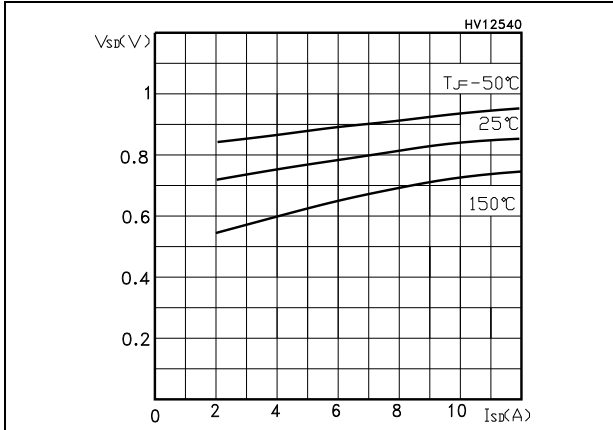


Figure 15. Normalized $V_{(BR)DSS}$ vs temperature

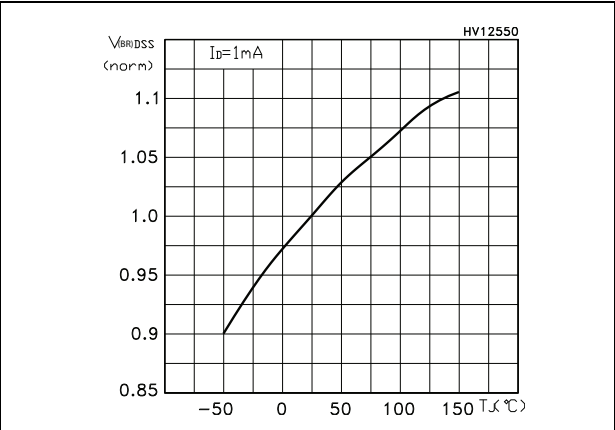
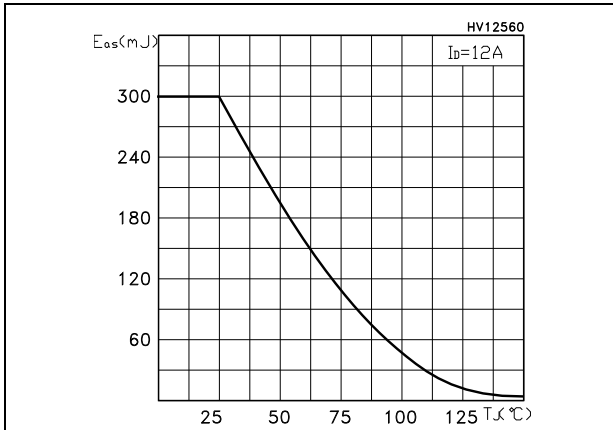
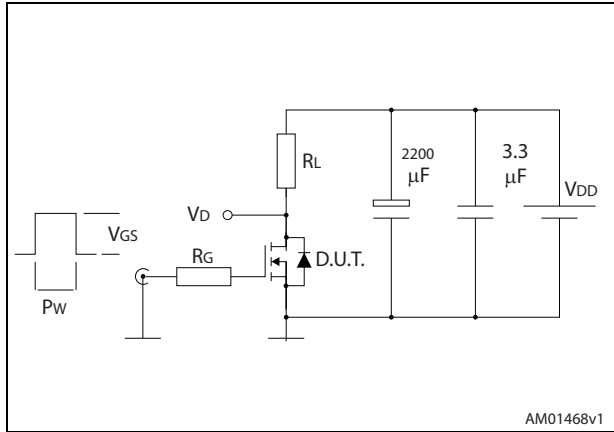


Figure 16. Maximum avalanche energy vs temperature



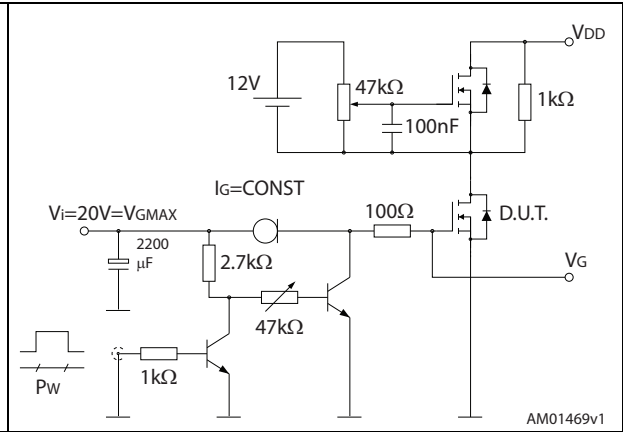
3 Test circuits

Figure 17. Switching times test circuit for resistive load



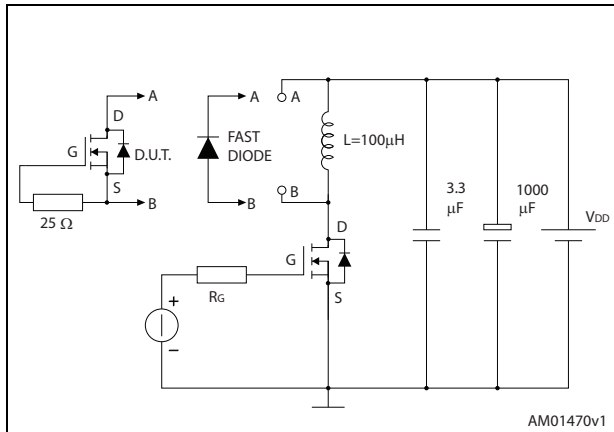
AM01468v1

Figure 18. Gate charge test circuit



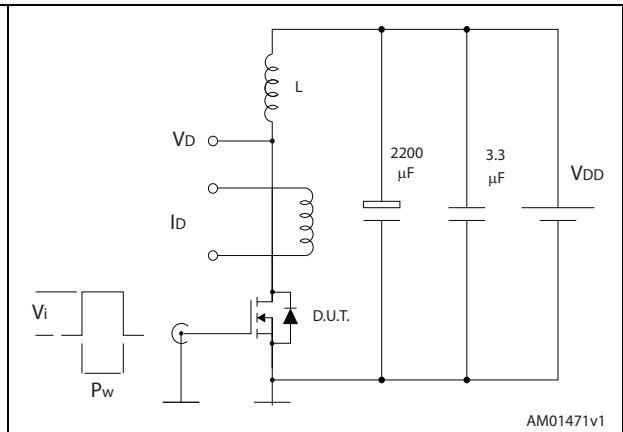
AM01469v1

Figure 19. Test circuit for inductive load switching and diode recovery times



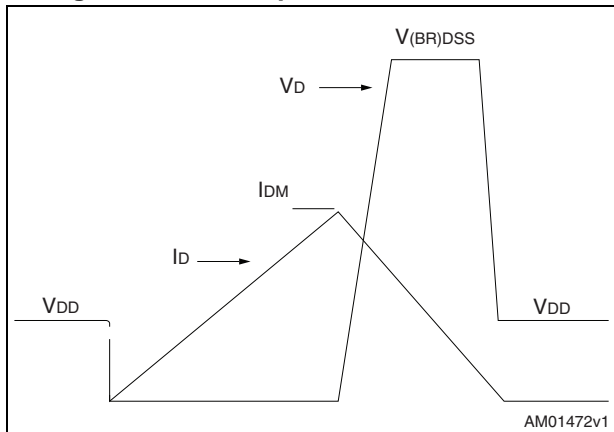
AM01470v1

Figure 20. Unclamped inductive load test circuit



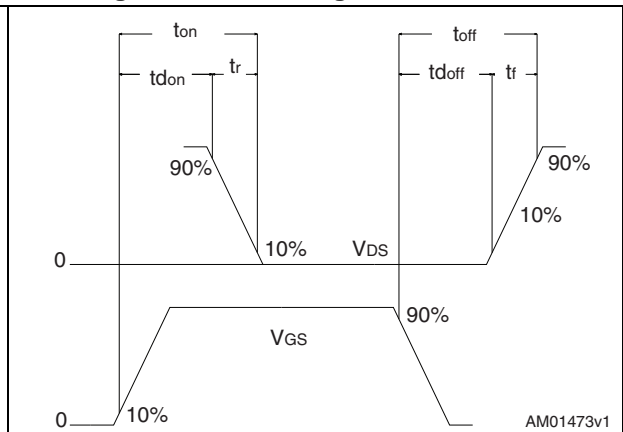
AM01471v1

Figure 21. Unclamped inductive waveform



AM01472v1

Figure 22. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 D²PAK, STB14NK60ZT4

Figure 23. D²PAK (TO-263) drawing

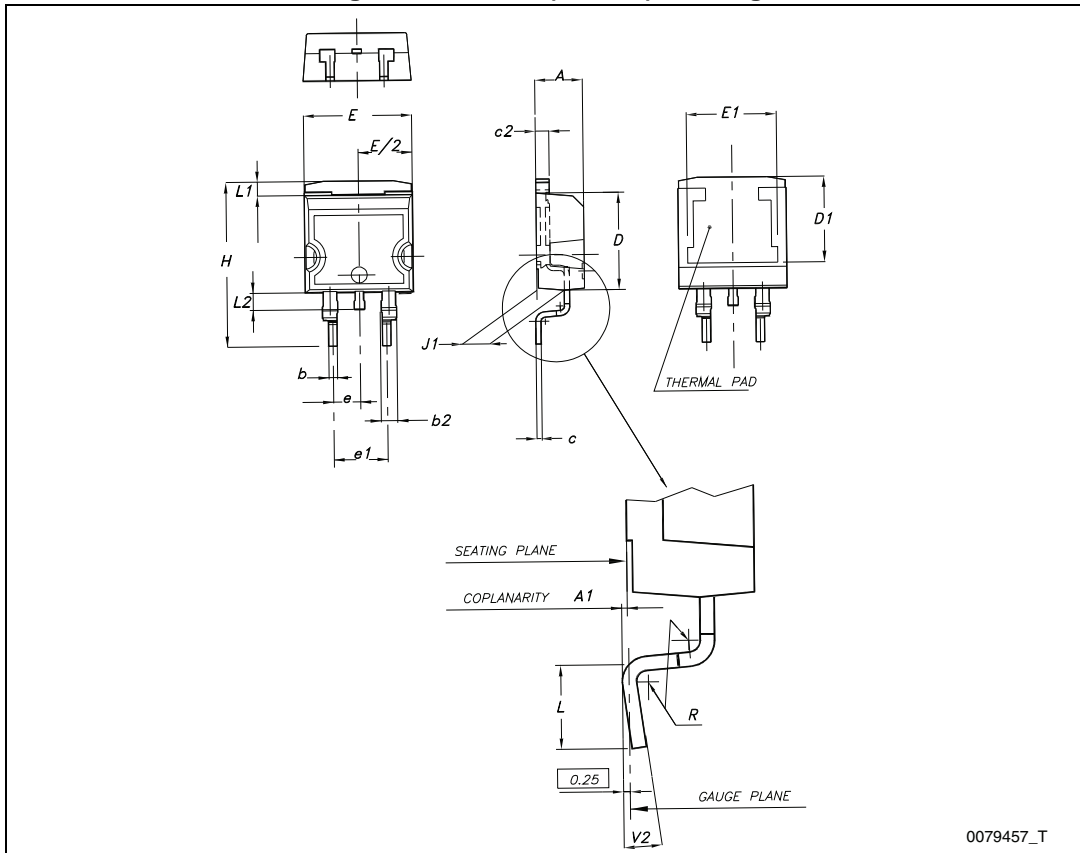
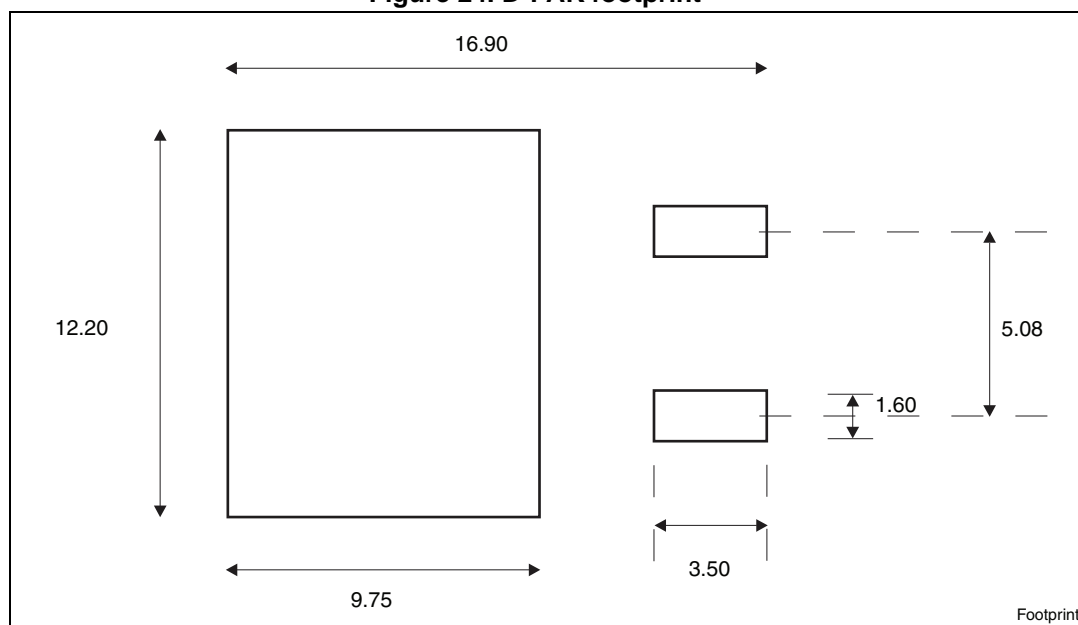


Table 10. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

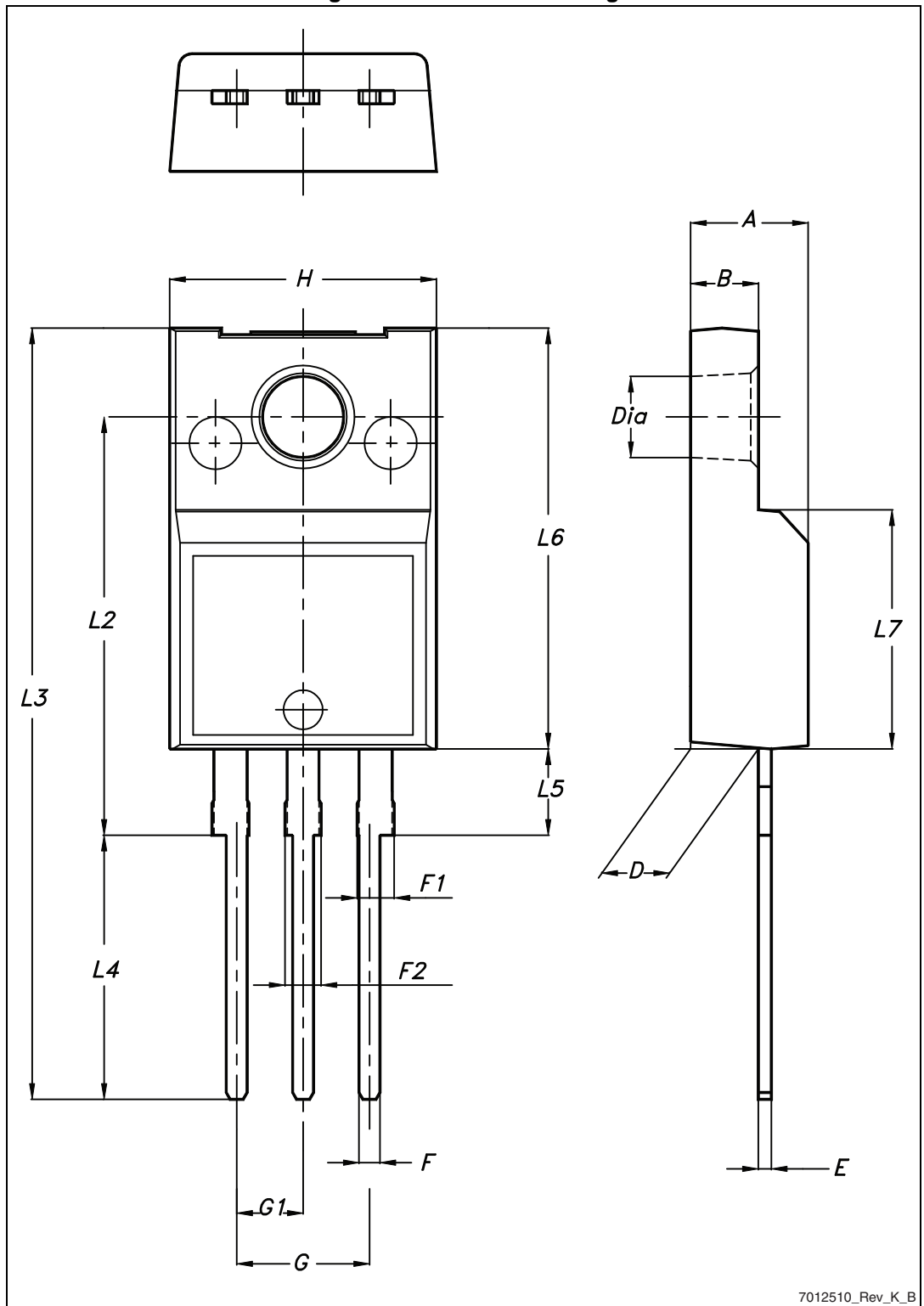
Figure 24. D²PAK footprint^(a)



a. All dimension are in millimeters

4.2 TO-220FP, STP14NK60ZFP

Figure 25. TO-220FP drawing



7012510_Rev_K_B

Table 11. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Ø	3		3.2

5 Packaging mechanical data

Figure 26. Tape

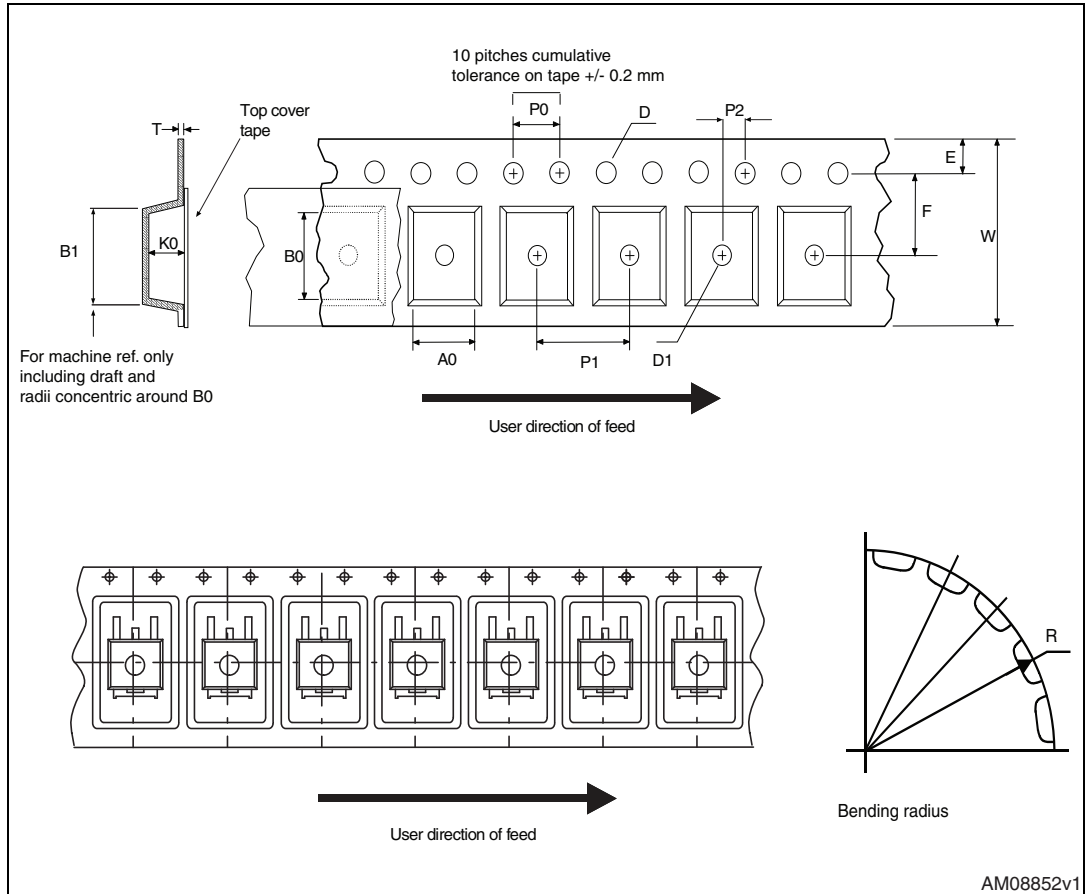


Figure 27. Reel

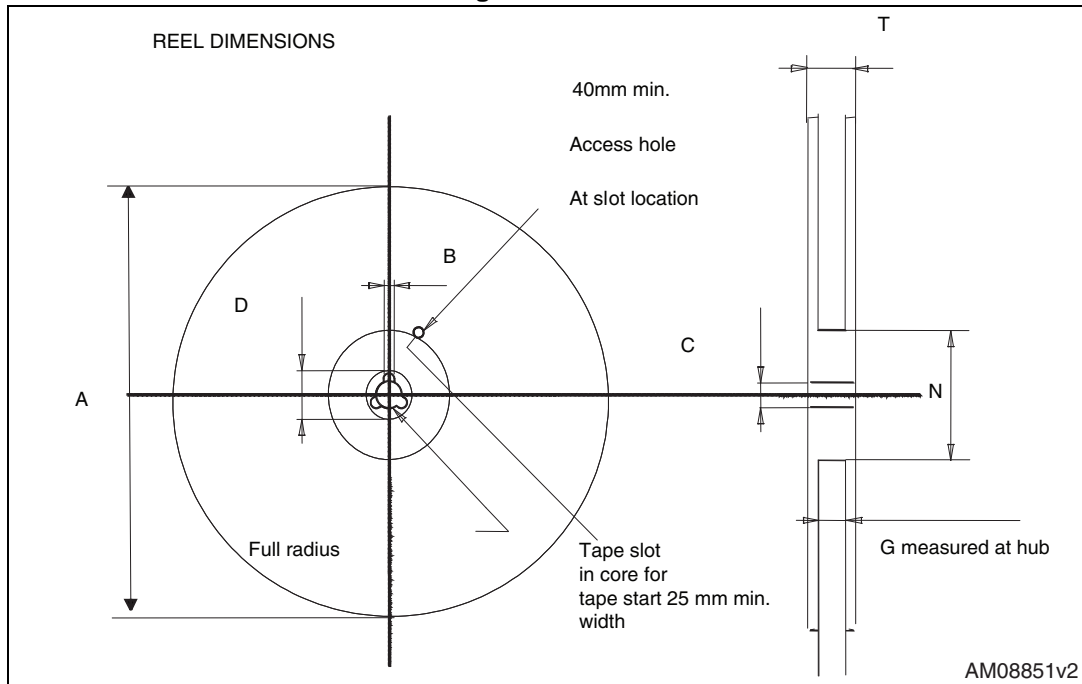


Table 12. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 13. Document revision history

Date	Revision	Changes
06-May-2014	1	Initial release. Part numbers previously included in datasheet DocID8984

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