



**THE DATASHEET OF
STD100NH02LT4**





STD100NH02L STD100NH02L-1

N-channel 24V - 0.0042Ω - 60A - DPAK - IPAK
STripFET™ II Power MOSFET

General features

Type	V _{DSSS}	R _{DS(on)}	I _D
STD100NH02L	24V	<0.0048Ω	60A ⁽¹⁾
STD100NH02L-1	24V	<0.0048Ω	60A ⁽¹⁾

1. Value limited by wire bonding

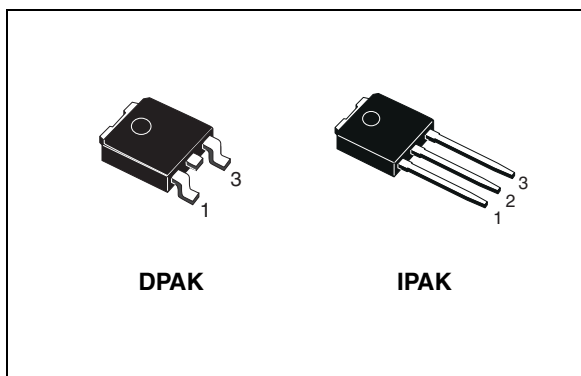
- R_{DS(on)} * Qg industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

Description

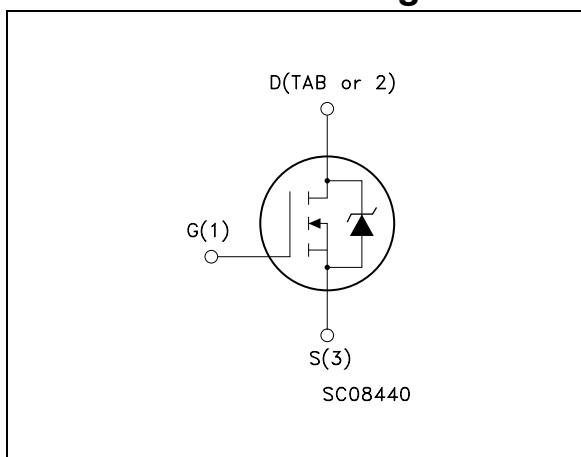
This device utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD100NH02LT4	D100NH02L	DPAK	Tape & reel
STD100NH02L-1	D100NH02L	IPAK	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuit	8
4	Package mechanical data	9
5	Packaging mechanical data	12
6	Revision history	15

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{\text{spike}}^{(1)}$	Drain-source voltage rating	30	V
V_{DS}	Drain-source voltage ($V_{\text{GS}} = 0$)	24	V
V_{DGR}	Drain-gate voltage ($R_{\text{GS}} = 20\text{K}\Omega$)	24	V
V_{GS}	Drain-source voltage	± 20	V
$I_{\text{D}}^{(2)}$	Drain current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$	60	A
$I_{\text{D}}^{(2)}$	Drain current (continuous) at $T_{\text{C}}=100^{\circ}\text{C}$	60	A
$I_{\text{DM}}^{(3)}$	Drain current (pulsed)	240	A
P_{TOT}	Total dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$	100	W
	Derating factor	0.67	W/ $^{\circ}\text{C}$
$E_{\text{AS}}^{(4)}$	Single pulse avalanche energy	800	mJ
T_{stg}	Storage temperature	-55 to 175	$^{\circ}\text{C}$
T_{J}	Max. operating junction temperature		

1. Guaranteed when external $R_{\text{g}} = 4.7 \Omega$ and $t_{\text{f}} < t_{\text{fmax}}$.

2. Value limited by wire bonding.

3. Pulse width limited by safe operating area

4. Starting $T_{\text{J}} = 25^{\circ}\text{C}$, $I_{\text{D}} = 30\text{A}$, $V_{\text{DD}} = 15\text{V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case Max	1.5	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance junction-ambient Max	100	$^{\circ}\text{C}/\text{W}$
T_{I}	Maximum lead temperature for soldering purpose	275	$^{\circ}\text{C}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 25mA, V_{GS} = 0$	24			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 20$ $V_{DS} = 20, T_C = 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.8		V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 30A$ $V_{GS} = 5V, I_D = 15A$		0.0042 0.005	0.0048 0.009	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10 V, I_D = 30A$		50		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 15V, f = 1 MHz,$ $V_{GS} = 0$		3940 1020 110		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 10V, I_D = 30A$ $V_{GS} = 10V$		62 12 8	84	nC nC nC
$Q_{oss}^{(2)}$	Output charge	$V_{DS} = 16V, V_{GS} = 0V$		24		nC
$Q_{gls}^{(3)}$	Third-quadrant gate charge	$V_{DS} < 0V, V_{GS} = 10V$		56.5		nC
R_G	Gate input resistance	$f = 1MHz$ gate DC Bias = 0 Test signal level = 20mV Open drain		1.1		Ω

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%
2. $Q_{oss} = C_{oss} * \Delta V_{in}$, $C_{oss} = C_{gd} + C_{ds}$. See [Chapter Appendix A](#)
3. Gate charge for synchronous operation

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10V, I_D = 30A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ <i>Figure 13 on page 8</i>		15		ns
t_r	Rise time			200		ns
$t_{d(off)}$	Turn-off delay time			60		ns
t_f	Fall time			35	47	ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				60	A
I_{SDM}	Source-drain current (pulsed)				240	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 30A, V_{GS} = 0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 60A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 15V, T_J = 150^\circ C$ <i>Figure 15 on page 8</i>		47		ns
Q_{rr}	Reverse recovery charge			58		μC
I_{RRM}	Reverse recovery current			2.5		A

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

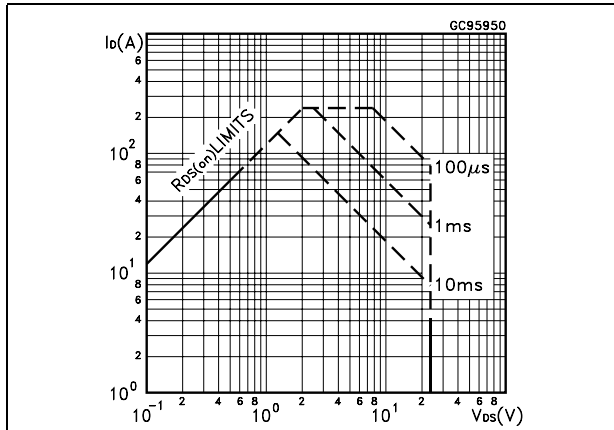


Figure 2. Thermal impedance

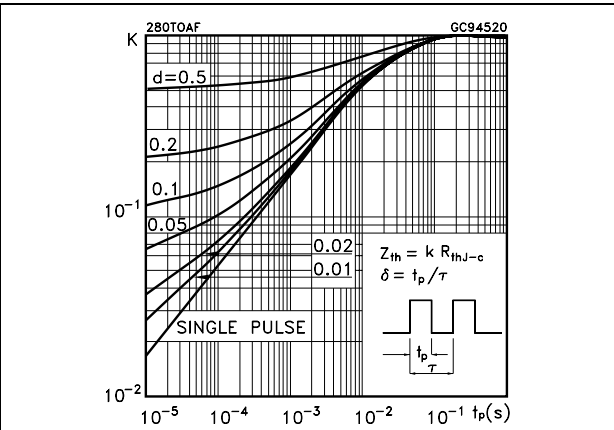


Figure 3. Output characteristics

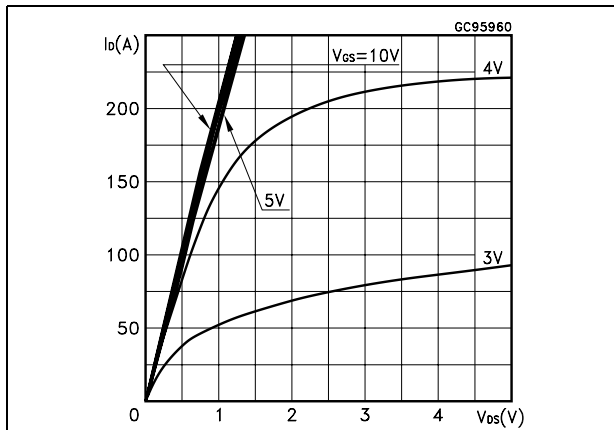


Figure 4. Transfer characteristics

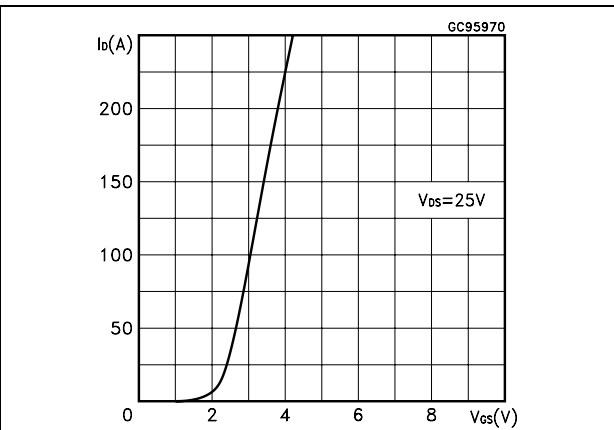


Figure 5. Transconductance

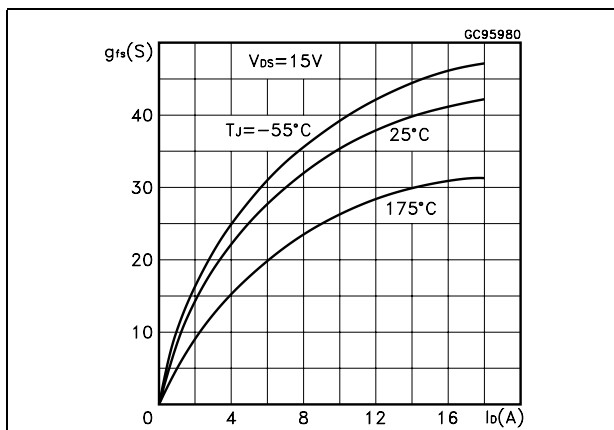


Figure 6. Static drain-source on resistance

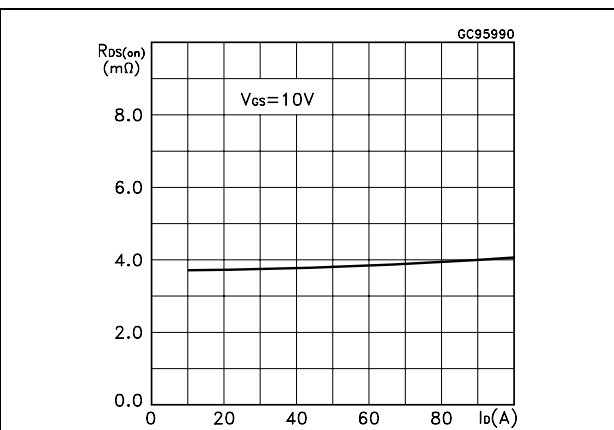


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

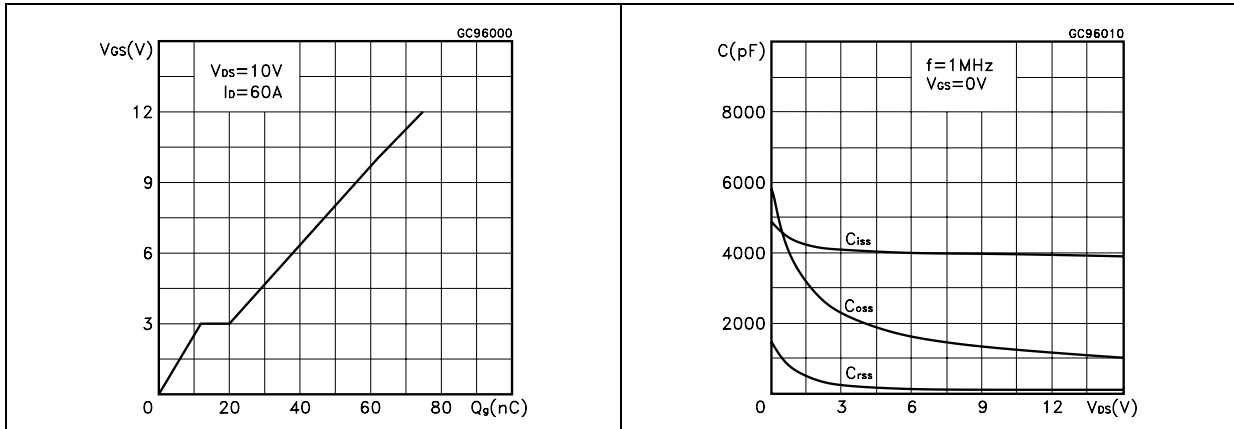


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

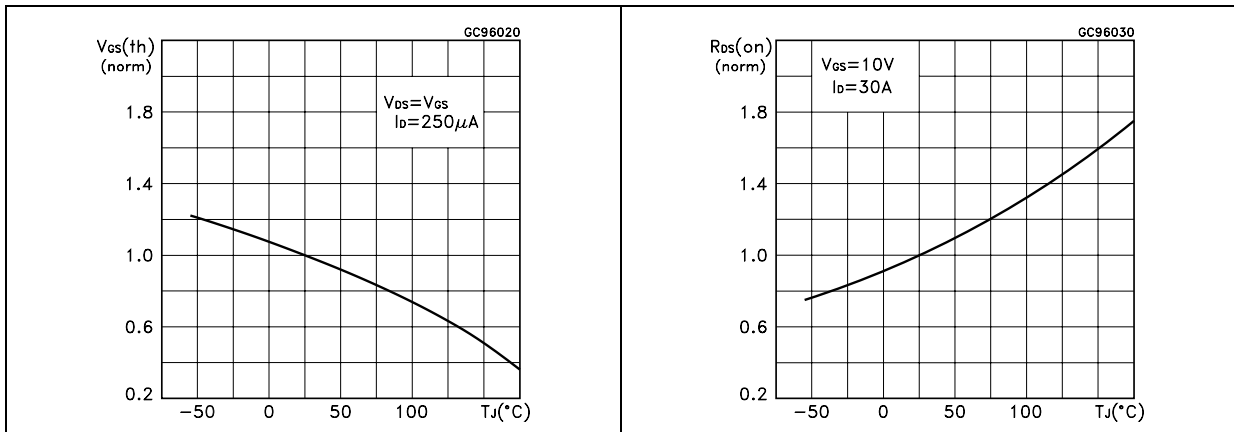
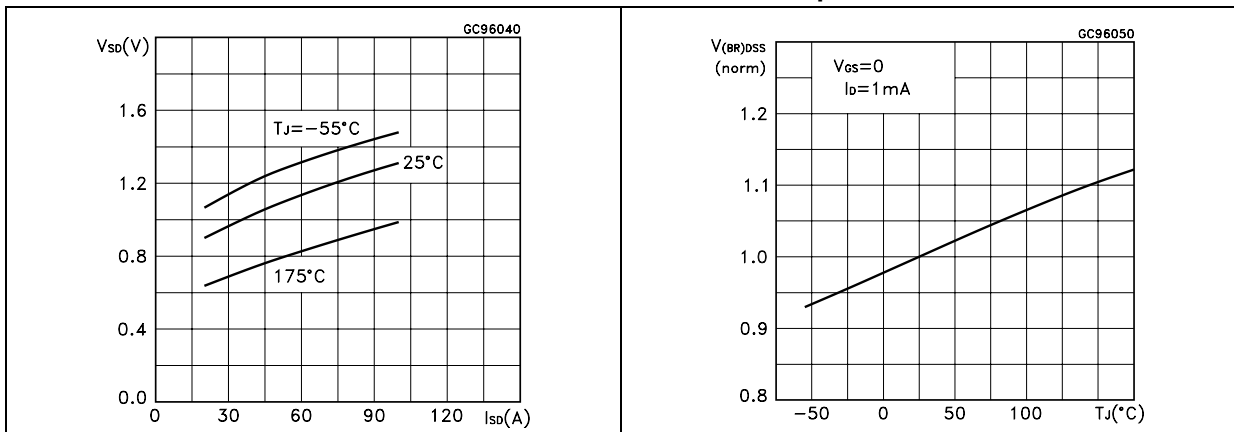


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

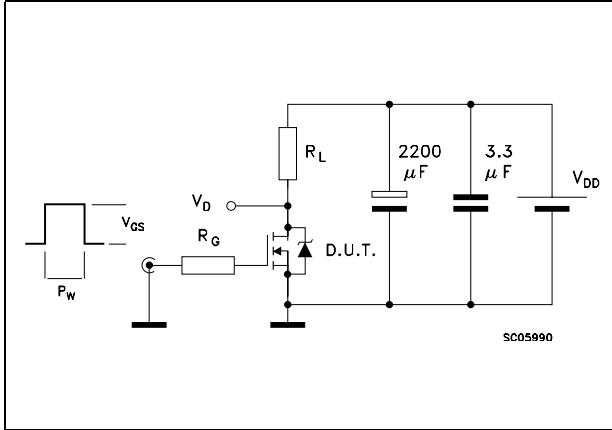


Figure 14. Gate charge test circuit

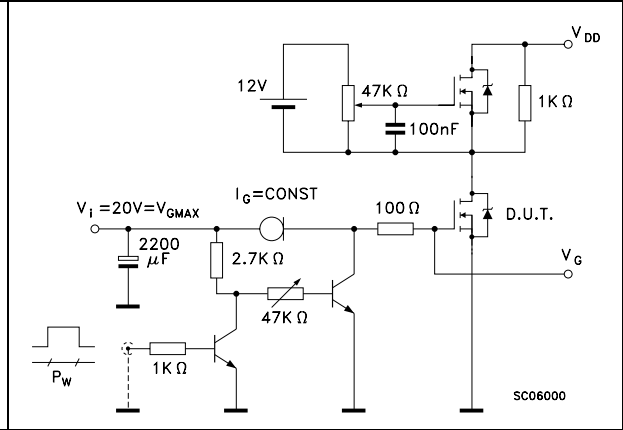


Figure 15. Test circuit for inductive load switching and diode recovery times

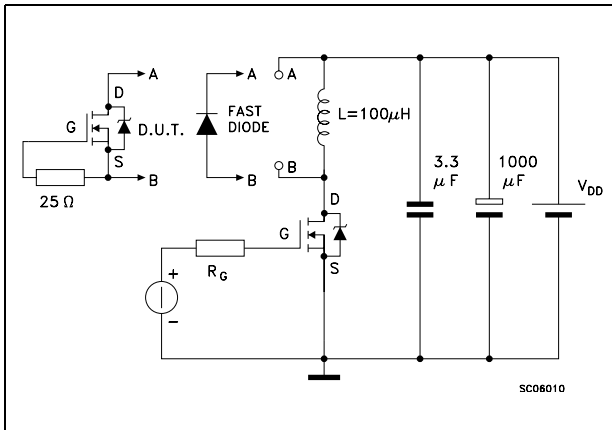


Figure 16. Unclamped Inductive load test circuit

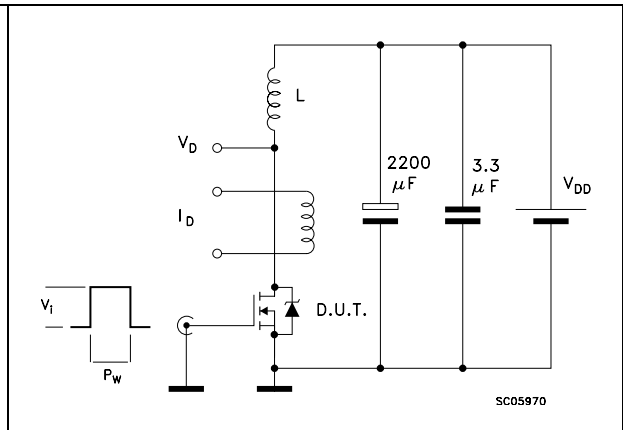
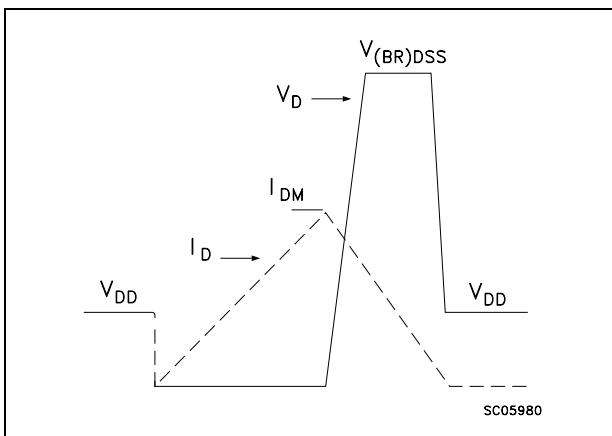


Figure 17. Unclamped inductive waveform

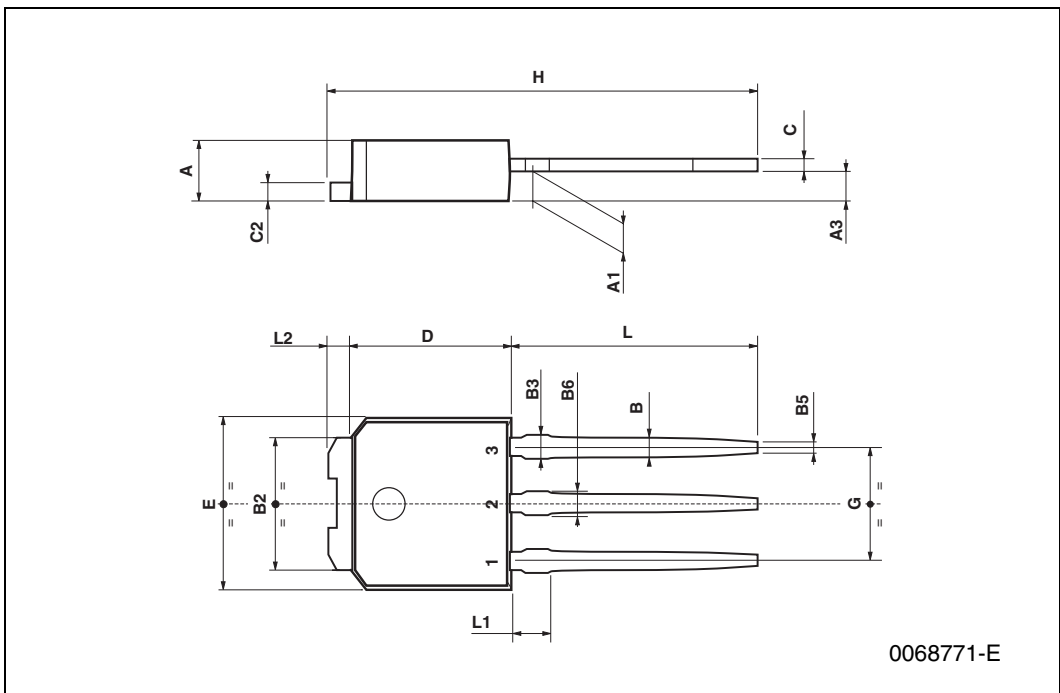


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

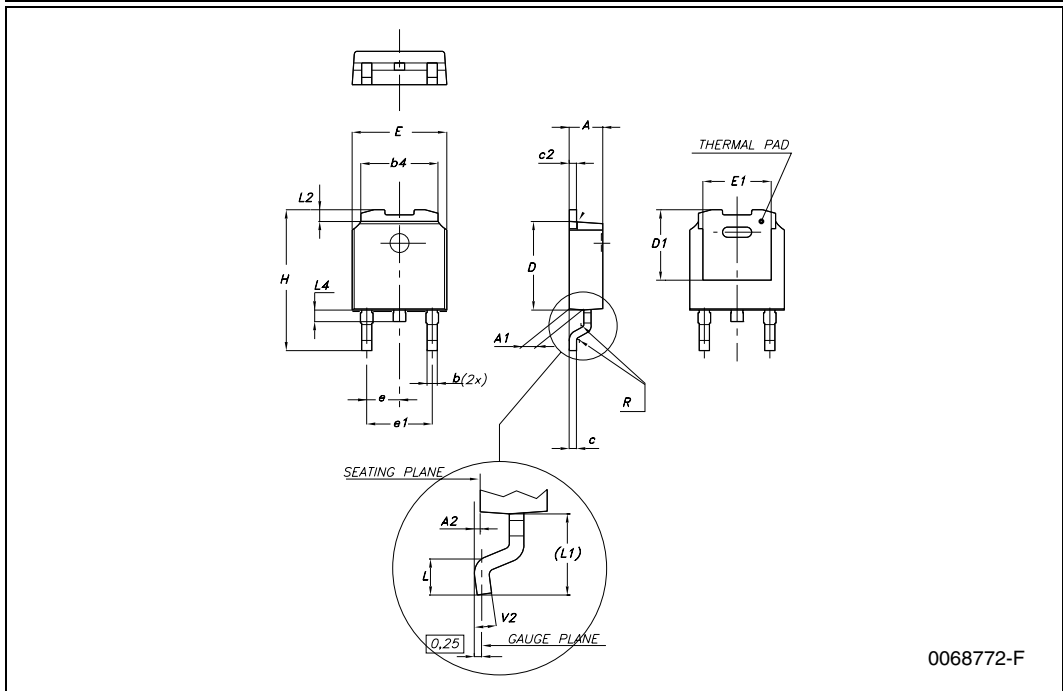
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



DPAK MECHANICAL DATA

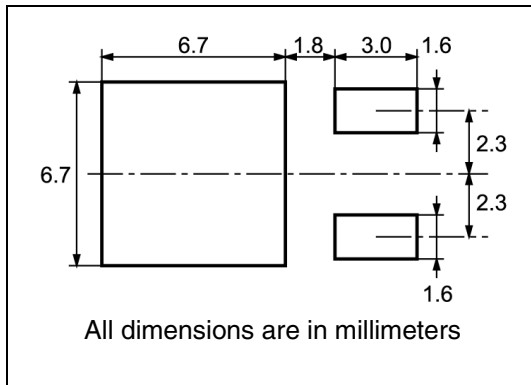
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

For machine ref. only including draft and radii concentric around B0

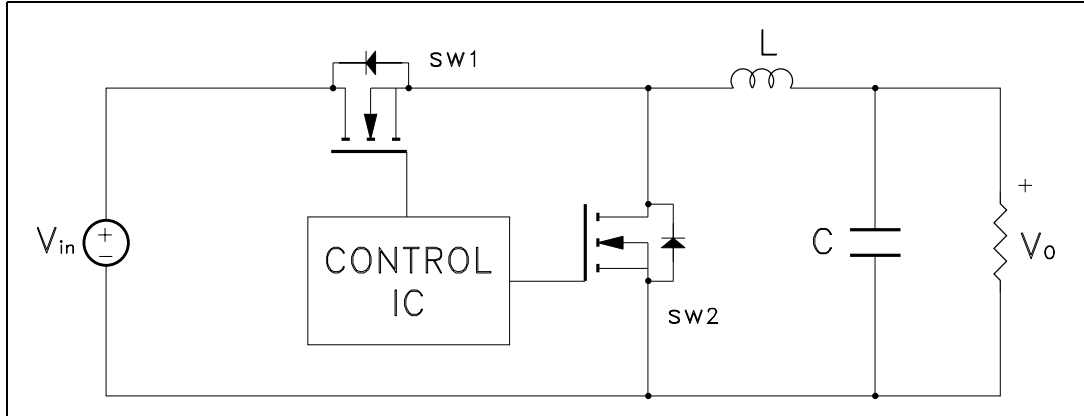
TRL

FEED DIRECTION

Bending radius R min.

Appendix A Buck converter - power losses estimation

Figure 18. Buck converter: power losses estimation



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
 - Very low $R_{DS(on)}$ to reduce conduction losses
 - Small Q_{gl} to reduce the gate charge losses
 - Small C_{oss} to reduce losses due to output capacitance
 - Small Q_{rr} to reduce losses on SW1 during its turn-on
 - The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
 - Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
 - Small Q_g to have a faster commutation and to reduce gate charge losses
 - Low $R_{DS(on)}$ to reduce the conduction losses.

Table 7. Power losses calculation

		High side switching (SW1)	Low side switch (SW2)
Pconduction		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1 - \delta)$
Pswitching		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
Pdiode	Recovery (1)	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
Pgate(QG)		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
PQoss		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

Table 8. Paramiters meaning

Parameter	Meaning
d	Duty-cycle
Qgsth	Post threshold gate charge
Qgls	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
PQoss	Output capacitance losses

6 Revision history

Table 9. Revision history

Date	Revision	Changes
09-Sep-2004	9	Complete version
08-Aug-2006	10	The document has been reformatted, updated SOA Figure 1 .
18-Dev-2006	11	Typo mistake on Table 3 .

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2006 STMicroelectronics - All rights reserved



STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View STD100NH02LT4 on WIN SOURCE](#)
-  [STMicroelectronics Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management