



# THE DATASHEET OF STF24N60M2



N-channel 600 V, 0.168  $\Omega$  typ., 18 A MDmesh II Plus™ low  $Q_g$  Power MOSFETs in TO-220FP, I<sup>2</sup>PAKFP and TO-3PF packages

Datasheet – production data

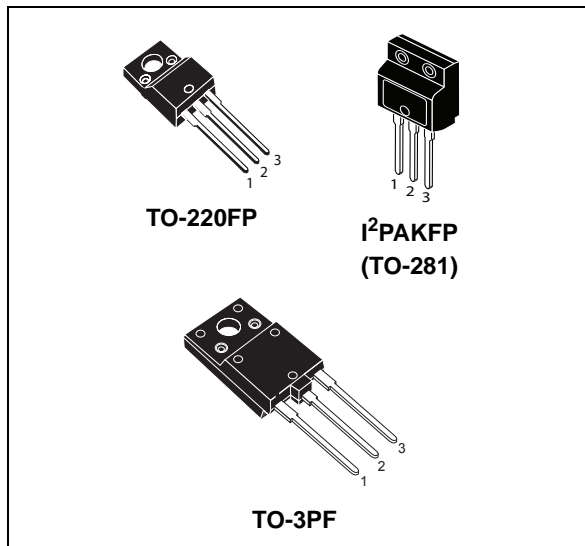
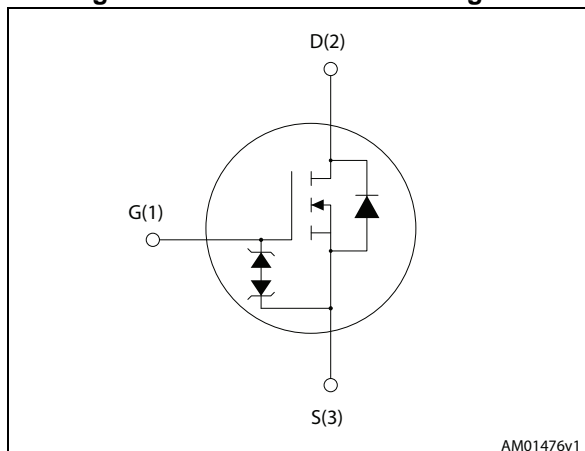


Figure 1. Internal schematic diagram



## Features

Order codes	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	$I_D$
STF24N60M2	650 V	0.19 $\Omega$	18 A
STFI24N60M2			
STFW24N60M2			

- Extremely low gate charge
- Lower  $R_{DS(on)}$  x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications
- LLC converters, resonant converters

## Description

These devices are N-channel Power MOSFETs developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low  $Q_g$ . These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF24N60M2	24N60M2	TO-220FP	Tube
STFI24N60M2		I <sup>2</sup> PAKFP (TO-281)	
STFW24N60M2		TO-3PF	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220FP, I <sup>2</sup> PAKFP	TO-3PF	
V <sub>GS</sub>	Gate-source voltage	± 25		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	18 <sup>(1)</sup>		A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	12 <sup>(1)</sup>		A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	72 <sup>(1)</sup>		A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	30	48	W
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15		V/ns
dv/dt <sup>(4)</sup>	MOSFET dv/dt ruggedness	50		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)	2500	3500	V
T <sub>stg</sub>	Storage temperature	- 55 to 150		°C
T <sub>j</sub>	Max. operating junction temperature			

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. I<sub>SD</sub> ≤ 18 A, di/dt ≤ 400 A/μs; V<sub>DS peak</sub> < V<sub>(BR)DSS</sub>; V<sub>DD</sub> = 400 V.
4. V<sub>DS</sub> ≤ 480 V

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220FP, I <sup>2</sup> PAKFP	TO-3PF	
R <sub>thj-case</sub>	Thermal resistance junction-case max	4.2	2.6	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max	62.5	50	°C/W

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by T <sub>jmax</sub> )	3.5	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> =25°C, I <sub>D</sub> = I <sub>AR</sub> ; V <sub>DD</sub> =50)	180	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$		0.168	0.19	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	1060	-	pF
$C_{oss}$	Output capacitance		-	55	-	pF
$C_{rss}$	Reverse transfer capacitance		-	2.2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0$	-	258	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0$	-	7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 18\text{ A}, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> )	-	29	-	nC
$Q_{gs}$	Gate-source charge		-	6	-	nC
$Q_{gd}$	Gate-drain charge		-	12	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 9\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> and <a href="#">21</a> )	-	14	-	ns
$t_r$	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
$t_f$	Fall time		-	15	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		18	A
$I_{SDM}^{(1),(2)}$	Source-drain current (pulsed)		-		72	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 18\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 18\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 18</a> )	-	332		ns
$Q_{rr}$	Reverse recovery charge		-	4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	24		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 18\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 18</a> )	-	450		ns
$Q_{rr}$	Reverse recovery charge		-	5.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	25		A

1. The value is rated according to  $R_{thj-case}$  and limited by package.
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration =  $300\ \mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP and I<sup>2</sup>PAKFP

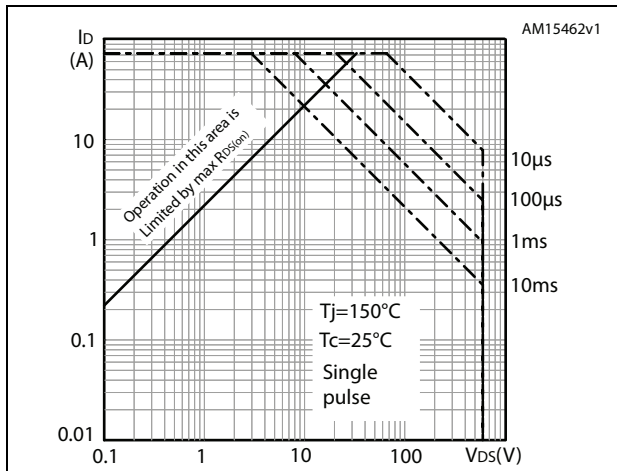


Figure 3. Thermal impedance for TO-220FP and I<sup>2</sup>PAKFP

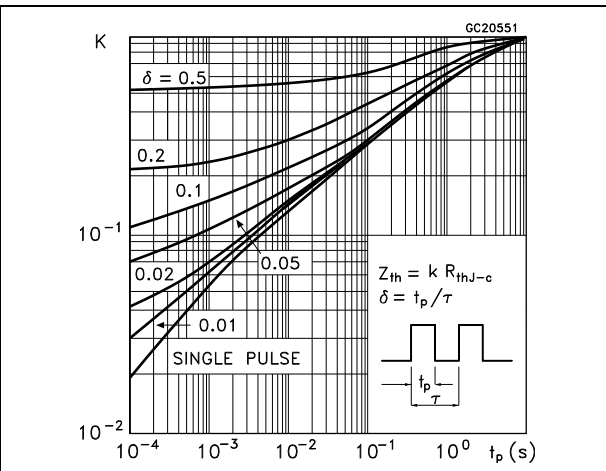


Figure 4. Safe operating area for TO-3PF

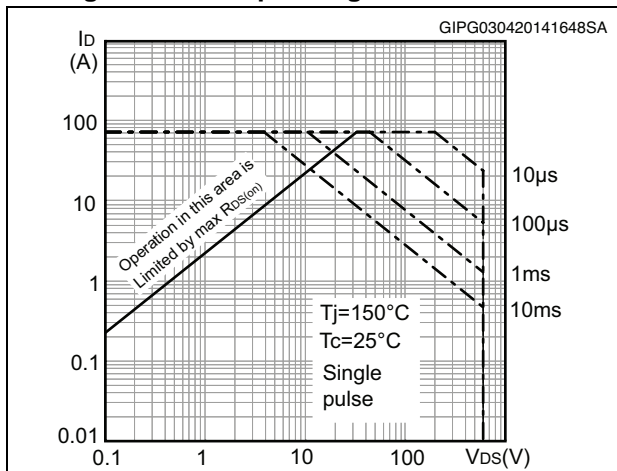


Figure 5. Thermal impedance for TO-3PF

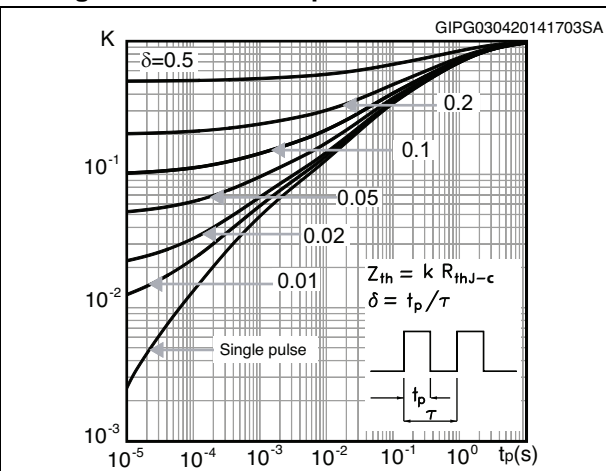


Figure 6. Output characteristics

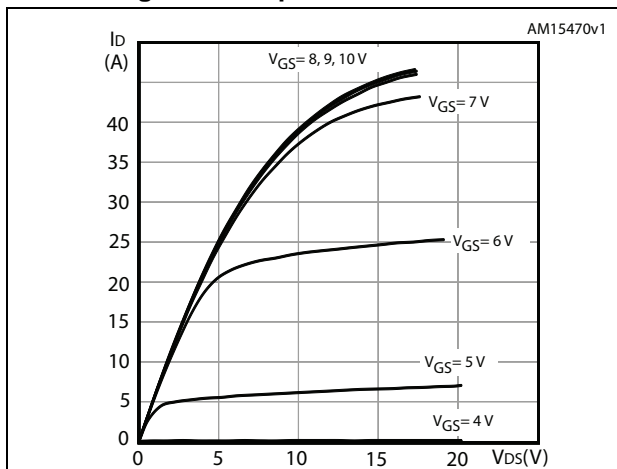


Figure 7. Transfer characteristics

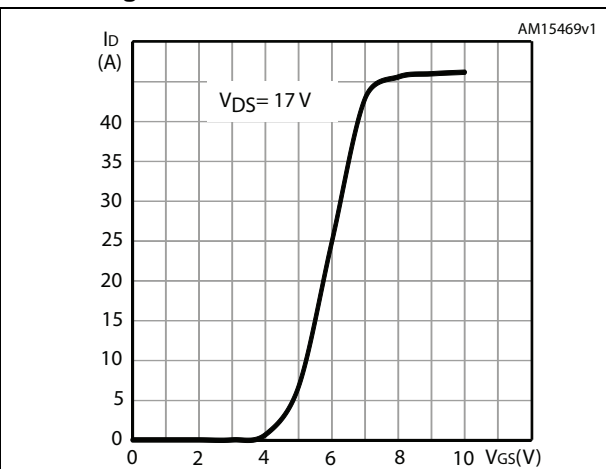


Figure 8. Gate charge vs gate-source voltage

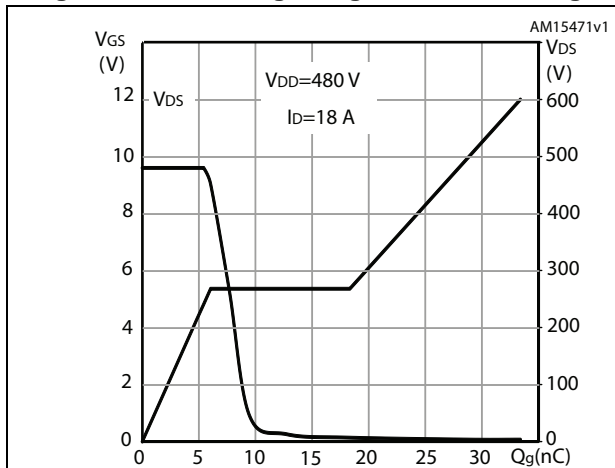


Figure 9. Static drain-source on-resistance

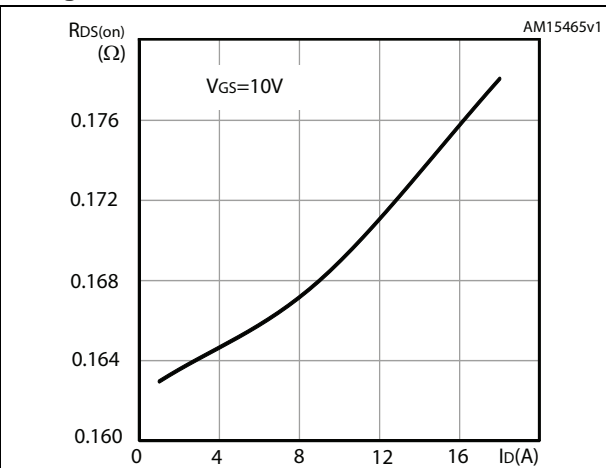


Figure 10. Capacitance variations

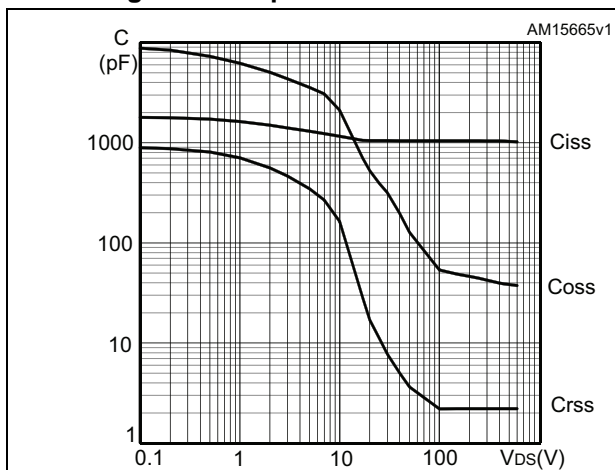


Figure 11. Output capacitance stored energy

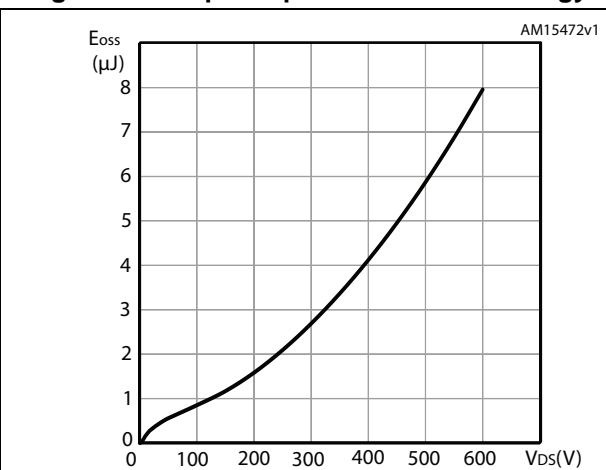


Figure 12. Normalized gate threshold voltage vs temperature

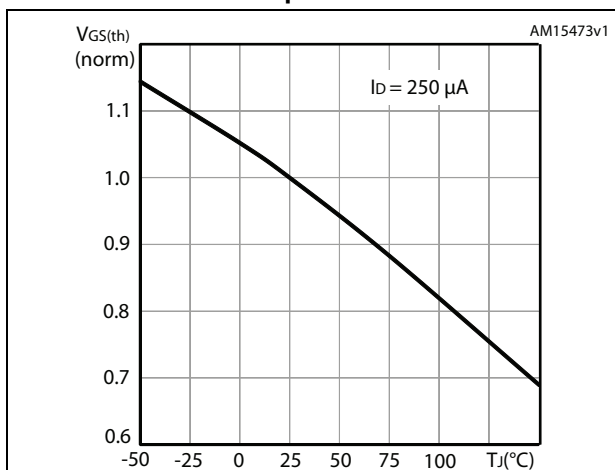


Figure 13. Normalized on-resistance vs temperature

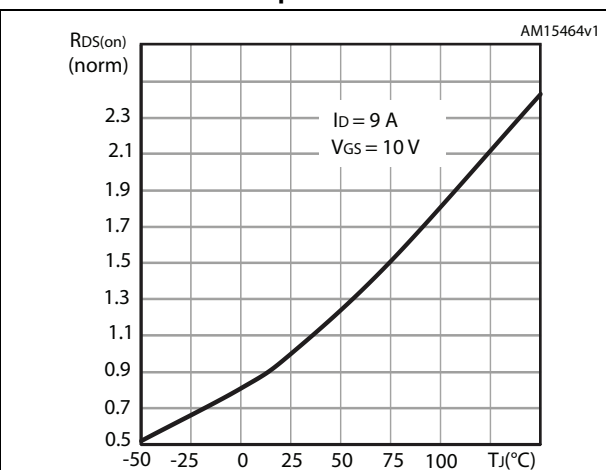


Figure 14. Source-drain diode forward characteristics

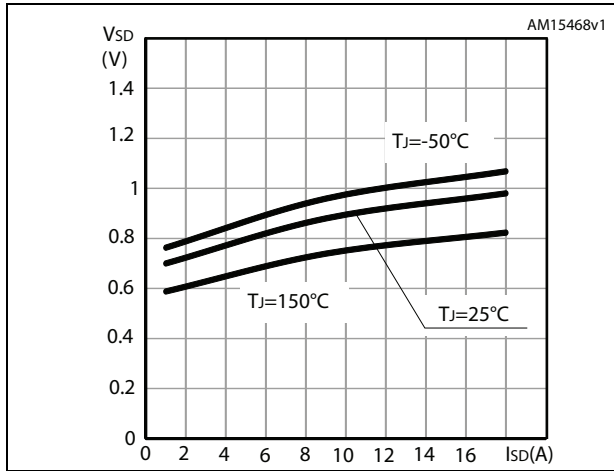
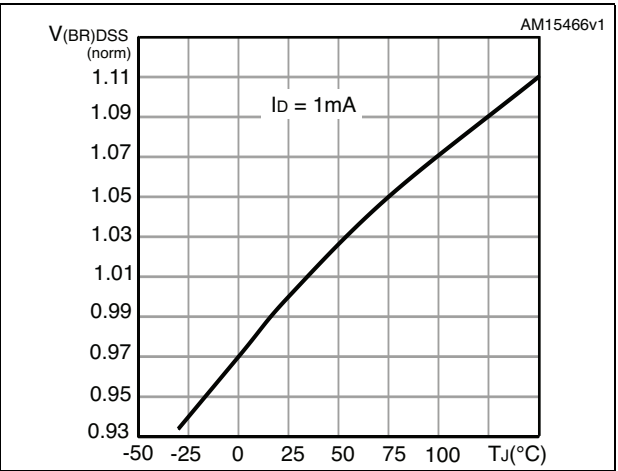


Figure 15. Normalized V<sub>(BR)DSS</sub> vs temperature



### 3 Test circuits

Figure 16. Switching times test circuit for resistive load

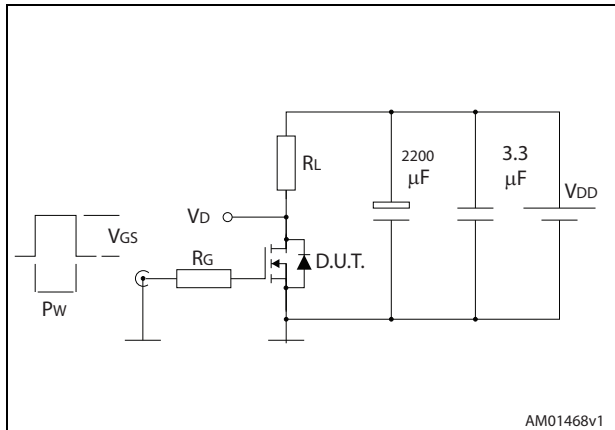


Figure 17. Gate charge test circuit

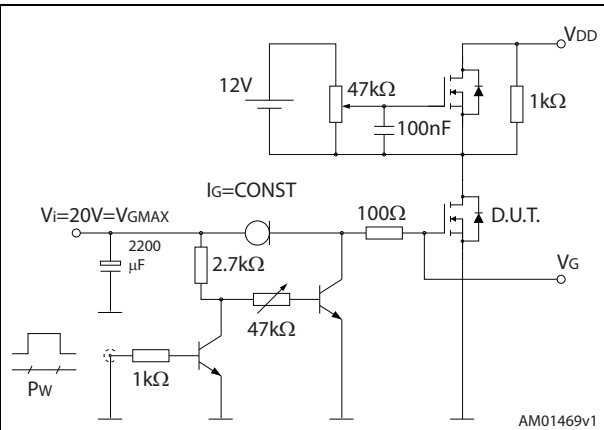


Figure 18. Test circuit for inductive load switching and diode recovery times

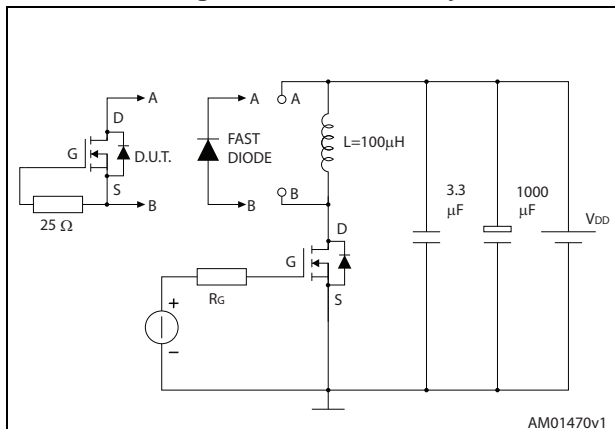


Figure 19. Unclamped inductive load test circuit

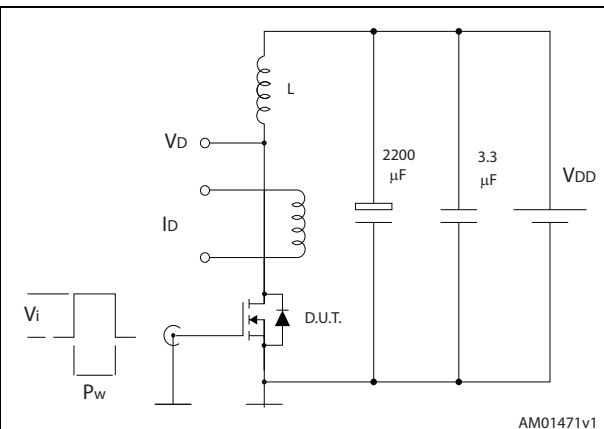


Figure 20. Unclamped inductive waveform

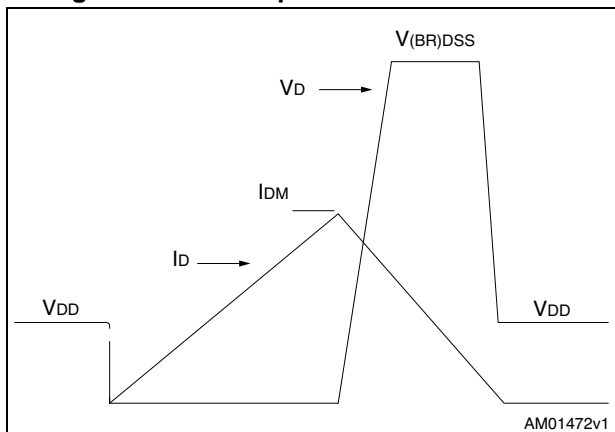
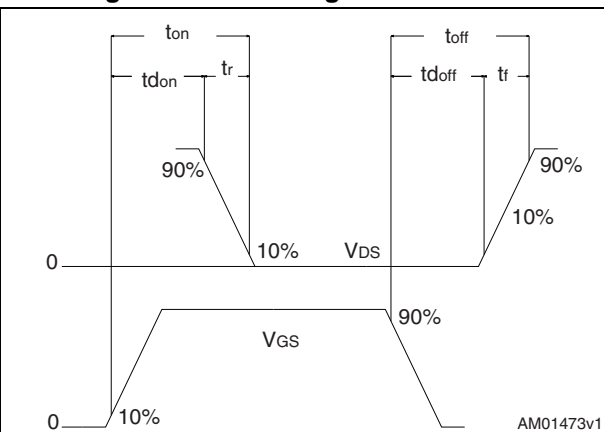


Figure 21. Switching time waveform

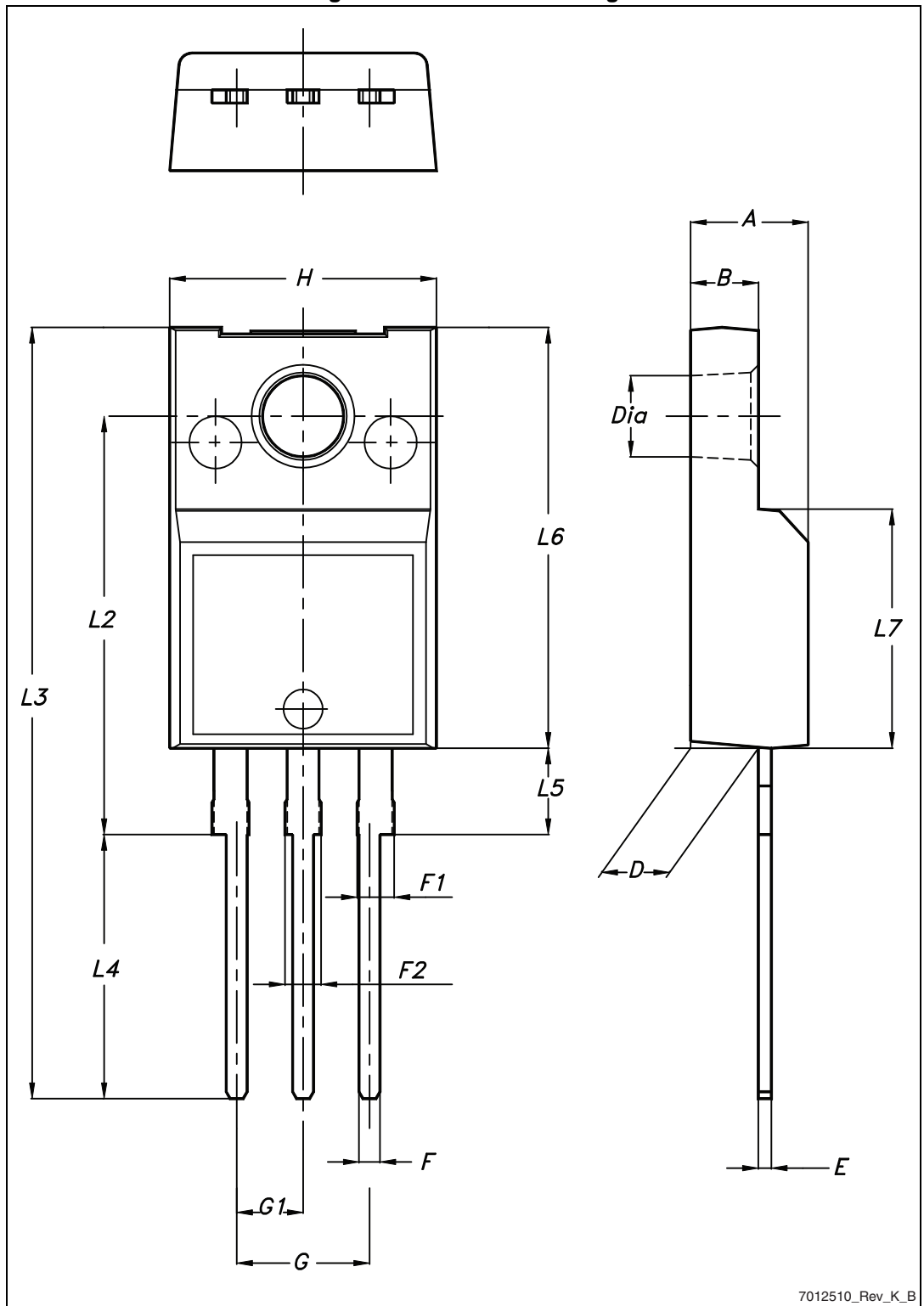


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 TO-220FP, STF24N60M2

Figure 22. TO-220FP drawing



7012510\_Rev\_K\_B

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

### 4.2 I<sup>2</sup>PAKFP, STFI24N60M2

Figure 23. I<sup>2</sup>PAKFP (TO-281) drawing

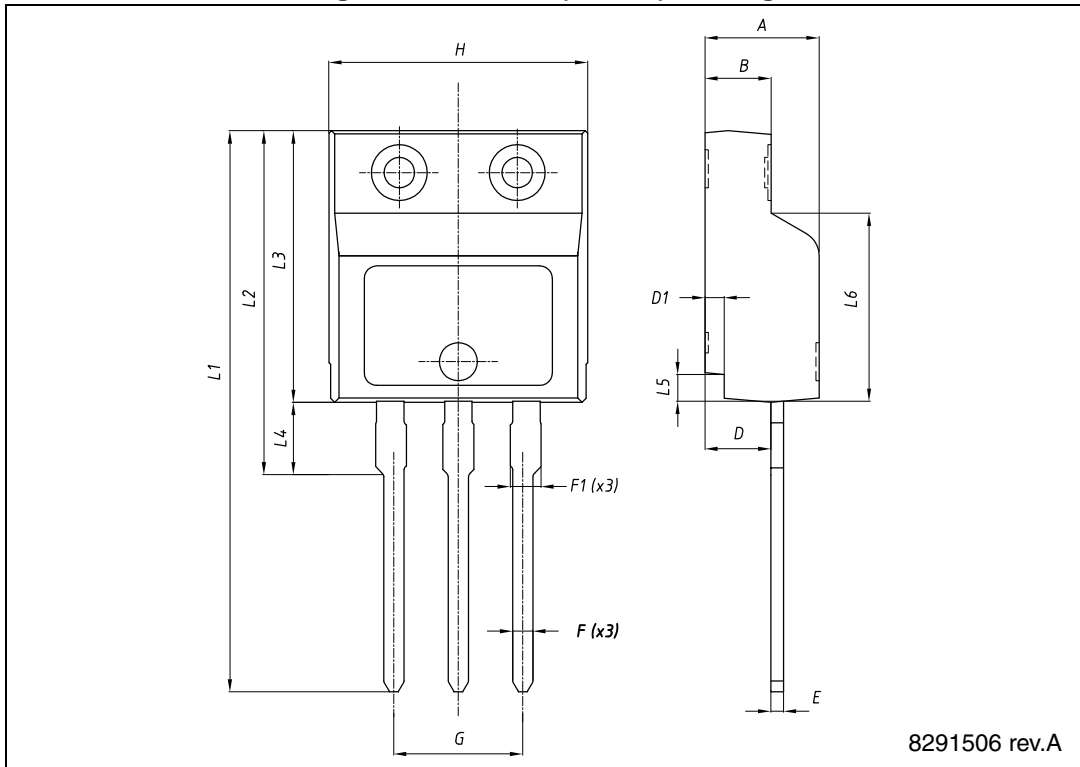


Table 10. I<sup>2</sup>PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

### 4.3 TO-3PF, STFW24N60M2

Figure 24. TO-3PF drawing

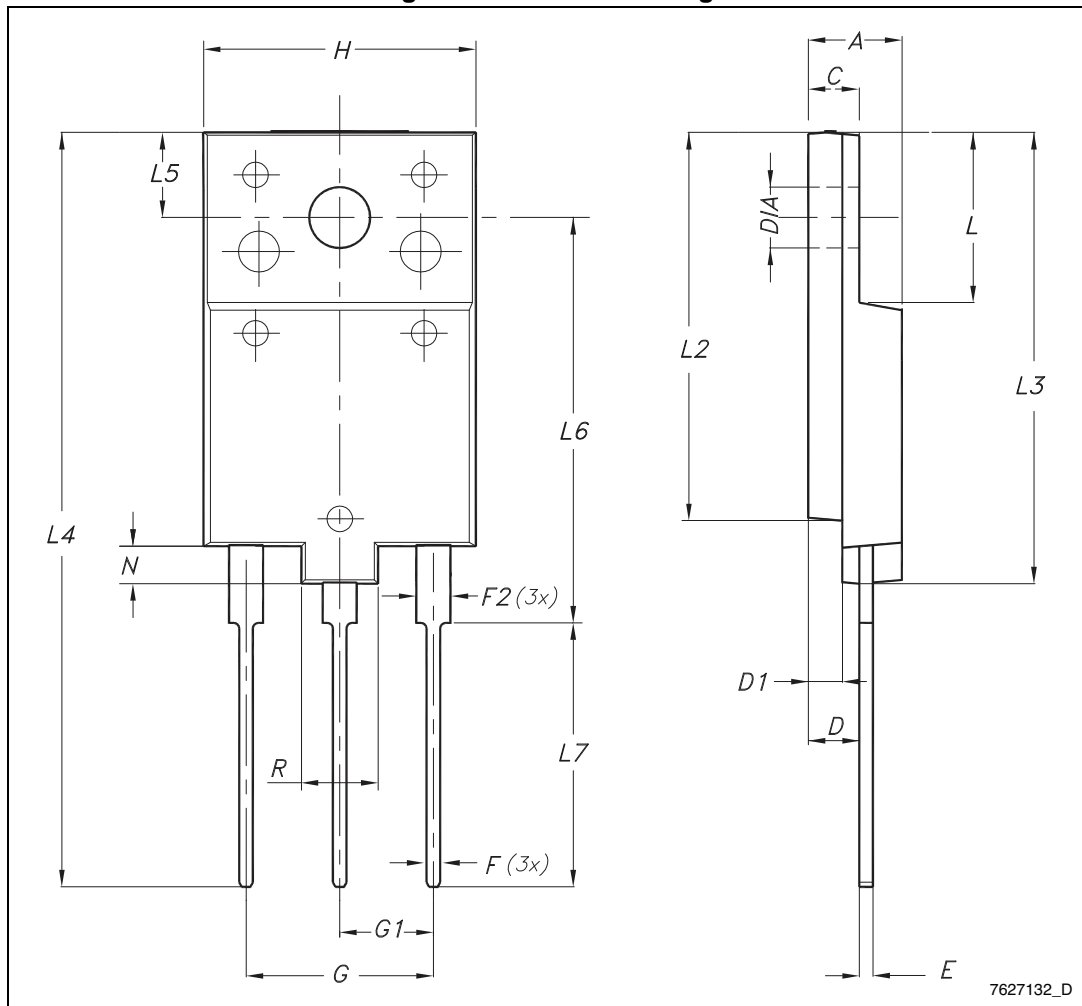


Table 11. TO-3PF mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9.80	10	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

## 5 Revision history

Table 12. Document revision history

Date	Revision	Changes
10-Dec-2012	1	First release.
20-Dec-2012	2	Added MOSFET dv/dt ruggedness in <a href="#">Table 2: Absolute maximum ratings</a> .
14-Jan-2013	3	Modified: <a href="#">Figure 16, 17</a>
28-May-2013	4	<ul style="list-style-type: none"> <li>– Modified: <a href="#">Figure 16, 17, 18 and 19</a></li> <li>– Minor text changes</li> </ul>
28-Feb-2014	5	<ul style="list-style-type: none"> <li>– Modified: <math>R_{thj-case}</math> value in <a href="#">Table 3</a></li> <li>– Modified: <a href="#">Figure 12</a></li> <li>– Minor text changes</li> </ul>
07-Apr-2014	6	<ul style="list-style-type: none"> <li>– Added: TO-3PF package</li> <li>– Added: <a href="#">Section 4.3: TO-3PF, STF24N60M2</a></li> <li>– Minor text changes</li> </ul>

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