



**THE DATASHEET OF  
74LVC245ABQ**



# 74LVC245A; 74LVCH245A

Octal bus transceiver; 3-state

Rev. 13 — 8 August 2023

Product data sheet

## 1. General description

The 74LVC245A; 74LVCH245A is an 8-bit transceiver with 3-state outputs. The device features an output enable ( $\overline{OE}$ ) and send/receive (DIR) for direction control. A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- Bus hold on all data inputs (74LVCH245A only)
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74LVC245AD</a> <a href="#">74LVCH245AD</a>	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	<a href="#">SOT163-1</a>
<a href="#">74LVC245APW</a> <a href="#">74LVCH245APW</a>	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	<a href="#">SOT360-1</a>
<a href="#">74LVC245ABQ</a> <a href="#">74LVCH245ABQ</a>	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	<a href="#">SOT764-1</a>
<a href="#">74LVC245ABZ</a>	-40 °C to +125 °C	DHXQFN20	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 20 terminals; 0.4 mm pitch; body 2 mm × 3.2 mm × 0.48 mm	<a href="#">SOT8020-1</a>

### 4. Functional diagram

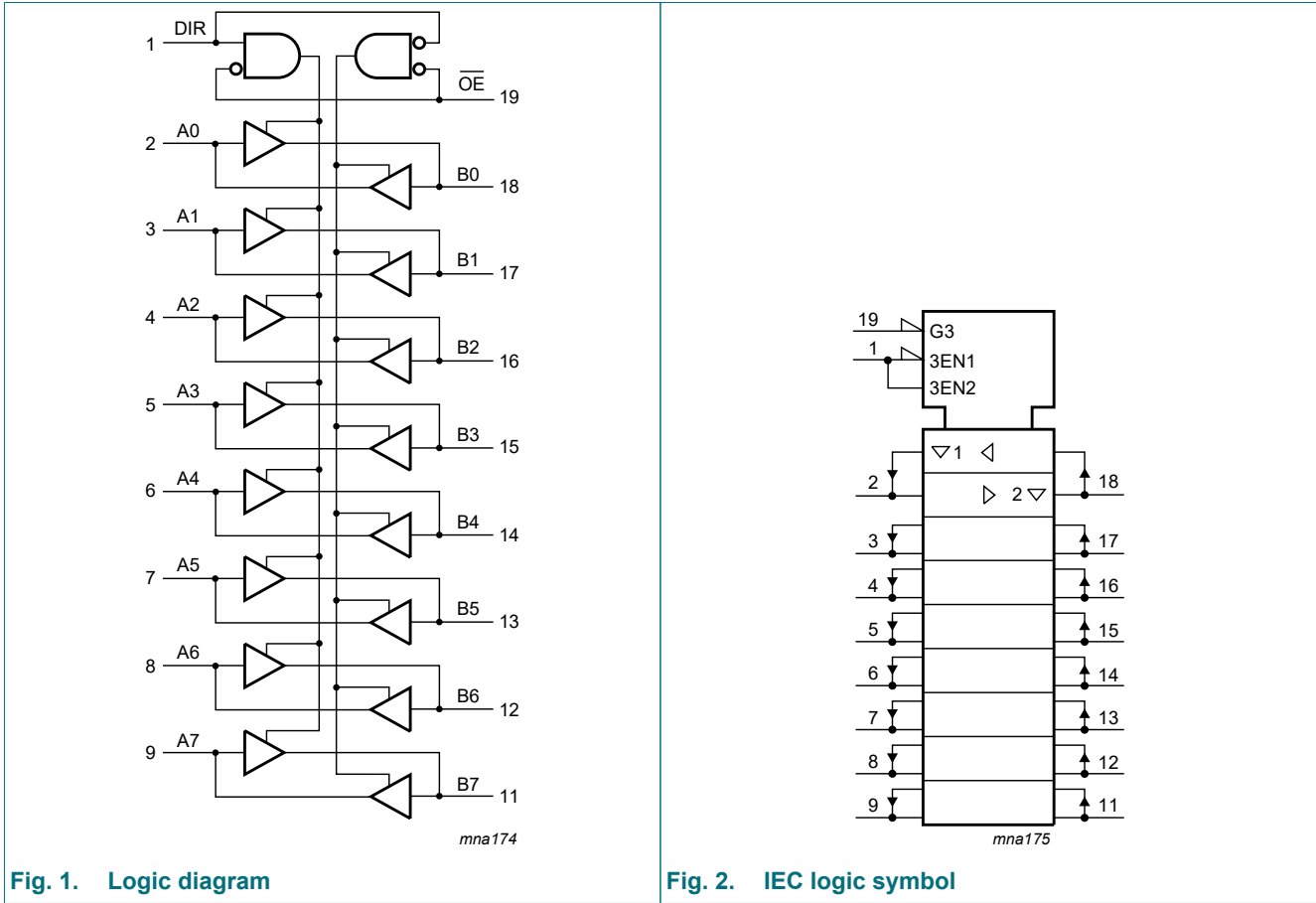
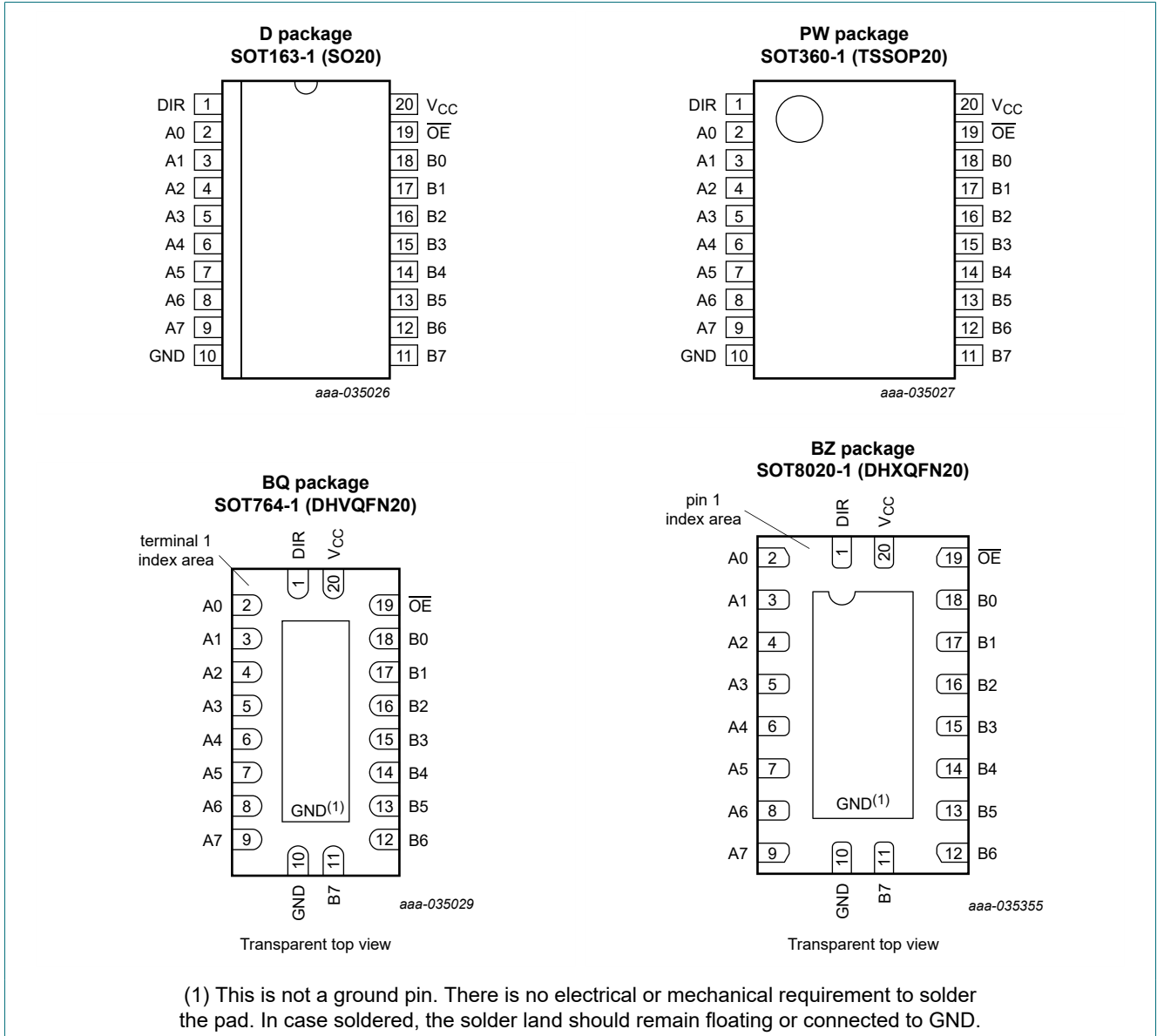


Fig. 1. Logic diagram

Fig. 2. IEC logic symbol

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
OE	19	output enable input (active LOW)
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

**Table 3. Function selection**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance OFF-state.*

Inputs		Inputs/outputs	
OE	DIR	An	Bn
L	L	An = Bn	inputs
L	H	inputs	Bn = An
H	X	Z	Z

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW [2]	-0.5	$V_{CC} + 0.5$	V
		output 3-state [2]	-0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		SOT163-1 (SO20) [3]	-	500	mW
		SOT360-1 (TSSOP20) [4]			
		SOT764-1 (DHVQFN20) [5]			
		SOT8020-1 (DHXQFN20)	-	250	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT163-1 (SO20) package:  $P_{tot}$  derates linearly with 12.3 mW/K above 109 °C.

[4] For SOT360-1 (TSSOP20) package:  $P_{tot}$  derates linearly with 10.0 mW/K above 100 °C.

[5] For SOT764-1 (DHVQFN20) package:  $P_{tot}$  derates linearly with 12.9 mW/K above 111 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.2 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	0.65V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V [2]	-	±0.1	±5	-	±20	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V [3]	-	±0.1	±5	-	±20	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0.0 V	-	±0.1	±10	-	±20	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 3.6 V	-	0.1	10	-	40	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.7 V to 3.6 V	-	5	500	-	5000	µA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	4.0	-	-	-	pF
C <sub>I/O</sub>	input/output capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	10	-	-	-	pF
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 1.65; V <sub>I</sub> = 0.58 V [4] [5]	10	-	-	10	-	µA
		V <sub>CC</sub> = 2.3; V <sub>I</sub> = 0.7 V	30	-	-	25	-	µA
		V <sub>CC</sub> = 3.0; V <sub>I</sub> = 0.8 V	75	-	-	60	-	µA
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 1.65; V <sub>I</sub> = 1.07 V [4] [5]	-10	-	-	-10	-	µA
		V <sub>CC</sub> = 2.3; V <sub>I</sub> = 1.7 V	-30	-	-	-25	-	µA
		V <sub>CC</sub> = 3.0; V <sub>I</sub> = 2.0 V	-75	-	-	-60	-	µA
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 1.95 V [4] [6]	200	-	-	200	-	µA
		V <sub>CC</sub> = 2.7 V	300	-	-	300	-	µA
		V <sub>CC</sub> = 3.6 V	500	-	-	500	-	µA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 1.95 V [4] [6]	-200	-	-	-200	-	µA
		V <sub>CC</sub> = 2.7 V	-300	-	-	-300	-	µA
		V <sub>CC</sub> = 3.6 V	-500	-	-	-500	-	µA

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

[2] The bus hold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub> allowing 5.5 V on the input terminal.

[3] For I/O ports the parameter I<sub>OZ</sub> includes the input leakage current.

[4] Valid for data inputs of bus hold parts only (74LVCH245A). Note that control inputs do not have a bus hold circuit.

[5] The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.

[6] The specified overdrive current at the data input forces the data input to the opposite input state.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 5.

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nAn to nBn; nBn to nAn; see Fig. 3 [2]						
		V <sub>CC</sub> = 1.2 V	-	17.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	6.5	14.6	1.5	16.9	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.4	7.6	1.0	8.7	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.4	7.3	1.5	9.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	2.9	6.3	1.5	8.0	ns
t <sub>en</sub>	enable time	n $\overline{O}E$ to nAn, nBn; see Fig. 4 [2]						
		V <sub>CC</sub> = 1.2 V	-	22.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.9	8.3	19.5	1.9	22.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	4.6	10.7	1.5	12.4	ns
		V <sub>CC</sub> = 2.7 V	1.5	4.8	9.5	1.5	12.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	3.7	8.5	1.5	11.0	ns
t <sub>dis</sub>	disable time	n $\overline{O}E$ to nAn, nBn; see Fig. 4 [2]						
		V <sub>CC</sub> = 1.2 V	-	12.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.9	5.5	12.3	2.9	14.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.1	7.1	1.0	8.2	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.9	8.0	1.5	10.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.7	3.6	7.0	1.7	9.0	ns
t <sub>sk(o)</sub>	output skew time	[3]	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation capacitance	per input; V <sub>I</sub> = GND to V <sub>CC</sub> [4]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	7.7	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	11.3	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	14.4	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

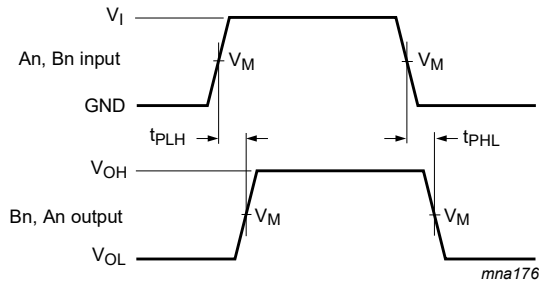
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

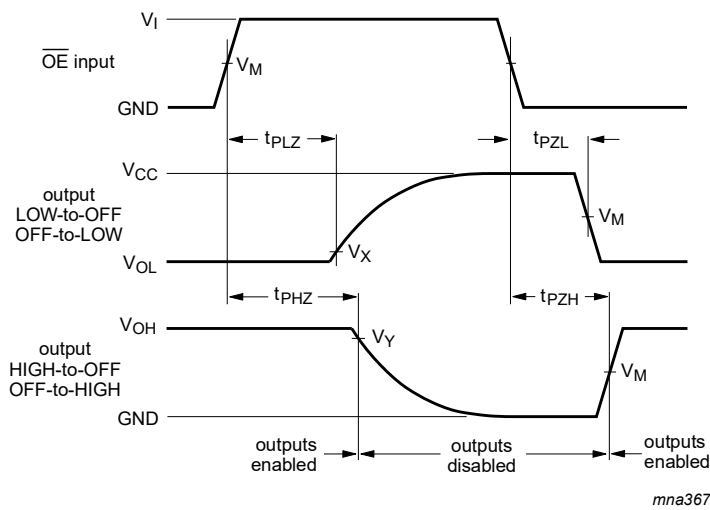
10.1. Waveforms and test circuit



See Table 8 for measurement points.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 3. Input (An, Bn) to output (Bn, An) propagation delays and output transition times



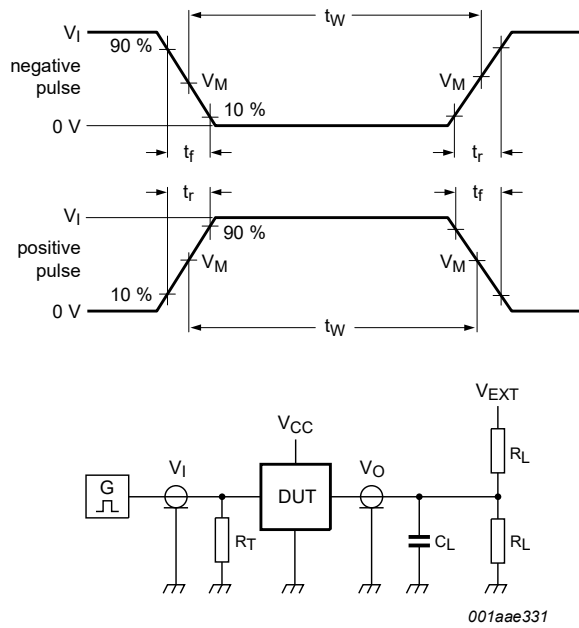
See Table 8 for measurement points.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 4. Enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
$V_{CC}$	$V_M$	$V_I$	$V_M$	$V_X$	$V_Y$
1.2 V	$0.5 \times V_{CC}$	$V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	1.5 V	2.7 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 5. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig. 6. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

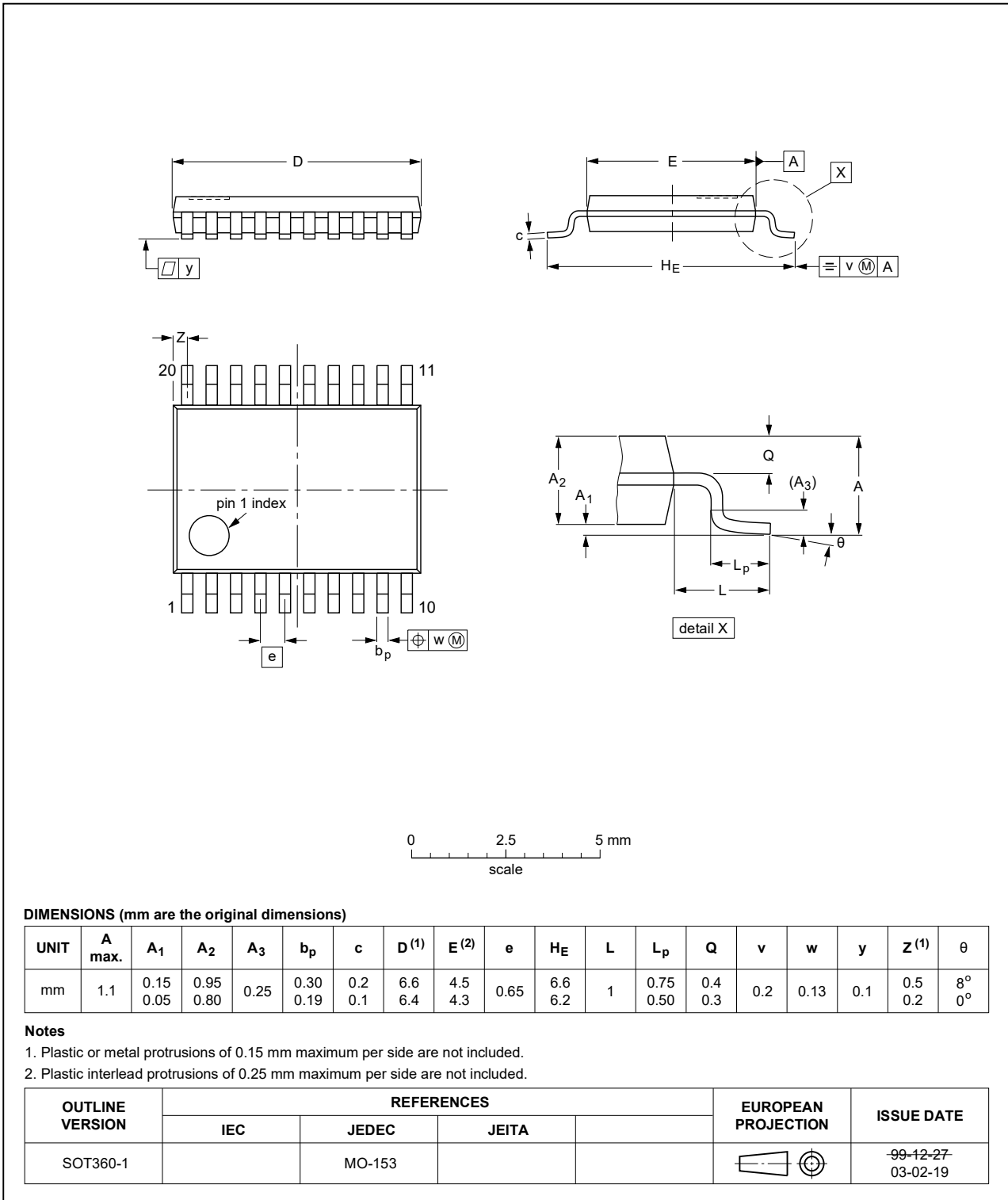


Fig. 7. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig. 8. Package outline SOT764-1 (DHVQFN20)

DHXQFN20: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 20 terminals; 0.4 mm pitch; body 2 mm x 3.2 mm x 0.48 mm

SOT8020-1

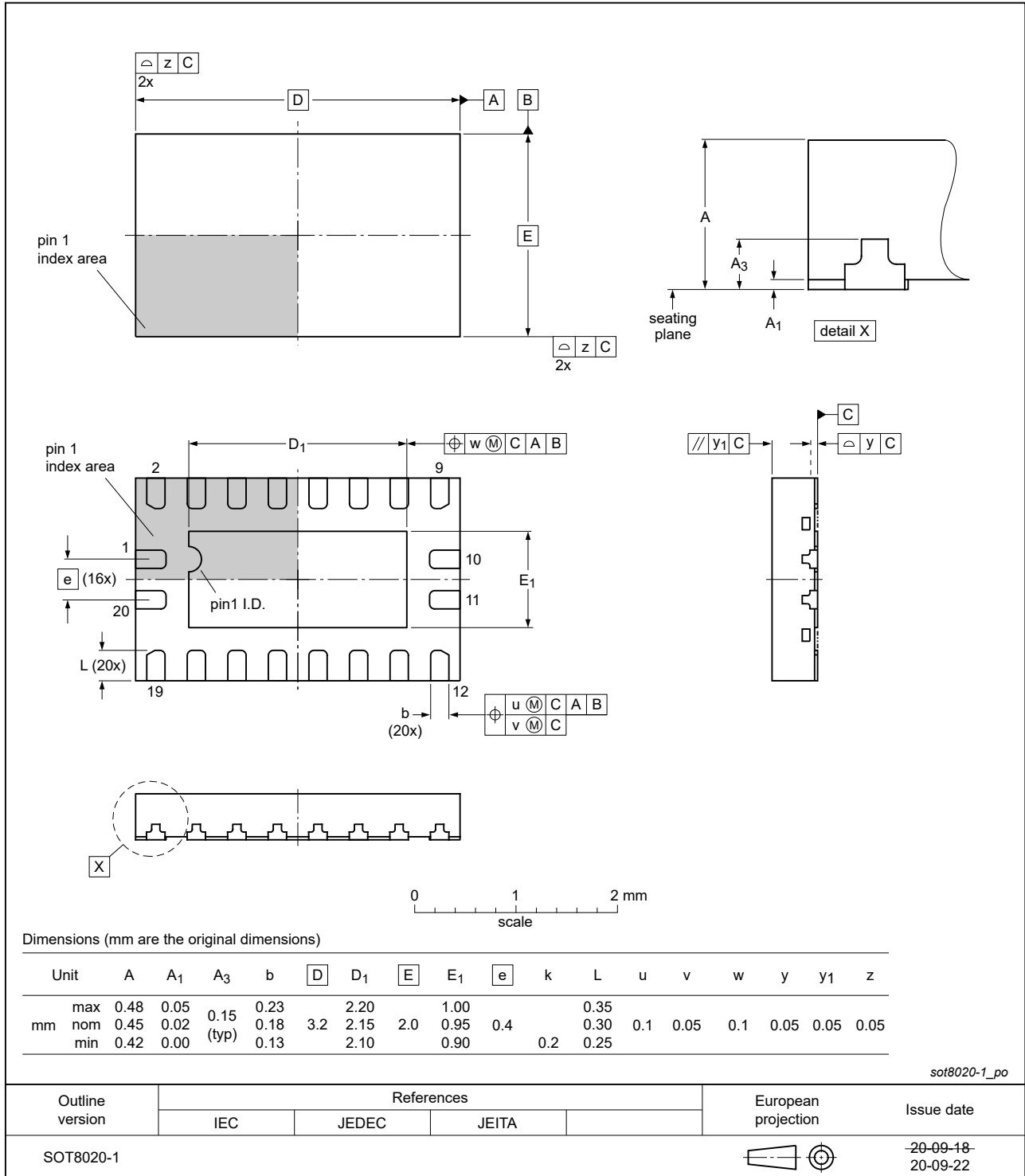


Fig. 9. Package outline SOT8020-1 (DHXQFN20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH245A v.13	20230808	Product data sheet	-	74LVC_LVCH245A v.12
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74LVC_LVCH245A v.12	20210916	Product data sheet	-	74LVC_LVCH245A v.11
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74LVC245ADB and 74LVCH245ADB (SOT339-1/SSOP20) removed.</li> </ul>			
74LVC_LVCH245A v.11	20210429	Product data sheet	-	74LVC_LVCH245A v.10
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LVC245ABZ (SOT8020-1 / DHXQFN20) added.</li> </ul>			
74LVC_LVCH245A v.10	20200805	Product data sheet	-	74LVC_LVCH245A v.9
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 1</a> updated.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li><a href="#">Table 8</a> corrected (Errata).</li> </ul>			
74LVC_LVCH245A v.9	20180911	Product data sheet	-	74LVC_LVCH245A v.8
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74LVC245ABX and 74LVCH245ABX (SOT1045-2) removed.</li> <li><a href="#">Fig. 8</a>: Package outline drawing of SOT764-1 updated.</li> </ul>			
74LVC_LVCH245A v.8	20130628	Product data sheet	-	74LVC_LVCH245A v.7
Modifications:	<ul style="list-style-type: none"> <li>For type numbers 74LVC245ABX and 74LVCH245ABX DHXQFN20U (SOT1045-1) has changed to DHXQFN20 (SOT1045-2).</li> </ul>			
74LVC_LVCH245A v.7	20120405	Product data sheet	-	74LVC_LVCH245A v.6
Modifications:	<ul style="list-style-type: none"> <li>Table note 4 of <a href="#">Table 6</a>: corrected (errata)</li> </ul>			
74LVC_LVCH245A v.6	20111125	Product data sheet	-	74LVC_LVCH245A v.5
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 4</a>, <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a>, and <a href="#">Table 9</a>: values added for lower voltage ranges.</li> </ul>			
74LVC_LVCH245A v.5	20090825	Product data sheet	-	74LVC_LVCH245A v.4
74LVC_LVCH245A v.4	20090703	Product data sheet	-	74LVC_LVCH245A v.3
74LVC_LVCH245A v.3	20030507	Product specification	-	74LVC245A_74LVCH245A v.2
74LVC245A_74LVCH245A v.2	20020620	Product specification	-	74LVC245A_74LVCH245A v.1
74LVC245A_74LVCH245A v.1	19971219	Product specification	-	-

## 14. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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