



# THE DATASHEET OF STS4DNF60L





# STS4DNF60L

N-channel 60 V, 0.045  $\Omega$ , 4 A, SO-8  
STripFET™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS4DNF60L	60V	<0.055 $\Omega$	4A

- Standard outline for easy automated surface mount assembly
- Low threshold drive

## Application

- Switching applications

## Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

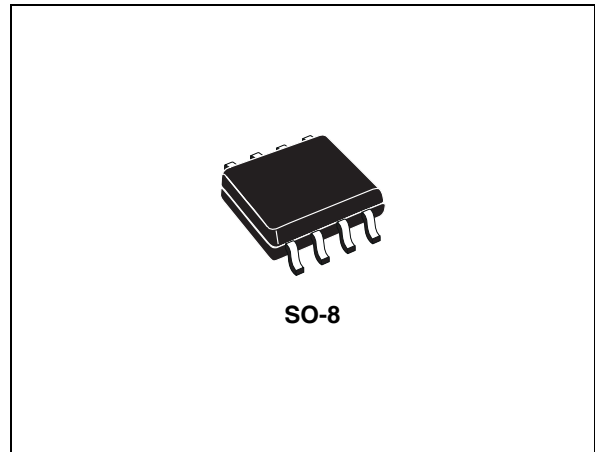


Figure 1. Internal schematic diagram

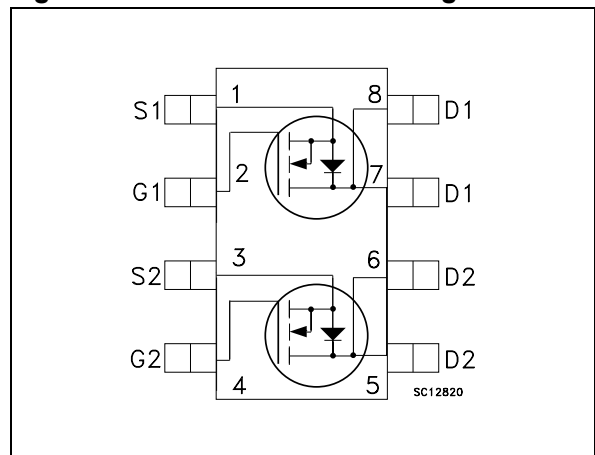


Table 1. Device summary

Order code	Marking	Package	Packaging
STS4DNF60L	4DF60L	SO-8	Tape & reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	60	V
$V_{GS}$	Gate- source voltage	$\pm 15$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	4	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	2.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	16	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	80	mJ
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	- 55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2.  $P_{TOT}=1.6\text{ W}$  for single operation
3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = 4\text{ A}$ ,  $V_{DD} = 30\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$	Thermal resistance junction-pcb D.O. <sup>(1)</sup>	62.5	$^\circ\text{C/W}$

1. When mounted on inch<sup>2</sup> FR-4 board, 2 Oz Cu,  $t \leq 10\text{sec}$ , dual operation

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	60			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 15\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 2\text{ A}$		0.045 0.050	0.055 0.065	$\Omega$ $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}$	Forward transconductance	$V_{DS} = 25\text{ V}$ , $I_D = 2\text{ A}$	-	25	-	S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1030 140 40	-	pF pF pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 48\text{ V}$ , $I_D = 4\text{ A}$ , $V_{GS} = 4.5\text{ V}$ (see <a href="#">Figure 13</a> )	-	15 4 4	-	nC nC nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD} = 30\text{ V}$ , $I_D = 2.2\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 12</a> )	-	15 28	-	ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time		-	45 10	-	ns ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4\text{ A}$ , $V_{GS} = 0$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		85		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 20\text{ V}$	-	85		nC
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 17</a> )		2		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

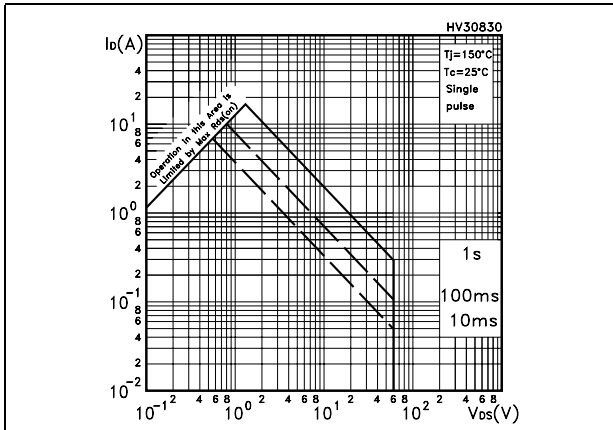


Figure 3. Thermal impedance

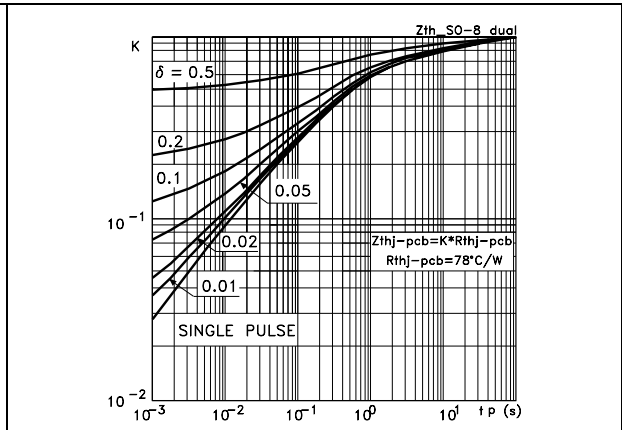


Figure 4. Output characteristics

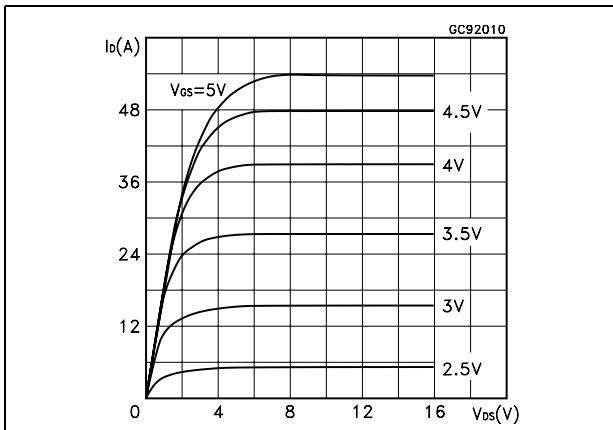


Figure 5. Transfer characteristics

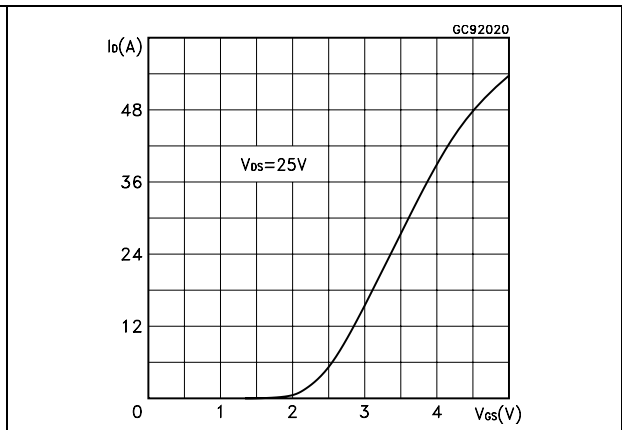


Figure 6. Source-drain diode forward characteristics

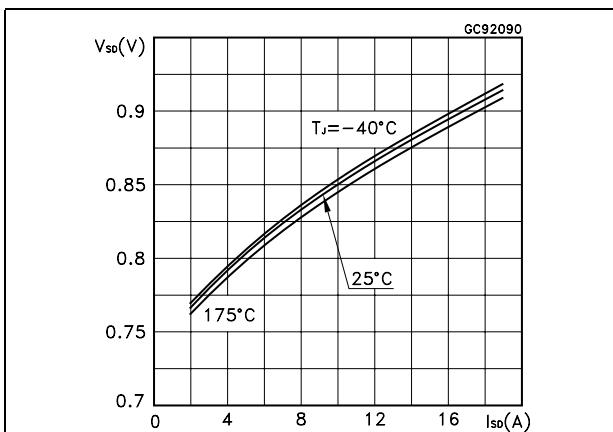


Figure 7. Static drain-source on resistance

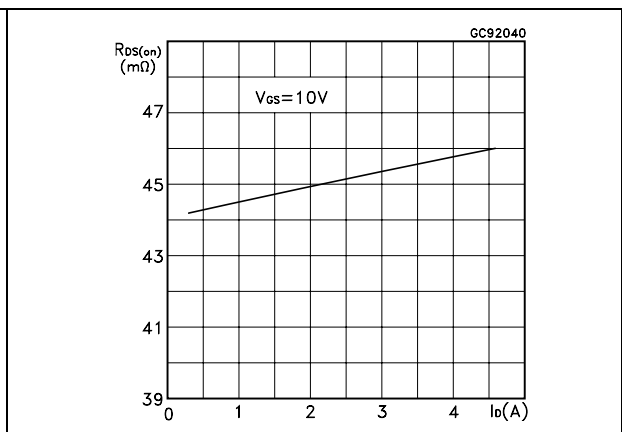


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

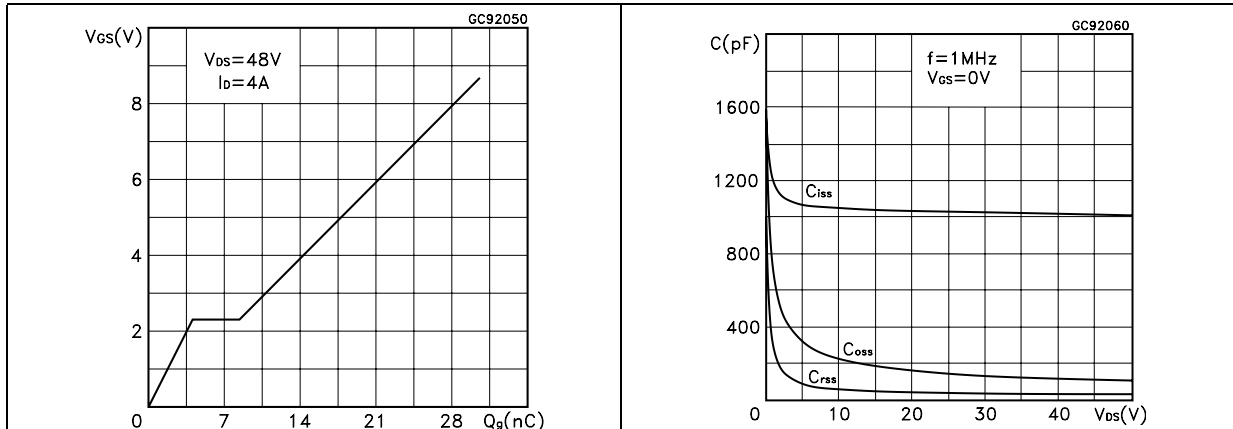
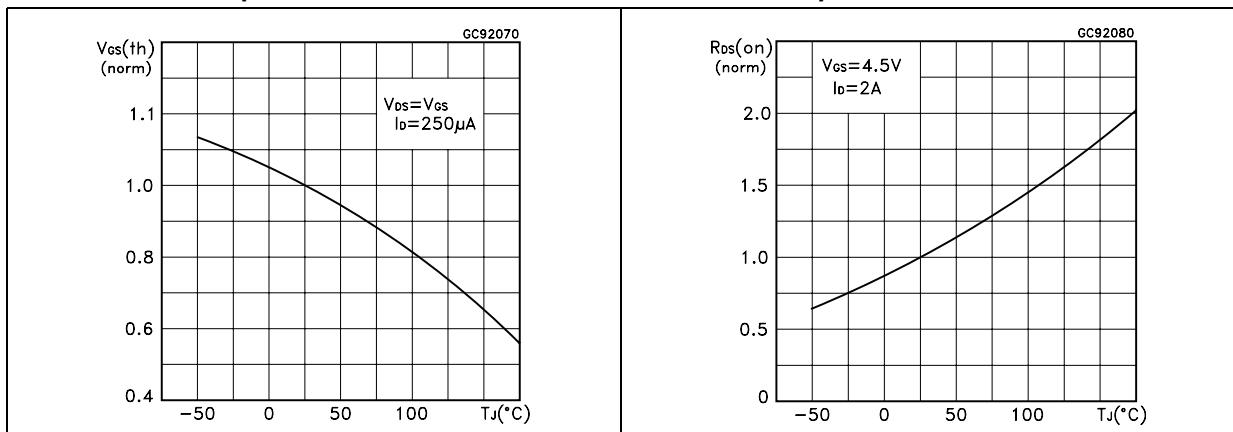
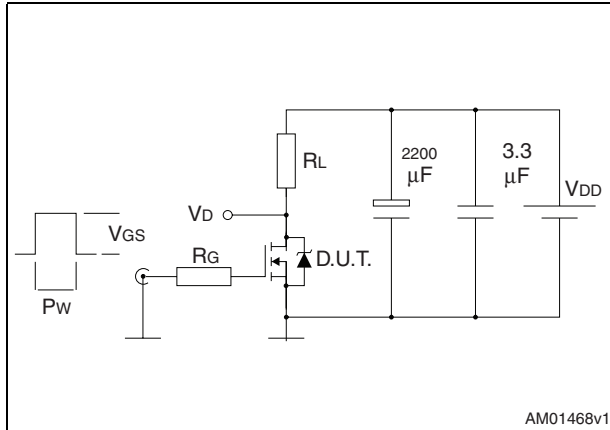


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

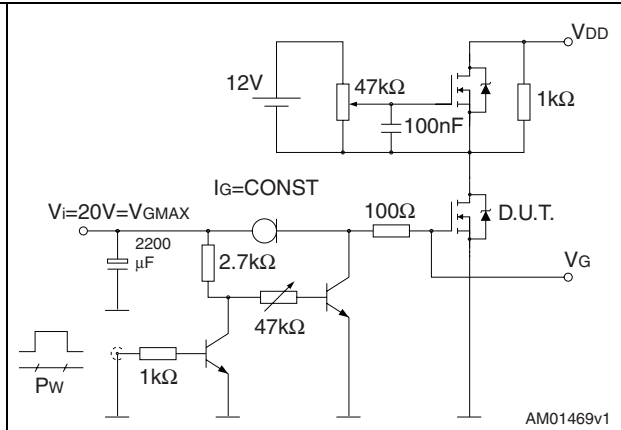


### 3 Test circuits

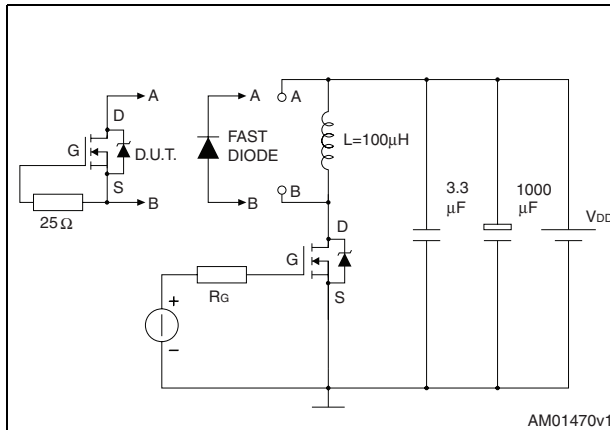
**Figure 12. Switching times test circuit for resistive load**



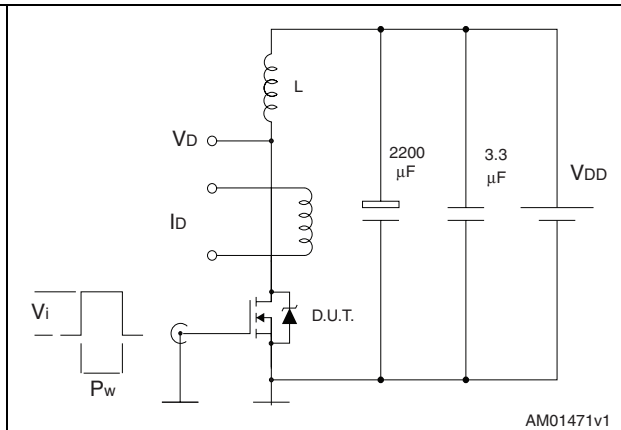
**Figure 13. Gate charge test circuit**



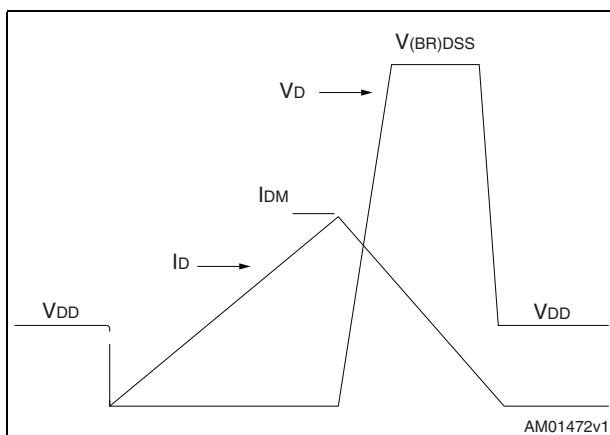
**Figure 14. Test circuit for inductive load switching and diode recovery times**



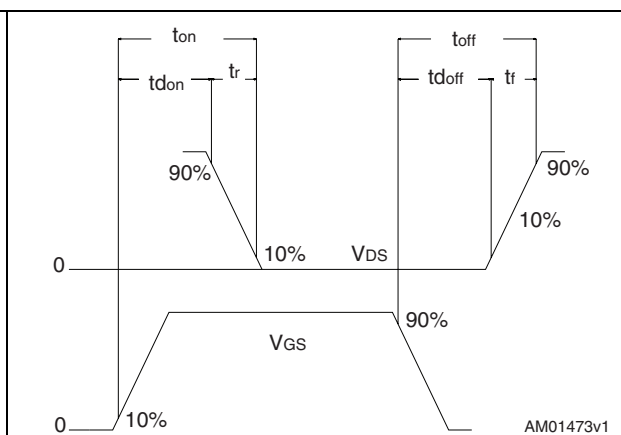
**Figure 15. Unclamped Inductive load test circuit**



**Figure 16. Unclamped inductive waveform**



**Figure 17. Switching time waveform**

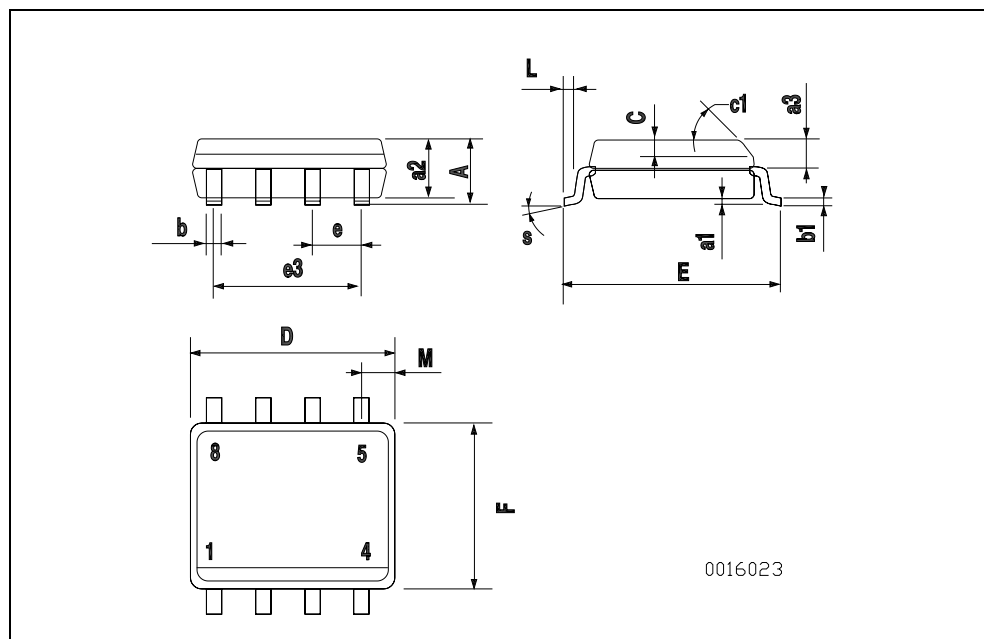


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
30-May-2005	5	Initial electronic version
29-Mar-2006	6	Modified <a href="#">Figure 2</a> and <a href="#">Figure 3</a>
16-May-2006	7	Modified internal schematic diagram
29-Aug-2007	8	Marking has been updated
30-Mar-2010	9	Inserted $E_{AS}$ value in <a href="#">Table 2: Absolute maximum ratings</a>

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