



**THE DATASHEET OF
74LVCH32245ABF8**





3.3V CMOS 32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

IDT74LVCH32245A

FEATURES:

- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels ($0.4\mu W$ typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in 96-ball LFBGA package

DRIVE FEATURES:

- Balanced Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

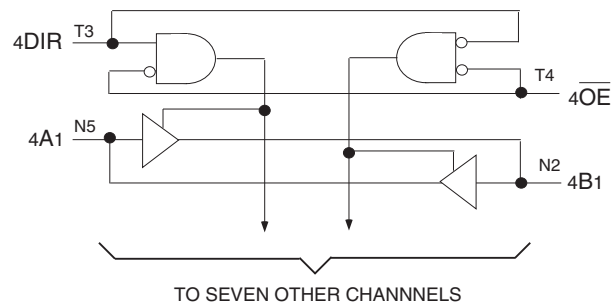
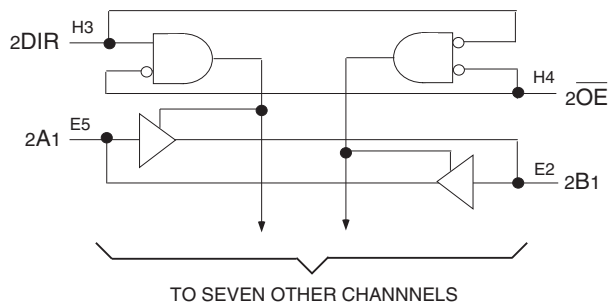
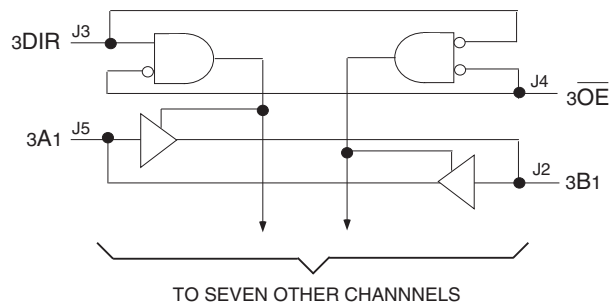
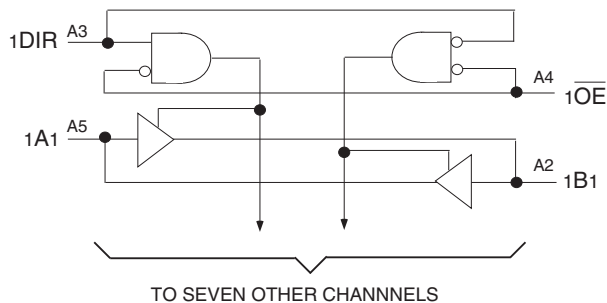
This 32-bit bus transceiver is built using advanced dual metal CMOS technology. This high-speed, low power transceiver is ideal for asynchronous communication between two busses (A and B). The Direction and Output Enable controls are designed to operate the device as either four independent 8-bit transceivers or one 32-bit transceiver. The direction control pins (DIR) control the direction of data flow. The output enable pins (OE) override the direction control and disable both ports. All inputs are designed with hysteresis for improved noise margin.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH32245A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance

The LVCH32245A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

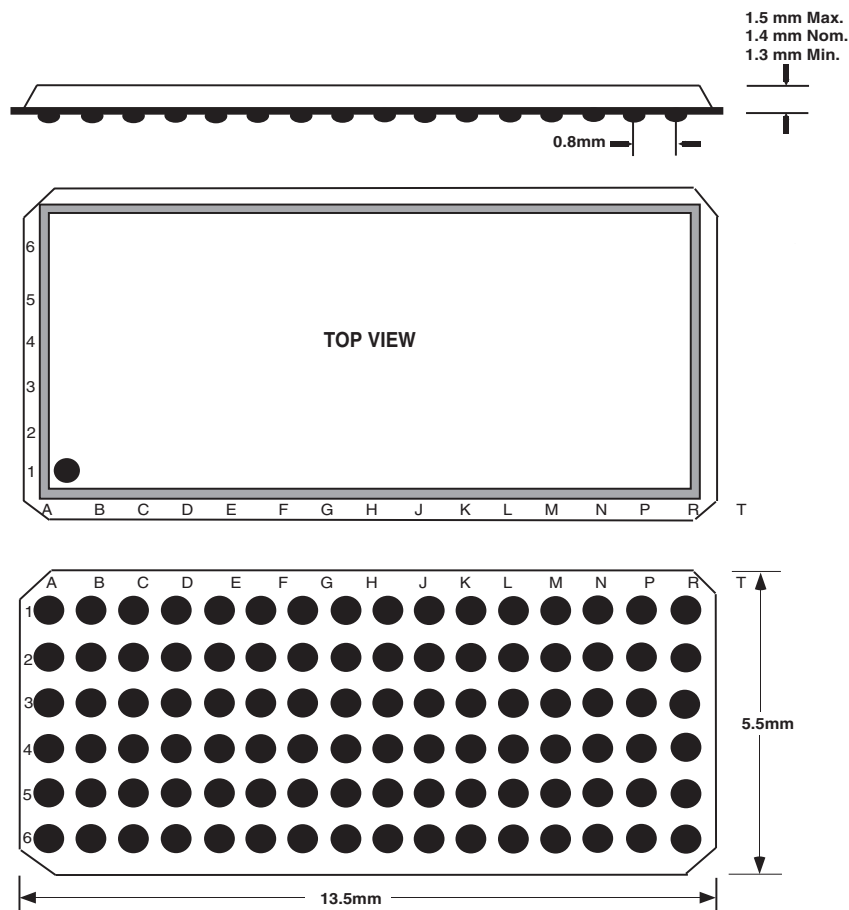


PIN CONFIGURATION

| | | | | | | | | | | | | | | | | |
|---|-------------------|-----|-----|-----|-----|-----|-----|-------------------|-------------------|-----|-----|-----|-----|-----|-----|-------------------|
| 6 | 1A2 | 1A4 | 1A6 | 1A8 | 2A2 | 2A4 | 2A6 | 2A7 | 3A2 | 3A4 | 3A6 | 3A8 | 4A2 | 4A4 | 4A6 | 4A7 |
| 5 | 1A1 | 1A3 | 1A5 | 1A7 | 2A1 | 2A3 | 2A5 | 2A8 | 3A1 | 3A3 | 3A5 | 3A7 | 4A1 | 4A3 | 4A5 | 4A8 |
| 4 | 1 \overline{OE} | GND | VCC | GND | GND | VCC | GND | 2 \overline{OE} | 3 \overline{OE} | GND | VCC | GND | GND | VCC | GND | 4 \overline{OE} |
| 3 | 1DIR | GND | VCC | GND | GND | VCC | GND | 2DIR | 3DIR | GND | VCC | GND | GND | VCC | GND | 4DIR |
| 2 | 1B1 | 1B3 | 1B5 | 1B7 | 2B1 | 2B3 | 2B5 | 2B8 | 3B1 | 3B3 | 3B5 | 3B7 | 4B1 | 4B3 | 4B5 | 4B8 |
| 1 | 1B2 | 1B4 | 1B6 | 1B8 | 2B2 | 2B4 | 2B6 | 2B7 | 3B2 | 3B4 | 3B6 | 3B8 | 4B2 | 4B4 | 4B6 | 4B7 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T |

LFBGA
TOPVIEW

96 BALL LFBGA PACKAGE ATTRIBUTES



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|------------------------------------|---|--------------|------|
| VTERM | Terminal Voltage with Respect to GND | -0.5 to +6.5 | V |
| TSTG | Storage Temperature | -65 to +150 | °C |
| IOUT | DC Output Current | -50 to +50 | mA |
| I _{IK} I _{OK} | Continuous Clamp Current, V _I < 0 or V _O < 0 | -50 | mA |
| I _{CC} I _{SS} | Continuous Current through each V _{CC} or GND | ±100 | mA |

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 4.5 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 6.5 | 8 | pF |
| C _{I/O} | I/O Port Capacitance | V _{IN} = 0V | 6.5 | 8 | pF |

NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

| Pin Names | Description |
|------------------|---|
| \overline{xOE} | Output Enable Input (Active LOW) |
| xDIR | Direction Control Input |
| xAx | Side A Inputs or 3-State Outputs ⁽¹⁾ |
| xBx | Side B Inputs or 3-State Outputs ⁽¹⁾ |

NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE⁽¹⁾

| Inputs | | Outputs |
|------------------|------|---------------------|
| \overline{xOE} | xDIR | |
| L | L | Bus B data to Bus A |
| L | H | Bus A data to Bus B |
| H | X | Z |

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

BUS-HOLD CHARACTERISTICS

| Symbol | Parameter ⁽¹⁾ | Test Conditions | Min. | Typ. ⁽²⁾ | Max. | Unit |
|----------------|----------------------------------|------------------------|-----------------------------|---------------------|------|------------|
| IBHH IBHL | Bus-Hold Input Sustain Current | V _{CC} = 3V | V _I = 2V -75 | — | — | μA |
| | | | V _I = 0.8V 75 | — | — | |
| IBHH IBHL | Bus-Hold Input Sustain Current | V _{CC} = 2.3V | V _I = 1.7V — | — | — | μA |
| | | | V _I = 0.7V — | — | — | |
| IBHHO IBHLO | Bus-Hold Input Overdrive Current | V _{CC} = 3.6V | V _I = 0 to 3.6V | — | — | ±500 μA |

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--|--|---|---|------|---------------------|------|------|
| V _{IH} | Input HIGH Voltage Level | V _{CC} = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | V _{CC} = 2.7V to 3.6V | | 2 | — | — | |
| V _{IL} | Input LOW Voltage Level | V _{CC} = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | V _{CC} = 2.7V to 3.6V | | — | — | 0.8 | |
| I _{IH} I _{IL} | Input Leakage Current | V _{CC} = 3.6V | V _I = 0 to 5.5V | — | — | ±5 | μA |
| I _{OZH} I _{OZL} | High Impedance Output Current (3-State Output pins) | V _{CC} = 3.6V | V _O = 0 to 5.5V | — | — | ±10 | μA |
| I _{OFF} | Input/Output Power Off Leakage | V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V | | — | — | ±50 | μA |
| V _{IK} | Clamp Diode Voltage | V _{CC} = 2.3V, I _{IN} = -18mA | | — | -0.7 | -1.2 | V |
| V _H | Input Hysteresis | V _{CC} = 3.3V | | — | 100 | — | mV |
| I _{CC1} I _{CC2} I _{CC3} | Quiescent Power Supply Current | V _{CC} = 3.6V | V _{IN} = GND or V _{CC} | — | — | 10 | μA |
| | | | 3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾ | — | — | 10 | |
| ΔI _{CC} | Quiescent Power Supply Current Variation | One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND | | — | — | 500 | μA |

NOTES:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|-----------------|---------------------|--------------------------------|--------------------------|-----------------------|------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} = 2.3V to 3.6V | I _{OH} = -0.1mA | V _{CC} - 0.2 | — | V |
| | | V _{CC} = 2.3V | I _{OH} = -6mA | 2 | — | |
| | | V _{CC} = 2.3V | I _{OH} = -12mA | 1.7 | — | |
| | | V _{CC} = 2.7V | | 2.2 | — | |
| | | V _{CC} = 3V | | 2.4 | — | |
| | | V _{CC} = 3V | I _{OH} = -24mA | 2.2 | — | |
| V _{OL} | Output LOW Voltage | V _{CC} = 2.3V to 3.6V | I _{OL} = 0.1mA | — | 0.2 | V |
| | | V _{CC} = 2.3V | I _{OL} = 6mA | — | 0.4 | |
| | | | I _{OL} = 12mA | — | 0.7 | |
| | | V _{CC} = 2.7V | I _{OL} = 12mA | — | 0.4 | |
| | | V _{CC} = 3V | I _{OL} = 24mA | — | 0.55 | |

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

| Symbol | Parameter | Test Conditions | Typical | Unit |
|--------|--|---------------------------|---------|------|
| CPD | Power Dissipation Capacitance per Transceiver Outputs enabled | $C_L = 0pF$, $f = 10MHz$ | 76 | pF |
| CPD | Power Dissipation Capacitance per Transceiver Outputs disabled | | 8 | |

SWITCHING CHARACTERISTICS⁽¹⁾

| Symbol | Parameter | $V_{CC} = 2.7V$ | | $V_{CC} = 3.3V \pm 0.3V$ | | Unit |
|------------------------|---|-----------------|------|--------------------------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t_{PLH} t_{PHL} | Propagation Delay xAx to xBx, xBx to xAx | 1.5 | 4.7 | 1 | 4 | ns |
| t_{PZH} t_{PZL} | Output Enable Time \overline{xOE} to xAx or xBx | 1.5 | 6.7 | 1.5 | 5.5 | ns |
| t_{PHZ} t_{PLZ} | Output Disable Time \overline{xOE} to xAx or xBx | 1.5 | 7.1 | 1.5 | 6.6 | ns |
| t_{PZH} t_{PZL} | Output Enable Time xDIR to xAx or xBx | 1.5 | 7 | 1.5 | 5.5 | ns |
| t_{PHZ} t_{PLZ} | Output Disable Time xDIR to xAx or xBx | 1.5 | 7.4 | 1.5 | 6.6 | ns |
| tsk(o) | Output Skew ⁽²⁾ | — | — | — | 500 | ps |

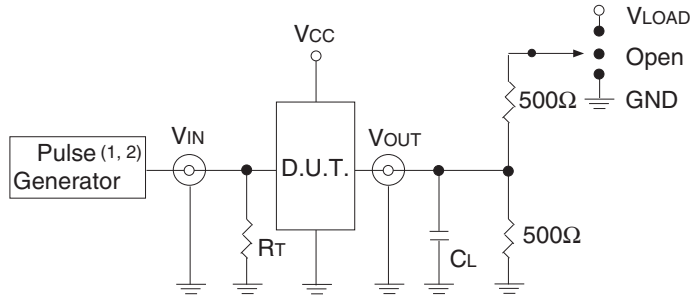
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. $T_A = -40^\circ C$ to $+85^\circ C$.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

| Symbol | V _{CC} ⁽¹⁾ =3.3V±0.3V | V _{CC} ⁽¹⁾ =2.7V | V _{CC} ⁽²⁾ =2.5V±0.2V | Unit |
|-------------------|---|--------------------------------------|---|------|
| V _{LOAD} | 6 | 6 | 2 x V _{CC} | V |
| V _{IH} | 2.7 | 2.7 | V _{CC} | V |
| V _T | 1.5 | 1.5 | V _{CC} / 2 | V |
| V _{LZ} | 300 | 300 | 150 | mV |
| V _{HZ} | 300 | 300 | 150 | mV |
| C _L | 50 | 50 | 30 | pF |



Test Circuit for All Outputs

DEFINITIONS:

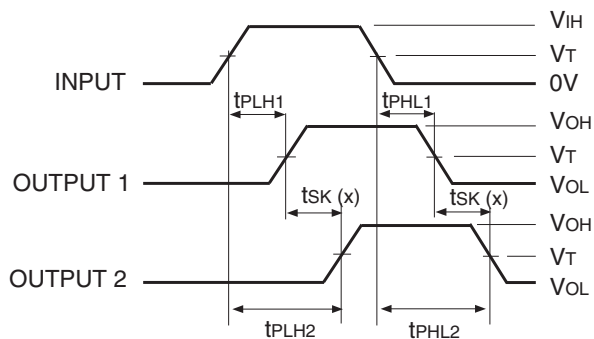
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

| Test | Switch |
|---|-------------------|
| Open Drain Disable Low Enable Low | V _{LOAD} |
| Disable High Enable High | GND |
| All Other Tests | Open |

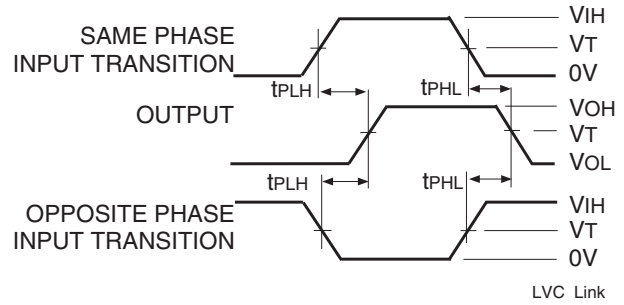


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

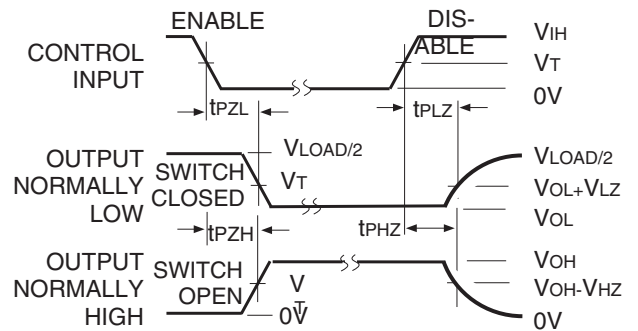
Output Skew - tsk(x)

NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



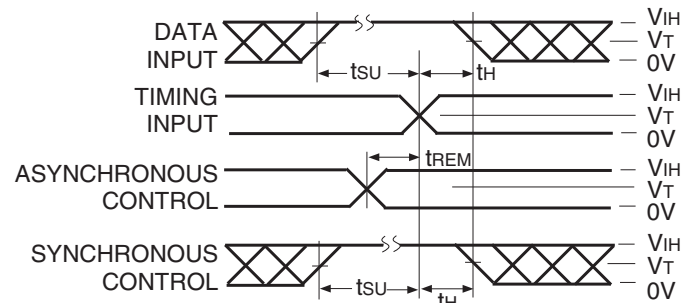
Propagation Delay



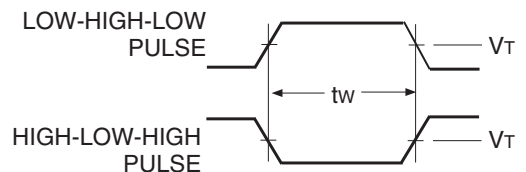
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

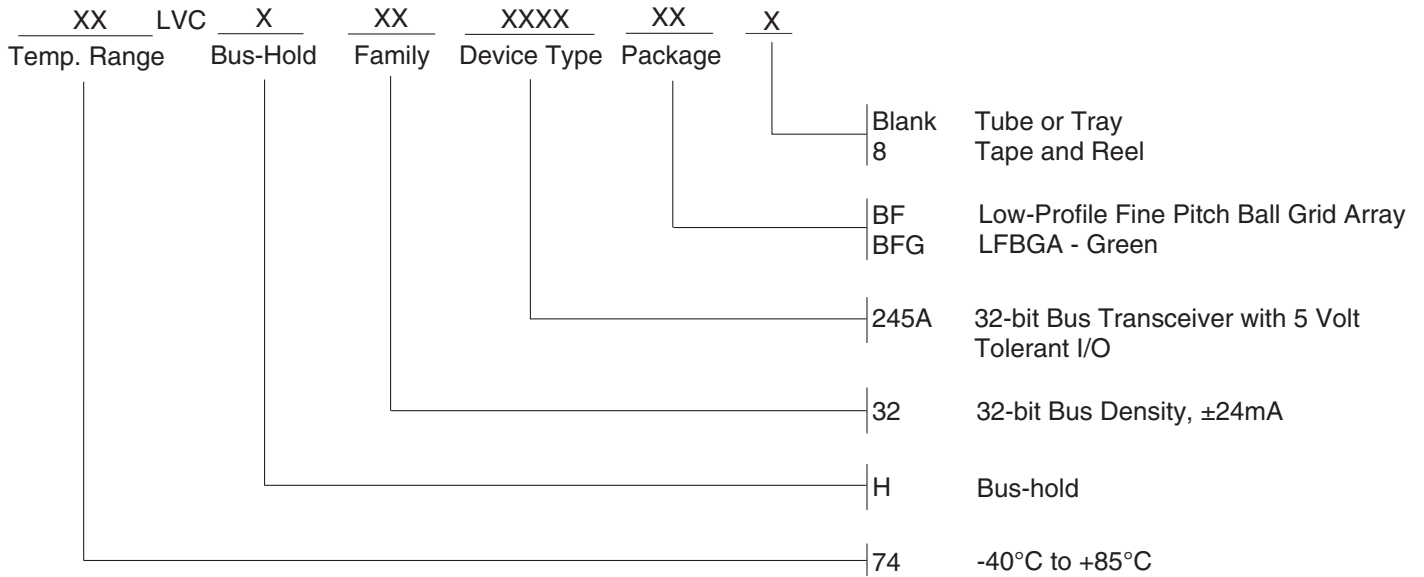


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



Datasheet Document History

02/29/2016 Pg.7 Updated the ordering information by adding Tape and Reel.



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