THE DATASHEET OF

STW5093CYLT

www.win-source.net 0086-755-83957316

STw5093

2.7V SUPPLY 14-BIT LINEAR CODEC WITH HIGH-PERFORMANCE AUDIO FRONT-END

FEATURES:

Complete CODEC and FILTER system including:

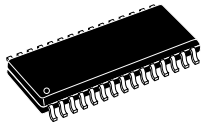
- 14 BIT LINEAR ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS.
- 8 BIT COMPANDED ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS A-LAW OR μ-LAW.
- TRANSMIT AND RECEIVE BAND-PASS FILTERS
- ACTIVE ANTIALIAS NOISE FILTER.

Phone Features:

- ONE MICROPHONE BIASING OUTPUT
- REMOTE CONTROL (REMOCON) FUNCTION
- THREE SWITCHABLE MICROPHONE AMPLIFIER INPUTS. GAIN PROGRAMMABLE:0 . . 42.5 dB AMPLIFIER, 1.5 dB STEPS (+ MUTE).
- EARPIECE AUDIO OUTPUT. ATTENUATION PROGRAMMABLE: 0 . . 30 dB, 2 dB STEPS.
- EXTERNAL AUDIO OUTPUT. ATTENUATION PROGRAMMABLE: 0 . . 30 dB, 2 dB STEPS.
- DRIVING CAPABILITY: 140mW OVER 8Ω
- TRANSIENT SUPRESSION SIGNAL DURING POWER ON AND DURING AMPLIFIER SWITCHING.
- INTERNAL PROGRAMMABLE SIDETONE CIRCUIT. ATTENUATION PROGRAMMABLE: 16 dB RANGE, 1 dB STEP.
- INTERNAL RING, TONE AND DTMF GENERATOR, SINEWAVE OR SQUAREWAVE WAVEFORMS. ATTENUATION PROGRAMMABLE: 27dB RANGE, 3dB STEP. THREE FREQUENCY RANGES:
  - a) 3.9Hz . . . . 996Hz, 3.9Hz STEP
  - b) 7.8Hz . . . . 1992Hz, 7.8Hz STEP
  - c) 15.6Hz . . . . 3984Hz, 15.6Hz STEP
- PROGRAMMABLE PULSE WIDTH MODULATED BUZZER DRIVER OUTPUT.

General Features:

- SINGLE 2.7V to 3.3V SUPPLY
- EXTENDED TEMPERATURE RANGE OPERATION (*) -40°C to 85°C.
- 1.0μW STANDBY POWER (TYP. AT 2.7V).
- 13mW OPERATING POWER (TYP. AT 2.7V).



TSSOP30
ORDERING NUMBER: STw5093

- **1.8V TO 3.3V CMOS COMPATIBLE DIGITAL INTERFACES.**
- PROGRAMMABLE PCM AND CONTROL INTERFACE MICROWIRE COMPATIBLE.

APPLICATIONS:

- GSM/DCS1800/PCS1900/JDC DIGITAL CELLULAR TELEPHONES.
- CDMA CELLULAR TELEPHONES.
- DECT/CT2/PHS DIGITAL CORDLESS TELEPHONES.
- BATTERY OPERATED AUDIO FRONT-ENDS FOR DSPs.

(*) Functionality guaranteed in the range - 40°C to +85°C; Timing and Electrical Specifications are guaranteed in the range - 30°C to +85°C.

GENERAL DESCRIPTION

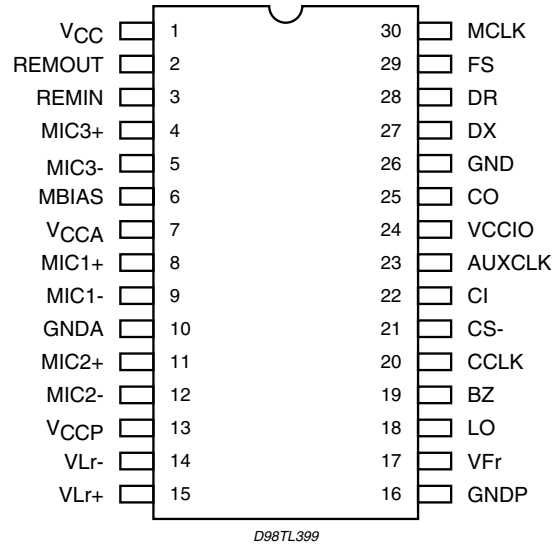
STw5093 is a high performance low power combined PCM CODEC/FILTER device tailored to implement the audio front-end functions required by low voltage/low power consumption digital cellular terminals. STw5093 offers a number of programmable functions accessed through a serial control channel that easily interfaces to any classical microcontroller. The PCM interface supports both non-delayed (normal and reverse) and delayed frame synchronization modes.

STw5093 can be configurated either as a 14-bit linear or as an 8-bit companded PCM coder.

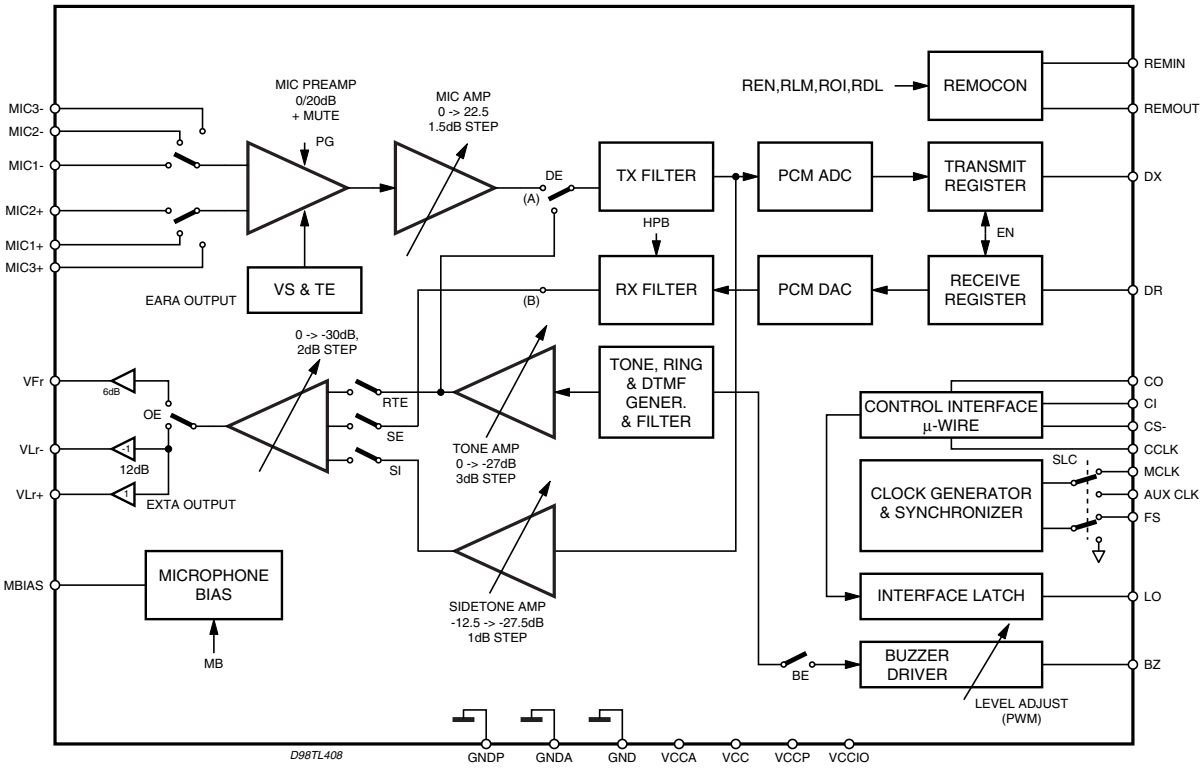
Additionally to the CODEC/FILTER function, STw5093 includes a Tone/Ring/DTMF generator, a sidetone generation, and a buzzer driver output.STw5093 fulfills and exceeds D3/D4 and CCITT recommendations and ETSI requirements for digital handset terminals.

Main applications include digital mobile phones, as cellular and cordless phones, or any battery powered equipment that requires audio codecs operating at low single supply voltages.

PIN CONNECTIONS (Top view)



BLOCK DIAGRAM



PIN FUNCTION

N°	Pin	Description
1	V_{CC}	Power supply input for the digital section.
2	REMOUT	Remocon function digital output.
3	REMIN	Remocon function input. An high level at this pin is detected as a non pressed key, while a low level is detected as a pressed key.
4	MIC3+	Third positive high impedance input to transmit preamplifier for microphone connection.
5	MIC3-	Third negative high impedance input to transmit preamplifier for microphone connection.
6	MBIAS	Microphone Biasing Switch.
7	V_{CCA}	Power supply input for the analog section. V_{CC} and V_{CCA} can be directly connected together for low cost applications (see STw5093 Power Supply Notes).
8	MIC1+	Positive high impedance input to transmit pre-amplifier for microphone connection.
9	MIC1-	Negative high impedance input to transmit pre-amplifier for microphone connection.
10	GNDA	Analog Ground: All analog signals are referenced to this pin. GND and GNDA can be connected together for low cost applications (see STw5093 Power Supply Notes).
11	MIC2+	Second Positive high impedance input to transmit pre-amplifier for microphone connection.
12	MIC2-	Second negative high impedance input to transmit pre-amplifier for microphone connection.
13	V_{CCP}	Power supply input for the V_{Fr} and V_{Lr} drivers. V_{CCP} and V_{CCA} must be connected together.
14,15	V_{Lr-}, V_{Lr+}	Receive analog extra amplifier complementary outputs. These outputs can drive directly earpiece transductor of 8Ω or 50nF. The signal at these outputs can be the sum of: - Receive Speech signal from DR, - Internal Tone generator, - Sidetone signal.
16	GNDP	Power ground. V_{Fr} and V_{Lr} drivers are referenced to this pin. GNDP and GNDA must be connected together.
17	V_{Fr}	Receive analog earpiece amplifier output. This output can drive directly earpiece transductor of 30Ω or 50nF. The signal at this output can be the sum of: - Receive Speech signal from D_R, - Internal Tone Generator, - Sidetone signal.
18	LO	A logic 1 written into DO (CR1) appears at LO pin as a logic 0 A logic 0 written into DO (CR1) appears at LO pin as a logic 1.
19	BZ	Pulse width modulated buzzer driver output.
20	CCLK	Control Clock input: This clock shifts serial control information into CI and out from CO when the CS- input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
21	CS-	Chip Select input: When this pin is low, control information is written into and out from the STw5093 via CI and CO pins.
22	CI	Control data Input: Serial Control information is shifted into the STw5093 on this pin when CS- is low on the rising edges of CCLK.
23	AUXCLK	Auxiliary Clock Input. Values must be 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz selected by means of Control Register CR0. AUXCLK is not used to shift in and out data

PIN FUNCTION (continued)

N°	Pin	Description
24	VCCIO	Power supply Input for the Digital I/O's.
25	CO	Control data Output: Serial control/status information is shifted out from the STw5093 on this pin when CS- is low on the falling edges of CCLK.
26	GND	Ground: All digital signals are referenced to this pin.
27	D_X	Transmit Data ouput: Data is shifted out on this pin during the assigned transmit time slots. Elsewhere DX output is in the high impedance state. In delayed and non-delayed normal frame synchr. modes, voice data byte is shifted out from TRISTATE output DX at the MCLK on the rising edge of MCLK, while in non-delayed reverse frame synchr mode voice data byte is shifted out on the falling edge of MCLK.
28	D_R	Receive data input: Data is shifted in during the assigned Received time slots In delayed and non-delayed normal frame synchr. modes voice data byte is shifted in at the MCLK frequency on the falling edges of MCLK, while in non-delayed reverse frame synchr. mode voice data byte is shifted in at the MCLK frequency on the rising edges of MCLK.
29	FS	Frame Sync input: This signal is a 8kHz clock which defines the start of the transmit and receive frames. Any of three formats may be used for this signal: non delayed normal mode, delayed mode, and non delayed reverse mode.
30	MCLK	Master Clock Input: This signal is used by the switched capacitor filters and the encoder/decoder sequencing logic. Values must be 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz selected by means of Control Register CR0. MCLK is used also to shift-in and out data.

1.0 FUNCTIONAL DESCRIPTION

1.1 DEVICE OPERATION

1.1.1 Power on initialization:

When power is first applied, power on reset circuitry initializes STw5093 and puts it into the power down state. Gain Control Registers for the various programmable gain amplifiers and programmable switches are initialized as indicated in the Control Register description section. All CODEC functions are disabled.

The desired selection for all programmable functions may be intialized prior to a power up command using the MICROWIRE control channel.

Note: after register programming, a subsequent activation of the internal Power on Reset can be detected by programming to 1 the DO bit in the CR1 register; this sets to the logic level 0 the LO output. If an internal Power on Reset occurs, LO automatically switches to logic level 1.

1.1.2 Power up/down control:

Following power-on initialization, power up and power down control may be accomplished by writing any of the control instructions listed in Table 1 into STw5093 with "P" bit set to 0 for power up or 1 for power down.

Normally, it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or in a separate single byte instruction.

Any of the programmable registers may also be modified while STw5093 is powered up or down by setting "P" bit as indicated. When power up or down control is entered as a single byte instruction, bit 1 must be set to a 0.

When a power up command is given, all de-activated circuits are activated, but output DX will remain in the high impedance state until the second Fs pulse after power up.

1.1.3 Power down state:

Following a period of activity, power down state may be reentered by writing a power down instruction.

Control Registers remain in their current state and can be changed by MICROWIRE control interface.

In addition to the power down instruction, detection of loss MCLK (no transition detected) automatically enters the device in "reset" power down state with DX output in the high impedance state.

1.1.4 Transmit section:

Transmit analog interface is designed in two stages to enable gains up to 42.5 dB to be realized. Stage 1 is a low noise differential amplifier providing a selectable 0 or 20 dB gain via bit 1 (PG) of register CR4. A microphone may be capacitevely connected to MIC1+, MIC1- inputs, while the MIC2+ MIC2Ä and MIC3+ MIC3- inputs may be used to capacitively connect a second microphone or a third microphone respectively or an auxiliary audio circuit. MIC1 or MIC2 or MC3 or transmit mute is selected with bits 6 and 7 of register CR4.

In the mute case, the analog transmit signal is grounded and the sidetone path is also disabled. Following the first stage is a programmable gain amplifier which provides from 0 to 22.5 dB of additional gain in 1.5dB step. The total transmit gain should be adjusted so that, at reference point A, see Block Diagram description, the internal 0 dBm0 voltage is 0.49 Vrms (overload level is 0.7 Vrms). Second stage amplifier gain can be programmed with bits 4 to 7 of CR5.

An active RC prefilter then precedes the 8th order band pass switched capacitor filter. A/D converter can be either a 14-bit linear (bit CM = 0 in register CR0) or can have a compressing characteristics (bit CM = 1 in register CR0) according to CCITT A or MU255 coding laws. A precision on chip voltage reference ensures accurate and highly stable transmission levels.

Any offset voltage arising in the gain-set amplifier, the filters or the comparator is cancelled by an internal autozero circuit.

Each encode cycle begins immediatly at the beginning of the selected Transmit time slot. The total signal delay referenced to the start of the time slot is approximatively 195 µs (due to the transmit filter) plus 125 µs (due to encoding delay), which totals 320 µs. Voice data is shifted out on DX during the selected time slot on the trans-

mit rising edges of MCLK in delayed or non-delayed normal mode or on the falling edges of MCLK in non-delayed reverse mode.A separate MBIAS output can be used to bias a microphone (bit MB = 1 in register CR10)

1.1.5 Receive section:

Voice Data is shifted into the decoder's Receive voice data Register via the DR pin during the selected time slot on the falling edges of MCLK in delayed or non-delayed normal mode or on the rising edges of MCLK in non-delayed reverse mode.

The decoder consists of either a 14-bit linear or an expanding DAC with A or MU255 law decoding characteristic. Following the Decoder is a 3400 Hz 8th order band-pass switched capacitor filter with integral Sin X/X correction for the 8 kHz sample and hold.

0 dBmO voltage at this (B) reference point (see Block Diagram description) is 0.49 Vrms. A transcient suppressing circuitry ensure interference noise suppression at power up.

The analog speech signal output can be routedeither to earpiece (VFR output) or to an extra analog output (V_{Lr+}, V_{Lr-} outputs) by setting bits OE1, OE2, and SE (4, 3, and 0 of CR4).

Total signal delay is approximatively 190µs (filter plus decoding delay) plus 62.5µs (1/2 frame) which gives approximatively 252µs.

Output VFR is intended to directly drive an earpiece. Preceding the outputs is a programmable attenuation amplifier, which must be set by writing to bits 4 to 7 in register CR6. Attenuations in the range 0 to -30 dB relative to the maximum level in 2 dB step can be programmed. The input of this programmable amplifier is the sum of several signals which can be selected by writing to register CR4.:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- Sidetone signal, the amplitude of which is programmed with bits 0 to 3 of register CR5

V_{Fr} is capable of driving output power levels up to 16.5mW into a 30Ω load impedance capacitively connected between V_{Fr+} and GND. Piezoceramic receivers up to 50nF can also be driven.

Differential outputs V_{Lr+},V_{Lr-} are intended to directly drive an extra output. Preceding the outputs is a programmable attenuation amplifier, which must be set by writing to bits 0 to 3 in register CR6. Attenuations in the range 0 to -30 dB relative to the maximum level in 2.0 dB step can be programmed. The input of this programmable amplifier can be the sum of signals which can be selected by writing to register CR4:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- Sidetone signal, the amplitude of which is programmed with bits 0 to 3 of register CR5.

V_{Lr+} and V_{Lr-} outputs are capable of driving output power level up to140mW into differentially connected load impedance of 8 Ω. Piezoceramic receivers up to 50nF can also be driven.

BUZZER OUTPUT:

Single ended output BZ is intended to drive a buzzer, via an external BJT, with a squarewave pulse width modulated (PWM) signal the frequency of which is stored into register CR8.

For some applications it is also possible to amplitude modulate this PWM signal with a squarewave signal having a frequency stored in register CR9.

Maximum load for BZ is 5kΩ and 50pF.

1.1.6 Digital Interface (Fig. 1)

F_S Frame Sync input determines the beginning of frame. It may have any duration from a single cycle of MCLK to a squarewave. Three different relationships may be established between the Frame Sync input and the first time slot of frame by setting bits DM1 and DM0 in register CR1. In non delayed data mode (long frame timing) the first time slot begins nominally coincident with the rising edge of F_S. Alternative is to use delayed data mode (short frame sync timing) in which FS input must be high at least a half cycle of MCLK earlier the frame beginning In the case of linear code (bit CM = 0 in register CR0) the MSB is the first bit that is transmitted and received.

In the case of companded code only (bit CM = 1 in register CR0) a time slot assignment circuit on chip may be used with all timing modes, allowing connection to one of the two B1 and B2 voice data channels.

Two data formats are available: in Format 1, time slot B1 corresponds to the 8 MCLK cycles following immediately the rising edge of FS, while time slot B2 corresponds to the 8 MCLK cycles following immediately time slot B1.

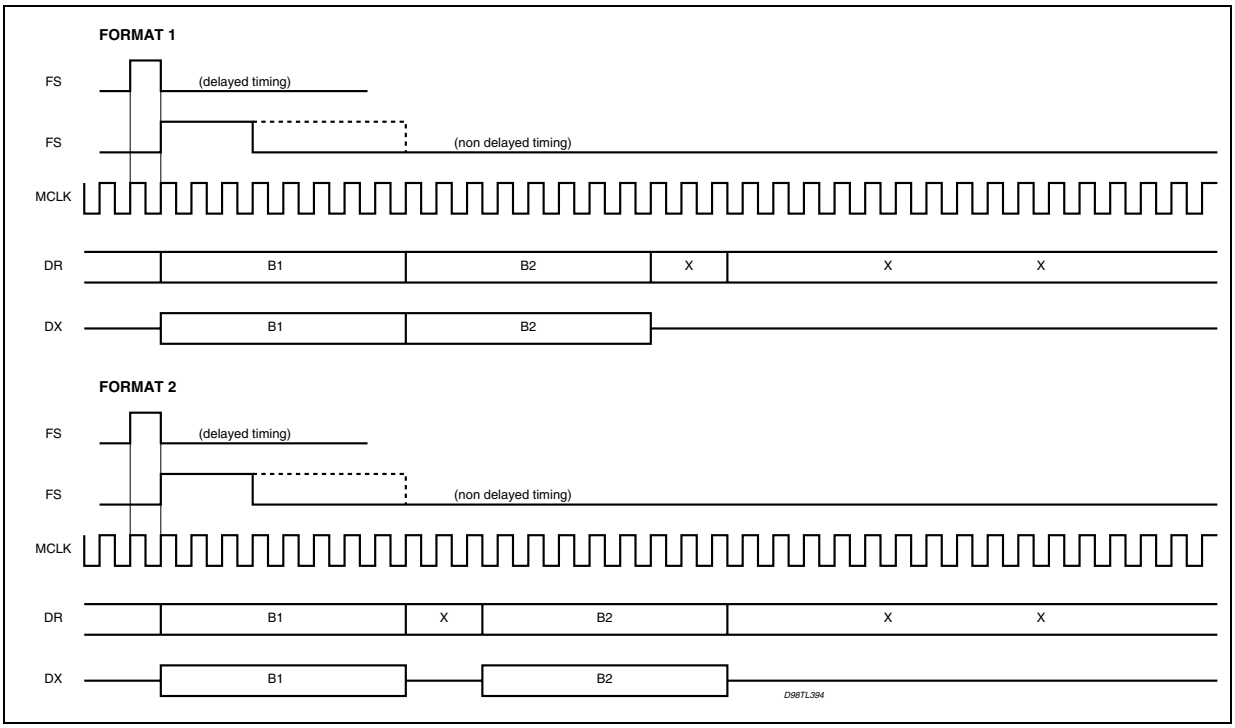
In Format 2, time slot B1 is identical to Format 1. Time slot B2 appears two bit slots after time slot B1. This two bits space is left available for insertion of the D channel data.

Data format is selected by bit FF (2) in register CR0. Time slot B1 or B2 is selected by bit TS (1) in Control Register CR1.

Bit EN (2) in control register CR1 enables or disables the voice data transfer on D_X and D_R as appropriate. During the assigned time slot, DX output shifts data out from the voice data register on the rising edges of MCLK in the case of delayed and non-delayed normal modes or on the falling edges of MCLK in the case of non-delayed reverse mode. Serial voice data is shifted into DR input during the same time slot on the falling edges of MCLK in the case of delayed and non-delayed normal modes or on the rising edges of MCLK in the case of non-delayed reverse mode.

D_X is in the high impedance Tristate condition when in the non selected time slots.

Figure 1. Digital Interface Format (significant only for companded code)



1.1.7 Control Interface:

Control information or data is written into or read-back from STw5093 via the serial control port consisting of control clock CCLK, serial data input CI and output CO, and Chip Select input, CS-. All control instructions require 2 bytes as listed in Table 1, with the exception of a single byte power-up/down command.

To shift control data into STw5093, CCLK must be pulsed high 8 times while CS- is low. Data on CI input is shifted into the serial input register on the rising edge of each CCLK pulse. After all data is shifted in, the content of the input shift register is decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide CS- pulse or may follow the first contiguously, i.e. it is not mandatory for CS- to return high in between the first and second control bytes. At the end of the 2nd control byte, data is loaded into the appropriate programmable register. CS- must return high at the end of the 2nd byte.

To read-back status information from STw5093, the first byte of the appropriate instruction is strobed in during the first CS- pulse, as defined in Table 1. CS- must be set low for a further 8 CCLK cycles, during which data is shifted out of the CO pin on the falling edges of CCLK.

When CS- is high, CO pin is in the high impedance Tri-state, enabling CO pins of several devices to be multiplexed together.

Thus, to summarise, 2 byte READ and WRITE instructions may use either two 8-bit wide CS- pulses or a single 16 bit wide CS- pulse.

1.1.8 Control channel access to PCM interface:

It is possible to access the B channel previously selected in Register CR1 in the case of companded code only.

A byte written into Control Register CR3 will be automatically transmitted from DX output in the following frame in place of the transmit PCM data.

A byte written into Control Register CR2 will beautomatically sent through the receive path to the Receive amplifiers.

In order to implement a continuous data flow from the Control MICROWIRE interface to a B channel, it is necessary to send the control byte on each PCM frame.

A current byte received on D_R input can be read in the register CR2. In order to implement a continuous data flow from a B channel to MICROWIRE interface, it is necessary to read register CR2 at each PCM frame.

1.1.9 AUXCLK usage:

The Auxiliary clock AUXCLK is only used to keep active the tone and buzzer generation functions to the Earpiece or to the Extra amplifier outputs when the Master Clock MCLK is not available, and there is no voice activity both in transmit and receive channels. When AUXCLK is selected, the PCM digital interface is inactive (DX in tristate and DR is not read). The selection between AUXCLK and MCLK is done by bit SLC in register CR1The input frequency of AUXCLK is selected via bits F1 and F0 of register CR0 as for the MCLK signal.

1.1.10 REMOCON function:

The REMOCON (Remote Control) function can be used to detect the status of an headset button.

The REMOCON function is enabled by setting bit REN (7 of CR10). If enabled, this function is active also when the STw5093 is in Power-down state.

At REMIN input an high level is detected as a non pressed button, while a low level is detected as a pressed button.

The "Pressed Button" information can be treated in 2 ways depending on bit RLM (6 of CR10):

- if RLM = 0 (Transparent mode) the information at REMIN is seen at REMOUT after a debounce time of 50ms maximum.
- if RLM = 1 (Latched Mode) the information stored in bit RDL (4 of CR10) is seen at REMOUT.When a low level at REMIN is detected RDL is set after a debounce time of 50ms maximum.RDL is reset at power on reset and can also be reset writing CR10.

The REMOUT output polarity can be inverted setting bit ROI (5 of CR10):the pressed button information is presented at REMOUT output as a logic 1 if bit ROI = 0. If ROI = 1 the polarity is inverted.

2.0 PROGRAMMABLE FUNCTIONS

The programmable functions are configured by writing to a number of registers using a 2-byte write cycle. Most of these registers can also be read-back for verification. Byte one is always register address, while byte two is Data. Table 1 lists the register set and their respective adresses.

Table 1. Programmable Register Intructions

Function	Address byte								Data byte
	7	6	5	4	3	2	1	0	
Single byte Power up/down	P	X	X	X	X	X	0	X	none
Write CR0	P	0	0	0	0	0	1	X	see CR0 TABLE 2
Read-back CR0	P	0	0	0	0	1	1	X	see CR0
Write CR1	P	0	0	0	1	0	1	X	see CR1 TABLE 3
Read-back CR1	P	0	0	0	1	1	1	X	see CR1
Write Data to receive path	P	0	0	1	0	0	1	X	see CR2 TABLE 4
Read data from DR	P	0	0	1	0	1	1	X	see CR2
Write Data to DX	P	0	0	1	1	0	1	X	see CR3 TABLE 5
Write CR4	P	0	1	0	0	0	1	X	see CR4 TABLE 6
Read-back CR4	P	0	1	0	0	1	1	X	see CR4
Write CR5	P	0	1	0	1	0	1	X	see CR5 TABLE 7
Read-back CR5	P	0	1	0	1	1	1	X	see CR5
Write CR6	P	0	1	1	0	0	1	X	see CR6 TABLE 8
Read-back CR6	P	0	1	1	0	1	1	X	see CR6
Write CR7	P	0	1	1	1	0	1	X	see CR7 TABLE 9
Read-back CR7	P	0	1	1	1	1	1	X	see CR7
Write CR8	P	1	0	0	0	0	1	X	see CR8 TABLE 10
Read-back CR8	P	1	0	0	0	1	1	X	see CR8
Write CR9	P	1	0	0	1	0	1	X	see CR9 TABLE 11
Read-back CR9	P	1	0	0	1	1	1	X	see CR9
Write CR10	P	1	0	1	0	0	1	X	see CR10 TABLE 12
Read-back CR10	P	1	0	1	0	1	1	X	see CR10
Write CR11	P	1	0	1	1	0	1	X	see CR11 TABLE 13
Read-back CR11	P	1	0	1	1	1	1	X	see CR11
Write Test Register CR12	P	1	1	0	0	0	1	X	reserved
Write Test Register CR13	P	1	1	0	1	0	1	X	reserved
Write Test Register CR14	P	1	1	1	0	0	1	X	reserved

Notes: 1. bit 7 of the address byte and data byte is always the first bit clocked into or out from: CI and CO pins when MICROWIRE serial port is enabled.
X = reserved: write 0
2. "P" bit is Power up/down Control bit. P = 1 Means Power Down.Bit 1 indicates, if set, the presence of a second byte.
3. Bit 2 is write/read select bit.
4. Registers CR12, CR13, and CR14 are not accessible.

Table 2. Control Register CR0 Functions

7	6	5	4	3	2	1	0	Function	
F1	F0	CM	MA	IA	FF	B7	DL		
0 0 1 1	0 1 0 1							MCLK or AUXCLK = 512 kHz * MCLK or AUXCLK = 1.536 MHz MCLK or AUXCLK = 2.048 MHz MCLK or AUXCLK = 2.560 MHz	
		0 1						Linear code * Companded code	
								Linear Code	Companed Code
			0 0 1 1	0 1 0 1				2-complement * sign and magnitude 2-complement 1-complement	MU-law: CCITT D3-D4 * MU-law: Bare Coding A-law including even bit inversion A-law: Bare Coding
					0 1			B1 and B2 consecutive * (1) B1 and B2 separated (1)	
						0 1		8 bits time-slot * (1) 7 bits time-slot (1)	
							0 1	Normal operation * Digital Loop-back *	

*: state at power on initialization
(1): significant in companded mode only

Table 3. Control Register CR1 Functions

7	6	5	4	3	2	1	0	Function
DM1	DM0	DO	MR	MX	EN	TS	SLC	
0 1 1	X 0 1							delayed data timing * non-delayed normal data timing non-delayed reverse data timing
		0 1						L0 latch set to 1 * L0 latch set to 0
			0 1					D_R connected to rec. path * CR2 connected to rec. path (1)
				0 1				Trans path connected to D_X * CR3 connected to D_X (1)
					0 1			voice data transfer disable * voice data transfer enable
						0 1		B1 channel selected * B2 channel selected (1)
							0 1	MCLK Master Clock and FS Frame Sync inputs are selected * AUXCLK Auxiliary Clock input is selected

*: state at power on initialization
(1): significant in companded mode only
X: reserved: write 0

Table 4. Control Register CR2 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	Data sent to Receive path or Data received from DR input (1)

(1) Significant in companded mode only.

Table 5. Control Registers CR3 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	DX data transmitted (1)

(1) Significant in companded mode only.

Table 6. Control Register CR4 Functions

7	6	5	4	3	2	1	0	Function
VS	TE	SI	OE1	OE2	RTE	HPB	SE	
0 0 1 1	0 1 0 1							Transmit input muted * MIC1 Selected MIC2 Selected MIC3 Selected
		0 1						Internal sidetone disabled * Internal sidetone enabled
			0 0 1 1	0 1 0 1				Receive output muted * VFr output selected VLr output selected NOT ALLOWED
					0 1			Ring / Tone to V_{Fr} or V_{Lr} disabled * Ring / Tone to V_{Fr} or V_{Lr} enabled
						0 1		Receive High Pass filter enabled * Receive High Pass filter disabled
							0 1	Receive Signal to V_{Fr} or V_{Lr} disabled * Receive Signal to V_{Fr} or V_{Lr} enabled

*: state at power on initialization

Table 7. Control Register CR5 Functions

7	6	5	4	3	2	1	0	Function
Transmit amplifier				Sidetone amplifier				
0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1				lsb	0 dB gain * 1.5 dB gain in 1.5 dB step 22.5 dB gain
				0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1	-12.5 dB gain * -13.5 dB gain in 1 dB step -27.5 dB gain

*: state at power on initialization

Table 8. Control Register CR6 Functions

7	6	5	4	3	2	1	0	Function
Earpiece ampifier [EARA]				Extra amplifier [EXTA]				
0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1				lsb	0 dB gain * -2 dB gain in 2 dB step -30 dB gain
				0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1	0 dB gain * -2 dB gain in 2 dB step -30 dB gain

*: state at power on initialization

Table 9. Control Register CR7 Functions

7	6	5	4	3	2	1	0	Function		
Tone gain				F1	F2	SN	DE	Attenuation	f1 V_{PP}	f2 V_{PP}
0 0 0 0 0 0 0 0 1 1	0 0 0 0 1 1 1 1 X X	0 0 1 1 0 0 1 1 X X	0 1 0 1 0 1 0 1 0 1					0 dB * -3 dB -6 dB - 9 dB -12 dB -15 dB -18 dB -21 dB -24 dB -27 dB	1.6(2) 0.066	1.26(2) 0.053
				0 0 1 1	0 1 0 1			f1 and f2 muted * f2 selected f1 selected f1 and f2 in summed mode		
						0 1		Squarewave signal selected * Sinewave signal selected		
							0 1	Normal operation Tone / Ring Generator connected toTransmit path *		

*: state at power on initialization
(2): value provided if f1 or f2 is selected alone.if f1 and f2 are selected in the summed mode, f1=0.89 Vpp while f2=0.7 Vpp.
X reserved: write 0

Table 10. Control Register CR8 Functions

7	6	5	4	3	2	1	0	Function
f17	f16	f15	f14	f13	f12	f11	f10	
msb							lsb	Binary equivalent of the decimal number used to calculate f1

Table 11. Control Register CR9 Functions

7	6	5	4	3	2	1	0	Function
f27	f26	f25	f24	f23	f22	f21	f20	
msb							lsb	Binary equivalent of the decimal number used to calculate f2

Table 12. Control Register CR10 Functions

7	6	5	4	3	2	1	0	Function	
REN	RLM	ROI	RDL	PG	MB	DFT	HFT		
0 1								Remocon Function disabled Remocon Function enabled	*
	0 1							Remocon output in transparent mode Remocon output in latched mode	*
		0 1						Remocon output not inverted Remocon output inverted	*
			0 1					Remocon detection latch reset by µP Remocon detection latch set by internal logic	*
				0 1				20dB preamplifier gain 0dB preamplifier gain	*
					0 1			MBIAS output disabled MBIAS output enabled	*
						0 0 1 1	0 1 0 1	Standard Frequency Tone Range Halved Frequency Tone Range Doubled Frequency Tone Range Forbidden	*

(*) Default values inserted into the Register at Power On.

Table 13. Control Register CR11 Functions

7	6	5	4	3	2	1	0	Function	
BE	BI	BZ5	BZ4	BZ3	BZ2	BZ1	BZ0		
0 1								Buzzer output disabled (set to 0) Buzzer output enabled	*
	0 1							Duty Cycle is intended as the relative width of logic 1 Duty cycle is intended as the relative width of logic 0	*
		msb					lsb	Binary equivalent of the decimal number used to calculate the duty cycle.	

* state at power on initialization

CONTROL REGISTER CR0

First byte of a READ or a WRITE instruction to Control Register CR0 is as shown in TABLE 1.
Second byte is as shown in TABLE 2.

Master Clock / Auxiliary Clock Frequency Selection

A master clock must be provided to STw5093 to activate all the functions. In the case MCLK is absent, AUXCLK can be provide to STw5093 for activating tone or buzzer functions only.
MCLK or AUXCLK frequency can be either 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz..
Bit F1 (7) and F0 (6) must be set during initialization to select the correct internal divider.Default value is 512 kHz. Any clock different from the default one must be selected prior a Power-Up instruction.

Coding Law Selection

Bits MA (4) and IA (3) permit selection of Mu-255 law or A law coding with or without even bit inversion if companded code (bit CM = 1) is selected. Bits MA(4) and IA(3) permit selection of 2-complement, 1-complement or sign and magnitude if linear code (bit CM = 0) is selected.

Coding Selection

Bit CM (5) permits selection either of linear coding (14-bit) or companded coding (8-bit). Default value is linear coding.

Digital Interface format (1)

Bit FF(2) = 0 selects digital interface in Format 1 where B1 and B2 channel are consecutive. FF=1 selects Format 2 where B1 and B2 channel are separated by two bits. (See digital interface format section.)

56+8 selection (1)

Bit 'B7' (1) selects capability for STw5093 to take into account only the seven most significant bits of the PCM data byte selected.
When 'B7' is set, the LSB bit on DR is ignored and LSB bit on DX is high impedance. This function allows connection of an external "in band" data generator directly connected on the Digital Interface.

Digital loopback

Digital loopback mode is entered by setting DL bit(0) equal 1.
In Digital Loopback mode, data written into Receive PCM Data Register from the selected received time-slot is read-back from that Register in the selected transmit time-slot on D_X.
No PCM decoding or encoding takes place in this mode. Transmit and Receive amplifier stages are muted.

CONTROL REGISTER CR1

First byte of a READ or a WRITE instruction to Control Register CR1 is as shown in TABLE 1. Second byte is as shown in TABLE 3.

Digital Interface Timing

Bit DM1(7) = 0 selects digital interface in delayed timing mode, while DM1 = 1 and DM0 = 0 selects non-delayed normal data timing mode, and DM1 = 1 and DM0 = 1 selects non-delayed reverse data timing mode.Default is delayed data timing.

(1) Significant in companded mode only

Latch output control

Bit DO controls directly logical status of latch output LO: ie, a "ZERO" written in bit DO puts the output LO at logical 1, while a "ONE" written in bit DO sets the output LO to zero.

Microwire access to B channel on receive path (1)

Bit MR (4) selects access from MICROWIRE Register CR2 to Receive path. When bit MR is set high, data written to register CR2 is decoded each frame, sent to the receive path and data input at DR is ignored.
In the other direction, current PCM data input received at DR can be read from register CR2 each frame.

Microwire access to B channel on transmit path (1)

Bit MX (3) selects access from MICROWIRE write only Register CR3 to DX output. When bit MX is set high, data written to CR3 is output at DX every frame and the output of PCM encoder is ignored.

	Mu 255 law								**True A law even bit inversion**								**A law without even bit inversion**							
	msb							**lsb**	**msb**							**lsb**	**msb**							**lsb**
Vin = + full scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1
Vin = 0V	1 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 0	1 1	1 0	1 1	1 0	1 1	1 0	1 1	1 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
Vin = - full scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1

MSB is always the first PCM bit shifted in or out of: STw5093.

Transmit/Receive enabling/disabling

Bit 'EN' (2) enables or disables voice data transfer on DX and DR pins. When disabled, PCM data from DR is not decoded and PCM time-slots are high impedance on DX. Default value is disabled.

B-channel selection (1)

Bit TS(1) permits selection between B1 or B2 channels. Default value is B1 channel.

Clock Selection

Bit SLC(0) allows the selection between MCLK and AUXCLK. Default value is MCLK.

CONTROL REGISTER CR2(1)

Data sent to receive path or data received from DR input. Refer to bit MR(4) in "Control Register CR1" paragraph.

CONTROL REGISTER CR3 (1)

DX data transmitted. Refer to bit MX(3) in "Control Register CR1" paragraph.

CONTROL REGISTER CR4

First byte of a READ or a WRITE instruction to Control Register CR4 is as shown in TABLE 1. Second byte is as shown in TABLE 6.

(1) Significant in companded mode only

Transmit Input Selection

MIC1 or MIC2 or MIC3 or transmit mute can be selected with bits 6 and 7 (VS and TE).
Transmit gain can be adjusted within a 22.5 dB range in 1.5 dB step with Register CR5.

Sidetone Selection

Bit "SI" (5) enables or disables Sidetone circuitry. When enabled, sidetone gain can be adjusted with Register (CR5). When Transmit path is disabled, sidetone circuit is also disabled.

Output Driver Selection

Bits OE1(4) and OE2(3) provide the selection among the earpiece output or the extra amplifier output or both outputs muted.OE1 = 1 and OE2 = 1 is not allowed.

Ring/Tone signal selection

Bit RTE (2) provide select capability to connect on-chip Ring/Tone generator either to an extra amplifier input or to earpiece amplifier input.

Receiver High Pass Filter Selection

Bit HPB(1) provides the selection of the receiver high pass filter cutoff frequency.

PCM receive data selection

Bits "SE" (0) provide select capability to connect received speech signal either to an extra amplifier input or to earpiece amplifier input.

CONTROL REGISTER CR5

First byte of a READ or a WRITE instuction to Control Register CR5 is as shown in TABLE 1. Second byte is as shown in TABLE 7.

Transmit gain selection

Transmit amplifier can be programmed for a gain from 0dB to 22.5dB in 1.5dB step with bits 4 to 7.
0 dBmO level at the output of the transmit amplifier (A reference point) is 0.492 Vrms (overload voltage is 0.707 Vrms).

Sidetone attenuation selection

Transmit signal picked up after the switched capacitor low pass filter may be fed back into both Receive amplifiers.
Attenuation of the signal at the output of the sidetone attenuator can be programmed from Ä12.5dB to -27.5dB relative to reference point A in 1 dB step with bits 0 to 3.

CONTROL REGISTER CR6

First byte of a READ or a WRITE instruction to Control Register CR6 is as shown in TABLE 1. Second byte is as shown in TABLE 8.

Earpiece amplifier gain selection:

Earpiece Receive gain can be programmed in 2 dB step from 0 dB to -30 dB relative to the maximum with bits 4 to 7.
0 dBmO voltage at the output of the amplifier on pin VFr is 0.9825 Vrms when 0dB gain is selected down to 30.925 Vrms when -30dB gain is selected.

Extra amplifier gain selection:

Extra Receive amplifier gain can be programmed in 2 dB step from 0 dB to -30 dB relative to the maximum with bits 0 to 3.
0 dBmO voltage on the output of the amplifier on pins V_{Lr+} and V_{Lr-} 1.965 Vrms when 0 dB gain is selected down to 61.85 mVrms when -30 dB gain is selected.

CONTROL REGISTER CR7:

First byte of a READ or a WRITE instruction to Control Register CR7 is as shown in TABLE 1. Second byte is as shown in TABLE 9.

Tone/Ring amplifier gain selection

Output level of Ring/Tone generator, before attenuation by programmable attenuator is 1.6 Vpk-pk when f1 generator is selected alone or summed with the f2 generator and 1.26 Vpk-pk when f2 generator is selected alone. Selected output level can be attenuated down to -27 dB by programmable attenutator by setting bits 4 to 7.

Frequency mode selection

Bits 'F1' (3) and 'F2' (2) permit selection of f1 and/or f2 frequency generator according to TABLE 9.
When f1 (or f2) is selected, output of the Ring/Tone is a squarewave (or a sinewave) signal at the frequency selected in the CR8 (or CR9) Register.
When f1 and f2 are selected in summed mode, output of the Ring/Tone generator is a signal where f1 and f2 frequency are summed.
In order to meet DTMF specifications, f2 output level is attenuated by 2dB relative to the f1 output level.
Frequency temporization must be controlled by the microcontroller.

Waveform selection

Bit 'SN' (1) selects waveform of the output of the Ring/Tone generator. Sinewave or squarewave signal can be selected.

DTMF selection

Bit DE (0) permits connection of Ring/Tone/DTMF generator on the Transmit Data path instead of the Transmit Amplifier output. Earpiece or extra receive output feed-back may be provided by sidetone circuitry by setting bit SI or directly by setting bit RTE in Register CR4. Loudspeaker feed-back may be provided directly by setting bit RTL in Register CR4.

CONTROL REGISTERS CR8 AND CR9

First byte of a READ or a WRITE instruction to Control Register CR8 or CR9 is as shown in TABLE 1. Second byte is respectively as shown in TABLE 10 and 11.
If "standard frequency tone range" is selected, Tone or Ring signal frequency value is defined by the formula:

$$f1 = CR8 / 0.128 \text{ Hz}$$

and

$$f2 = CR9 / 0.128 \text{ Hz}$$

where CR8 and CR9 are decimal equivalents of the binary values of the CR8 and CR9 registers respectively. Thus, any frequency between 7.8 Hz and 1992 Hz may be selected in 7.8 Hz step.
If "halved frequency tone range"is selected, Tone or Ring signal frequency value is defined by the formula:

$$f1 = CR8 / 0.256 \text{ Hz}$$

and

$$f2 = CR9 / 0.256 \text{ Hz}$$

This any frequency between 3.9Hz and 996Hz may be selected in 3.9Hz step.
If "doubled frequency tone range"is selected, Tone or Ring signal frequency value is defined by the formula:

$$f1 = CR8 / 0.064 \text{ Hz}$$

and

$$f2 = CR9 / 0.064 \text{ Hz}$$

Thus any frequency between 15.6Hz and 3984Hz may be selected in 15.6Hz step.

TABLE 12 gives examples for the main frequencies usual for Tone or Ring generation.

CONTROL REGISTER CR10

Remocon Function Enable

Bit REN(7) enables or disables the RemoconFunction. Default value is disabled.

Remocon Mode Selection

Bit RLM(6) is used to select between a transparent pressed button information and a latched pressed button information at REMOUT. In both cases a debounce circuit (50ms max.) is active.

Remocon Output Inversion

Bit ROI(5) is used to invert or not the information at REMOUT. Default value is not inverted (i.e. pressed button information is a logic 1 at REMOUT.

Remocon Detection Latch

Bit RDL(4) is set by the internal Remocon Function logic, after the debounce time, when a low level on REMIN is detected. It can be reset by the mP writing CR10.

Preamplifier Gain Selection

Bit PG(3) provides the selection between 0dB and 20dB gain of the preamplifier. Default value is 20dB.

Microphone Bias Disabling/Enabling

Bit MB (2) enables or disables a switch for microphone biasing.
Default value is disabled.

Tone Frequency Range Selection

Bit DFT(1) and HFT(0) permits the selection among "standard frequency tone range" (i.e. from 7.8Hz to 1992Hz in 7.8Hz step), "halved frequency tone range" (i.e. from 3.9Hz to 996Hz in 3.9Hz step), and "doubled frequency

tone range" (i.e. from 15.6Hz to 3984Hz in 15.6Hz step) according to the values described in CONTROL REGISTER CR8 and CR9.

CONTROL REGISTER CR11

Bit BE(7) permits connection of a f1 squarewave PWM Ring signal, amplitude modulated or not by a f2 squarewave signal, to buzzer driver output BZ. Bits BZ5 to BZ0 define the duty cycle of the PWM squarewave, according to the following formula:

Duty Cycle = CR11(5 to 0) x 0.78125%

where CR11(5 to 0) is the decimal equivalent of the binary value BZ5 to BZ0.

When BE = 1, if bits F1 = 1 and F2 = 0 in register CR7, a f1 PWM ring signal is present at the buzzer output, while if bits F1 = 1 and F2 = 1 in register CR7 the f1 PWM ring signal is also amplitude modulated by a f2 squarewave frequency. Bit BI (6) allows to chose the logic level at which the duty cycle is referred: BI = 0 means that duty cycle is intended as the relative width of the logic1, while BI = 1 means that duty cycle is intended as the relative width of the logic 0. When BE = 0 (or during power down) BZ = 0 if BI = 0 or BZ = 1 if BI = 1.

Table 14. Examples of Usual Frequency Selection (Standard frequency tone range)

Description	f1 value (decimal)	Theoretic value (Hz)	Typical value (Hz)	Error%
Tone 250 Hz	32	250	250	-.00
Tone 330 Hz	42	330	328.2	-.56
Tone 425 Hz	54	425	421.9	-.73
Tone 440 Hz	56	440	437.5	-.56
Tone 800 Hz	102	800	796.9	-.39
Tone 1330 Hz	170	1330	1328.1	-.14
DTMF 697Hz	89	697	695.3	-.24
DTMF 770 Hz	99	770	773.4	+.44
DTMF 852 Hz	109	852	851.6	-.05
DTMF 941 Hz	120	941	937.5	-.37
DTMF 1209 Hz	155	1209	1210.9	+.16
DTMF 1336 Hz	171	1336	1335.9	-.01
DTMF 1477 Hz	189	1477	1476.6	.00
DTMF 1633 Hz	209	1633	1632.8	.00
SOL	50	392	390.6	-.30
LA	56	440	437.5	-.56
SI	63	494	492.2	-.34
DO	67	523.25	523.5	+.04
RE	75	587.33	586.0	-.23
MI flat	80	622.25	625.0	+.45
MI	84	659.25	656.3	-.45
FA	89	698.5	695.3	-.45
FA sharp	95	740	742.2	+.30
SOL	100	784	781.3	-.34
SOL sharp	106	830.6	828.2	-.29
LA	113	880	882.9	+.33
SI	126	987.8	984.4	-.34
DO	134	1046.5	1046.9	+.04
RE	150	1174.66	1171.9	-.23
MI	169	1318.5	1320.4	+.14

TIMING DIAGRAM

Figure 2. Non Delayed Data Timing Mode (Normal) (*)

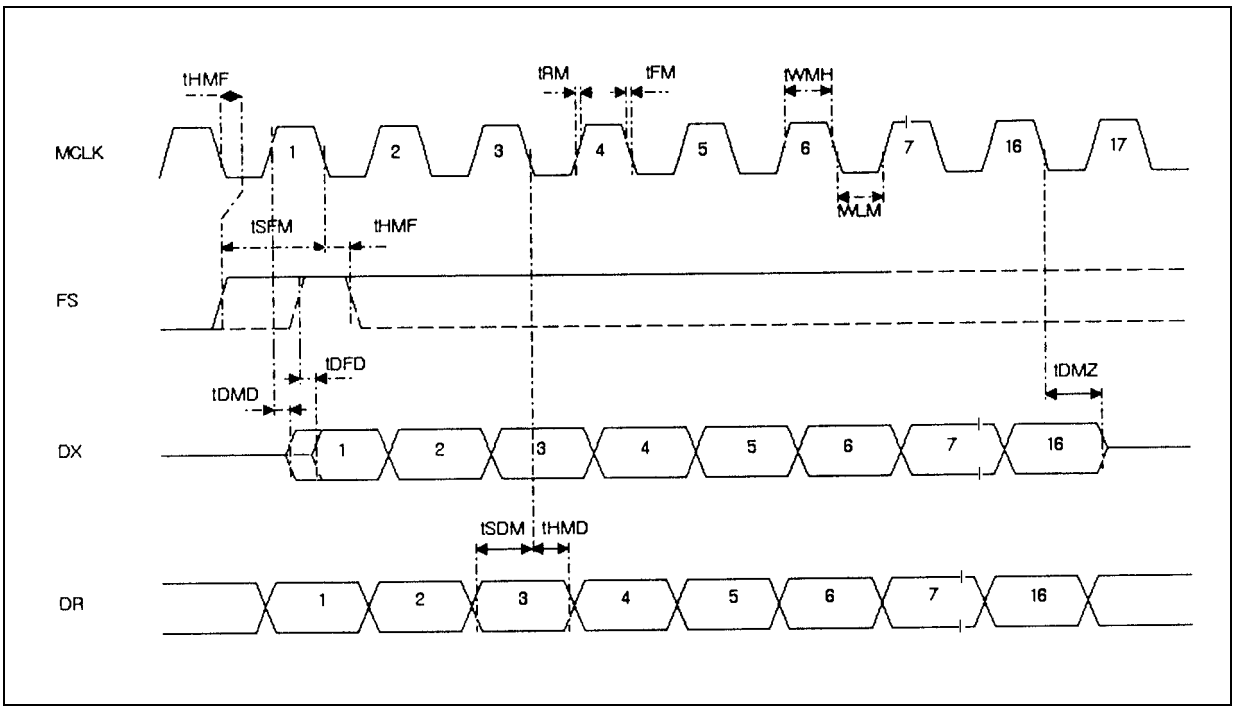
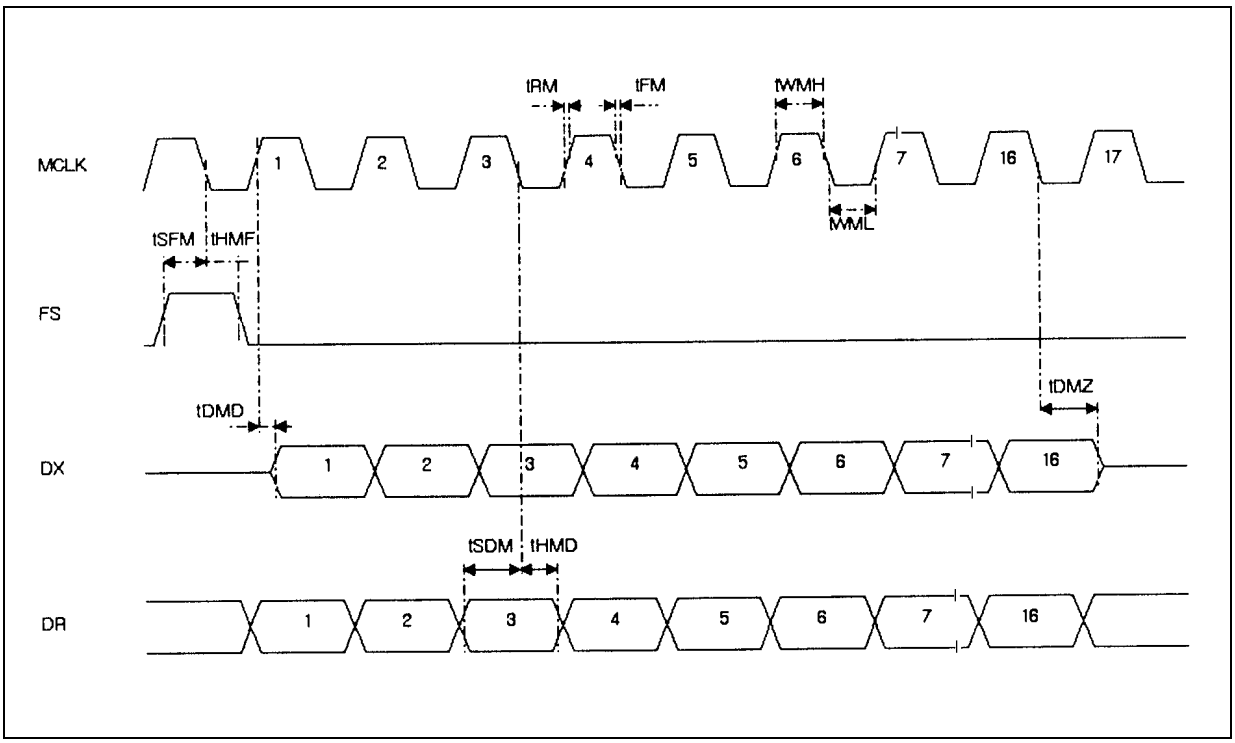


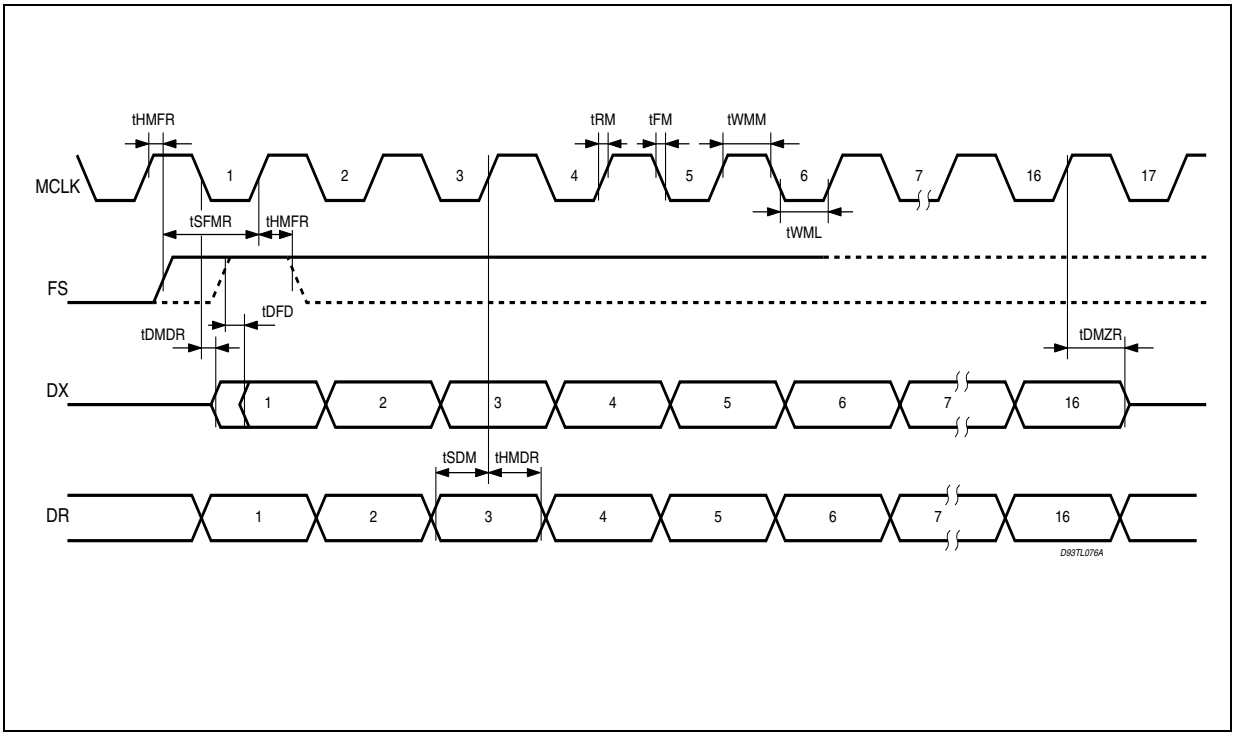
Figure 3. Delayed Data Timing Mode (*)



(*) In the case of companded code the timing is applied to 8 bits instead of 16 bits.

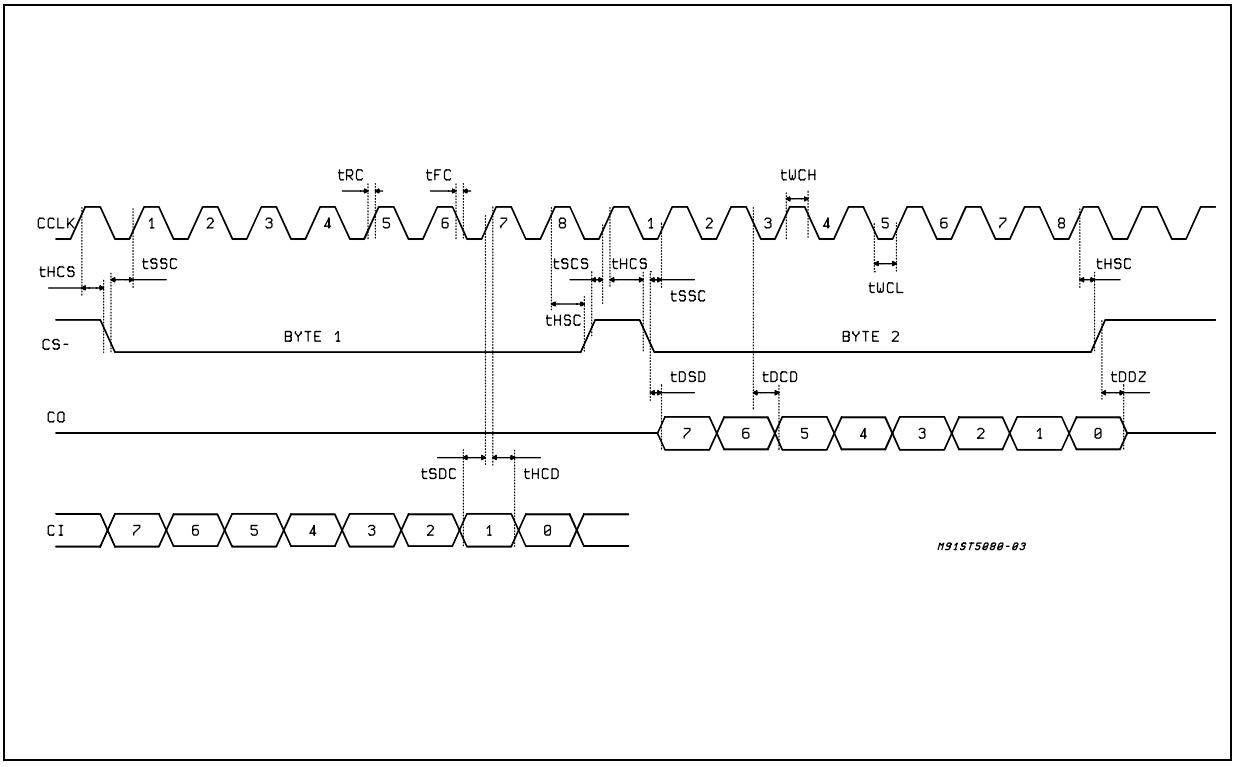
TIMING DIAGRAM

Figure 4. Non Delayed Reverse Data Timing Mode (*



(*) In the case of companded code the timing is applied to 8 bits instead of 16 bits.

Figure 5. Serial Control Timing (MICROWIRE MODE)



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	4.6	V
Voltage at MIC ($V_{CC} \leq 3.3V$)	V_{CC} +0.5 to GND -0.5	V
Current at V_{Fr} and V_{Lr}	± 100	mA
Current at any digital output	± 50	mA
Voltage at any digital input ($V_{CCIO} \leq 3.3V$); limited at ± 50mA	V_{CCIO} + 0.5 to GND -0.5	V
Storage temperature range	- 65 to + 150	°C
Lead Temperature (wave soldering, 10s)	+ 260	°C

OPERATIVE SUPPLY VOLTAGES

Symbol	Min.	Max.	Unit
$V_{CC} = V_{CCA} = V_{CCP}$	2.7	3.3	V
V_{CCIO}	1.8	V_{CC}	V

TIMING SPECIFICATIONS (unless otherwise specified, V_{CCIO} = 1.8V to 3.3V ,T_{amb} = -30°C to 85°C ; typical characteristics are specified at V_{CCIO} = 3.0V, T_{amb} = 25 °C; all signals are referenced to GND, see Note 5 for timing definitions)

NOTICE: All timing specifications can be changed.

MASTER CLOCK TIMING

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK	Selection of frequency is programmable (see table 2)		512 1.536 2.048 2.560		kHz MHz MHz MHz
t_{WMH}	Period of MCLK high	Measured from V_{IH} to V_{IH}	150			ns
t_{WML}	Period of MCLK low	Measured from V_{IL} to V_{IL}	150			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns

PCM INTERFACE TIMING

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{HMF}	Hold Time MCLK low to FS low		0			ns
t_{SFM}	Setup Time, FS high to MCLK low		30			ns
t_{DMD}	Delay Time, MCLK high to data valid	Load = 20pF			100	ns

TIMING SPECIFICATIONS (continued)

PCM INTERFACE TIMING (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{DMZ}	Delay Time, MCLK low to DX disabled		10		100	ns
t_{DFD}	Delay Time, FS high to data valid	Load = 20pF; Applies only if FS rises later than MCLK rising edge in Non Delayed Mode only			100	ns
t_{SDM}	Setup Time, DR valid to MCLK receive edge		20			ns
t_{HMD}	Hold Time, MCLK low to D_R invalid		10			ns
t_{HMFR}	Hold Time MCLK High to FS low		30			ns
t_{SFMR}	Setup Time, FS high to MCLK High		30			ns
t_{DMDR}	Delay Time, MCLK low to data valid	Load = 20pF			100	ns
t_{DMZR}	Delay Time, MCLK High to DX disabled		10		100	ns
t_{HMDR}	Hold Time, MCLK High to D_R invalid		20			ns

SERIAL CONTROL PORT TIMING

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK				2.048	MHz
t_{WCH}	Period of CCLK high	Measured from V_{IH} to V_{IH}	160			ns
t_{WCL}	Period of CCLK low	Measured from V_{IL} to V_{IL}	160			ns
t_{RC}	Rise Time of CCLK	Measured from V_IL to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK high to CS- low		10			ns
t_{SSC}	Setup Time, CS- low to CCLK high		50			ns
t_{SDC}	Setup Time, CI valid to CCLK high		50			ns
t_{HCD}	Hold Time, CCLK high to CI invalid		50			ns
t_{DCD}	Delay Time, CCLK low to CO data valid	Load = 20pF			80	ns
t_{DSD}	Delay Time, CS-low to CO data valid				50	ns

TIMING SPECIFICATIONS (continued)

SERIAL CONTROL PORT TIMING (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{DDZ}	Delay Time CS-high or 8th CCLK low to CO high impedance whichever comes first		10		80	ns
t_{HSC}	Hold Time, 8th CCLK high to CS-high		100			ns
t_{SCS}	Set up Time, CS- high to CCLK high		100			ns

Note 5:

A signal is valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}. For the purposes of this specification the following conditions apply:

a) All input signal are defined as: $V_{IL} = 0.2V_{CCIO}$, $V_{IH} = 0.8V_{CCIO}$, $t_R < 10ns$, $t_F < 10ns$.

b) Delay times are measured from the inputs signal valid to the output signal valid.

c) Setup times are measured from the data input valid to the clock input invalid.

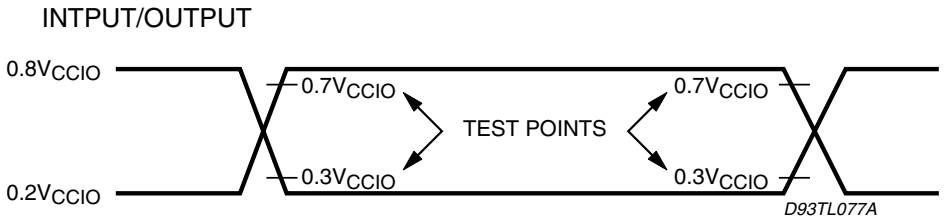
d) Hold times are measured from the clock signal valid to the data input invalid.

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CCIO} = 1.8V to 3.3V, T_{amb} = -30°C to 85°C; typical characteristic are specified at V_{CCIO} = 3.0V, T_{amb} = 25°C ; all signals are referenced to GND)

DIGITAL INTERFACES

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All digital inputs except REMIN DC AC			 $0.3V_{CCIO}$ $0.2V_{CCIO}$	 V V
V_{IH}	Input High Voltage	All digital inputs except REMIN DC AC	 $0.7V_{CCIO}$ $0.8V_{CCIO}$			 V V
V_{ILREM}	Input Low Voltage	REMIN input			0.5	V
V_{IHREM}	Input High Voltage	REMIN input	1.4			V
V_{OL}	Output Low Voltage	All digital outputs, I_L = 10µA All digital outputs, I_L = 2mA			0.1 0.4	V V
V_{OH}	Output High Voltage	All digital outputs, I_L = 10µA All digital outputs, I_L = 2mA	V_{CCIO}-0.1 V_{CCIO}-0.4			V V
I_{IL}	Input Low Current	Any digital input, GND < V_{IN} < V_{IL}	-10		10	µA
I_{IH}	Input High Current	Any digital input, V_{IH} < V_{IN} < V_{CCIO}	-10		10	µA
I_{OZ}	Output Current in High impedance (Tri-state)	DX and CO	-10		10	µA

Figure 6. A.C. TESTING INPUT, OUTPUT WAVEFORM



AC Testing: inputs are driven at $0.8V_{CCIO}$ for a logic "1"and $0.2V_{CCIO}$ for a logic "0 ".
Timing measurements are made at $0.7V_{CCIO}$ for a logic "1"and $0.3V_{CCIO}$ for a logic "0".

ANALOG INTERFACES

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{MBIAS}	Switch Resistance for Microphone bias	MBIAS 100mV under V_{CC}			150	Ω
I_{MIC}	Input Leakage	GND < V_{MIC} < V_{CC}	-100		+100	µA
R_{MIC}	Input Resistance	GND < V_{MIC} < V_{CC}	50			kΩ
R_{LVFr}	Load Resistance		30			Ω
C_{LVFr}	Load Capacitance			50		nF
R_{OVFr0}	Output Resistance	Steady zero PCM code applied to DR; I = ±1mA		1.0		Ω
R_{LvLr}	Load Resistance	V_{Lr+} to V_{Lr-}	8			Ω
C_{LvLr}	Load Capacitance	from V_{Lr+} to V_{Lr-}		50		nF
R_{OLVrO}	Output Resistance	Steady zero PCM code applied to DR; I ± 1mA		1		Ω
V_{OSVLrO}	Differential offset Voltage at V_{Lr+}, V_{Lr-}	Alternating ± zero PCM code applied to DR maximum receive gain; R_L = 50Ω	-50		+50	mV

TRANSMISSION CHARACTERISTICS (unless otherwise specified, V_{CC} = 2.7V to 3.3V, T_{amb} = -30°C to 85°C; typical characteristics are specified at V_{CC} = 3.0V, T_{amb} = 25°C, MIC1/2/3 = 0dBm0, D_R = -6dBm0 PCM code, f = 1015.625 Hz; all signal are referenced to GND)

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Transmit path - Absolute levels at MIC1 / MIC2 / MIC3

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	0 dBm0 level	Transmit Amps connected for 20dB gain		49.26		mV_{RMS}
	Overload level			70.71		mV_{RMS}
	0 dBm0 level	Transmit Amps connected for 42.5dB gain		3.694		mV_{RMS}
	Overload level			5.302		mV_{RMS}

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at V_{Fr}

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	0 dBM0 level	Receive Amp programmed for 0dB attenuation		0.9825		V_{RMS}
	0 dBM0 level	Receive Amp programmed for30dB attenuation		30.925		mV_{RMS}

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at VLr (Differentially measured)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	0 dBM0 level	Receive Amp programmed for 0dB attenuation		1.965		V_{RMS}
	0 dBM0 level	Receive Amp programmed for 30dB attenuation		61.85		mV_{RMS}

AMPLITUDE RESPONSE
Transmit path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for minimum.Measure deviation of Digital PCM Code from ideal $0dB_{m0}$ PCM code at D_X	-0.5		0.5	dB
G_{XAG}	Transmit Gain Variation with programmed gain	Measure Transmit Gain over the range from Maximum to minimum setting.Calculate the deviation from the programmed gain relative to GXA, i.e. $G_{AXG} = G_{actual} - G_{prog.} - G_{XA}$	-0.5		0.5	dB
G_{XAT}	Transmit Gain Variation with temperature	Measured relative to G_{XA}. min. gain < G_X < Max. gain	-0.1		0.1	dB
G_{XAV}	Transmit Gain Variation with supply	Measured relative to G_{XA} G_X = Minimum gain	-0.1		0.1	dB

AMPLITUDE RESPONSE(continued)
Transmit path (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{XAF}	Transmit Gain Variation with frequency	Relative to 1015,625 Hz, multitone test technique used.min. gain < G_X < Max. gain				
		f = 60 Hz			-30	dB
		f = 100 Hz			-20	dB
		f = 200 Hz			-6	dB
		f = 300 Hz	-1.5		0.5	dB
		f = 400 Hz to 3000 Hz	-0.5		0.5	dB
		f = 3400 Hz	-1.5		0.0	dB
		f = 4000 Hz			-14	dB
		f = 4600 Hz (*)			-35	dB
		f = 8000 Hz (*)			-47	dB
G_{XAL}	Transmit Gain Variation with signal level	Sinusoidal Test method.Reference Level = -10 dBm0				
		V_{MIC} = -40 dBm0 to +3 dBm0	-0.5		0.5	dB
		V_{MIC} = -50 dBm0 to -40 dBm0	-0.5		0.5	dB
		V_{MIC} = -55 dBm0 to -50 dBm0	-1.2		1.2	dB

(*) The limit at frequencies between 4600Hz and 8000Hz lies on a straight line connecting the two frequencies on a linear (dB) scale versus log (Hz) scale.

Receive path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{RAE}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply -6 dBm0 PCM code to DR Measure V_{Fr}	-0.5		0.5	dB
G_{RAL}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply -6 dBm0 PCM code to DR Measure $V_{Lr\pm}$	-0.5		0.5	dB
G_{RAGE}	Receive Gain Variation with programmed gain	Measure V_{Fr} Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to G_{RAE}, i.e. $G_{RAGE} = G_{actual} - G_{prog.} - G_{RAE}$	-0.5		0.5	dB
G_{RAGL}	Receive Gain Variation with programmed gain	Measure V_{Lr} Gain over the range from Maximum to minimum setting.Calculate the deviation from the programmed gain relative to G_{RAL}, i.e. $G_{RAGL} = G_{actual} - G_{prog.} - G_{RAL}$	-0.5		0.5	dB
G_{RAT}	Receive Gain Variation with temperature	Measured relative to GRA. (V_{Lr} and V_{Fr}) min. gain < G_R < Max. gain	-0.1		0.1	dB

AMPLITUDE RESPONSE(continued)
Receive path (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{RAV}	Receive Gain Variation with Supply	Measured relative to GRA. (V_{Lr} and V_{Fr}) G_R = Maximum Gain	-0.1		0.1	dB
G_{RAF}	Receive Gain Variation with frequency (V_{Lr} and V_{Fr}) HPB = 0	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_R < Max. gain f = 60Hz f = 100Hz f = 200 Hz f = 300 Hz f = 400 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -1.5 -0.5 -1.5		 -20 -12 -2 0.5 0.5 0.0 -14	 dB dB dB dB dB dB dB
	Receive Gain Variation with frequency (V_{Lr} and V_{Fr}) HPB = 1	Relative to 1015,625 Hz, multitone test technique used. Min. gain < G_R < Max. gain f = 50Hz f = 100 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -1.5 -0.5 -1.5		 0.5 0.5 0.0 -14	 dB dB dB dB
$G_{RAL\ E}$	Receive Gain Variation with signal level (V_{Fr})	Sinusoidal Test Method Reference Level = -10 dBm0 D_R = -40 dBm0 to -3 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.5 -0.5 -1.2		 0.5 0.5 1.2	 dB dB dB
$G_{RAL\ L}$	Receive Gain Variation with signal level (V_{Lr})	Sinusoidal Test Method Reference Level = -10 dBm0 D_R = -40 dBm0 to -3 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.5 -0.5 -1.2		 0.5 0.5 1.2	 dB dB dB

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DXA	Tx Delay, Absolute	f = 1600 Hz		320		µs
DXR	Tx Delay, Relative	f = 500 - 600 Hz f = 600 - 800 Hz f = 800 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		290 180 50 20 55 80 180		µs µs µs µs µs µs µs
DRA	Rx Delay, Absolute	f = 1600 Hz		280		µs
DRR	Rx Delay, Relative	f = 500 - 600 Hz f = 600 - 800 Hz f = 800 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		200 110 50 20 65 100 220		µs µs µs µs µs µs µs

NOISE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NXP	Tx Noise, P weighted (up to 35dB)	V_{MIC} = 0V, DE = 0		-75	-70	dBm0p
NRP	Rx Noise, linear weighted (*) (max. gain)	Receive PCM code = Positive Zero SI = 0 and RTE = 0		120	150	µVrms
NRS	Noise, Single Frequency	MIC = 0V, Loop-around measurament from f = 0 Hz to 100 kHz		-50		dBm0
PPSRx	PSRR, Tx	MIC = 0V, V_{CC} = 3.0 V_{DC} + 50 mVrms; f = 100Hz to 50KHz	30			dB
PPSRp	PSRR, Rx	PCM Code equals Positive Zero, V_{CC} = 3.0VDC + 50 mVrms, f = 100 Hz - 4 kHz f = 4 kHz - 50 kHz	 30 30			 dB dB
SOS	Spurious Out-Band signal at the output	DR input set to -6 dBm0 PCM code 300 - 3400 Hz Input PCM Code applied at D_R 4600 Hz - 5600 Hz 5600 Hz - 7600 Hz 7600 Hz - 8400 Hz			 -40 -50 -50	 dB dB dB

(*) 300 to 3400Hz bandwidth

CROSSTALK

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
C_{Tx-r}	Transmit to Receive	Transmit Level = 0 dBm0, f = 300 - 3400 Hz D_R = Quiet PCM Code		-100	-65	dB
C_{Tr-x}	Receive to Transmit	Receive Level = -6 dBm0, f = 300 - 3400 Hz MIC = 0V		-80	-65	dB

DISTORTION

Symbol	Parameter	Test Condition	Min.		Typ.	Max.	Unit
S_{TDX}(*)	Signal to Total Distortion (up to 35dB gain)	Sinusoidal Test Method (measured using linear 300 to 3400 weighting)		#			
	Typical values are measured with 30.5dB gain	Level = 0 dBm0	56	56	65		dB
		Level = -6 dBm0	50	50	64		dB
		Level = -10 dBm0	48	48	61		dB
		Level = -20 dBm0	43	43	52		dB
		Level = -30 dBm0	38	37.5	42		dB
		Level = -40 dBm0	29	28.5	31		dB
		Level = -45 dBm0	24	23	26		dB
		Level = -55 dBm0	15	13	16		dB
S_{DFx}	Single Frequency Distortion transmit	0 dBm0 input signal			-80	-56	dB
S_{TDRE}(*)	Signal to Total Distortion (V_{Fr}) (up to 20dB attenuation)	Sinusoidal Test Method (measured using linear 300 to 3400 weighting)					
	Typical values are measured with 20dB attenuation.	Level = -6 dBm0	50		64		dB
		Level = -10 dBm0	48		62		dB
		Level = -20 dBm0	43		53		dB
		Level = -30 dBm0	38		43		dB
		Level = -40 dBm0	29		33		dB
		Level = -45 dBm0	24		28		dB
		Level = -55 dBm0	15		18		dB
S_{DFr}	Single Frequency Distortion receive (V_{Fr})	-6 dBm0 input signal			-80	-50	dB
S_{TDRL}(*)	Signal to Total Distortion (V_{Lr}) (up to 20dB attenuation)	Sinusoidal Test Method (measured using linear 300 to 3400 weighting)					
	Typical values are measured with 20dB attenuation	Level = -6 dBm0	50		64		dB
		Level = -10 dBm0	48		62		dB
		Level = -20 dBm0	43		53		dB
		Level = -30 dBm0	38		43		dB
		Level = -40 dBm0	29		33		dB
		Level = -45 dBm0	24		28		dB
		Level = -55 dBm0	15		18		dB
S_{DLr}	Single Frequency Distortion receive (V_{Lr})	-6 dBm0 input signal			-80	-50	dB
MD	Intermodulation	Loop-around measurement Voltage at MIC = -10 dBm0 to -27 dBm0, 2 Frequencies in the range 300 - 3400 Hz			-75	-46	dB

(*) The limit curve shall be determined by straight lines joining successive coordinates given in the table.
(#) Lower limits used during the automatic testing to avoid unrealistic yield loss due to æ2dB imprecision of time-limited noise measurements.

POWER DISSIPATION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC0}	Power down Current	CCLK,CI = 0.1V; CS- = V_{CCIO}-0.1V REMOCON function disabled (REN = 0)		0.4	5	µA
I_{CC0R}	Power down Current	CCLK,CI = 0.1V; CS- = V_{CCIO}-0.1V REMOCON function enabled (REN = 1) REMIN = V_{ILREM} or REMIN = V_{IHREM}		2	10	µA
I_{CC1}	Power Up Current	V_{Lr+}, V_{Lr-} and V_{Fr} not loaded		5	8	mA

AUDIO CODEC APPLICATIONS

Figure 7. Application Note for Microphone Connections.

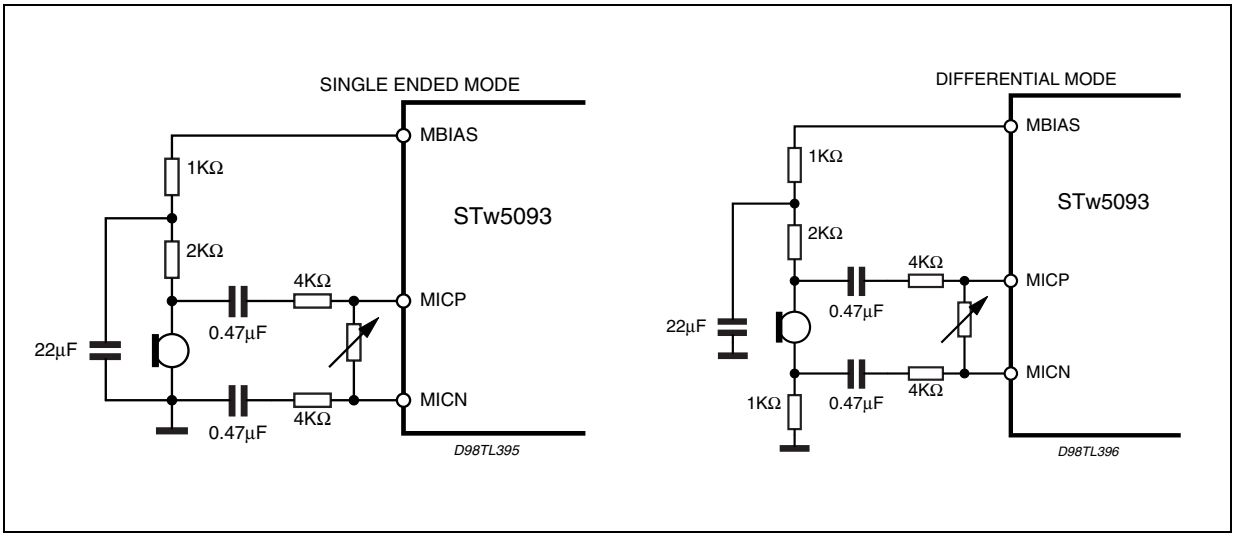


Figure 8. Application Note for V_{Lr} Connections.

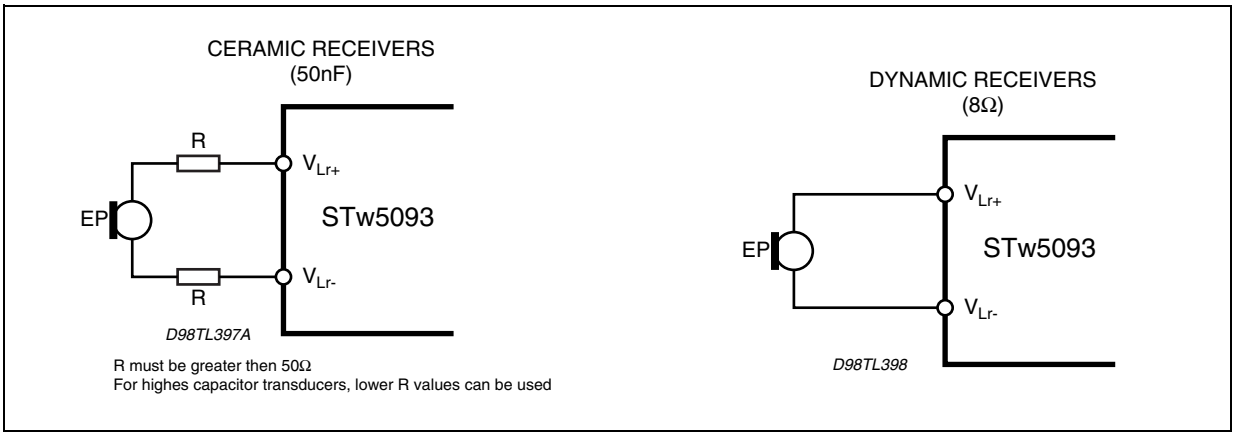
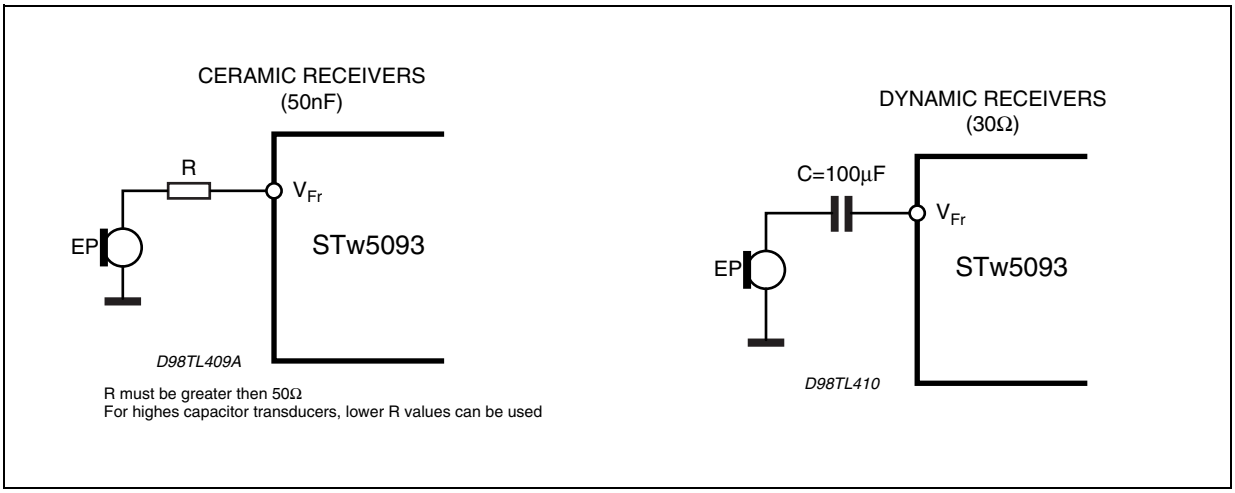


Figure 9. Application Note for V_{Fr} Connections.

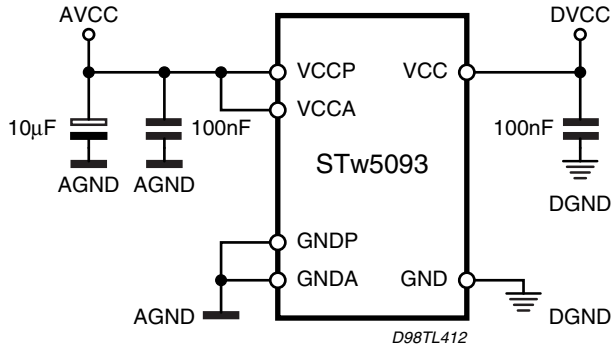


POWER SUPPLY NOTES

Two different strategies can be used to minimize power supply noise/interference.

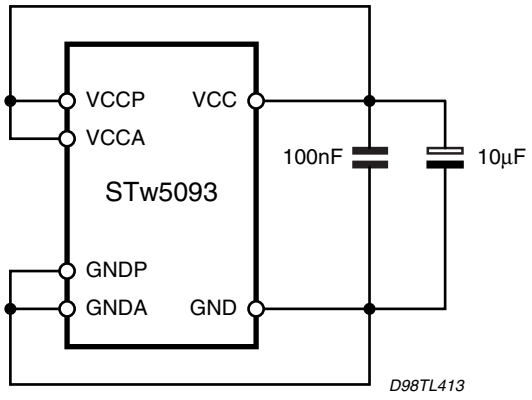
a) Recommended strategy: keep analog and digital power supply rails separate. This requires to use two sets of capacitors, one from AVCC to AGND and the other from DVCC to DGND.

Figure 10.



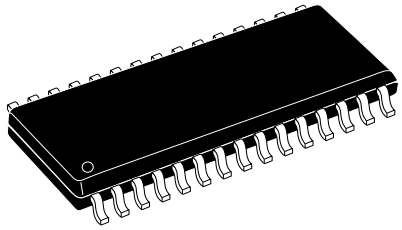
b) Low cost strategy: tie analog and digital power supplies together as close as possible to GND and VCC pins. This allows to use only one set of capacitors between VCC and GND.

Figure 11.

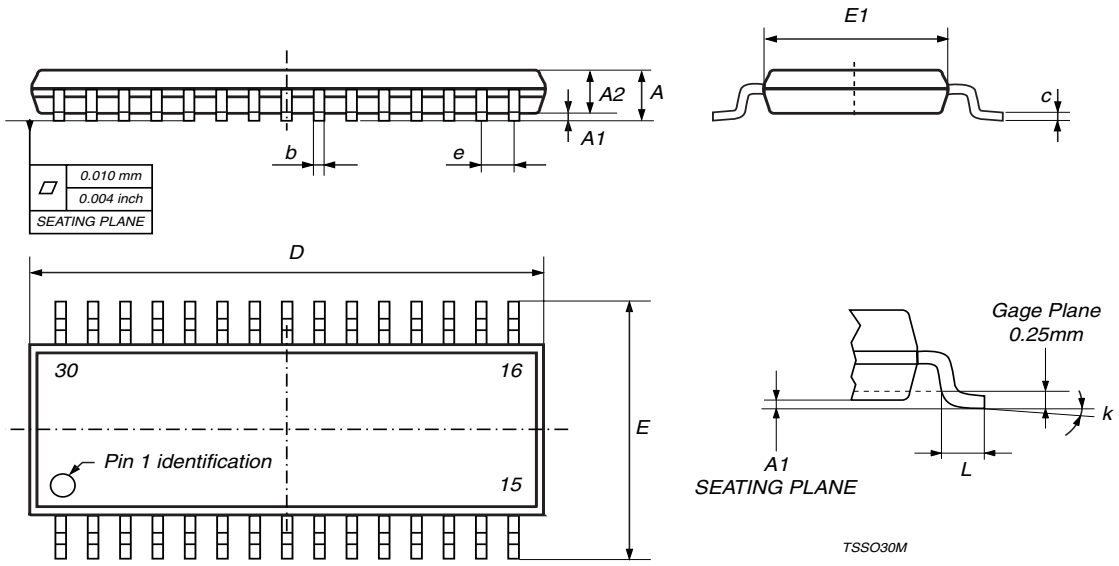


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.10			0.043
A1	0.05		0.15	0.002		0.006
A2	0.85	0.90	0.95	0.033	0.035	0.037
b	0.17		0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	7.70	7.80	7.90	0.303	0.307	0.311
E		6.40			0.252	
e		0.50			0.0197	
E1	4.30	4.40	4.50	0.169	0.173	0.177
L	0.50	0.60	0.70	0.020	0.024	0.028
K	0˚ (min.) 8˚ (max.)					

OUTLINE AND MECHANICAL DATA



TSSOP30 (Thin Shrink)



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