



# THE DATASHEET OF STY30NK90Z





# STY30NK90Z

N-channel 900V - 0.21Ω - 26A - Max247  
Zener-protected SuperMESH™ Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>W</sub>
STY30NK90Z	900V	<0.26Ω	28A	500W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability

## Description

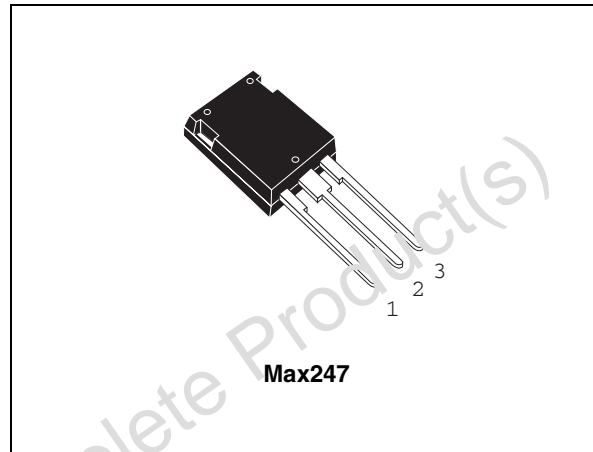
The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

## Applications

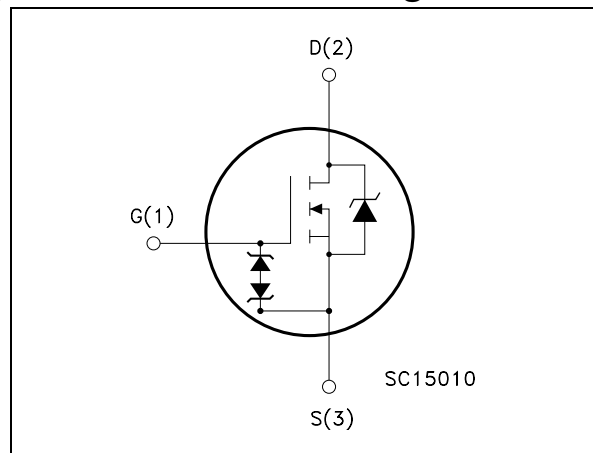
- Switching application

## Order codes

Part number	Marking	Package	Packaging
STY30NK90Z	Y30NK90Z	Max247	Tube



## Internal schematic diagram



# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
1.1	Protection features of gate-to-source zener diodes .....	4
<b>2</b>	<b>Electrical characteristics</b> .....	<b>5</b>
2.1	Electrical characteristics (curves) .....	7
<b>3</b>	<b>Test circuit</b> .....	<b>9</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>11</b>
<b>5</b>	<b>Revision history</b> .....	<b>13</b>

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	900	V
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	26	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	16	A
$I_{DM}^{(1)}$	Drain current (pulsed)	104	A
$P_{tot}$	Total dissipation at $T_C = 25^\circ\text{C}$	450	W
	Derating Factor	3.57	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6000	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	1.5	V/ns
$T_{stg}$	Storage temperature	-65 to 150	°C
$T_j$	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 26\text{A}$ ,  $di/dt \leq 400\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j = T_{j,MAX}$ .

**Table 2. Thermal data**

$R_{thj-case}$	Thermal resistance junction-case max	0.277	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	30	°C/W
$T_J$	Maximum lead temperature for soldering purpose	300	°C

**Table 3. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	26	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 35\text{V}$ )	500	mJ

**Table 4. Gate-source zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{mA}$ (open drain)	30			V

## 1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

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## 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1mA, V <sub>GS</sub> = 0	900			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = max rating V <sub>DS</sub> = max rating, T <sub>C</sub> = 125°C			10 100	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			± 100	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 150μA	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 14A		0.21	0.26	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward transconductance	V <sub>DS</sub> = 15V, I <sub>D</sub> = 14A		26		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 25V, f = 1MHz, V <sub>GS</sub> = 0		12000 852 166		pF pF pF
C <sub>oss eq</sub> (2)	Equivalent output capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 720V		377		pF
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	Turn-on delay time Rise time Turn-off delay time Fall time	V <sub>DD</sub> = 450V, I <sub>D</sub> = 13A R <sub>G</sub> = 4.7Ω V <sub>GS</sub> = 10V (see <a href="#">Figure 13</a> )		67 59 250 72		ns ns ns ns
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 720V, I <sub>D</sub> = 26A, V <sub>GS</sub> = 10V, R <sub>G</sub> = 4.7Ω (see <a href="#">Figure 14</a> )		350 51 190	490	nC nC nC

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
2. C<sub>oss eq</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				28 112	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 28A, V_{GS} = 0$			2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 26A, di/dt = 100A/\mu s,$ $V_{DD} = 100V, T_j = 25^\circ C$ (see <a href="#">Figure 15</a> )		1 18.9 36.6		$\mu s$ $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 26A, di/dt = 100A/\mu s,$ $V_{DD} = 100V, T_j = 150^\circ C$ (see <a href="#">Figure 15</a> )		1.33 25.2 37.8		$\mu s$ $\mu C$ A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

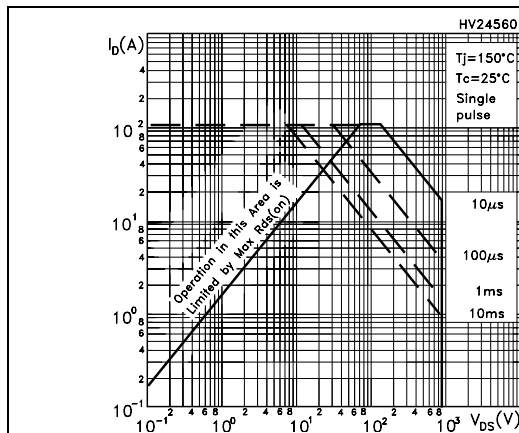


Figure 2. Thermal impedance

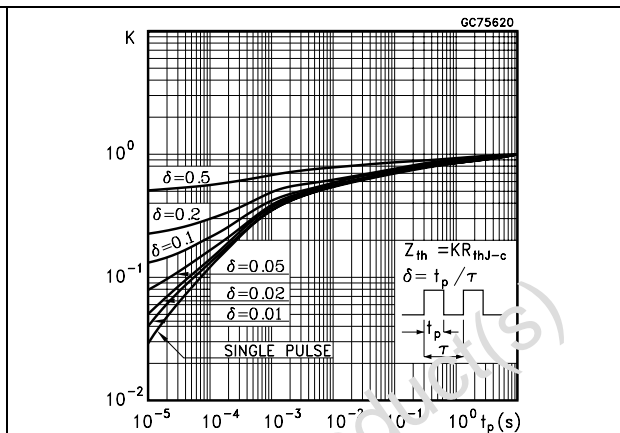


Figure 3. Output characteristics

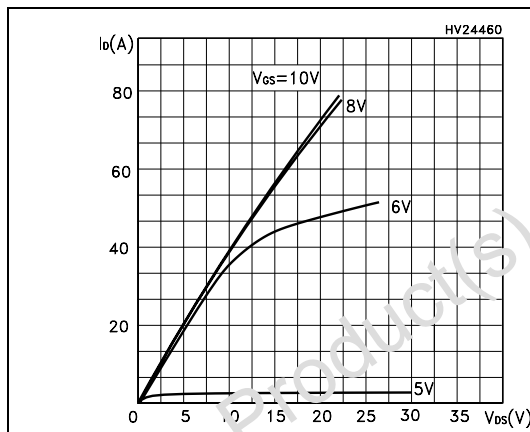


Figure 4. Transfer characteristics

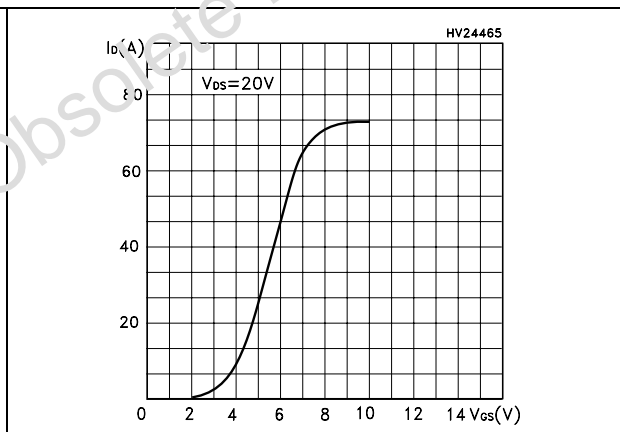


Figure 5. Transconductance

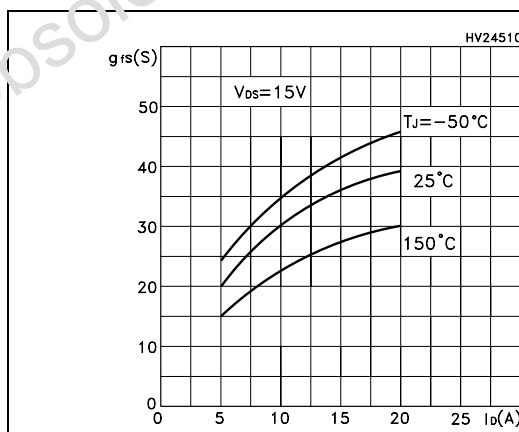


Figure 6. Static drain-source on resistance

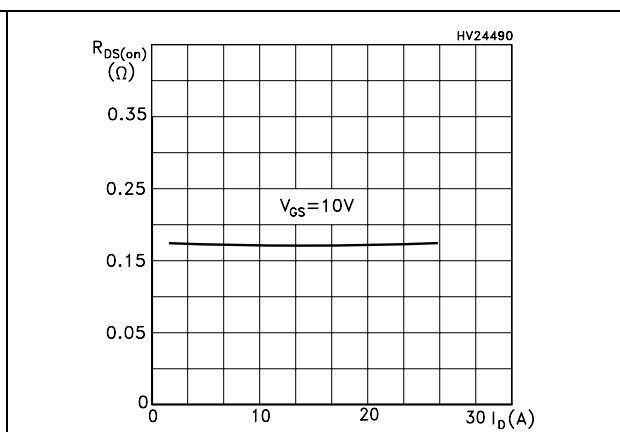


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

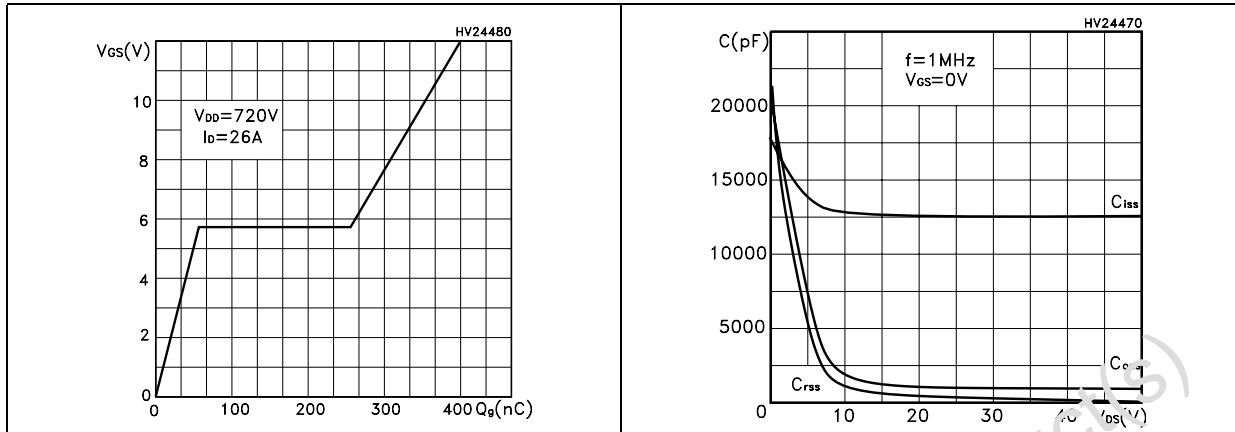


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

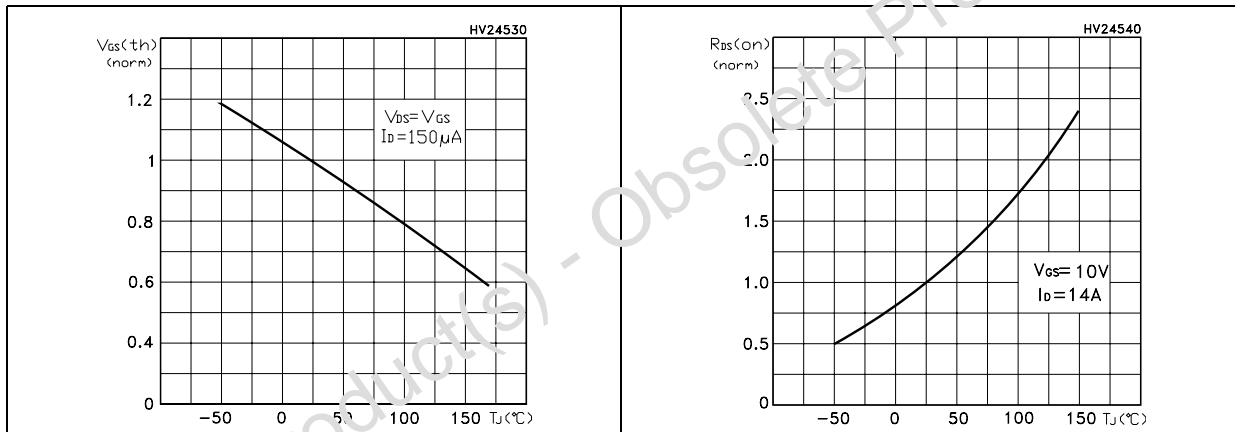
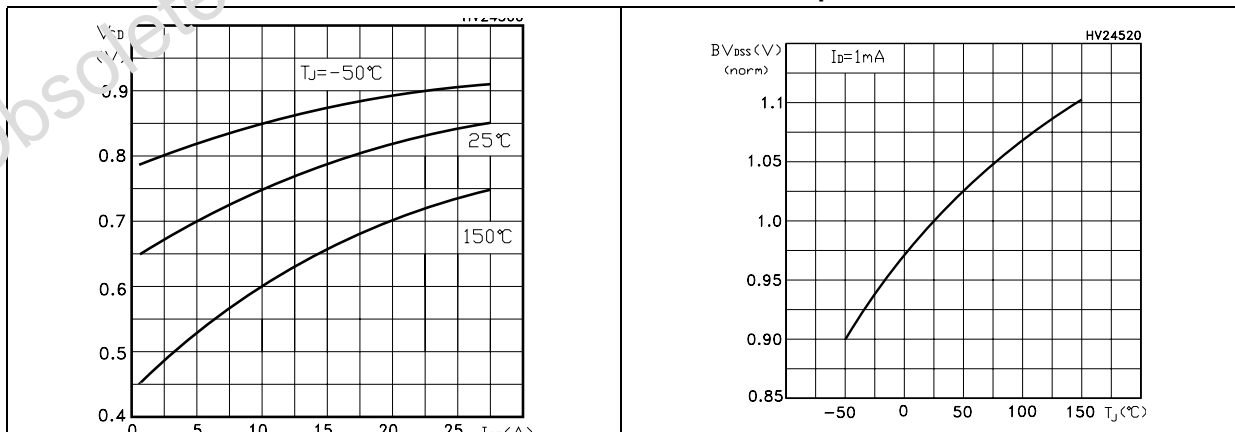


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

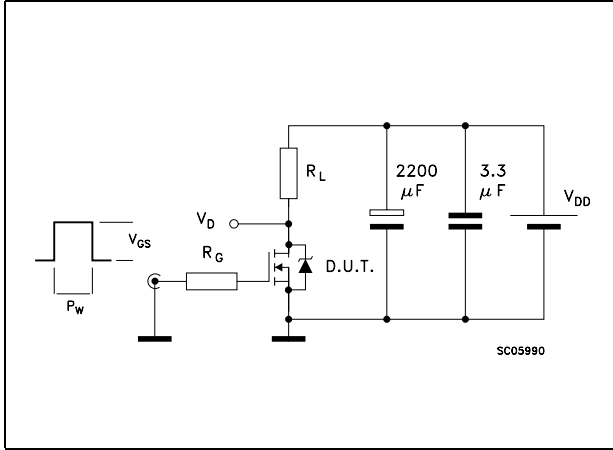


Figure 14. Gate charge test circuit

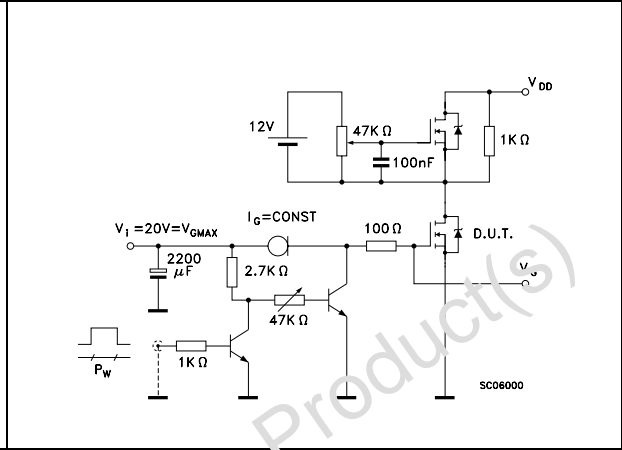


Figure 15. Test circuit for inductive load switching and diode recovery times

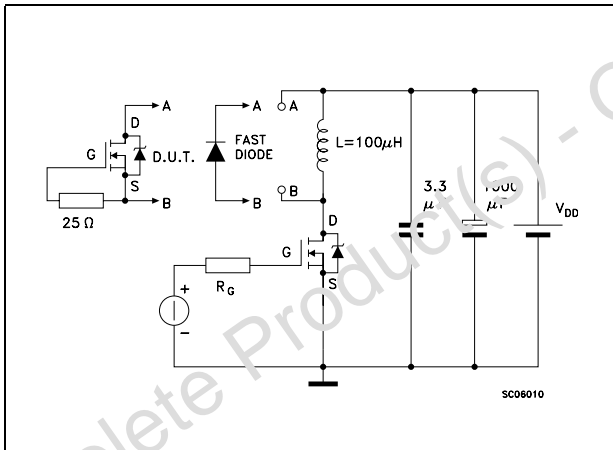


Figure 16. Unclamped Inductive load test circuit

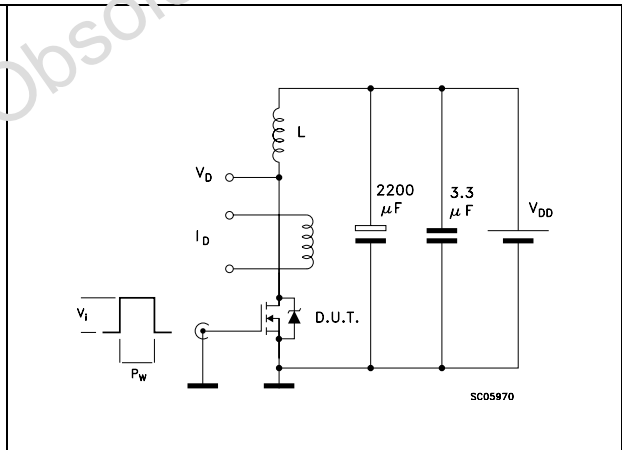
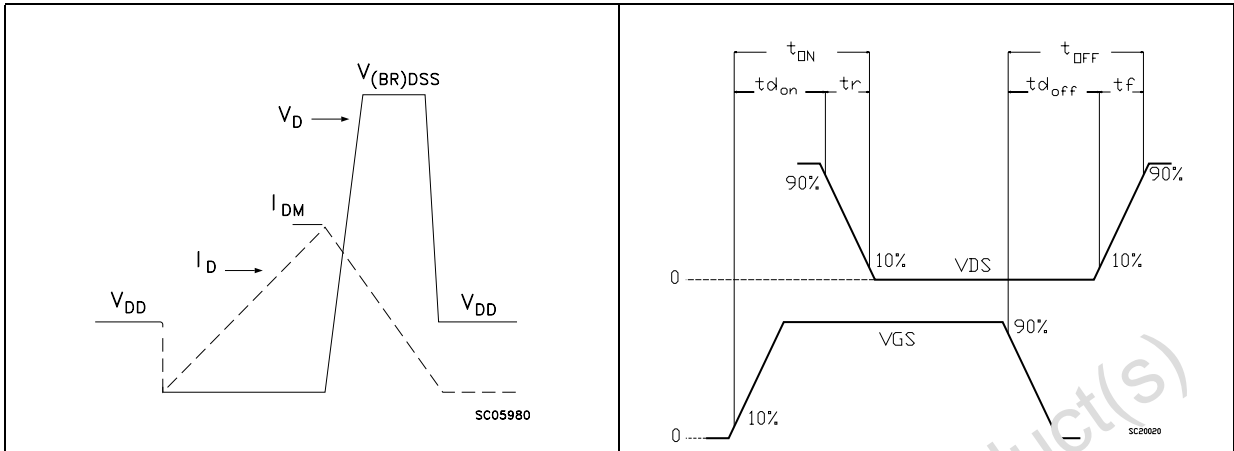


Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



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## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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## 5 Revision history

**Table 8. Revision history**

Date	Revision	Changes
16-Jul-2004	1	First release
23-Mar-2004	2	New ECOPACK label inserted
21-Jan-2005	3	Complete document with curves
16-Oct-2006	4	New template, no content change

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