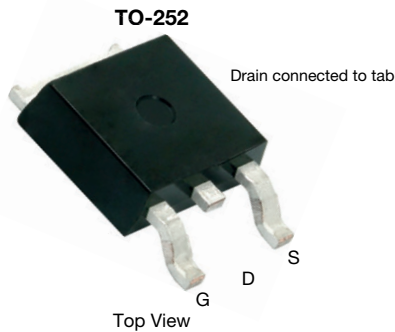




**THE DATASHEET OF  
SUD50P06-15-GE3**



## P-Channel 60 V (D-S) MOSFET



### FEATURES

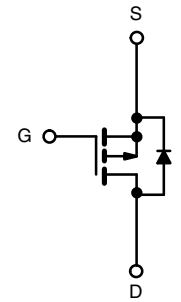
- TrenchFET® power MOSFET
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Load switch



P-Channel MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	-60
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -10$ V	0.015
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.020
$I_D$ (A) <sup>d</sup>	-50
Configuration	Single

### ORDERING INFORMATION

Package	TO-252
Lead (Pb)-free and halogen-free	SUD50P06-15-GE3
	SUD50P06-15-T4-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	-60	V	
Gate-source voltage	$V_{GS}$	$\pm 20$		
Continuous drain current ( $T_J = 175$ °C)	$T_C = 25$ °C	-50 <sup>d</sup>	A	
	$T_C = 125$ °C	-27.5		
Pulsed drain current	$I_{DM}$	-80		
Avalanche current	$I_{AS}$	-50	mJ	
Single pulse avalanche energy <sup>a</sup>	$L = 0.1$ mH	$E_{AS}$		125
Power dissipation	$T_C = 25$ °C	$P_D$	113 <sup>c</sup>	W
	$T_A = 25$ °C		2.5 <sup>b, c</sup>	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C	

### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-ambient <sup>b</sup>	$R_{thJA}$	$t \leq 10$ s	15	°C/W
		Steady state	40	
Junction-to-case	$R_{thJC}$	0.82	1.1	

#### Notes

- Duty cycle  $\leq 1\%$
- When mounted on 1" square PCB (FR4 material)
- See SOA curve for voltage derating
- Package limited



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-60	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1	-	-3	
Gate-body leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V	-	-	-1	μA
		V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C	-	-	-100	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -10 V	-50	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -17 A	-	0.012	0.015	Ω
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -50 A, T <sub>J</sub> = 125 °C	-	-	0.025	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -50 A, T <sub>J</sub> = 150 °C	-	-	0.028	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -14 A	-	-	0.020	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -17 A	-	61	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -25 V, f = 1 MHz	-	4950	-	pF
Output capacitance	C <sub>oss</sub>		-	480	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	405	-	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -50 A	-	110	165	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>		-	19	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>		-	28	-	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -30 V, R <sub>L</sub> = 0.6 Ω I <sub>D</sub> ≅ -50 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 6 Ω	-	15	23	ns
Rise time <sup>c</sup>	t <sub>r</sub>		-	70	105	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>		-	175	260	
Fall time <sup>c</sup>	t <sub>f</sub>		-	175	260	
<b>Source-Drain Diode Ratings and Characteristics T<sub>C</sub> = 25 °C <sup>b</sup></b>						
Continuous current	I <sub>S</sub>		-	-	-50	A
Pulsed current	I <sub>SM</sub>		-	-	-80	
Forward voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = -50 A, V <sub>GS</sub> = 0 V	-	-1	-1.6	V
Reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = -50 A, di/dt = 100 A/μs	-	45	70	ns

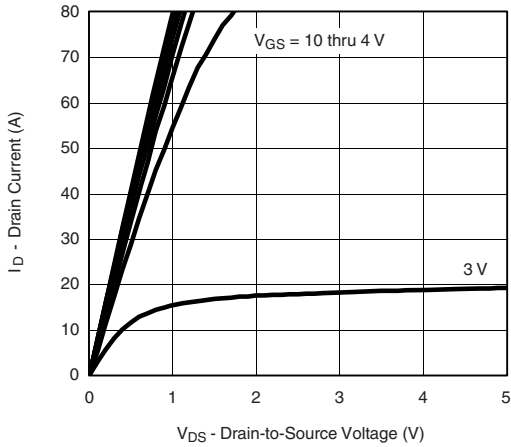
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

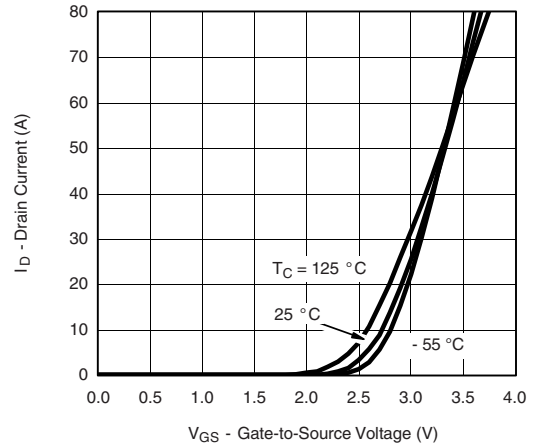
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



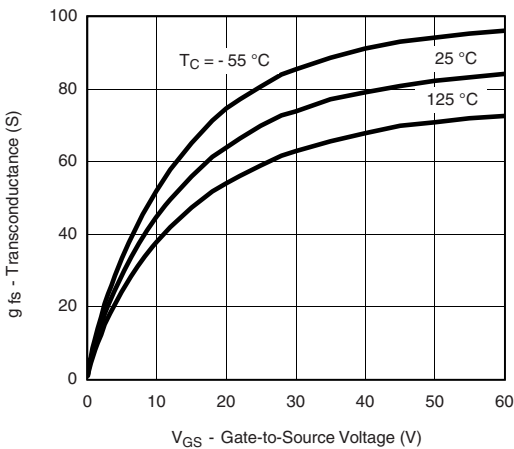
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



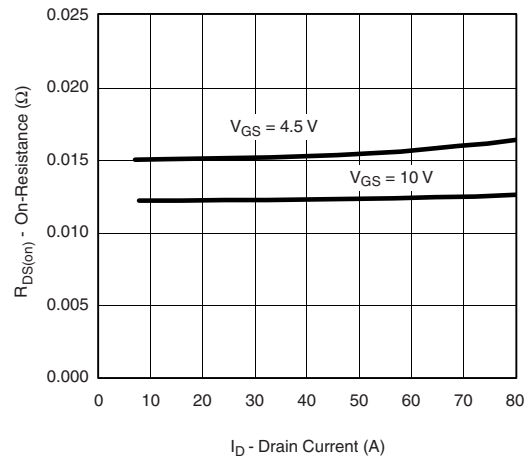
Output Characteristics



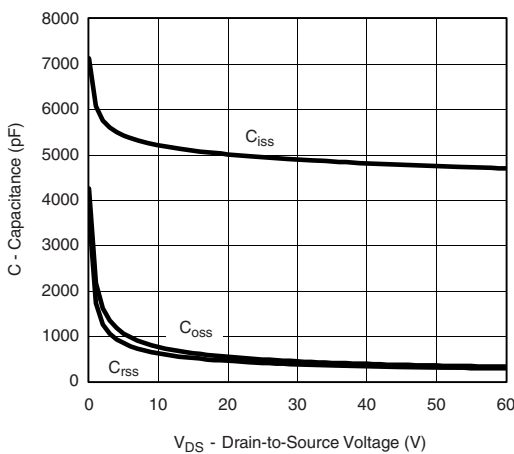
Transfer Characteristics



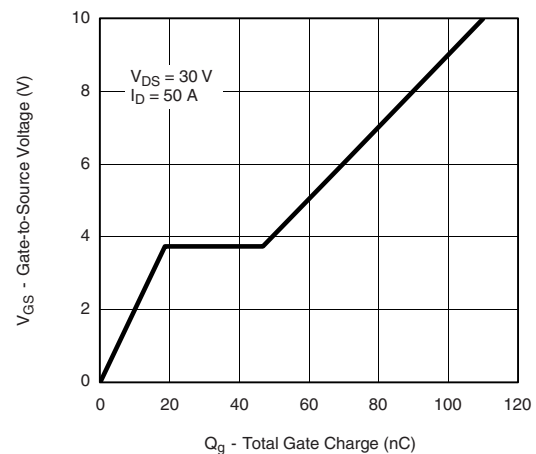
Transconductance



On-Resistance vs. Drain Current



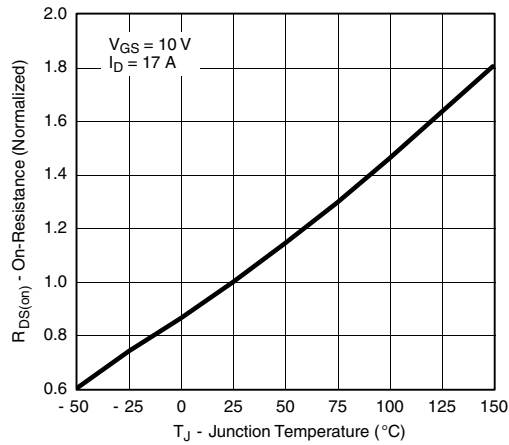
Capacitance



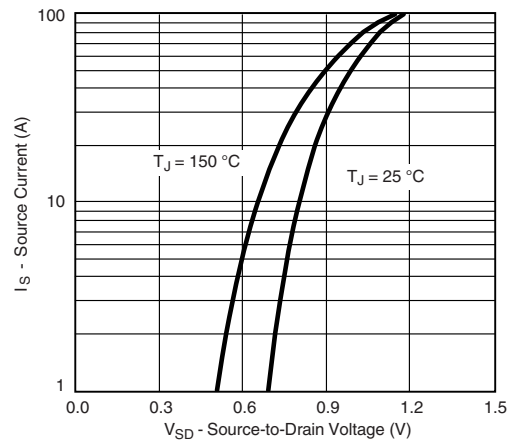
Gate Charge



TYPICAL CHARACTERISTICS

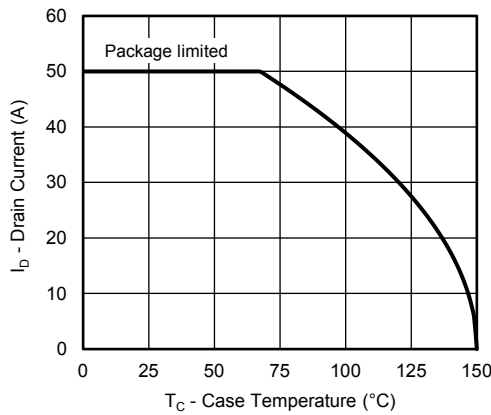


On-Resistance vs. Junction Temperature

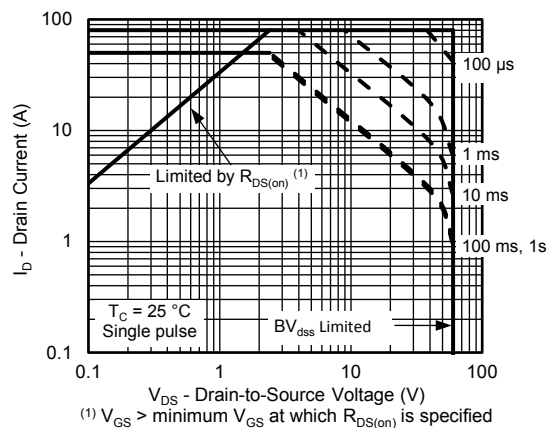


Source-Drain Diode Forward Voltage

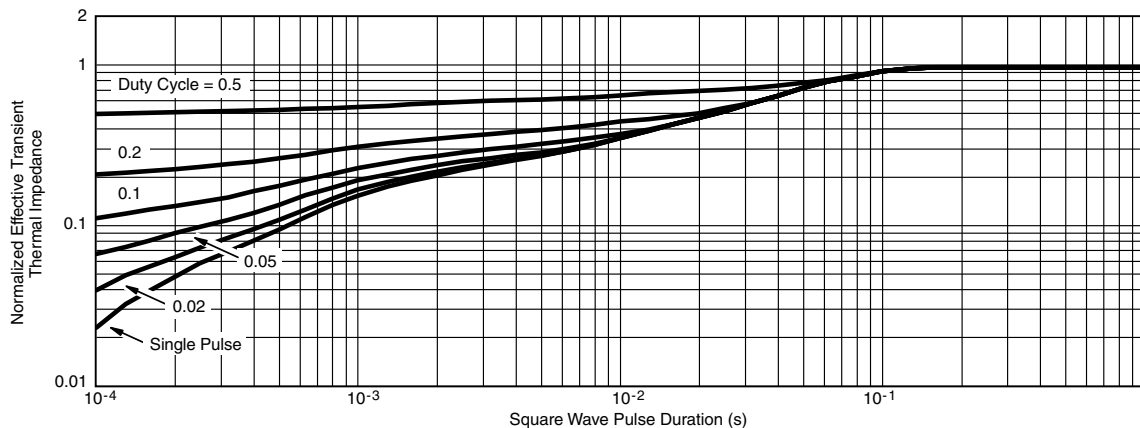
THERMAL RATINGS (25 °C, unless otherwise noted)



Drain Current vs. Case Temperature



Safe Operating Area

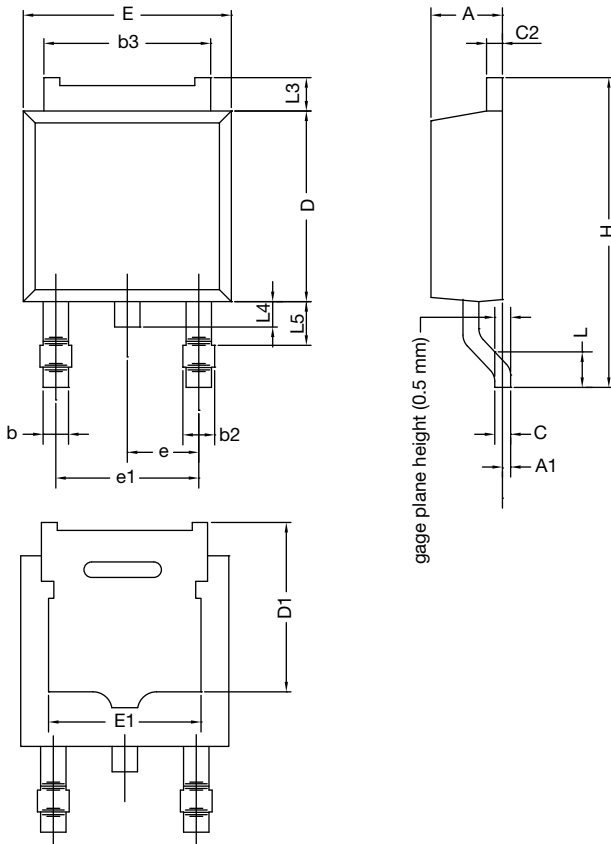


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for silicon technology and package reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?68940](http://www.vishay.com/ppg?68940).



### TO-252AA Case Outline

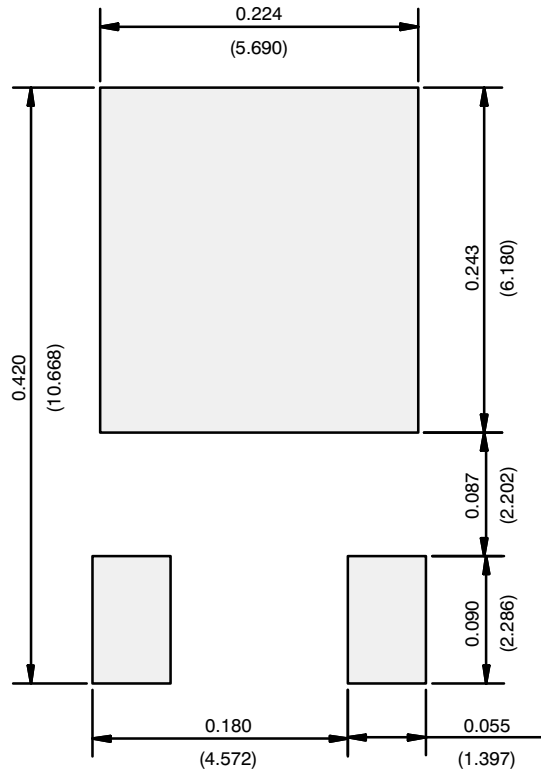


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16				
DWG: 5347				

**Notes**

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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