

74VHC74FT

1. Functional Description

- Dual D-Type Flip-Flop with Preset and Clear

2. General

The 74VHC74FT is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

$\overline{\text{CLR}}$ and $\overline{\text{PR}}$ are independent of the CK and are accomplished by setting the appropriate input low.

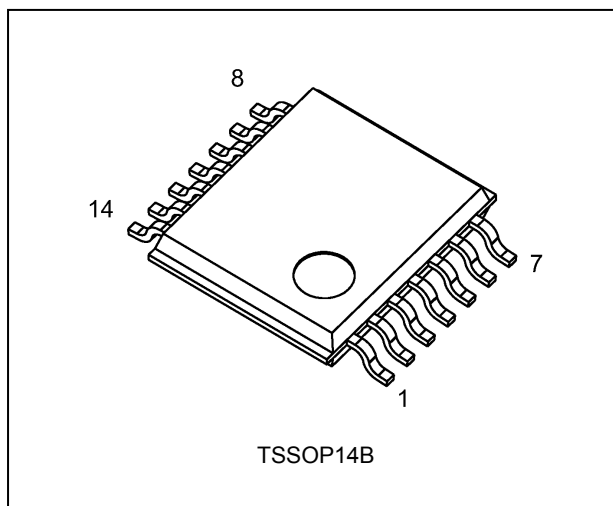
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range: $T_{\text{opr}} = -40$ to 125 °C
- (3) High speed: $f_{\text{MAX}} = 170$ MHz (typ.) at $V_{\text{CC}} = 5.0$ V
- (4) Low power dissipation: $I_{\text{CC}} = 2.0$ μA (max) at $T_a = 25$ °C
- (5) High noise immunity: $V_{\text{NIH}} = V_{\text{NIL}} = 28\%$ V_{CC} (min)
- (6) Power-down protection is provided on all inputs.
- (7) Balanced propagation delays: $t_{\text{PLH}} \approx t_{\text{PHL}}$
- (8) Wide operating voltage range: $V_{\text{CC(opr)}} = 2.0$ V to 5.5 V
- (9) Pin and function compatible with the 74 series (74AC/HC/AHC etc.) 74 type.

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

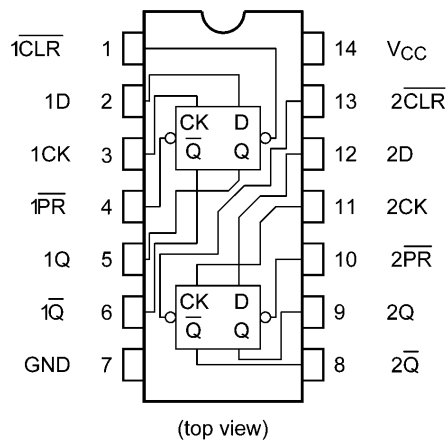
4. Packaging



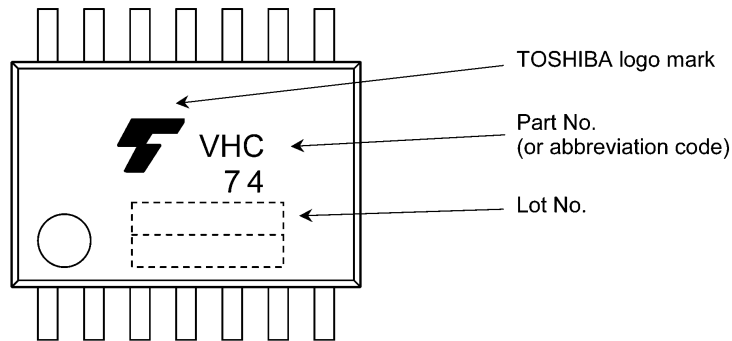
Start of commercial production

2013-05

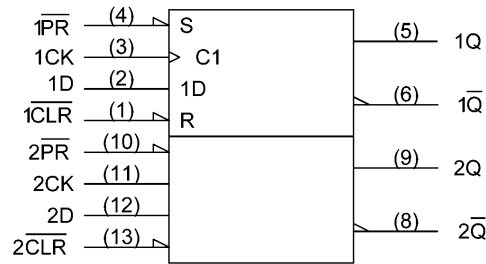
5. Pin Assignment



6. Marking



7. IEC Logic Symbol



8. Truth Table

Inputs				Outputs		Function
CLR	PR	D	CK	Q	Q [̄]	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q _n	Q _n [̄]	No Change

X: Don't care

9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to 7.0	V
Output voltage	V_{OUT}		-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}		-20	mA
Output diode current	I_{OK}		± 20	mA
Output current	I_{OUT}		± 25	mA
V_{CC} /ground current	I_{CC}		± 50	mA
Power dissipation	P_D	(Note 1)	180	mW
Storage temperature	T_{stg}		-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of $T_a = -40$ to $85^{\circ}C$. From $T_a = 85$ to $125^{\circ}C$ a derating factor of -3.25 mW/ $^{\circ}C$ shall be applied until 50 mW.

10. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}		2.0 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	V
Output voltage	V_{OUT}		0 to V_{CC}	V
Operating temperature	T_{opr}		-40 to 125	$^{\circ}C$
Input rise and fall times	dt/dv	$V_{CC} = 3.3 \pm 0.3$ V	0 to 100	ns/V
		$V_{CC} = 5.0 \pm 0.5$ V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				3.0 to 5.5	—	—	$V_{CC} \times 0.3$	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
			4.5	4.4	4.5	—		
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—	—	
			$I_{OH} = -8\text{ mA}$	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	—	0.36	
			$I_{OL} = 8\text{ mA}$	4.5	—	—	0.36	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND		0 to 5.5	—	—	± 0.1	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	—	2.0	

11.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $85\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				3.0 to 5.5	—	$V_{CC} \times 0.3$	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.48	—	
			$I_{OH} = -8\text{ mA}$	4.5	3.80	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.44	
			$I_{OL} = 8\text{ mA}$	4.5	—	0.44	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND		0 to 5.5	—	± 1.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND		5.5	—	20.0	

11.3. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $125\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				3.0 to 5.5	—	$V_{CC} \times 0.3$	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
				$I_{OH} = -4\text{ mA}$	3.0	2.40	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
				$I_{OL} = 4\text{ mA}$	3.0	—	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND		0 to 5.5	—	± 2.0	μA
				I_{CC}	$V_{IN} = V_{CC}$ or GND		

11.4. Timing Requirements (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	3.3 ± 0.3	6.0	ns
			5.0 ± 0.5	5.0	
Minimum pulse width (CLR, PR)	$t_{w(L)}$	—	3.3 ± 0.3	6.0	ns
			5.0 ± 0.5	5.0	
Minimum setup time	t_s	—	3.3 ± 0.3	6.0	ns
			5.0 ± 0.5	5.0	
Minimum hold time	t_h	—	3.3 ± 0.3	0.5	ns
			5.0 ± 0.5	0.5	
Minimum removal time (CLR, PR)	t_{rem}	—	3.3 ± 0.3	5.0	ns
			5.0 ± 0.5	3.0	

11.5. Timing Requirements (Unless otherwise specified, $T_a = -40$ to $85\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	3.3 ± 0.3	7.0	ns
			5.0 ± 0.5	5.0	
Minimum pulse width (CLR, PR)	$t_{w(L)}$	—	3.3 ± 0.3	7.0	ns
			5.0 ± 0.5	5.0	
Minimum setup time	t_s	—	3.3 ± 0.3	7.0	ns
			5.0 ± 0.5	5.0	
Minimum hold time	t_h	—	3.3 ± 0.3	0.5	ns
			5.0 ± 0.5	0.5	
Minimum removal time (CLR, PR)	t_{rem}	—	3.3 ± 0.3	5.0	ns
			5.0 ± 0.5	3.0	

11.6. Timing Requirements
 (Unless otherwise specified, $T_a = -40$ to $125\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	3.3 ± 0.3	7.0	ns
			5.0 ± 0.5	5.0	
Minimum pulse width (CLR, PR)	$t_{w(L)}$	—	3.3 ± 0.3	7.0	ns
			5.0 ± 0.5	5.0	
Minimum setup time	t_s	—	3.3 ± 0.3	8.0	ns
			5.0 ± 0.5	5.5	
Minimum hold time	t_h	—	3.3 ± 0.3	0.5	ns
			5.0 ± 0.5	0.5	
Minimum removal time (CLR, PR)	t_{rem}	—	3.3 ± 0.3	5.0	ns
			5.0 ± 0.5	3.0	

11.7. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time (CK-Q, \bar{Q})	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	—	6.7	11.9	ns
					50	—	9.2	15.4	
				5.0 ± 0.5	15	—	4.6	7.3	
					50	—	6.1	9.3	
Propagation delay time (CLR, PR, \bar{Q} , \bar{Q})	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	—	7.6	12.3	ns
					50	—	10.1	15.8	
				5.0 ± 0.5	15	—	4.8	7.7	
					50	—	6.3	9.7	
Maximum clock frequency	f_{MAX}		—	3.3 ± 0.3	15	80	125	—	MHz
					50	50	75	—	
				5.0 ± 0.5	15	130	170	—	
					50	90	115	—	
Input capacitance	C_{IN}		—			—	4	10	pF
Power dissipation capacitance	C_{PD}	(Note 1)	—			—	25	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

11.8. AC Characteristics

(Unless otherwise specified, $T_a = -40$ to 85 °C, Input: $t_r = t_f = 3$ ns)

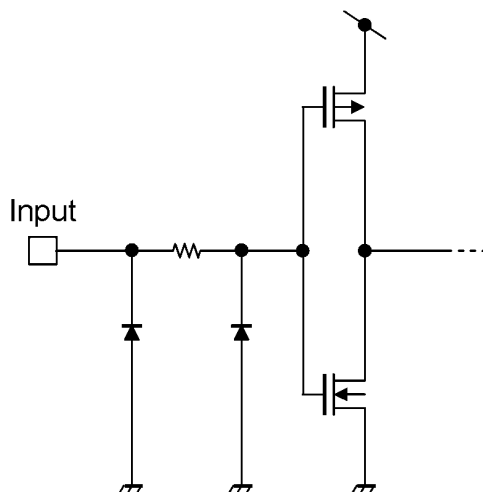
Characteristics	Symbol	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time (CK-Q, \bar{Q})	t_{PLH}, t_{PHL}	—	3.3 ± 0.3	15	1.0	14.0	ns
				50	1.0	17.5	
			5.0 ± 0.5	15	1.0	8.5	
				50	1.0	10.5	
Propagation delay time (CLR, PR-Q, \bar{Q})	t_{PLH}, t_{PHL}	—	3.3 ± 0.3	15	1.0	14.5	ns
				50	1.0	18.0	
			5.0 ± 0.5	15	1.0	9.0	
				50	1.0	11.0	
Maximum clock frequency	f_{MAX}	—	3.3 ± 0.3	15	70	—	MHz
				50	45	—	
			5.0 ± 0.5	15	110	—	
				50	75	—	
Input capacitance	C_{IN}	—			—	10	pF

11.9. AC Characteristics

(Unless otherwise specified, $T_a = -40$ to 125 °C, Input: $t_r = t_f = 3$ ns)

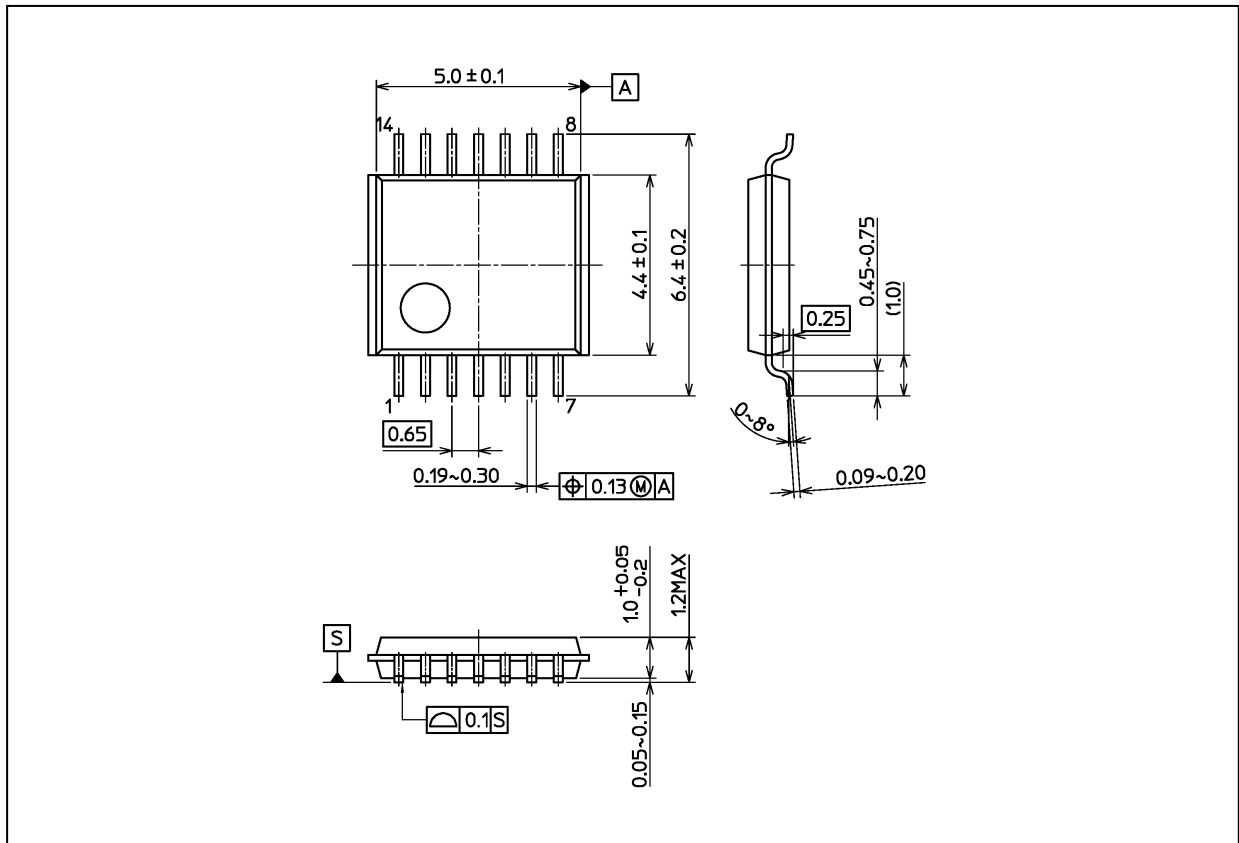
Characteristics	Symbol	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time (CK-Q, \bar{Q})	t_{PLH}, t_{PHL}	—	3.3 ± 0.3	15	1.0	16.0	ns
				50	1.0	19.5	
			5.0 ± 0.5	15	1.0	10.0	
				50	1.0	12.0	
Propagation delay time (CLR, PR-Q, \bar{Q})	t_{PLH}, t_{PHL}	—	3.3 ± 0.3	15	1.0	16.5	ns
				50	1.0	20.0	
			5.0 ± 0.5	15	1.0	10.5	
				50	1.0	12.5	
Maximum clock frequency	f_{MAX}	—	3.3 ± 0.3	15	60	—	MHz
				50	40	—	
			5.0 ± 0.5	15	100	—	
				50	70	—	
Input capacitance	C_{IN}	—			—	10	pF

12. Input Equivalent Circuit



Package Dimensions

Unit: mm



Weight: 0.054 g (typ.)

Package Name(s)
Nickname: TSSOP14B

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