THE DATASHEET OF

75119P

SLLS073D – MAY 1976 – REVISED MAY 1998

features common to all types

- Single 5-V Supply
- 3-State Driver Output Circuitry
- TTL-Compatible Driver Inputs
- TTL-Compatible Receiver Output
- Differential Line Operation
- Receiver Output Strobe (SN55116, SN75116, SN75117) or Enable (SN75118, SN75119)
- Designed for Party-Line (Data-Bus) Applications

additional features of the SN55116/SN75116

- Choice of Ceramic or Plastic Packages
- Independent Driver and Receiver
- Choice of Open-Collector or Totem-Pole Outputs on Both Driver and Receiver
- Dual Data Inputs on Driver
- Optional Line-Termination Resistor in Receiver
- ±15-V Receiver Common-Mode Capability
- Receiver Frequency-Response Control

additional features of the SN75117

- Driver Output Internally Connected to Receiver Input

The SN75118 is an SN75116 With 3-State Receiver Output Circuitry
The SN75119 is an SN75117 With 3-State Receiver Output Circuitry

description

These integrated circuits are designed for use in interfacing between TTL-type digital systems and differential data-transmission lines. They are especially useful for party-line (data-bus) applications. Each of these circuit types combine in one package a 3-state differential line driver and a differential-input line receiver, both of which operate from a single 5-V power supply. The driver inputs and the receiver outputs are TTL compatible. The driver employed is similar to the SN55113 and SN75113 3-state line drivers, and the receiver is similar to the SN55115 and SN75115 line receivers.

The SN55116, SN75116, and SN75118 offer all the features of the SN55113 and SN75113 drivers and the SN55115 and SN75115 receivers combined. The driver performs the dual input AND and NAND functions when enabled or presents a high impedance to the load when in the disabled state. The driver output stages are similar to TTL totem-pole outputs, but have the current-sinking portion separated from the current-sourcing portion and both are brought out to adjacent package terminals. This feature allows the user the option of using the driver in the open-collector output configuration, or, by connecting the adjacent source and sink terminals together, of using the driver in the normal totem-pole output configuration.

The receiver portion of the SN55116, SN75116, and SN75118 features a differential-input circuit having a common-mode voltage range of ±15 V. An internal 130-Ω equivalent resistor also is provided, which optionally can be used to terminate the transmission line. A frequency-response control terminal allows the user to reduce the speed of the receiver or to improve differential noise immunity. The receivers of the SN55116 and SN75116 have an output strobe and a split totem-pole output. The receiver of the SN75118 has an output-enable for the 3-state split totem-pole output. The receiver section of either circuit is independent of the driver section except for the V_{CC} and ground terminals.

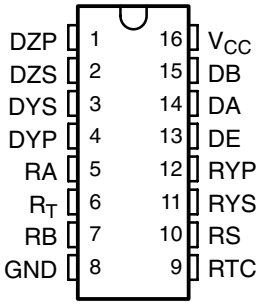
The SN75117 and SN75119 provide the basic driver and receiver functions of the SN55116, SN75116, and SN75118, but use a package that is only half as large. The SN75117 and SN75119 are intended primarily for party-line or bus-organized systems because the driver outputs are internally connected to the receiver inputs. The driver has a single data input and a single enable input. The SN75117 receiver has an output strobe, while the SN75119 receiver has a 3-state output enable. However, these devices do not provide output connection options, line-termination resistors, or receiver frequency-response controls.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

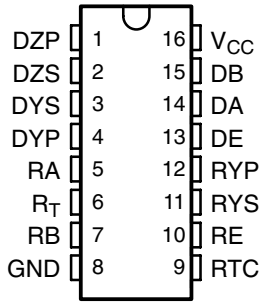
description (continued)

The SN55116 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75116, SN75117, SN75118, and SN75119 are characterized for operation from 0°C to 70°C.

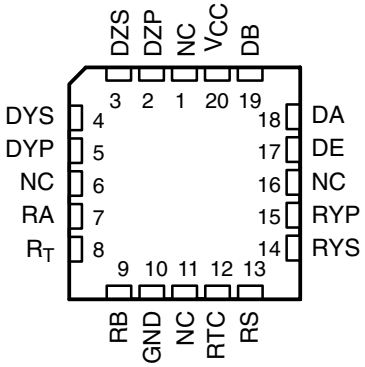
SN55116 . . . J PACKAGE
SN75116 . . . D OR N PACKAGE
(TOP VIEW)



SN75118 . . . D OR N PACKAGE
(TOP VIEW)

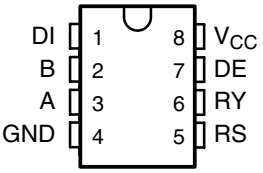


SN55116 . . . FK PACKAGE
(TOP VIEW)

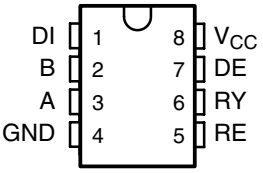


NC – No internal connection

SN75117 . . . D OR P PACKAGE
(TOP VIEW)



SN75119 . . . D OR P PACKAGE
(TOP VIEW)



Function Tables

'116, SN75118
DRIVER

INPUTS			OUTPUTS	
DE	DA	DB	DY	DZ
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L

SN75117, SN75119
DRIVER

INPUTS		OUTPUTS	
DI	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

'116, SN75118
RECEIVER

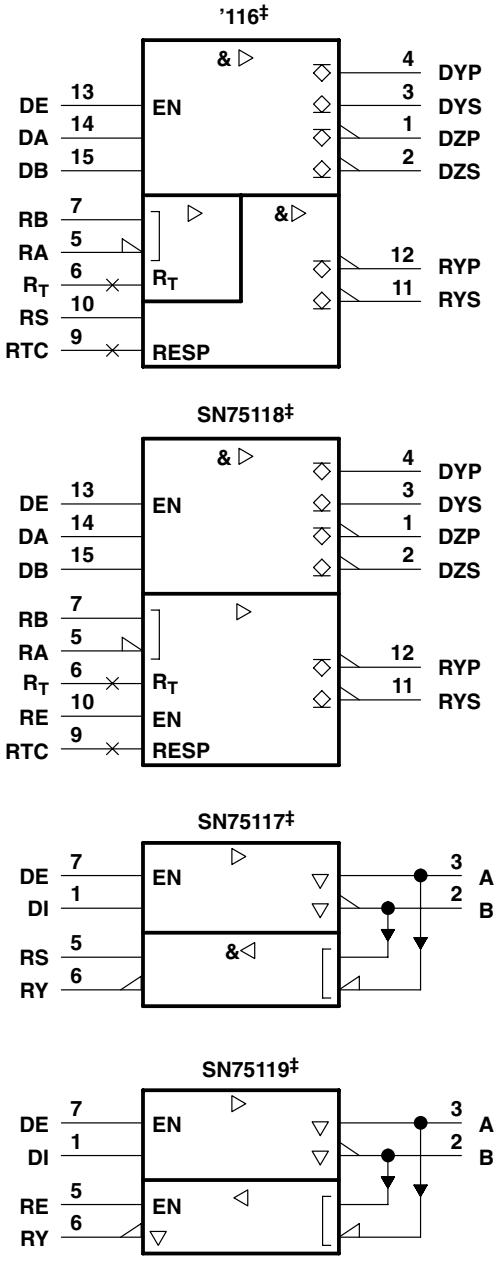
RS/RE	DIFF INPUT	OUTPUTS RY	
		'116	SN75118
L	X	H	Z
H	L	H	H
H	H	L	L

SN75117, SN75119
RECEIVER

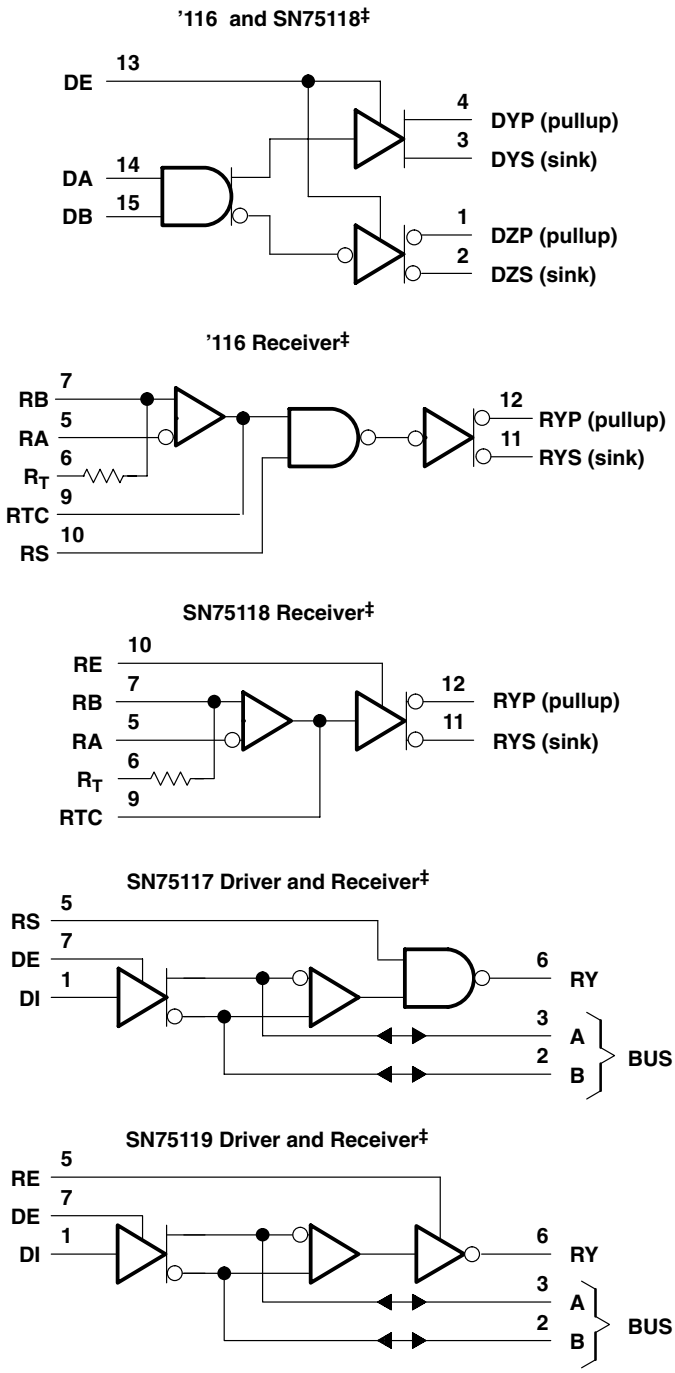
INPUTS			OUTPUT RY	
A	B	RS/RE	SN75117	SN75119
H	L	H	H	H
L	H	H	L	L
X	X	L	H	Z

H = high level ($V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max), L = low level ($V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max),
X = irrelevant, Z = high impedance (off)

logic symbol†



logic diagram (positive logic)

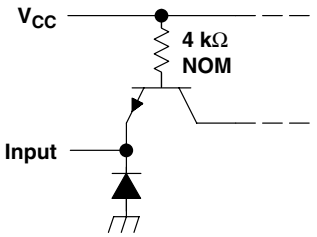


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

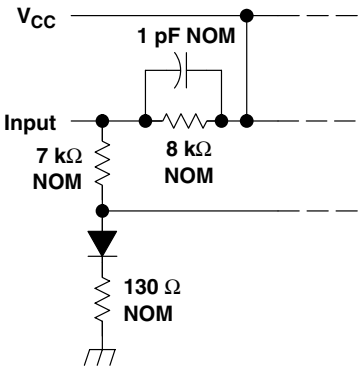
‡ Pin numbers shown for the SN55116 and SN75116 are for the D, J, and N packages, those shown for the SN75118 are for the D and N packages, and those shown for SN75117 and SN75119 are for the D and P packages.

schematics of inputs and outputs

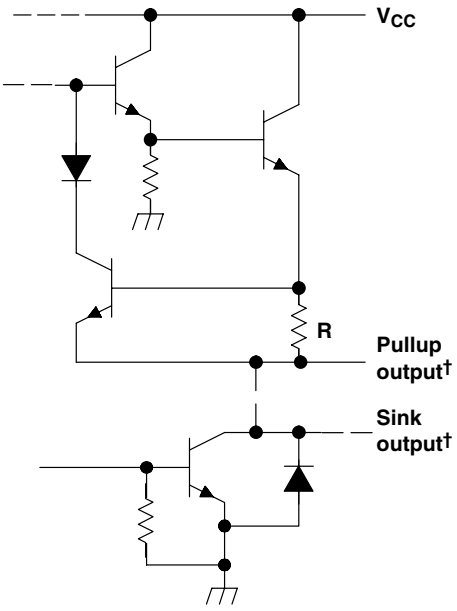
EQUIVALENT OF EACH DRIVER INPUT AND EACH RE AND RS INPUT



EQUIVALENT OF EACH RECEIVER INPUT (EXCLUDING ENABLES AND STROBES)



TYPICAL OF ALL OUTPUTS



Driver output R = 9 Ω NOM
Receiver output R = 20 Ω NOM

† On SN75117 and SN75119, common outputs replace the separate pullup and sink outputs.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage, V_{CC} (see Notes 1 and 2) . . . . . 7 V
Input voltage, V_I: DA, DB, DE, DI, RE, and RS . . . . . 5.5 V
RA, RB, R_T for ’116, SN75118 only . . . . . ±25 V
A and B for SN75117, SN75119 only . . . . . 0 to 6 V
Off-state voltage applied to open-collector outputs: ’116, SN75118 only . . . . . 12 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 60 seconds, T_C: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package . . . . . 260°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. In the FK and J packages, the SN55116 chip is alloy mounted. The SN75116, SN75117, SN75118, and SN75119 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	725 mW	5.8 mW/°C	464 mW	—
D (16 pin)	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

PARAMETER		SN55116			SN75116, SN75117, SN75118, SN75119			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High-level input voltage, V_{IH}	All inputs except differential inputs	2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
High-level output current, I_{OH}	Drivers			−40			−40	mA
	Receivers			−5			−5	
Low-level output current, I_{OL}	Drivers			40			40	mA
	Receivers			15			15	
Receiver input voltage, V_I	’116, SN75118			±15			±15	V
	SN75117, SN75119	0		6	0		6	
Common-mode receiver input voltage, V_{ICR}	’116, SN75118			±15			±15	V
	SN75117, SN75119	0		6	0		6	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

driver section

PARAMETER			TEST CONDITIONS†			'116, SN75118			SN75117, SN75119			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = –12 mA			–0.9	–1.5		–0.9	–1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{IH} = 2 V	T_A = 25°C (SN55116), T_A = 0°C to 70°C (SN75116, SN75117, SN75118, SN75119)	I_{OH} = –10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = –40 mA	2	3		2	3		
				T_A = –55°C to 125°C (SN55116)	I_{OH} = –10 mA	2			2			
					I_{OH} = –40 mA	1.8			1.8			
V_{OL}	Low-level output voltage		V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA			0.4			0.4	V
V_{OK}	Output clamp voltage		V_{CC} = MAX,	I_O = –40 mA,	DE at 0.8 V			–1.5			–1.5	V
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX, V_O = 12 V	T_A = 25°C			1	10				μA
				T_A = MAX	SN55116			200				
					SN75116, SN75118			20				
I_{OZ}	Off-state (high-impedance-state) output current		V_{CC} = MAX,	V_O = 0 to V_{CC},	DE at 0.8 V, T_A = 25°C			±10				μA
			V_{CC} = MAX, DE at 0.8 V, T_A = MAX	V_O = 0	SN55116			–300				
				V_O = 0.4 V to V_{CC}	SN55116			±150				
				V_O = 0 to V_{CC}	SN75116, SN75118			±20				
I_I	Input current at maximum input voltage	Driver or enable input	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V				–1.6			–1.6	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	V_O = 0,	T_A = 25°C	–40		–120	–40		–120	mA
I_{CC}	Supply current (driver and receiver combined)		V_{CC} = MAX,	T_A = 25°C			42	60	42		60	mA

† All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

driver section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation-delay time, low-to-high level output	See Figure 13		14	30	ns
t_{PHL}	Propagation-delay time, high-to-low level output			12	30	
t_{PZH}	Output-enable time to high level	R_L = 180 Ω, See Figure 14		8	20	ns
t_{PZL}	Output-enable time to low level	R_L = 250 Ω, See Figure 15		17	40	ns
t_{PHZ}	Output-disable time from high level	R_L = 180 Ω, See Figure 14		16	30	ns
t_{PLZ}	Output-disable time from low level	R_L = 250 Ω, See Figure 15		20	35	ns

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

receiver section

PARAMETER			TEST CONDITIONS†			'116, SN75118			SN75117, SN75119			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IT+}	Positive-going threshold voltage§		V_O = 0.4 V, See Note 3	I_{OL} = 15 mA,	V_{CC} = MIN, V_{ICR} = 0, See Note 4			0.5			0.5	V
					V_{CC} = 5 V, V_{ICR} = MAX, See Note 5			1			1	
V_{IT-}	Negative-going threshold voltage§		V_O = 2.4 V, See Note 3	I_{OL} = −5 mA,	V_{CC} = MIN, V_{ICR} = 0, See Note 4	−0.5¶			−0.5¶			V
					V_{CC} = 5 V, V_{ICR} = MAX, See Note 5	−1¶			−1¶			
V_I	Input voltage range#		V_{CC} = 5 V,	V_{ID} = −1 V or 1 V,	See Note 3	15 to −15			6 to 0			V
V_{OH}	High-level output voltage		I_{OH} = −5 mA, See Note 3	V_{CC} = MIN, V_{ICR} = 0,	V_{ID} = −0.5 V, See Notes 4 and 6	2.4			2.4			V
				V_{CC} = 5 V, V_{ICR} = MAX,	V_{ID} = −1 V, See Note 5	2.4			2.4			
V_{OL}	Low-level output voltage		I_{OL} = 15 mA, See Note 3	V_{CC} = MIN, V_{ICR} = 0,	V_{ID} = 0.5 V, See Notes 4 and 7			0.4			0.4	V
				V_{CC} = 5 V, V_{ICR} = MAX,	V_{ID} = 1 V, See Note 5			0.4			0.4	
$I_{I(rec)}$	Receiver input current		V_{CC} = MAX, See Note 3	V_I = 0,	Other input at 0 V		−0.5	−0.9		−0.5	−1	mA
				V_I = 0.4 V,	Other input at 2.4 V		−0.4	−0.7		−0.4	−0.8	
				V_I = 2.4 V,	Other input at 0.4 V		0.1	0.3		0.1	0.4	
I_I	Input current at maximum input voltage	Strobe	V_{CC} = MIN, V_{strobe} = 4.5 V	V_{ID} = −0.5 V,	'116, SN75117			5			5	μA
		Enable	V_{CC} = MAX,	V_I = 5.5 V	SN75118, SN75119			1			1	mA

† Unless otherwise noted, V_{strobe} = 2.4 V. All parameters, with the exception of off-state open-collector output current, are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

§ Differential voltages are at the B input terminal with respect to the A input terminal. Neither receiver input of the SN75117 or SN75119 should be taken negative with respect to GND.

¶ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

Input voltage range is the voltage range that, if exceeded at either input, will cause the receiver to cease functioning properly.

NOTES: 3. Measurement of these characteristics on the SN75117 and SN75119 requires the driver to be disabled with the driver enable at 0.8 V.
4. This applies with the less positive receiver input grounded.
5. For '116 and SN75118, this applies with the more positive receiver input at 15 V or the more negative receiver input at – 15 V. For SN75117 and SN75119, this applies with the more positive receiver input at 6 V.
6. For SN55116, V_{ID} = −1 V
7. For SN55116, V_{ID} = 1 V

receiver section (continued)

PARAMETER			TEST CONDITIONS†			’116, SN75118			SN75117, SN75119			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
I_{IH}	High-level input current	Enable	V_{CC} = MAX,	V_I = 2.4 V	SN75118, SN75119			40			40	µA
I_I	Low-level input current	Strobe	V_{CC} = MAX, V_{strobe} = 0.4 V,	V_{ID} = 0.5 V, See Notes 4 and 7	’116, SN75117			−2.4			−2.4	mA
		Enable	V_{CC} = MAX,	V_I = 0.4 V	SN75118, SN75119			−1.6			−1.6	
$I_{(RTC)}$	Response-time-control current (RTC)		V_{CC} = MAX, RC at 0 V,	V_{ID} = 0.5 V, See Notes 4 and 7	T_A = 25°C	−1.2						mA
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX, V_O = 12 V, V_{ID} = − 1 V	T_A = 25°C			1	10				µA
				T_A = MAX	SN55116			200				
					SN75116, SN75118			20				
I_{OZ}	Off-state (high-impedance-state) output current		V_{CC} = MAX, V_O = 0 to V_{CC}, RE at 0.4 V	T_A = 25°C	SN75118, SN75119			±10			±10	µA
				T_A = MAX	SN75118			±20				
					SN75119						±20	
R_T	Line-terminating resistance		V_{CC} = 5 V		T_A = 25°C	77		167				Ω
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_{ID} = − 0.5 V,	V_O = 0, See Notes 4 and 6	T_A = 25°C	−15		−80	−15		−80	mA
I_{CC}	Short current (driver and receiver combined)		V_{CC} = MAX, See Notes 4 and 7	V_{ID} = 0.5 V,	T_A = 25°C		42	60		42	60	mA

† Unless otherwise noted, V_{strobe} = 2.4 V. All parameters, with the exception of off-state open-collector output current, are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

§ Not more than one output should be shorted at a time.

NOTES: 4. This applies with the less positive receiver input grounded.
6. For SN55116, V_{ID} = − 1 V
7. For SN55116, V_{ID} = 1 V

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

receiver section

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation-delay time, low-to-high-level output		R_L = 400 Ω,	See Figure 16		20	75	ns
t_{PHL}	Propagation-delay time, high-to-low-level output		R_L = 400 Ω,	See Figure 16		17	75	ns
t_{PZH}	Output-enable time to high level	SN75118 and SN75119 only	R_L = 480 Ω,	See Figure 14		9	20	ns
t_{PZL}	Output-enable time to low level	SN75118 and SN75119 only	R_L = 250 Ω,	See Figure 15		16	35	ns
t_{PHZ}	Output-disable time from high level	SN75118 and SN75119 only	R_L = 480 Ω,	See Figure 14		12	30	ns
t_{PLZ}	Output-disable time from low level	SN75118 and SN75119 only	R_L = 250 Ω,	See Figure 15		17	35	ns

TYPICAL CHARACTERISTICS†

DRIVER
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

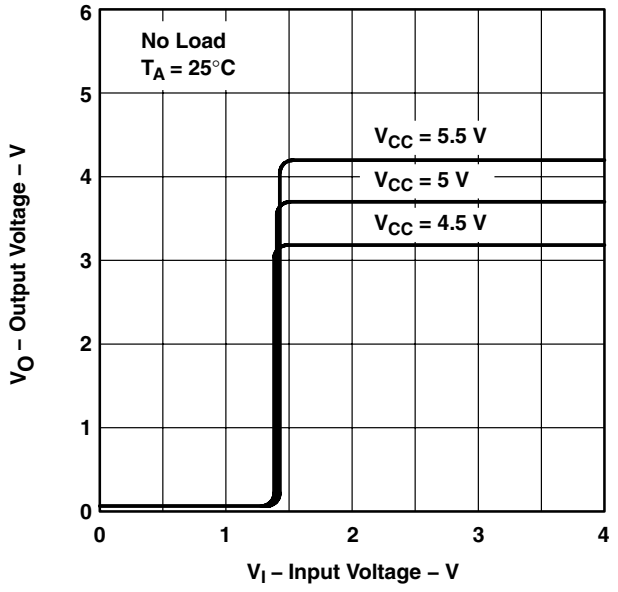


Figure 1

DRIVER
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

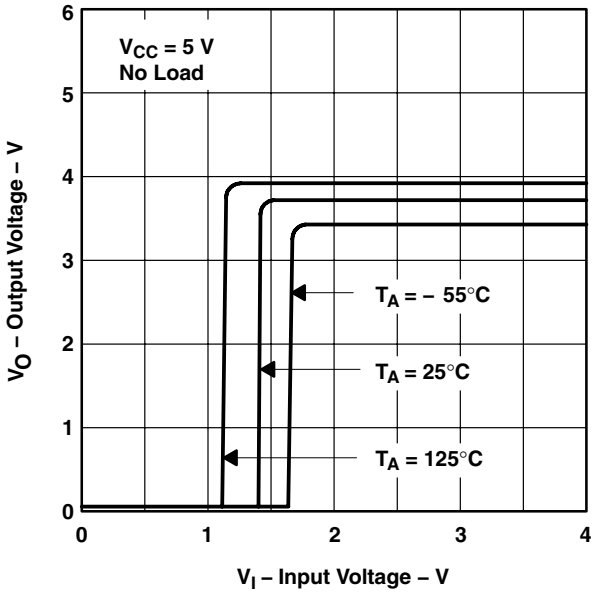


Figure 2

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

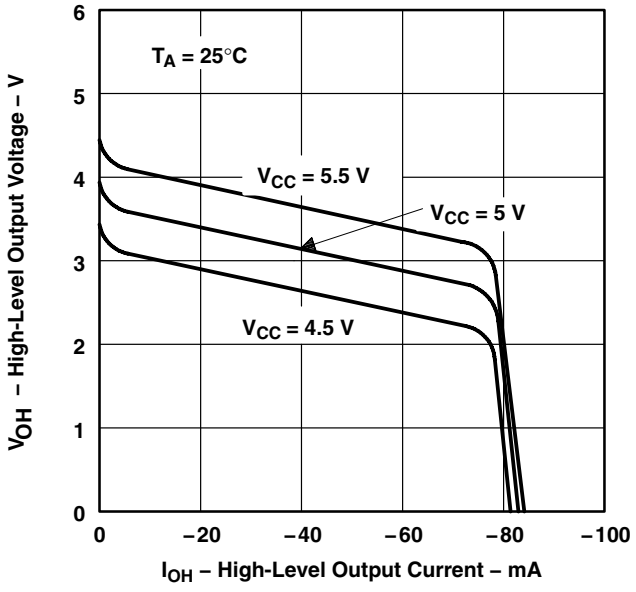


Figure 3

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

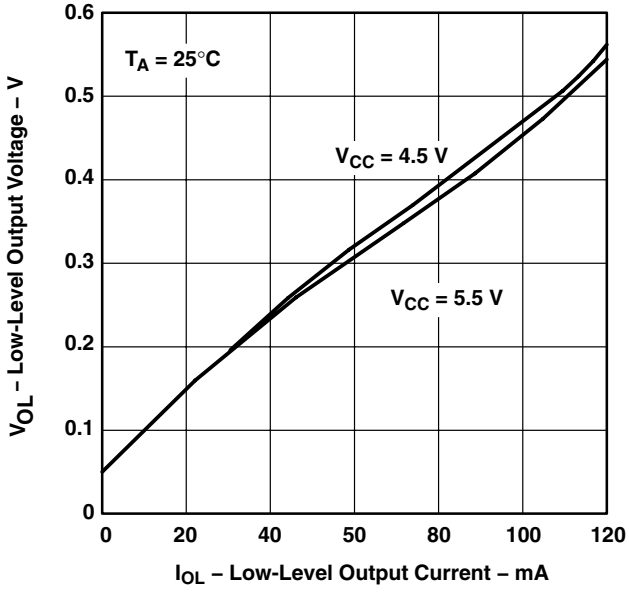


Figure 4

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

DRIVER
PROPAGATION-DELAY TIME
vs
FREE-AIR TEMPERATURE

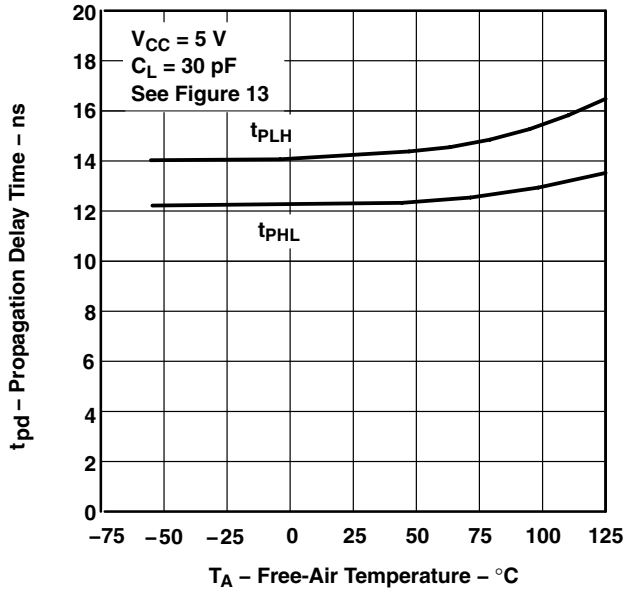
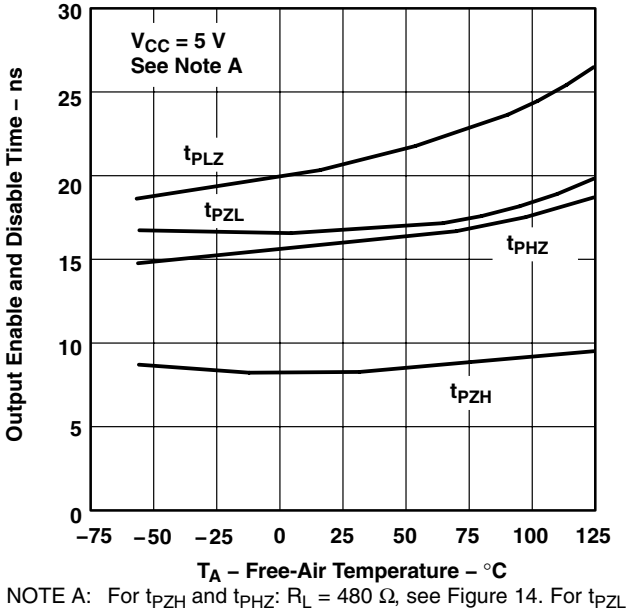


Figure 5

DRIVER
OUTPUT-ENABLE AND DISABLE TIME
vs
FREE-AIR TEMPERATURE



NOTE A: For t_{PZH} and t_{PHZ}: R_L = 480 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

Figure 6

RECEIVER
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

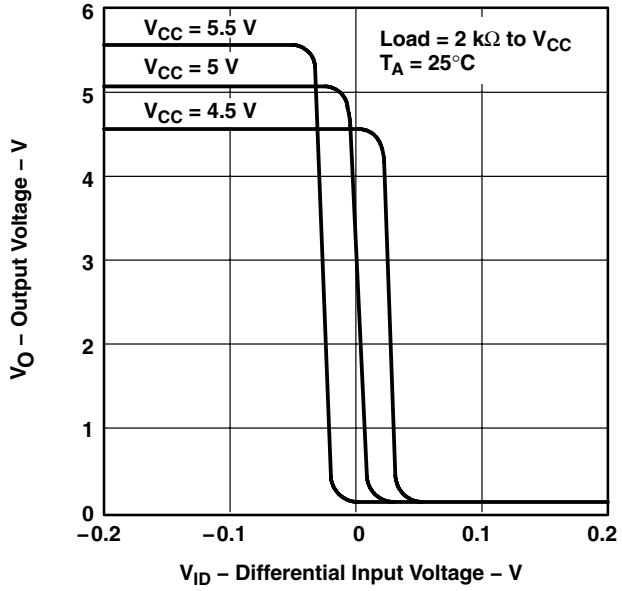


Figure 7

RECEIVER
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

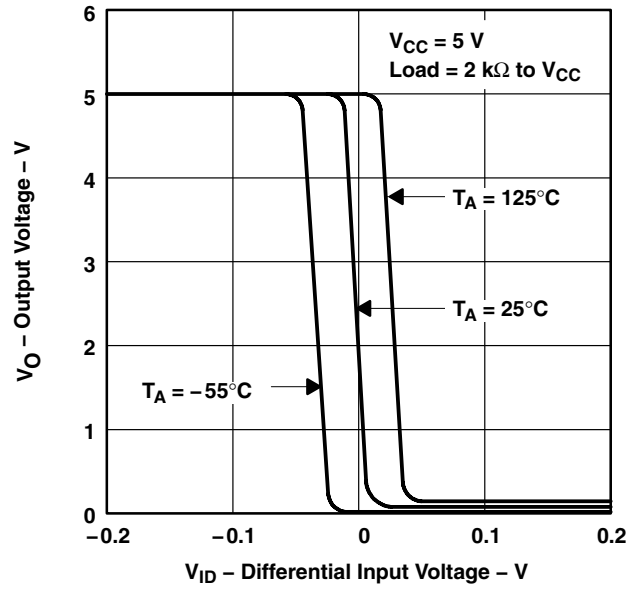


Figure 8

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

RECEIVER
PROPAGATION-DELAY TIME
vs
FREE-AIR TEMPERATURE

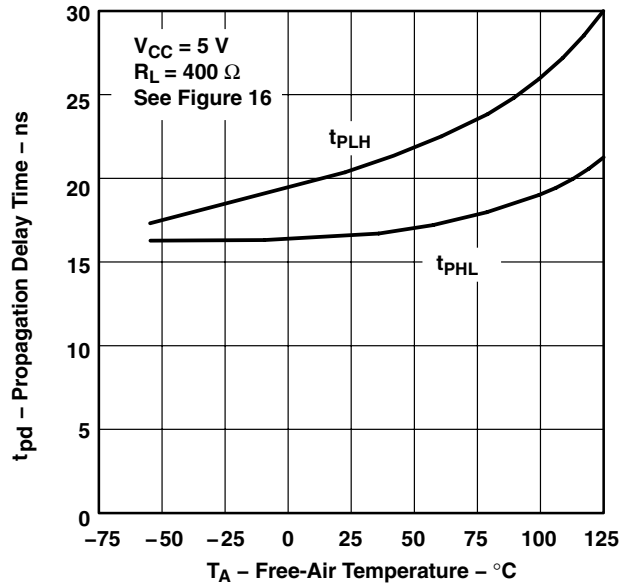
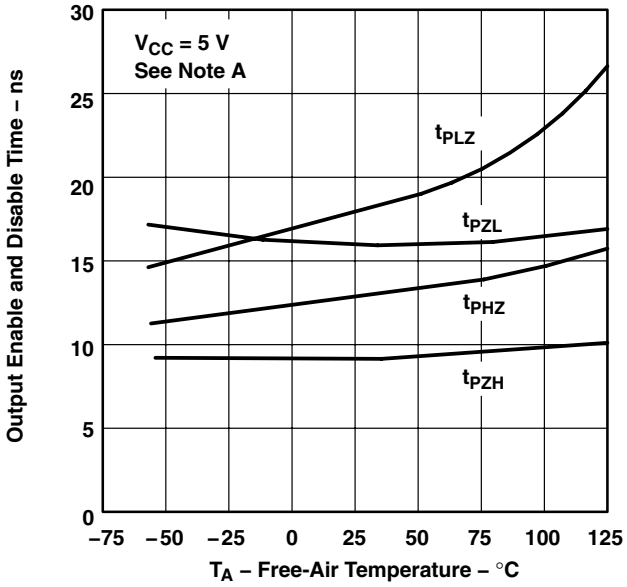


Figure 9

RECEIVER
OUTPUT-ENABLE AND DISABLE TIME
vs
FREE-AIR TEMPERATURE



NOTE A: For t_{PZH} and t_{PHZ} :R_L= 480 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

Figure 10

DRIVER AND RECEIVER
SUPPLY CURRENT
vs
SUPPLY VOLTAGE

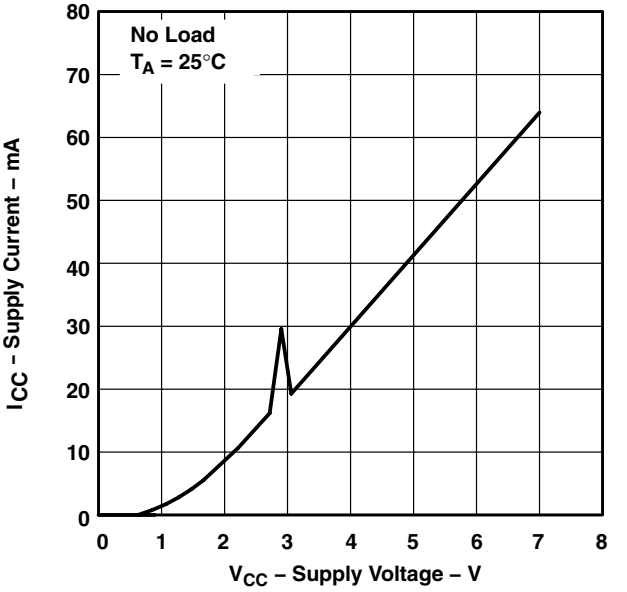


Figure 11

DRIVER AND RECEIVER
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

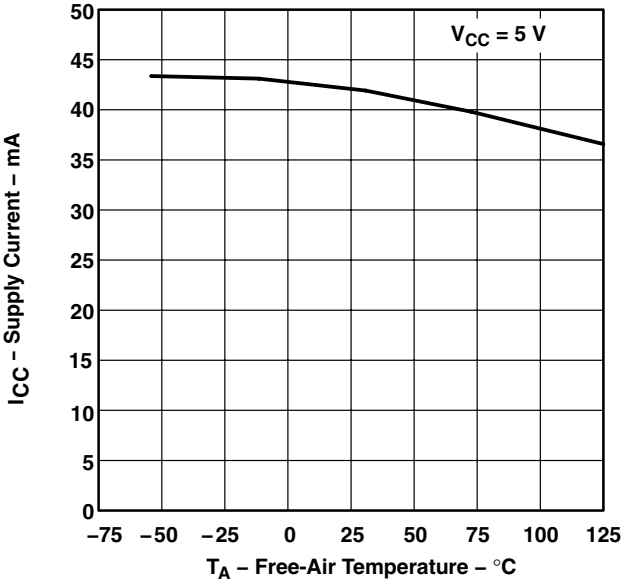
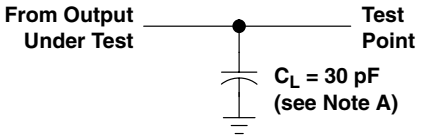


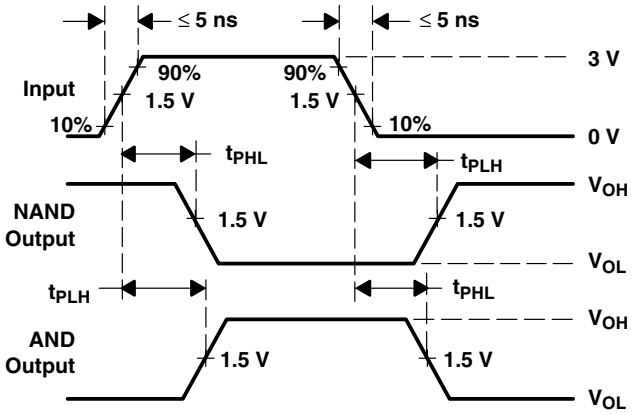
Figure 12

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

PARAMETER MEASUREMENT INFORMATION

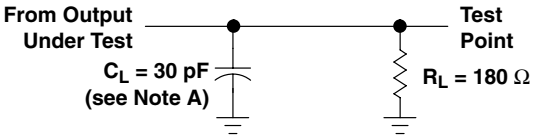


LOAD CIRCUIT

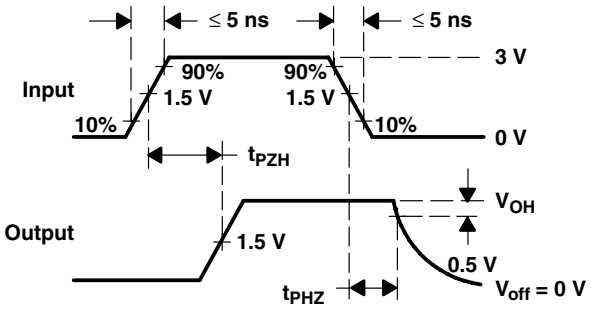


VOLTAGE WAVEFORMS
t_{PLH} and t_{PHL} (drivers only)

Figure 13

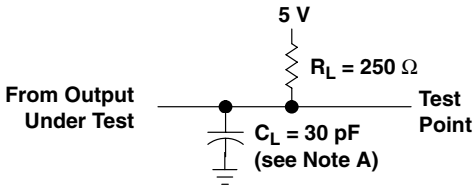


LOAD CIRCUIT

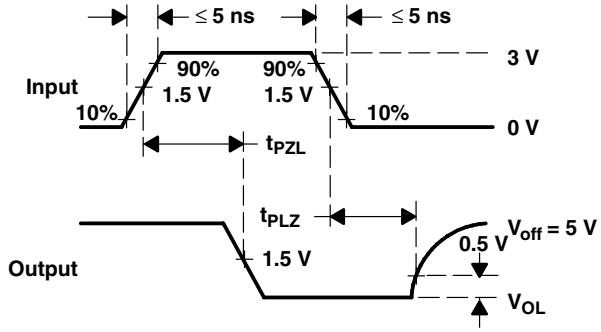


VOLTAGE WAVEFORMS
t_{PZH} and t_{PHZ}

Figure 14

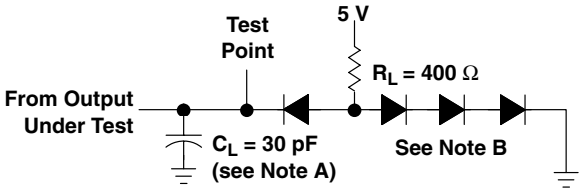


LOAD CIRCUIT

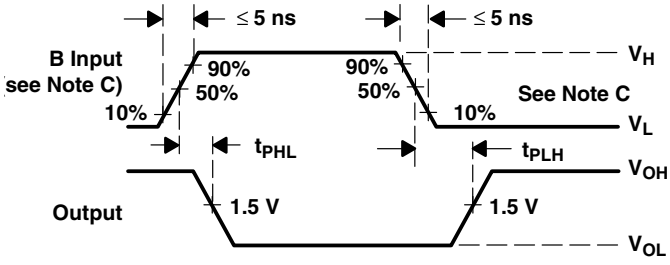


VOLTAGE WAVEFORMS
t_{PZL} and t_{PLZ}
(SN75118 and SN75119 receivers only)

Figure 15



LOAD CIRCUIT



VOLTAGE WAVEFORMS
t_{PLH} and t_{PHL} (receivers only)

Figure 16

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. For ’116 and SN75118, V_H = 3 V, V_L = – 3 V, the A input is at 0 V.
For SN75117 and SN75119, V_H = 3 V, V_L = 0, the A input is at 1.5 V.
D. When testing the ’116 and SN75118 receiver sections, the response-time control and the termination resistor pins are left open.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88511012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88511012A SNJ55116FK	Samples
5962-8851101EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8851101EA SNJ55116J	Samples
SN75116D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75116	Samples
SN75116N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75116N	Samples
SN75116NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75116	Samples
SN75117P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75117P	Samples
SN75118N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75118N	Samples
SN75119D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75119	Samples
SN75119P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75119P	Samples
SNJ55116FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88511012A SNJ55116FK	Samples
SNJ55116J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8851101EA SNJ55116J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN55116, SN75116 :

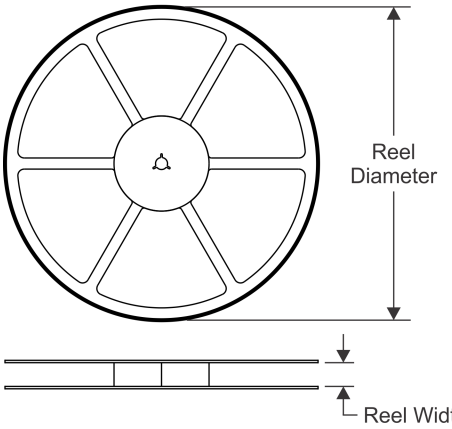
- Catalog: SN75116
- Military: SN55116

NOTE: Qualified Version Definitions:

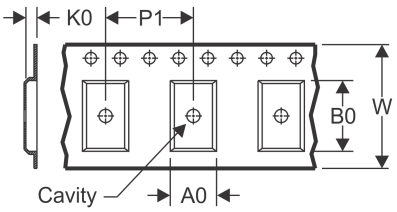
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

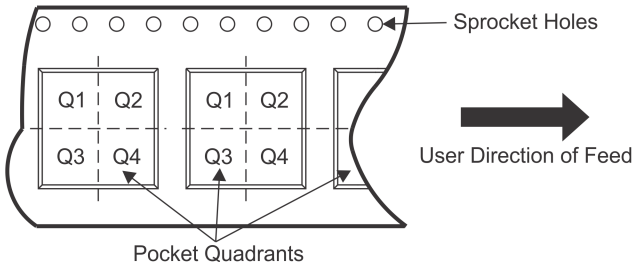


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

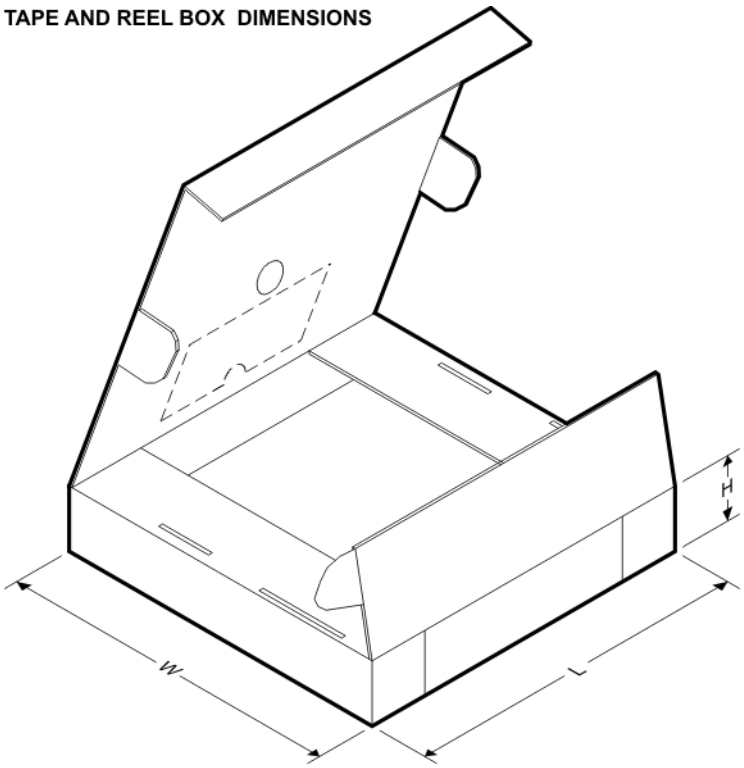
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75116NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

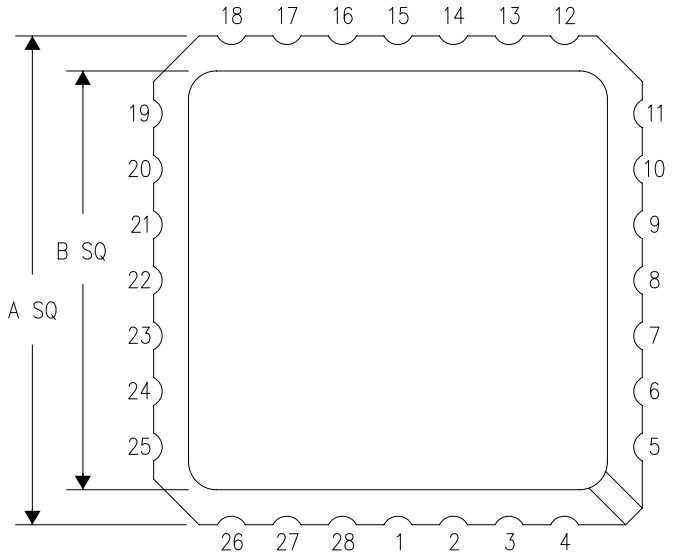


*All dimensions are nominal

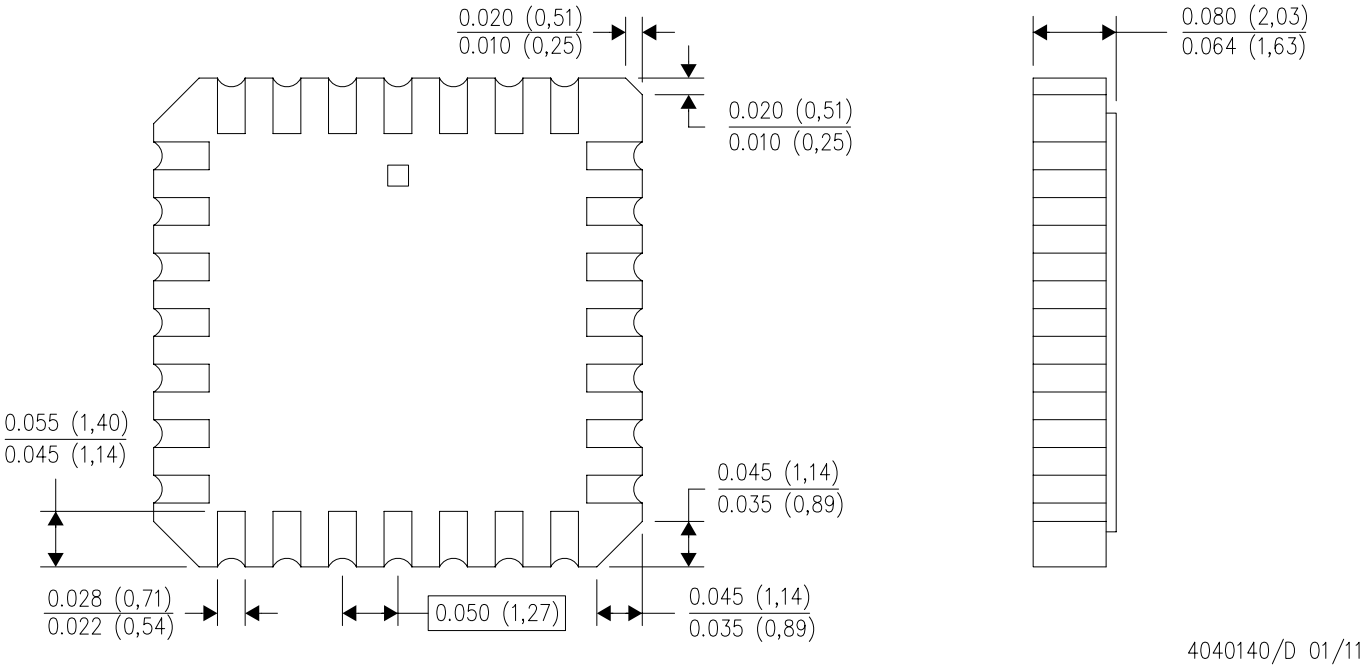
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75116NSR	SO	NS	16	2000	367.0	367.0	38.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



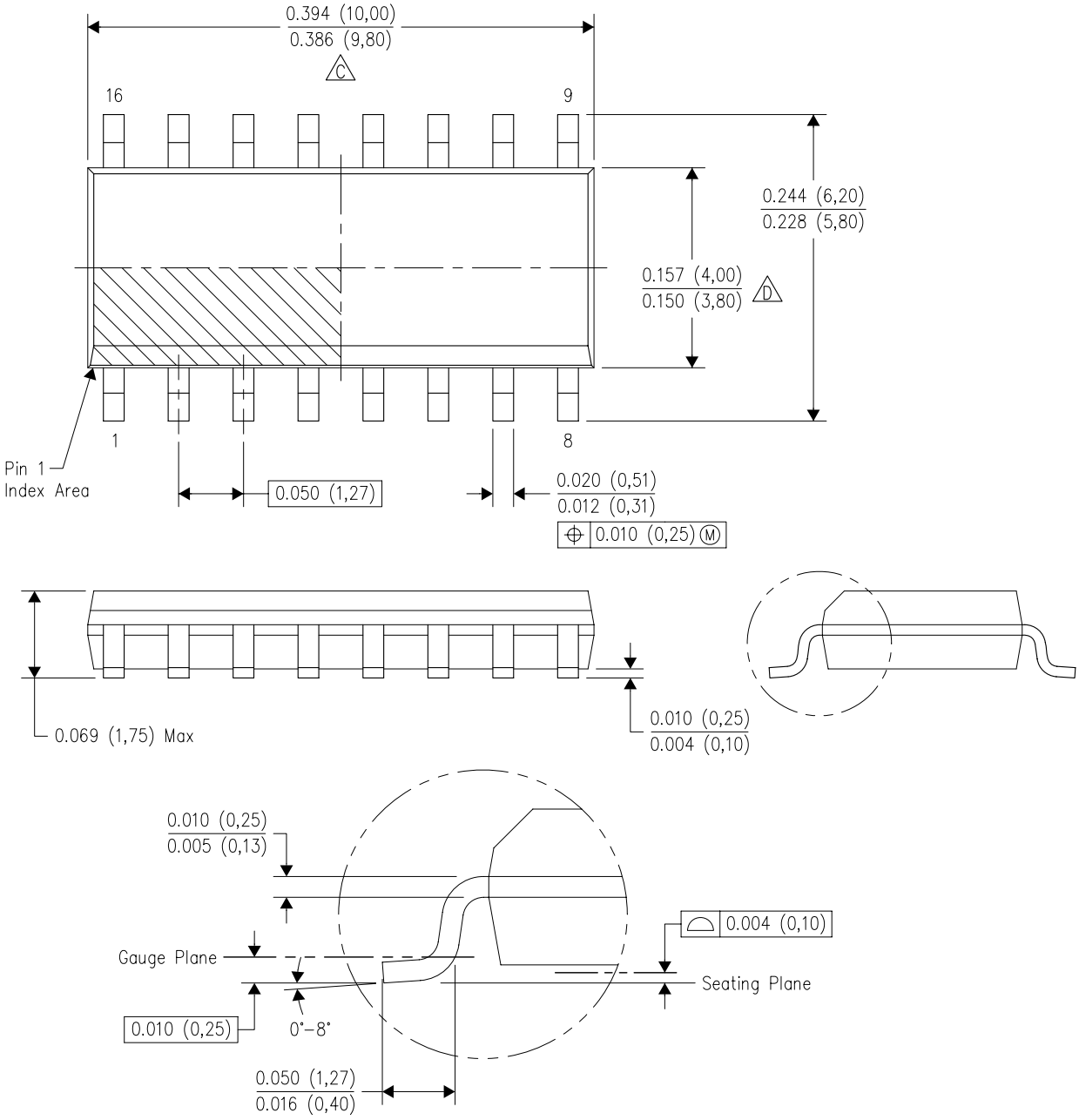
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

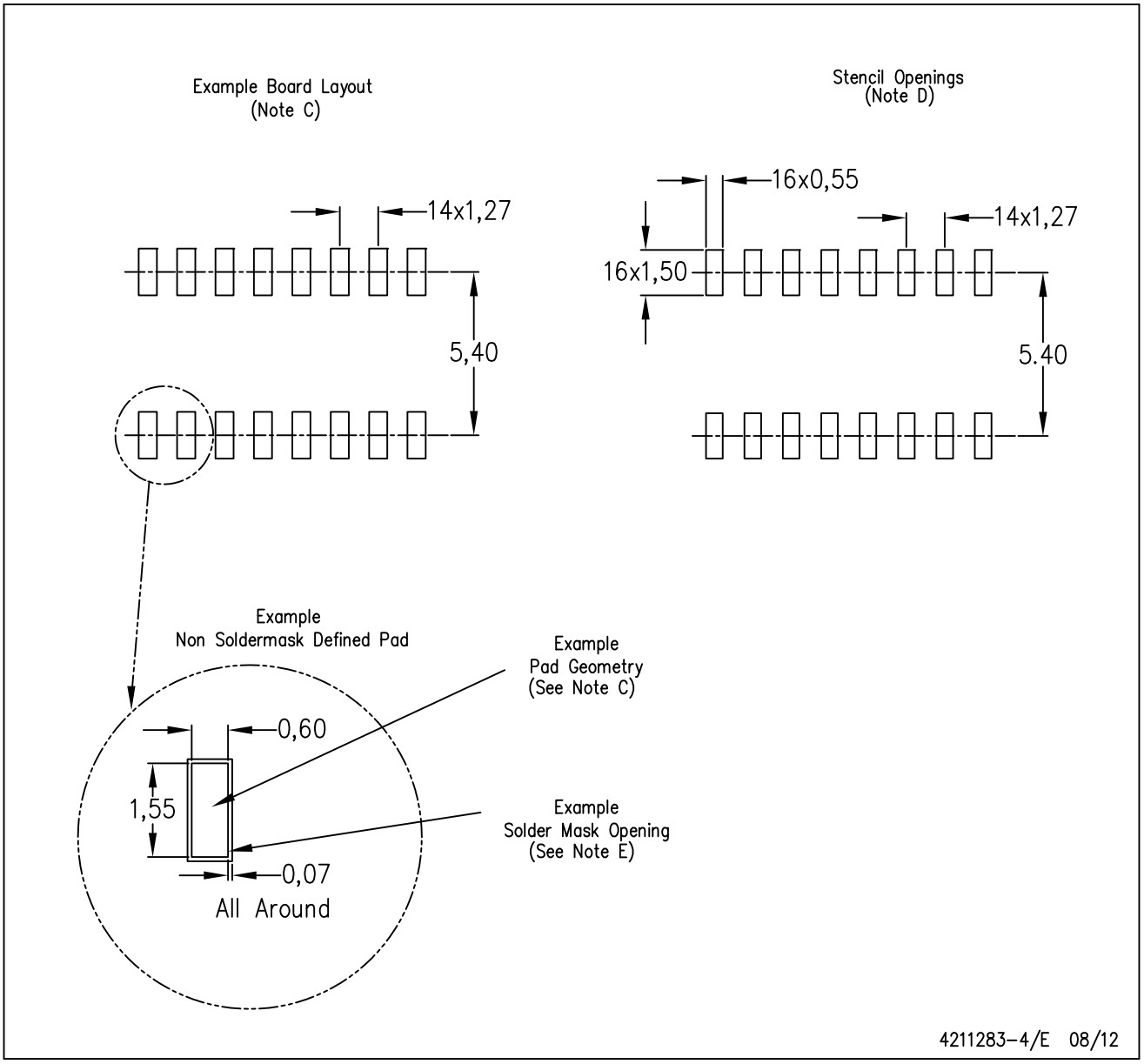
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

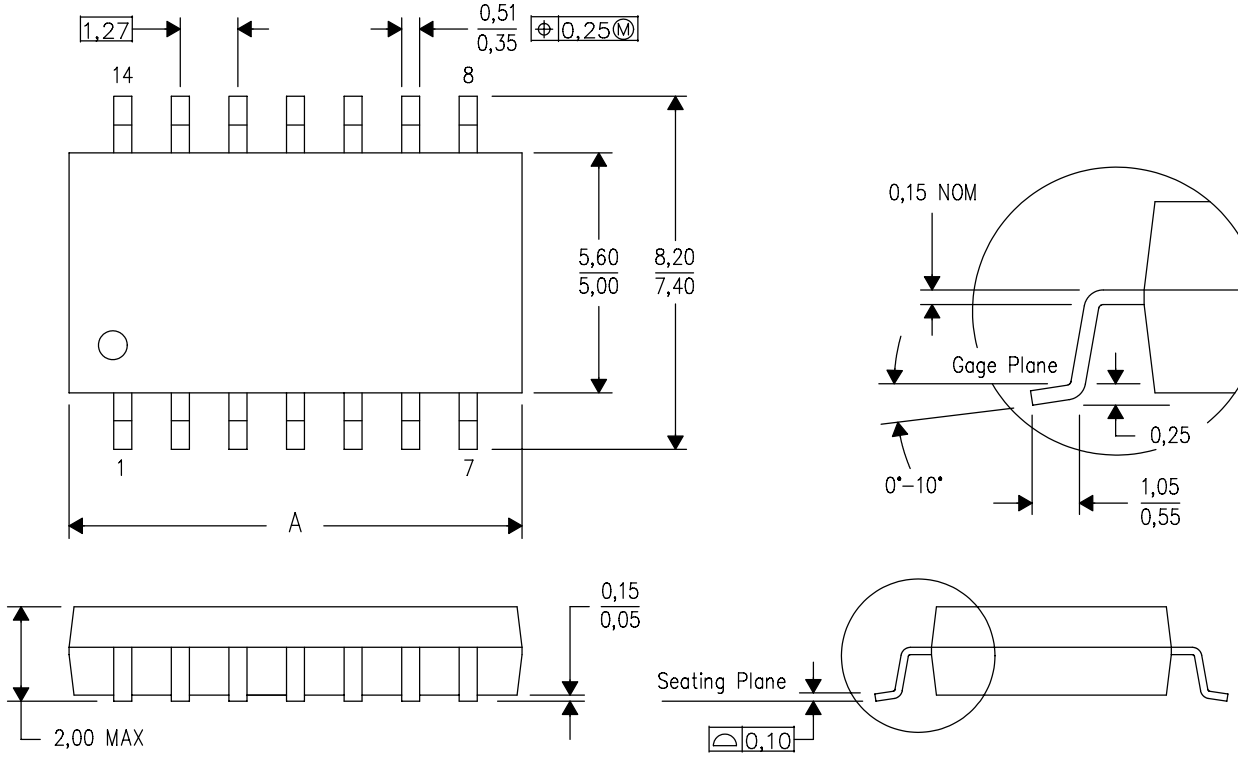


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

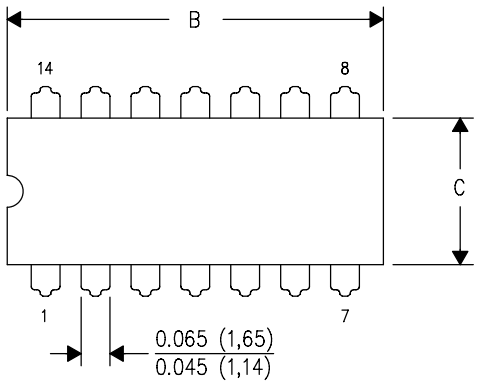
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

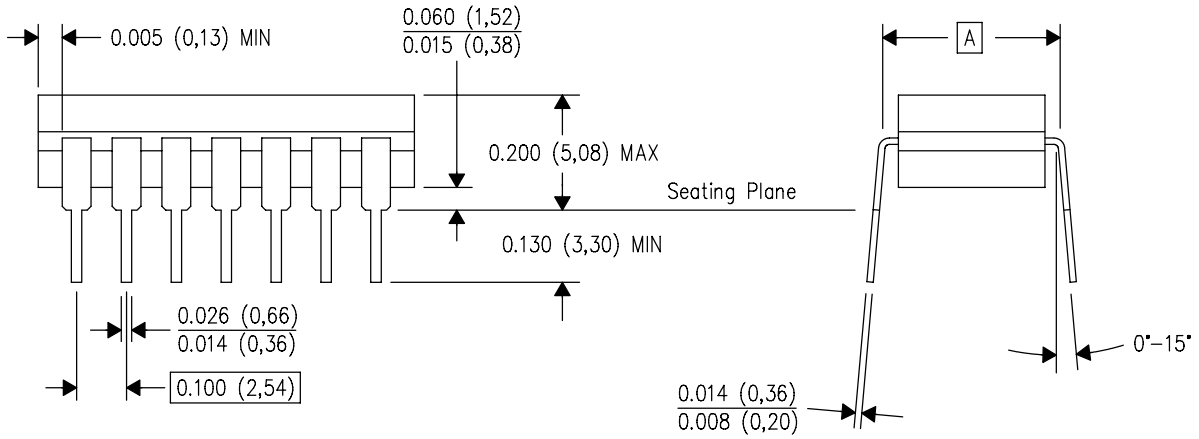
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE

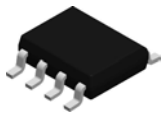


DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

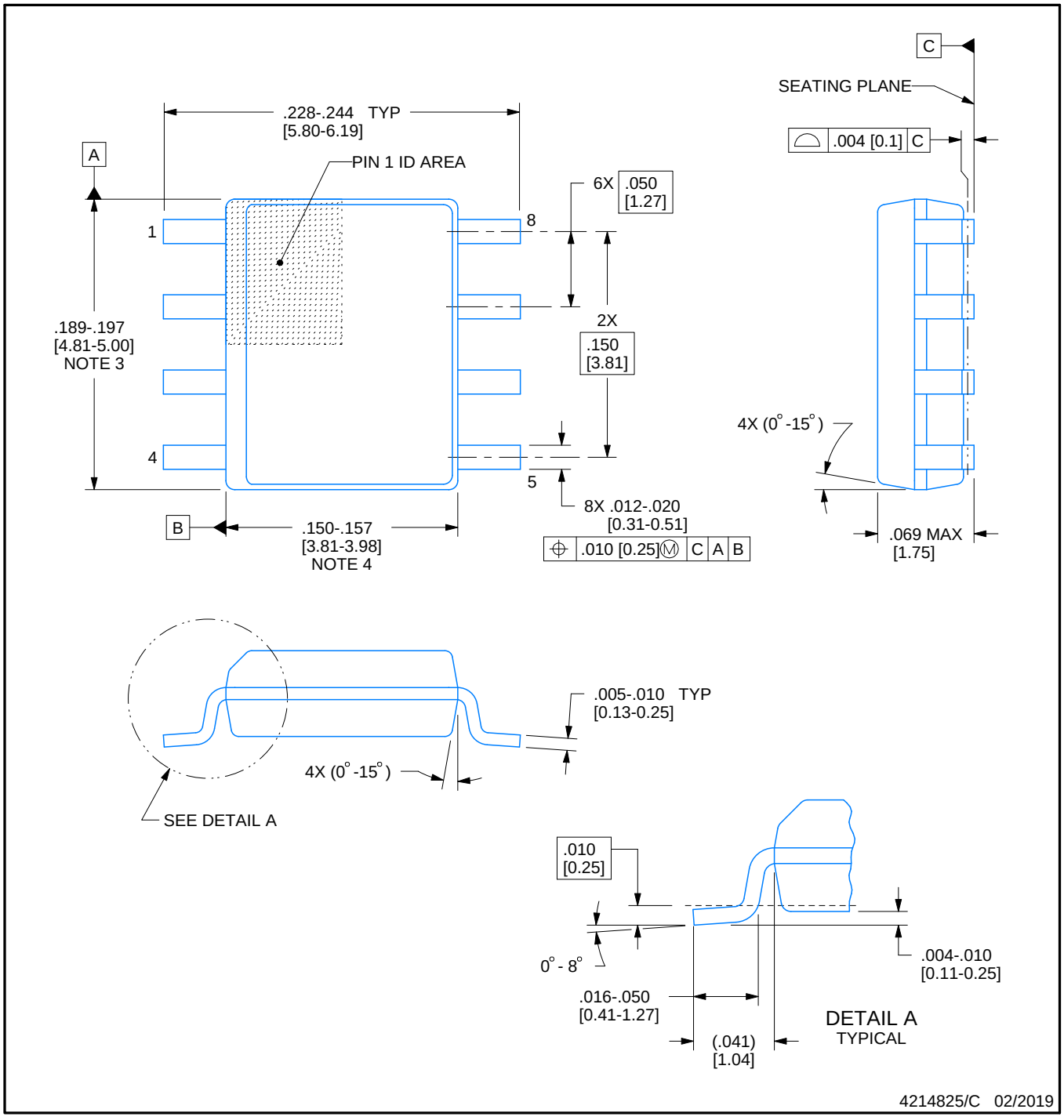


PACKAGE OUTLINE

D0008A

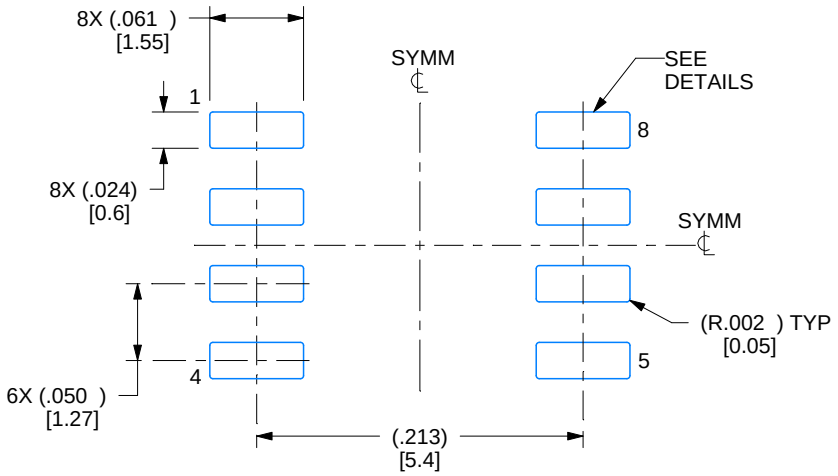
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

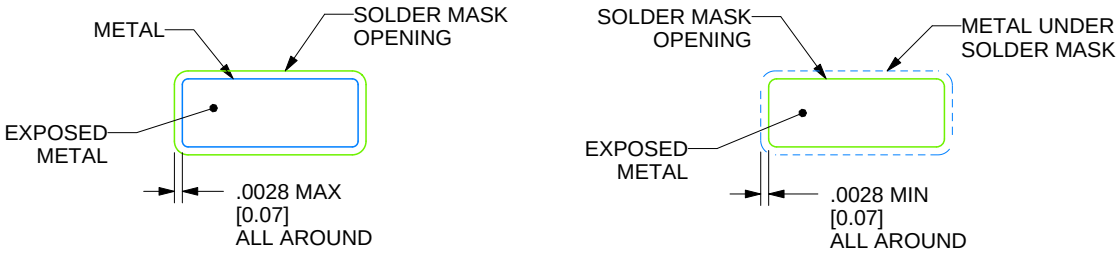


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

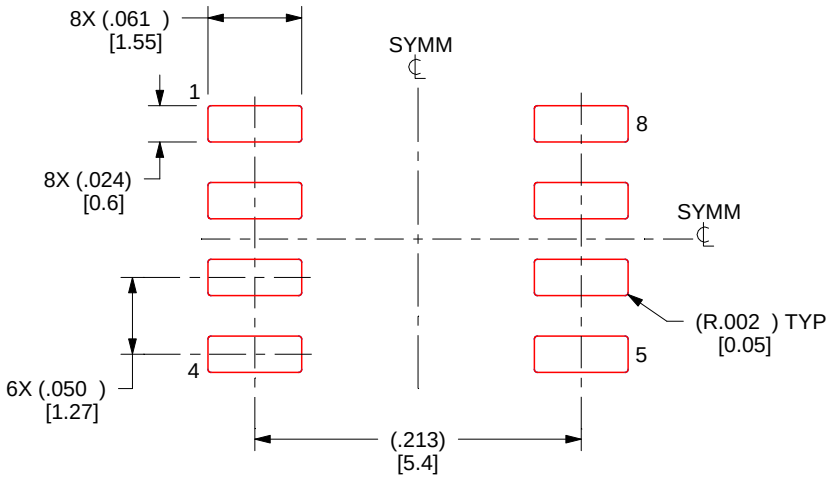
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



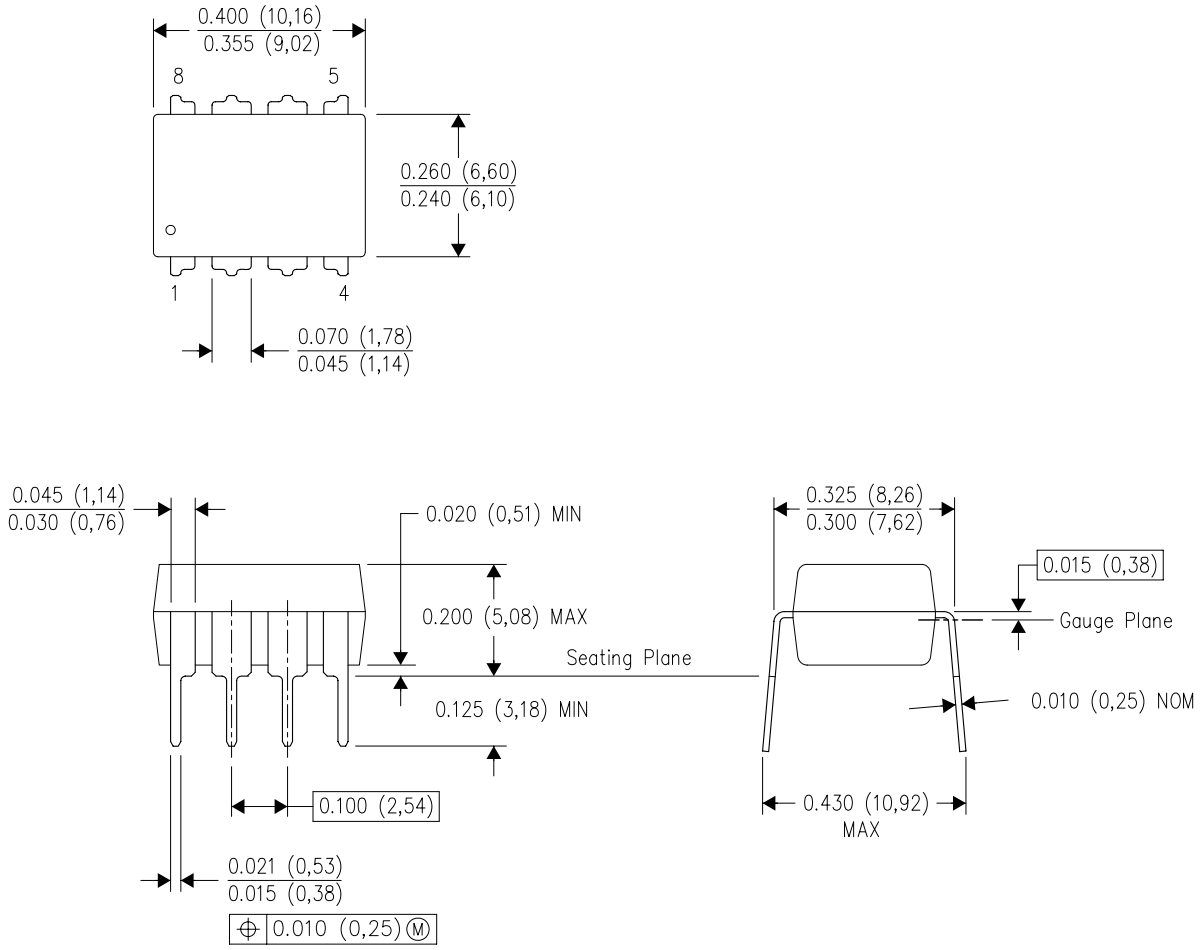
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

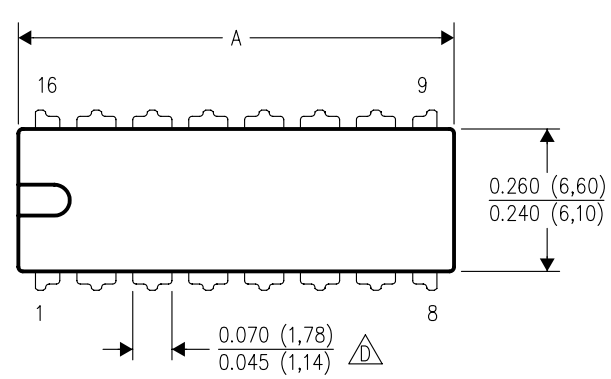


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

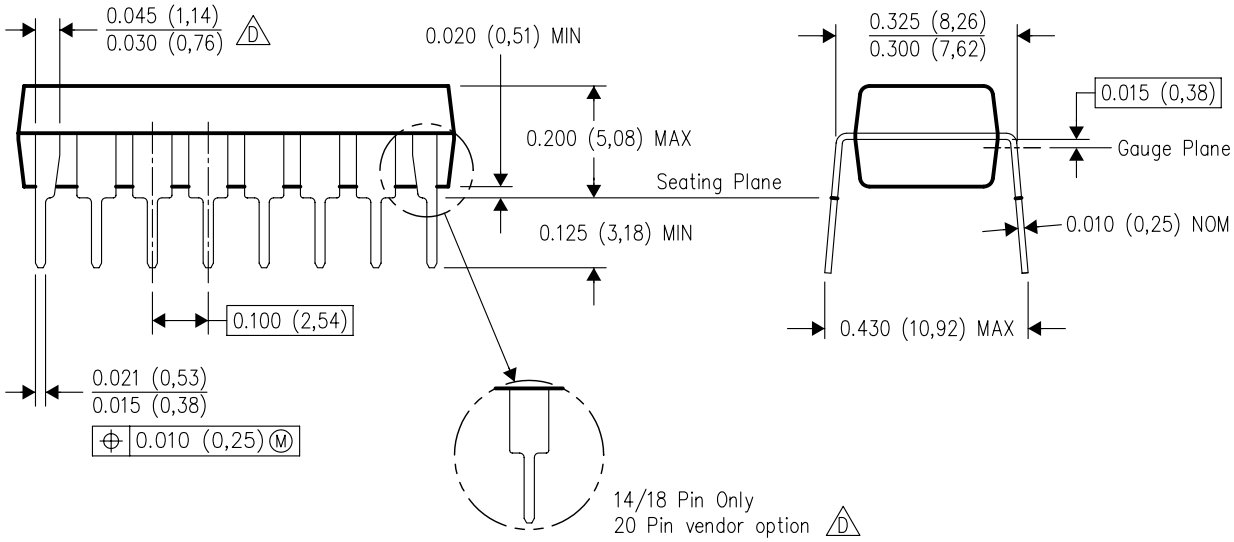
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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