



**THE DATASHEET OF
TDA7460NDTR**





TDA7460ND

Car radio signal processor

Not For New Design

Features

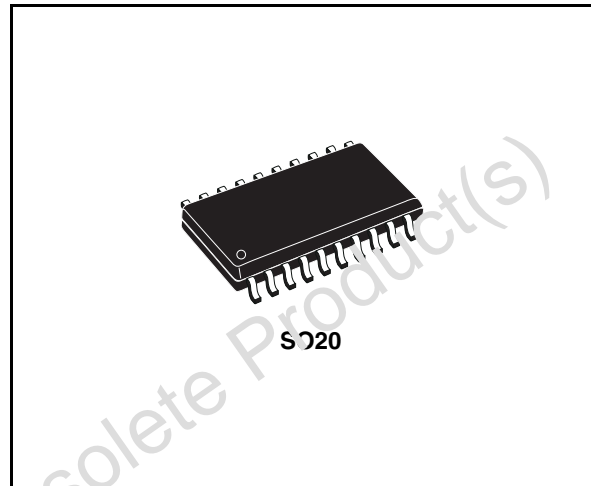
- Device includes audio processor, stereo decoder, noise blanker and multipath detector
- High performance signal processor
- No external components required
- Fully programmable via I²C bus
- Low distortion
- Low noise

Description

The TDA7460ND is a high performance signal processor specifically designed for car radio applications.

The device includes a complete audio processor and a stereo decoder with noise blanker, stereo blend and all signal processing functions necessary for state-of-the-art as well as future car radio systems.

Switched-capacitors design technique allows to obtain all these features without external components or adjustments.



This means that higher quality and reliability walks alongside an overall cost saving.

The CSP is fully programmable by I²C bus interface allowing to customize key device parameters and especially filter characteristics.

The BICMOS process combined with the optimized signal processing assure low noise and low distortion performances.

Table 1. Device summary

Order code	Package	Packing
TDA7460ND	SO20	Tube
TDA7460NDTR	SO20	Tape and reel

Contents

1	Block diagram	6
2	Pin description	7
3	Electrical specification	8
3.1	Absolute maximum ratings	8
3.2	Supply	8
3.3	ESD	8
3.4	Thermal data	8
3.5	Audio processor part features	8
3.5.1	Input multiplexer	8
3.5.2	Loudness	9
3.5.3	Volume control	9
3.5.4	Bass control	9
3.5.5	Treble control	9
3.5.6	Speaker control	9
3.5.7	Mute functions	9
3.6	Audio processor electrical characteristics	10
4	Description of the audio processor part	14
4.1	Programmable input matrix	14
4.1.1	How to find the right input configuration	15
4.1.2	Input stages	16
4.1.3	AutoZero	16
4.2	Mixing stage	16
4.2.1	Loudness	17
4.2.2	Soft mute	18
4.2.3	Soft step volume	18
4.2.4	Bass	19
4.2.5	DC mode	19
4.2.6	Treble	19
4.2.7	Speaker attenuator	19
5	Stereo decoder part	21

5.1	Stereo decoder feature	21
5.2	Stereo decoder electrical characteristics	21
5.3	Noise blanker part	24
5.4	Multipath detector	26
5.5	Description of stereo decoder	27
5.5.1	Stereo decoder mute	27
5.5.2	Input stages	28
5.5.3	Demodulator	28
5.5.4	De-emphasis and high cut	28
5.5.5	PLL and pilot tone detector	29
5.5.6	Fieldstrength control	29
5.5.7	Level input and gain	29
5.5.8	Stereo blend control	29
5.5.9	High cut control	30
5.6	Functional description of the noise blanker	30
5.6.1	Trigger path	31
5.6.2	Automatic noise controlled threshold adjustment (ATC)	31
5.6.3	Automatic threshold control	31
5.6.4	Over deviation detector	32
5.7	Functional description of the multipath detector	32
5.8	Test mode	32
6	I²C bus interface description	34
6.1	Interface protocol	34
6.2	Auto increment	35
7	Data byte specification	36
8	Package information	47
9	Revision history	48

List of tables

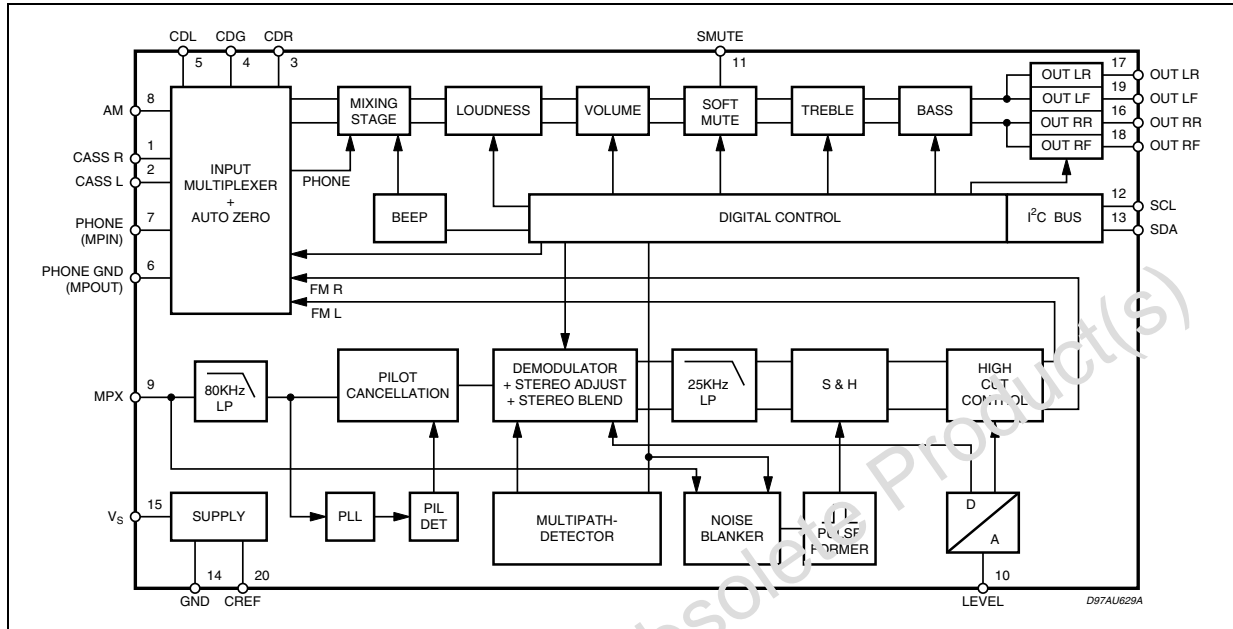
Table 1.	Device summary	1
Table 2.	Pin description	7
Table 3.	Absolute maximum ratings	8
Table 4.	Supply	8
Table 5.	Thermal data	8
Table 6.	Audio processor electrical characteristics	10
Table 7.	Input and source programming	15
Table 8.	Stereo decoder electrical characteristics	21
Table 9.	Noise blanker electrical characteristics	24
Table 10.	Multipath detector electrical characteristics	26
Table 11.	Transmitted data (send mode)	35
Table 12.	Subaddress (receive mode)	35
Table 13.	Input selector	36
Table 14.	Loudness	37
Table 15.	Mute, beep and mixing	38
Table 16.	Volume	39
Table 17.	Bass and treble attenuation	40
Table 18.	Bass and treble filter characteristics	41
Table 19.	Speaker attenuation (LF, LR, RF, RR)	42
Table 20.	Stereo decoder	43
Table 21.	Noise blanker	43
Table 22.	Field strength control	44
Table 23.	Configuration	44
Table 24.	Stereo decoder adjustment	45
Table 25.	Testing	46
Table 26.	Document revision history	48

List of figures

Figure 1.	Block diagram	6
Figure 2.	Pin connection (top view)	7
Figure 3.	Input configuration tree	14
Figure 4.	Input stages	16
Figure 5.	Loudness attenuation @ $f_c = 400$ Hz (second order)	17
Figure 6.	Loudness center frequency @ Attn. = 15 dB (second order)	17
Figure 7.	Loudness @ attn. = 15 dB, $f_c = 400$ Hz	17
Figure 8.	Soft mute timing	18
Figure 9.	Soft step timing	18
Figure 10.	Bass control @ $f_c = 80$ Hz, $Q = 1$	20
Figure 11.	Bass center @ Gain = 14 dB, $Q = 1$	20
Figure 12.	Bass quality factors @ gain = 14 dB, $f_c = 80$ Hz	20
Figure 13.	Bass normal and DC mode @ Gain = 14 dB, $f_c = 80$ Hz	20
Figure 14.	Treble control @ $f_c = 17.5$ KHz.	20
Figure 15.	Treble center freq. @ gain = 14 dB.	20
Figure 16.	Noise blanker diagram	25
Figure 17.	Trigger threshold vs. VPEAK	25
Figure 18.	Deviation controlled trigger adjustment	25
Figure 19.	Fieldstrength controlled trigger adjustment.	25
Figure 20.	Block diagram of the stereo decoder	26
Figure 21.	Block diagram of the stereo decoder	27
Figure 22.	Signals during stereo decoder's soft mute	28
Figure 23.	Internal stereo blend characteristics	29
Figure 24.	Relation between internal and external LEVEL voltage and setup of stereo blend	30
Figure 25.	High cut characteristics	30
Figure 26.	Block diagram of the noise blanker.	31
Figure 27.	Block diagram of the multipath detector	32
Figure 28.	Application example 1 (with phone input)	33
Figure 29.	Application example 2 (with multipath)	33
Figure 30.	Interface protocol diagram	34
Figure 31.	SO20 mechanical data and package dimensions.	47

1 Block diagram

Figure 1. Block diagram



2 Pin description

Figure 2. Pin connection (top view)

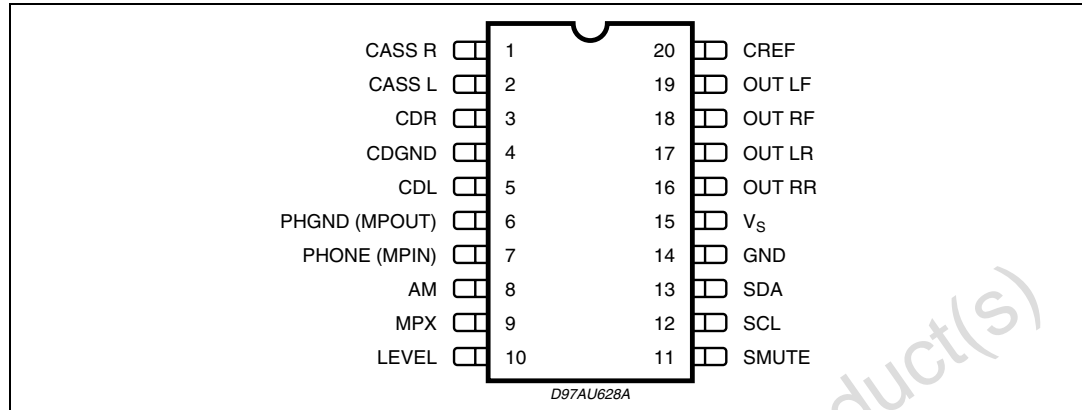


Table 2. Pin description

N.	Name	Function	Type
1	CASSR	Cassette input right	I
2	CASSL	Cassette input left	I
3	CDR	CD right channel input	I
4	CDGND	Ground reference CD	I
5	CDL	CD left channel input	I
6	PHGND	Phone ground (MPOUT selectable by SW ⁽¹⁾)	I
7	PHONE	Phone input (MPIN selectable by SW ⁽¹⁾)	I
8	AM	AM input	I
9	MPX	F.M input (MPX)	I
10	LEVEL	Level input stereo decoder	I
11	SMUTE	Soft mute drive	I
12	SCL	I ² C clock line	I/O
13	SDA	I ² C data line	I/O
14	GND	Supply ground	S
15	VS	Supply voltage	S
16	OUTRR	Right rear speaker output	O
17	OUTLR	Left rear speaker output	O
18	OUTRF	Right front speaker output	O
19	OUTLF	Left front speaker output	O
20	CREF	Reference capacitor pin	S

1. See [Figure 3: Input configuration tree](#) and [Section 7: Data byte specification](#)

Pin type legenda:

I = Input

O = Output

I/O = Input/Output

S = Supply

3 Electrical specification

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	10.5	V
T_{amb}	Operating ambient temperature range	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

3.2 Supply

Table 4. Supply

Symbol	Parameter	Test condition	Min	Typ.	Max.	Unit
V_S	Supply voltage		7.5	9	10	V
I_S	Supply current	$V_S = 9\text{ V}$	25	30	35	mA
SVRR	Ripple rejection @ 1 kHz	Audioprocessor (all filters flat)		60		dB
		Stereo decoder + Audioprocessor		45		dB

3.3 ESD

All pins are protected against ESD according to the MIL883 standard.

3.4 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{th-j\ pins}$	Thermal resistance junction to pins	max 85	°C/W

3.5 Audio processor part features

3.5.1 Input multiplexer

- Fully differential or quasi-differential CD and cassette stereo input
- AM mono or stereo input
- Phone differential or single ended input
- Internal beep with 2 frequencies (selectable)
- Mixable phone and beep signals

3.5.2 Loudness

- First or second order frequency response
- Programmable center frequency and quality factor
- 15 x 1 dB steps
- Selectable flat-mode (constant attenuation)

3.5.3 Volume control

- 1 dB attenuator
- Max. gain 20 dB
- Max. attenuation 79 dB
- Soft-step gain control

3.5.4 Bass control

- 2nd order frequency response
- Center frequency programmable in 4(5) steps
- DC gain programmable
- 7 x 2 dB steps

3.5.5 Treble control

- 2nd order frequency response
- Center frequency programmable in 4 steps
- 7 x 2 dB steps

3.5.6 Speaker control

- 4 independent speaker controls (1 dB steps control range 50 dB)

3.5.7 Mute functions

- Direct mute
- Digitally controlled soft mute with 4 programmable time constants

3.6 Audio processor electrical characteristics

Table 6. Audio processor electrical characteristics
($V_S = 9\text{ V}$; $T_{\text{amb}} = 25\text{ °C}$; $R_L = 10\text{ k}\Omega$; all gains = 0 dB; $f = 1\text{ KHz}$; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input selector						
R_{in}	Input resistance	All inputs except phone	70	100	130	$\text{k}\Omega$
V_{CL}	Clipping level		2.2	2.6		V_{RMS}
S_{IN}	Input separation		80	100		dB
$G_{\text{IN MIN}}$	Min. input gain		-1	0	1	dB
$G_{\text{IN MAX}}$	Max. input gain		13	14	15	dB
G_{STEP}	Step resolution		1	2	3	dB
V_{DC}	DC steps	Adjacent gain step	-5	0	+5	mV
		G_{MIN} to G_{MAX}	-5	1	+5	mV
Differential cd stereo input						
R_{in}	Input resistance	Differential	70	100	130	$\text{k}\Omega$
		Common mode	20	30	40	$\text{k}\Omega$
CMRR	Common mode rejection ratio	$V_{\text{CM}} = 1\text{ V}_{\text{RMS}}$ @ 1 kHz	45	70		dB
		$V_{\text{CM}} = 1\text{ V}_{\text{RMS}}$ @ 10 kHz	45	60		dB
e_{N}	Output noise @ speaker output	20 Hz to 20 KHz flat; all stages 0 dB		9	15	mV
Differential phone input						
R_{in}	Input resistance	Differential	10	15	20	$\text{k}\Omega$
		Common mode	20	30	40	$\text{k}\Omega$
CMRR	Common mode rejection ratio	$V_{\text{CM}} = 1\text{ V}_{\text{RMS}}$ @ 1 kHz	45	70		dB
		$V_{\text{CM}} = 1\text{ V}_{\text{RMS}}$ @ 10 kHz	45	60		dB
Beep control						
V_{BMS}	Beep level		250	350	500	mV
f_{BMIN}	Lower beep frequency		570	600	630	Hz
f_{BMAX}	Higher beep frequency		1.15	1.2	1.25	kHz
Mixing control						
M_{LEVEL}	Mixing level	Source	-1	0	1	dB
		Source	-5	-6	-7	dB
		Source	-10	-12	-14	dB
		Beep/Phone	-1	0	1	dB
Volume control						
G_{MAX}	Max gain		19	20	21	dB

Table 6. Audio processor electrical characteristics (continued) $(V_S = 9\text{ V}; T_{\text{amb}} = 25\text{ }^\circ\text{C}; R_L = 10\text{ k}\Omega; \text{all gains} = 0\text{ dB}; f = 1\text{ KHz}; \text{unless otherwise specified})$

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A_{MAX}	Max attenuation		-83	-79	-75	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
E_A	Attenuation set error	$G = -20\text{ to }20\text{ dB}$	-1.25	0	1.25	dB
		$G = -60\text{ to }20\text{ dB}$	-4	0	3	dB
E_T	Tracking error				2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-3	0.1	3	mV
		From 0 dB to GMIN	-7	0.5	+7	mV
Loudness control						
A_{STEP}	Step resolution		0.5	1	1.5	dB
A_{MAX}	Max. attenuation		-16	-15	-14	dB
f_{CMIN}	Lower center frequency		180	200	220	Hz
f_{CMAX}	Higher center frequency		360	400	440	Hz
Soft mute						
A_{MUTE}	Mute attenuation		60	100		dB
T_D	Delay time	T1		0.48	1	ms
		T2		0.96	2	ms
		T3	20	40.4	60	ms
		T4	200	324	600	ms
V_{THlow}	Low threshold for SM pin ⁽¹⁾				1	V
V_{THhigh}	High threshold for SM pin		2.5			V
R_{PU}	Internal pull-up resistor		70	100	130	k Ω
V_{PU}	Pull-up voltage			4.7		V
Soft step						
t_{CW}	Switch time		5	10	15	ms
Bass control						
C_{RANGE}	Control range		± 13	± 14	± 15	dB
A_{STEP}	Step resolution		1	2	3	dB
f_C	Center frequency	f_{C1}	54	60	66	Hz
		f_{C2}	63	70	77	Hz
		f_{C3}	72	80	88	Hz
		f_{C4}	90	100 ⁽²⁾	110	Hz

Table 6. Audio processor electrical characteristics (continued) $(V_S = 9\text{ V}; T_{\text{amb}} = 25\text{ }^\circ\text{C}; R_L = 10\text{ k}\Omega; \text{all gains} = 0\text{ dB}; f = 1\text{ KHz}; \text{unless otherwise specified})$

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Q_{BASS}	Quality factor	Q_1	0.9	1	1.1	
		Q_2	1.1	1.25	1.4	
		Q_3	1.3	1.5	1.7	
		Q_4	1.8	2	2.2	
DC_{GAIN}	Bass-Dc-gain	DC = off	-1	0	+1	dB
		DC = on	4	4.4	6	dB
Treble control						
C_{RANGE}	Control range		± 13	± 14	± 15	dB
A_{STEP}	Step resolution		1	2	3	dB
f_C	Center frequency	f_{C1}	8	10	12	kHz
		f_{C2}	10	12.5	15	kHz
		f_{C3}	12	15	18	kHz
		f_{C4}	14	17.5	21	kHz
Speaker attenuators						
C_{RANGE}	Control range		-53	-50	-47	dB
A_{STEP}	Step resolution		0.5	1	2	dB
A_{MUTE}	Output mute attenuation		80	90		dB
E_E	Attenuation set error		-2		2	dB
V_{DC}	DC steps	Adjacent attenuation steps		0.1	5	mV
Audio outputs						
V_{CLIP}	Clipping level	$d = 0.3\%$	2.2	2.6		V_{RMS}
R_L	Output load resistance		2			$k\Omega$
C_L	Output load capacitance				10	nF
R_{OUT}	Output impedance			30	100	Ω
V_{DC}	DC voltage level		3.6	3.8	4.0	V

Table 6. Audio processor electrical characteristics (continued) $(V_S = 9\text{ V}; T_{\text{amb}} = 25\text{ }^\circ\text{C}; R_L = 10\text{ k}\Omega; \text{all gains} = 0\text{ dB}; f = 1\text{ kHz}; \text{unless otherwise specified})$

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General						
e_{NO}	Output noise	BW = 20 Hz to 20 kHz output muted		3	15	μV
		BW = 20 Hz to 20 kHz all gain = 0 dB		6.5	15	μV
S/N	Signal to noise ratio	all gain = 0 dB flat; $V_O = 2V_{\text{RMS}}$		106		dB
		bass treble at 12 dB; $V_O = 2.6 V_{\text{RMS}}$		100		dB
d	Distortion	$V_{\text{IN}} = 1V_{\text{RMS}}$; all stages 0dB		0.002	0.1	%
		$V_{\text{IN}} = 1V_{\text{RMS}}$; bass & treble = 12 dB		0.05	0.1	%
S_C	Channel separation left/right		80	100		dB
E_T	Total tracking error	$A_V = 0$ to -20 dB	-1	0	1	dB
		$A_V = -20$ to -60 dB	-2	0	2	dB

1. The SM pin is active low (mute = 0)
2. See [Section 3.5.4: Bass control](#) and [Section 3.5.5: Treble control](#).

4 Description of the audio processor part

4.1 Programmable input matrix

The programmable input matrix of the TDA7460ND offers several possibilities to adapt the audioprocessor to the desired application. In to the standard application we have:

CD quasi differential

- Cassette stereo
- Phone differential
- AM mono
- Stereo decoder input.

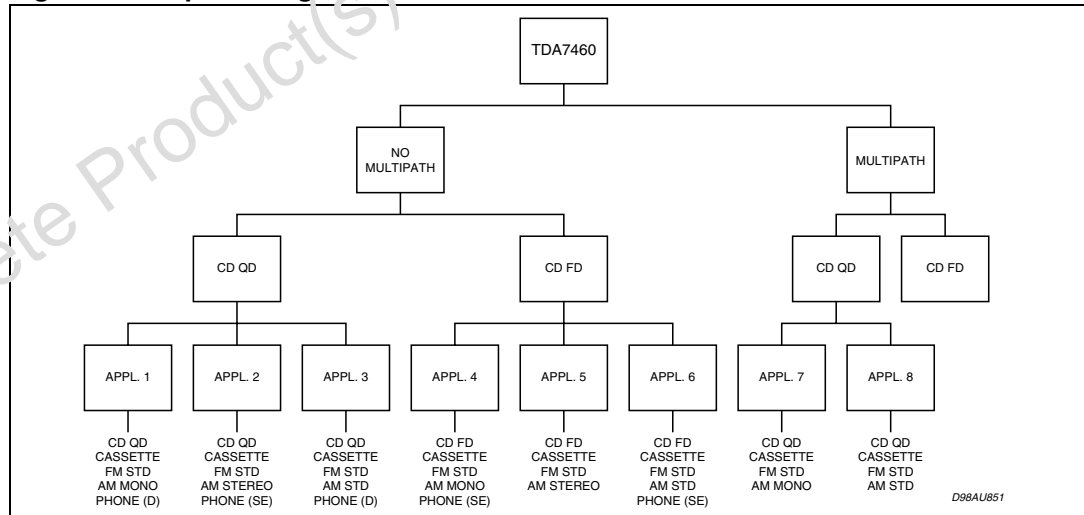
The input matrix can be configured by only 2 bits: bits 3 and 4 of subaddress 0. Basically the bit of subaddress 13 is fixed by the application and has to be programmed only once at the startup of the IC.

For many configurations the two bits are also fixed during one application (e.g. the standard application) and a change of the input source can be done by loading the first three bits of subaddress 0.

In other configurations for some sources a programming of bit 3 and 4 of subaddress 0 is necessary in addition to the three source selection bits. In every case only the subaddress 0 has to be changed to switch from one source to another.

The following picture shows the input and source programming flow:

Figure 3. Input configuration tree



1. Note: in AMSTD configuration the AM mono signal is lead through the FM stereo decoder part to use its additional filters and high-cut function.

Table 7. Input and source programming

Appl. no	Pin number				Programming ⁽¹⁾	
	4	6	7	8		
1	CD _{GND}	Phone _{GND}	Phone	AMMONO	Startup:	0/xxx11xxx
2	CD _{GND}	Phone	AMRIGHT	AMLEFT	Startup:	0/xxxx1xxx
					FM AM Phone	0/xxx11100 0/xxx01011 0/xxx11010
3	CD _{GND}	Phone _{GND}	Phone	AMSTD	Startup:	0/xxxx1xxx
					FM AM Phone	0/xxx11100 0/xxx01100 0/xxx11010
4	CD _R _{GND}	CD _L _{GND}	Phone	AMMONO	Startup:	0/xxxx0xxx
5	CD _R _{GND}	CD _L _{GND}	AMRIGHT	AMLEFT	Startup:	0/xxxx0xxx
					FM AM	0/xxx10100 0/xxx00011
6	CD _R _{GND}	CD _L _{GND}	Phone	AMSTD	Startup:	0/xxxx0xxx
					FM AM Phone	0/xxx10100 0/xxx00100 0/xxx10010
7	CD _{GND}	MPCUT	MPIN	AMMONO	Startup:	0/xxx11xxx
8	CD _{GND}	MPCUT	MPIN	AMSTD	Startup:	0/xxx1xxx
					FM AM	0/xxx11100 0/xxx01100

1. Syntax 0/xxx11100 means: SUBADDRESS = 0 - DATA BYTE = xxx11100 (x - don't care)

4.1.1 How to find the right input configuration

The best way to come to the desired configuration may be to go through the application tree from the top to the bottom while making the specific decisions.

This way will lead to one of the six possible applications. Then take the number of the application and go into the pinning table. Here you will find the special pinout as well as the special programming codes for selecting sources.

For example in Appl. 6 the TDA7460ND has to be configured while startup with the databyte 0/xxxx0xxx.

To select the FM, AM or phone source the last five significant bits of subaddress 0 have to be changed, for any other source the last three bits are sufficient (see [Section 7: Data byte specification on page 36](#)).

4.1.2 Input stages

Most of the input circuits are the same as in preceding ST audioprocessors with exception of the CD inputs (see [Figure 4](#)). In the meantime there are some CD players in the market having a significant high source impedance which affects strongly the common-mode rejection of the normal differential input stage. The additional buffer of the CD input avoids this drawback and offers the full common-mode rejection even with those CD players.

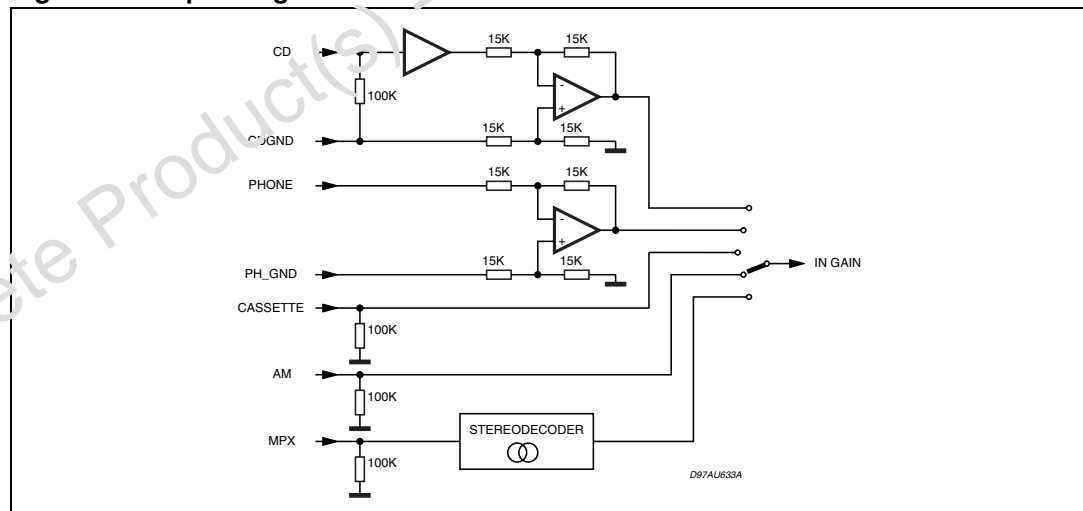
The TDA7460ND can be configured with an additional input; if the AC coupling before the speaker stage is not used (bit 7 in subaddress 5 set to "1") ACINL and ACINR pins can be used as an additional stereo input.

4.1.3 AutoZero

In order to reduce the number of pins there is no AC coupling between the In-Gain and the following stage, so that any offset generated by or before the In-Gain stage would be transferred or even amplified to the output.

To avoid that effect a special offset cancellation stage called AutoZero is implemented. To avoid audible clicks the audioprocessor is muted before the loudness stage during this time. In some cases, for example if the μP is executing a refresh cycle of the I²C bus programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications the TDA7460ND could be switched in the "Auto Zero Remain" mode (Bit 6 of the subaddress byte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment value remains.

Figure 4. Input stages



4.2 Mixing stage

This stage offers the possibility to mix the internal beep or the phone signal to any other source. Due to the fact that the mixing stage is also located behind the In-Gain stage fine adjustments of the main source level can be done in this way.

4.2.1 Loudness

There are four parameters programmable in the loudness stage (see *Figure 5.*, *Figure 6.* and *Figure 7.*):

- Attenuation
- Center Frequency
- Loudness Q

Flat Mode: in this mode the loudness stage works as a 0 - 15 dB attenuator.

Figure 5. Loudness attenuation @ $f_c = 400$ Hz (second order)

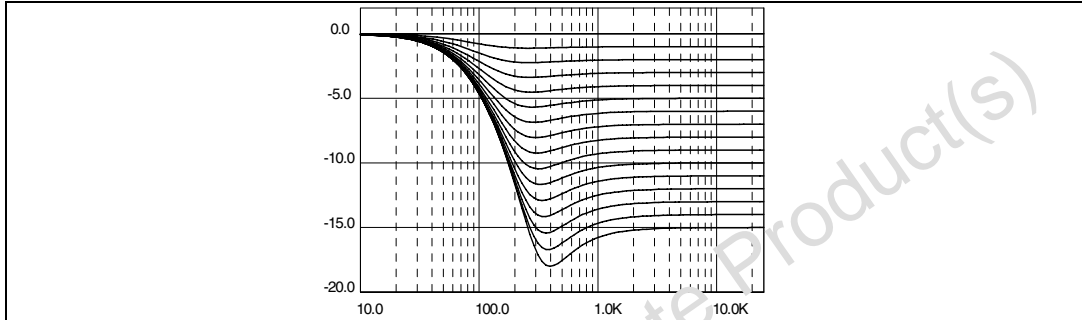


Figure 6. Loudness center frequency @ Attn. = 15 dB (second order)

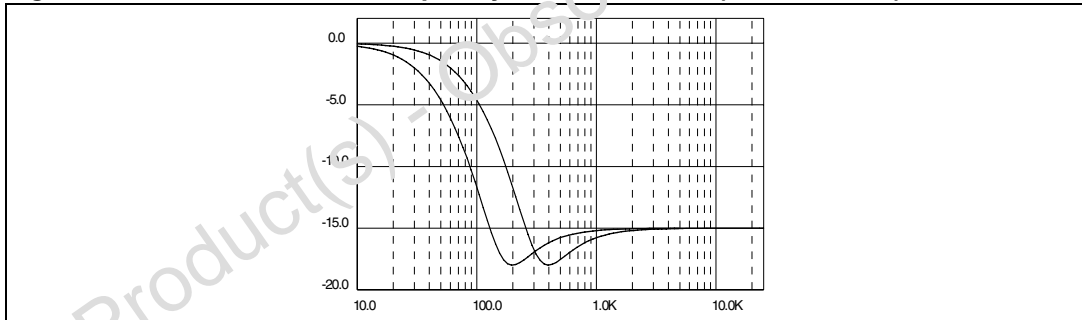
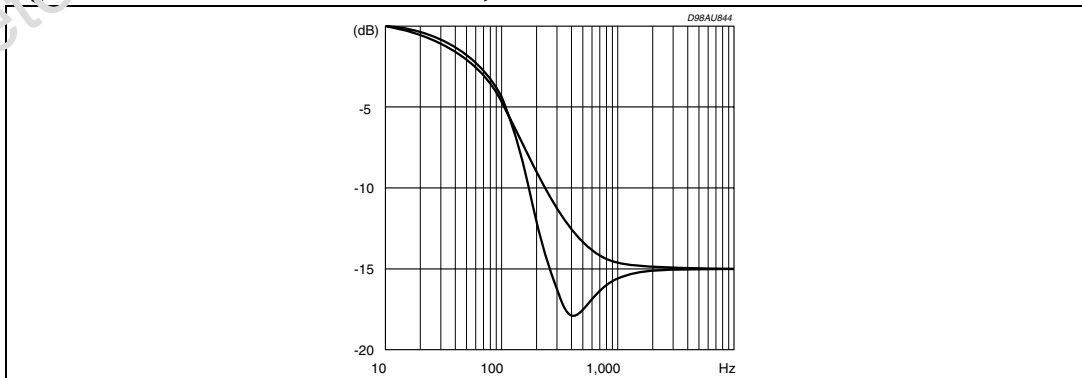


Figure 7. Loudness @ attn. = 15 dB, $f_c = 400$ Hz

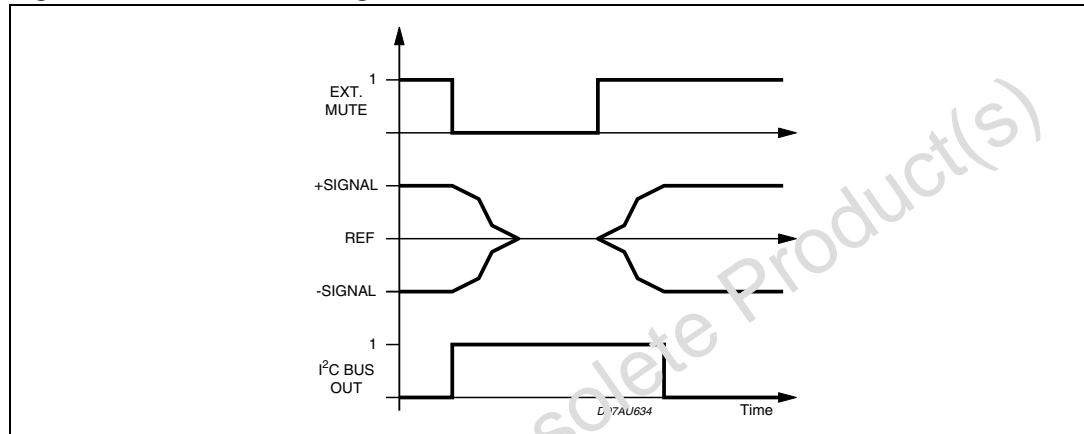


4.2.2 Soft mute

The digitally controlled soft mute stage allows muting/demuting the signal with a I²C bus programmable slope. The mute process can either be activated by the soft mute pin or by the I²C bus. The slope is realized in a special S shaped curve to mute slow in the critical regions (see [Figure 8](#)).

For timing purposes the Bit 3 of the I²C bus output register is set to 1 from the start of muting until the end of demuting.

Figure 8. Soft mute timing

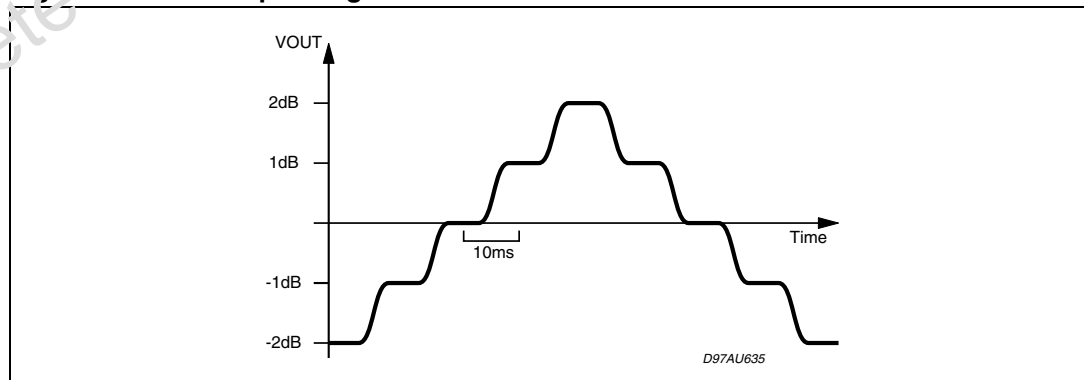


1. Please notice that a started Mute action is always terminated and could not be interrupted by a change of the mute signal.

4.2.3 Soft step volume

When volume level is changed often an audible click appears at the output. The root cause of those clicks could be either a DC offset before the volume stage or the sudden change of the envelope of the audio signal. With the Soft step feature both kinds of clicks could be reduced to a minimum and are no more audible (see [Figure 9](#)).

Figure 9. Soft step timing



2. For steps more than 1 dB the soft step mode should be deactivated because it could generate a 1 dB error during the blend-time

4.2.4 Bass

There are three parameters programmable in the bass stage (see [Figure 10.](#), [Figure 11.](#), [Figure 12.](#), [Figure 13.](#)):

- Attenuation
- Center Frequency (60, 70, 80 and 100 Hz)
- Quality Factors (1, 1.25, 1.5 and 2)

4.2.5 DC mode

In this mode the DC gain is increased by 4.4 dB. In addition the programmed center frequency and quality factor is decreased by 25% which can be used to reach alternative center frequencies or quality factors.

4.2.6 Treble

There are two parameters programmable in the treble stage (see [Figure 14.](#) and [Figure 15.](#)):

- Attenuation
- Center Frequency (10, 12.5, 15 and 17.5 kHz).

4.2.7 Speaker attenuator

Due to practical aspects the steps in the speaker attenuators are not linear over the full range. At attenuations more than 24 dB the steps increase from 1.5 dB to 10 dB (please see [Section 7: Data byte specification on page 36](#)).

Figure 10. Bass control @ $f_c = 80\text{ Hz}$, $Q = 1$

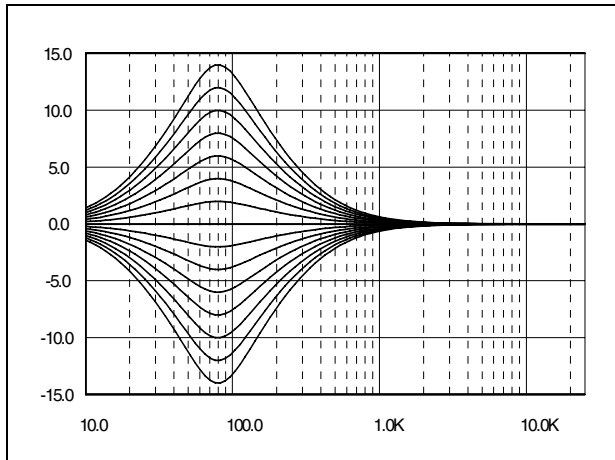


Figure 11. Bass center @ Gain = 14 dB, $Q = 1$

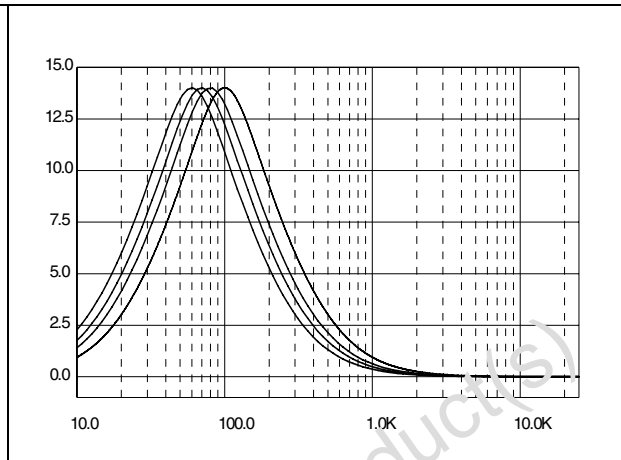


Figure 12. Bass quality factors @ gain = 14 dB, $f_c = 80\text{ Hz}$

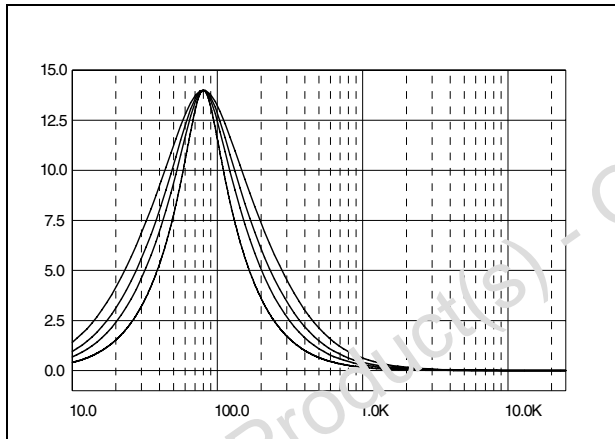


Figure 13. Bass normal and DC mode @ Gain = 14 dB, $f_c = 80\text{ Hz}$ ⁽¹⁾

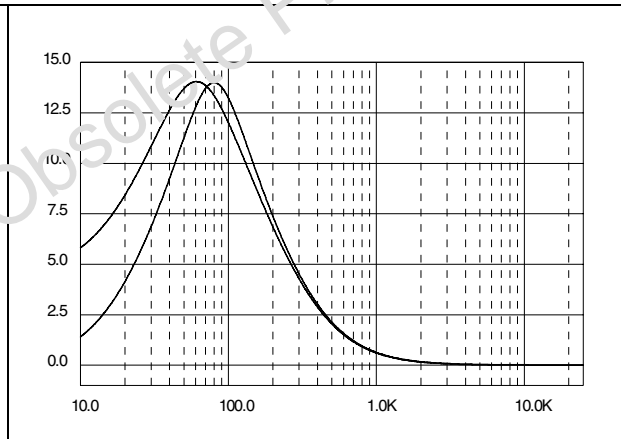


Figure 14. Treble control @ $f_c = 17.5\text{ KHz}$

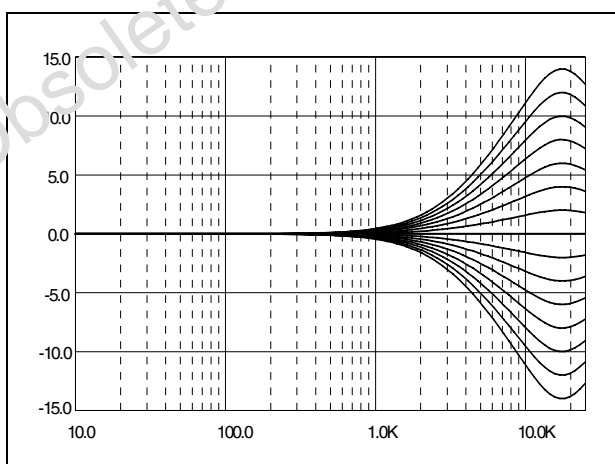
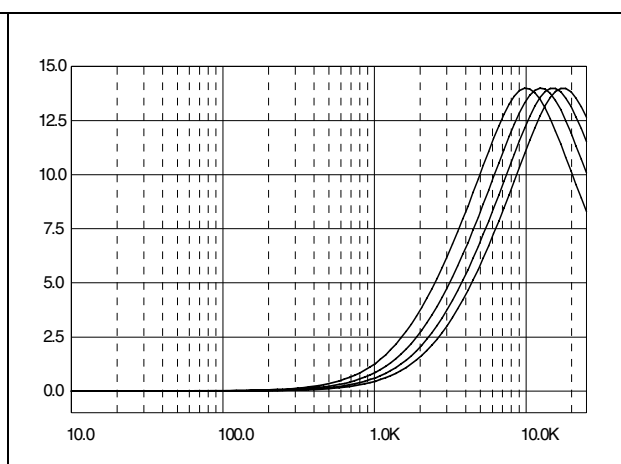


Figure 15. Treble center freq. @ gain = 14 dB



1. In general the center frequency, Q and DC-mode can be set independently. The exception from this rule is the mode (5/xx111xx) where the center frequency is set to 150 Hz instead of 100 Hz.

5 Stereo decoder part

5.1 Stereo decoder feature

- No external components necessary
- PLL with adjustment free fully integrated VCO
- Automatic pilot dependent mono/stereo switching
- Very high suppression of intermodulation and interference
- Programmable Roll-Off compensation
- Dedicated RDS soft mute
- High cut and stereo blend characteristics programmable in a wide range
- Internal noise blanker with threshold controls
- Multipath detector with programmable internal/external influence
- I²C bus control of all necessary functions

5.2 Stereo decoder electrical characteristics

Table 8. Stereo decoder electrical characteristics

(V_S = 9 V; de-emphasis time constant = 50 μs, V_{MPX} = 500 mV, 75 kHz deviation, f = 1 kHz. G_I = 6 dB, T_{amb} = 25 °C; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V _{IN}	MPX input level	Input gain = 3.5 dB		0.5	1.25	V _{RMS}
R _{in}	Input resistance		70	100	130	kΩ
G _{min}	Minimum input gain		1.5	3.5	4.5	dB
G _{max}	Max input gain		8.5	11	12.5	dB
G _{STEP}	Step resolution		1.75	2.5	3.25	dB
SVRR	Supply voltage ripple rejection	V _{ripple} = 100 mV, f = 1 kHz		55		dB
a	Max channel separation		30	50		dB
THD	Total harmonic distortion			0.02	0.3	%
$\frac{S + N}{N}$	Signal plus noise to noise ratio	S = 2 Vrms	80	91		dB
Mono/stereo switch						
V _{PTHST1}	Pilot threshold voltage	for stereo, PTH = 1	10	15	25	mV
V _{PTHST0}	Pilot threshold voltage	for stereo, PTH = 0	15	25	35	mV
V _{PTHMO1}	Pilot threshold voltage	for mono, PTH = 1	7	12	17	mV
V _{PTHMO0}	Pilot threshold voltage	for stereo, PTH = 0	10	19	25	mV
PLL						
Δf/f	Capture range		0.5			%

Table 8. Stereo decoder electrical characteristics (continued)
 ($V_S = 9\text{ V}$; de-emphasis time constant = $50\ \mu\text{s}$, $V_{MPX} = 500\text{ mV}$, 75 kHz deviation,
 $f = 1\text{ kHz}$. $G_I = 6\text{ dB}$, $T_{amb} = 25\text{ }^\circ\text{C}$; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
De-emphasis and high cut⁽¹⁾						
τ_{HC50}	De-emphasis time constant	Bit = 7, Subadr. 10 = 0VLEVEL >> VHCH	25	50	75	ms
τ_{HC75}	De-emphasis time constant	Bit = 7, Subadr. 10 = 1VLEVEL >> VHCH	50	75	100	ms
τ_{HC50}	High cut time constant	Bit = 7, Subadr. 10 = 0VLEVEL >> VHCL	100	150	200	ms
τ_{HC75}	High cut time constant	Bit = 7, Subadr. 10 = 1VLEVEL >> VHCL	150	225	300	ms
Stereo blend and high cut-control						
REF5V	Internal reference voltage		4.7	5	5.3	V
TC _{REF5V}	Temperature coefficient			3300		ppm
LG _{min}	Min. level gain		-1	0	+1	dB
LG _{max}	Max. level gain		8	10	12	dB
LG _{step}	Level gain step resolution		0.3	0.67	1.0	dB
VSBL _{min}	Min. voltage for mono		29	33	37	%REF 5V
VSBL _{max}	Max. voltage for mono		54	58	62	%REF 5V
VSBL _{step}	Step resolution		5.0	8.4	12	%REF 5V
Stereo blend and high cut control						
VHCH _{min}	Min. voltage for no high cut		36	42	46	%REF 5V
VHCH _{max}	Max. voltage for no high cut		62	66	70	%REF 5V
VHCH _{step}	Step resolution		5	8.4	12	%REF 5V
VHCL _{min}	Min. voltage for full high cut		13	17	21	%VHC H
VHCL _{max}	Max. voltage for full high cut		29	33	37	%VHC H
Carrier and harmonic suppression at the output						
α_{19}	Pilot signal	$f = 19\text{ kHz}$	40	50		dB
α_{38}	Sub carrier	$f = 38\text{ kHz}$		75		dB
α_{57}	Sub carrier	$f = 5\text{ kHz}$		62		dB
α_{76}	Subcarrier	$f = 76\text{ kHz}$		90		dB

Table 8. Stereo decoder electrical characteristics (continued)
 ($V_S = 9\text{ V}$; de-emphasis time constant = $50\ \mu\text{s}$, $V_{MPX} = 500\text{ mV}$, 75 kHz deviation,
 $f = 1\text{ kHz}$. $G_I = 6\text{ dB}$, $T_{amb} = 25\text{ }^\circ\text{C}$; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Intermodulation⁽²⁾						
$\alpha 2$	Pilot signal	$f_{mod} = 10\text{ kHz}$; $f_{spur} = 1\text{ kHz}$;		65		dB
$\alpha 3$		$f_{mod} = 13\text{ kHz}$; $f_{spur} = 1\text{ kHz}$;		75		dB
Traffic radio⁽³⁾						
$\alpha 57$	Signal	$f = 57\text{ kHz}$		70		dB
SCA - Subsidiary communications authorization⁽⁴⁾						
$\alpha 67$	Signal	$f = 67\text{ kHz}$		75		dB
ACI - Adjacent channel interference⁽⁵⁾						
$\alpha 114$	Signal	$f = 114\text{ kHz}$		95		dB
$\alpha 190$	Signal	$f = 190\text{ kHz}$		84		dB

1. By design/characterization but functionally guaranteed through dedicated test mode structure.
2. Intermodulation suppression: measured with: 91% pilot signal; $f_m = 10\text{ kHz}$ or 13 kHz .
3. Traffic radio (V.F.) suppression: measured with: 91% stereo signal; 9% pilot signal; $f_m = 1\text{ kHz}$; 5% sub carrier ($f = 57\text{ kHz}$, $f_m = 23\text{ Hz AM}$, $m = 60\%$).
4. SCA (subsidiary communications authorization) measured with: 80% mono signal; 9% pilot signal; $f_m = 1\text{ kHz}$; 10%SCA - sub carrier ($f_s = 67\text{ kHz}$, unmodulated).
5. ACI (Adjacent channel interference) measured with: 90% mono signal; 9% pilot signal; $f_m = 1\text{ kHz}$; 1% spurious signal ($f_s = 110\text{ kHz}$ or 186 kHz , unmodulated).

5.3 Noise blanker part

- Internal 2nd order 140 kHz high pass filter
- Programmable trigger threshold
- Additional circuits for trigger adjustment (deviation, field-strenght)
- Very low offset current during hold time
- Four selectable pulse suppression times

Table 9. Noise blanker electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	
V _{TR}	Trigger threshold (1), (2)	meas. with V _{PEAK} = 0.9 V	NBT = 111		30		mV _{OP}
			NBT = 110		35		mV _{OP}
			NBT = 101		40		mV _{OP}
			NBT = 100		45		mV _{OP}
			NBT = 011		50		mV _{OP}
			NBT = 010		55		mV _{OP}
			NBT = 001		60		mV _{OP}
V _{TRNOISE}	Noise controlled trigger threshold (3)	meas. with V _{PEAK} = 1.5 V	NCT = 00		260		mV _{OP}
			NCT = 01		220		mV _{OP}
			NCT = 10		180		mV _{OP}
			NCT = 11		140		mV _{OP}
V _{RECT}	Rectifier voltage	V _{MPX} = 0 mV	0.5	0.9	1.3	V	
		V _{MPX} = 50 mV; f = 150 kHz	1.5	1.7	2.1	V	
		V _{MPX} = 100 mV; f = 150 kHz	2.2	2.5	2.9	V	
V _{RECT DEV}	Deviation dependent rectifier voltage (4)	means. with V _{MPX} = 800 mV (75 KHz dev.)	OVD = 11	0.5	0.9(off)	1.3	V _{OP}
			OVD = 10	0.9	1.2	1.5	V _{OP}
			OVD = 01	1.7	2.0	2.3	V _{OP}
			OVD = 00	2.5	2.8	3.1	V _{OP}
V _{RECT FS}	Fieldstrength controlled rectifier voltage (5)	means. with V _{MPX} = 0mV V _{LEVEL} << V _{SBL} (fully mono)	FSC = 11	0.5	0.9(off)	1.3	V
			FSC = 10	1.0	1.3	1.6	V
			FSC = 01	1.5	1.8	2.1	V
			FSC = 00	2.0	2.3	2.6	V

1. All thresholds are measured using a pulse with TR = 2 ms, THIGH = 2 ms and TF = 10 ms.
2. All thresholds are measured using a pulse with TR = 2 ms, THIGH = 2 ms and TF = 10 ms.
3. NAT represents the Noise blanker-Byte bit pair D4,D3 for the noise controlled trigger adjustment.
4. OVD represents the Noise blanker-Byte bit pair D7,D6 for the over deviation detector.
5. FSC represents the Fieldstrength-Byte bit pair D1,D0 for the fieldstrength control.

Figure 16. Noise blanker diagram

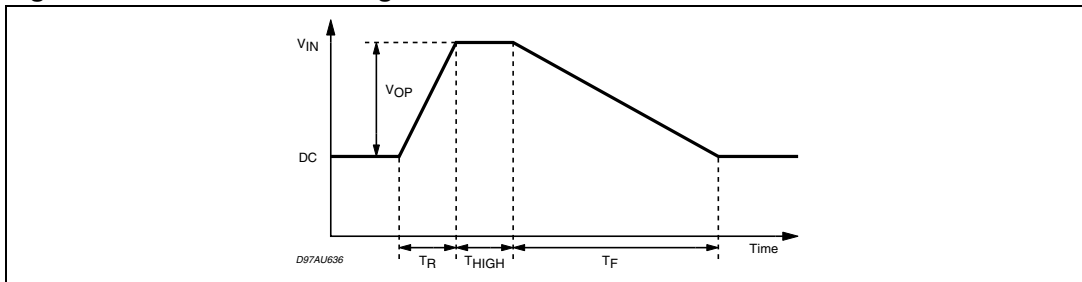


Figure 17. Trigger threshold vs. VPEAK

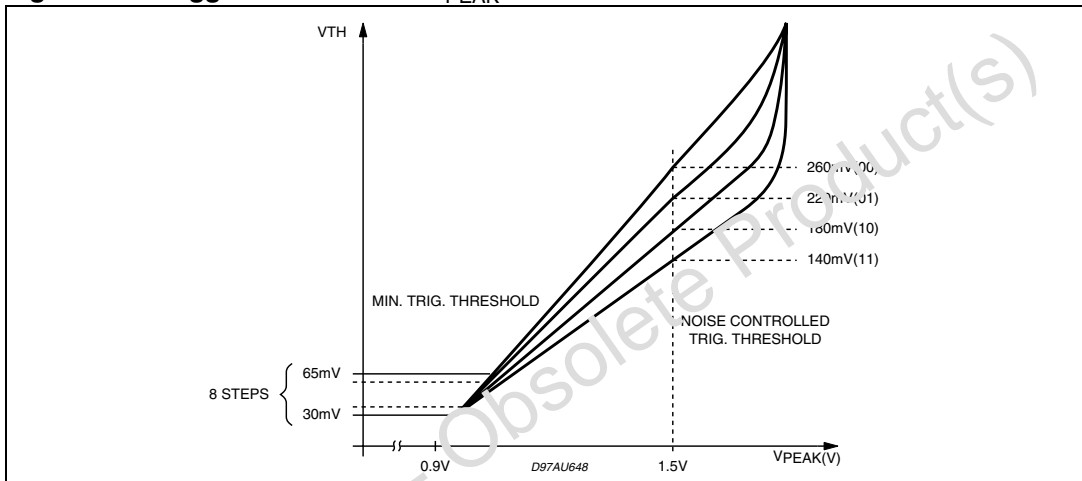


Figure 18. Deviation controlled trigger adjustment

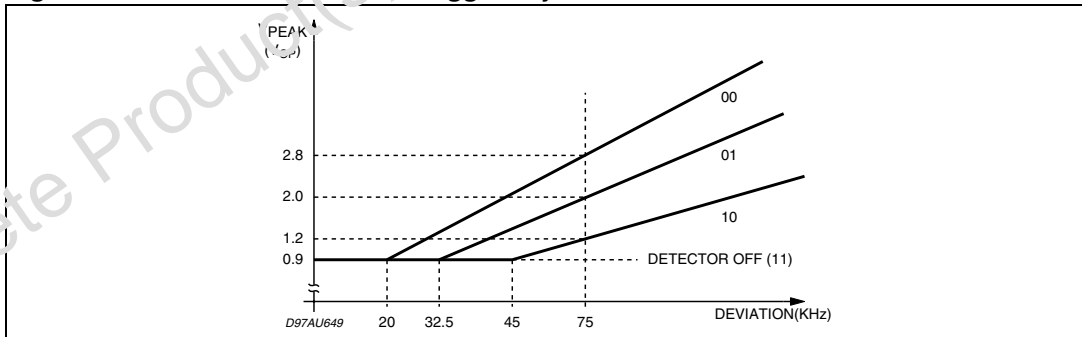
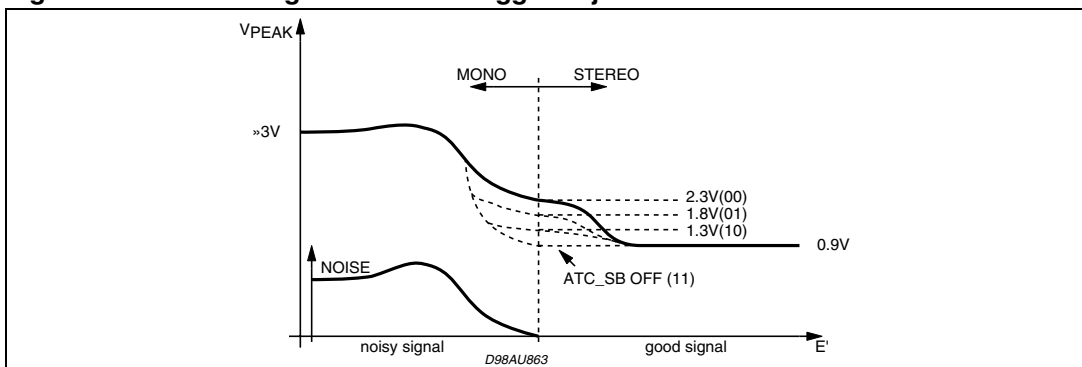


Figure 19. Fieldstrength controlled trigger adjustment



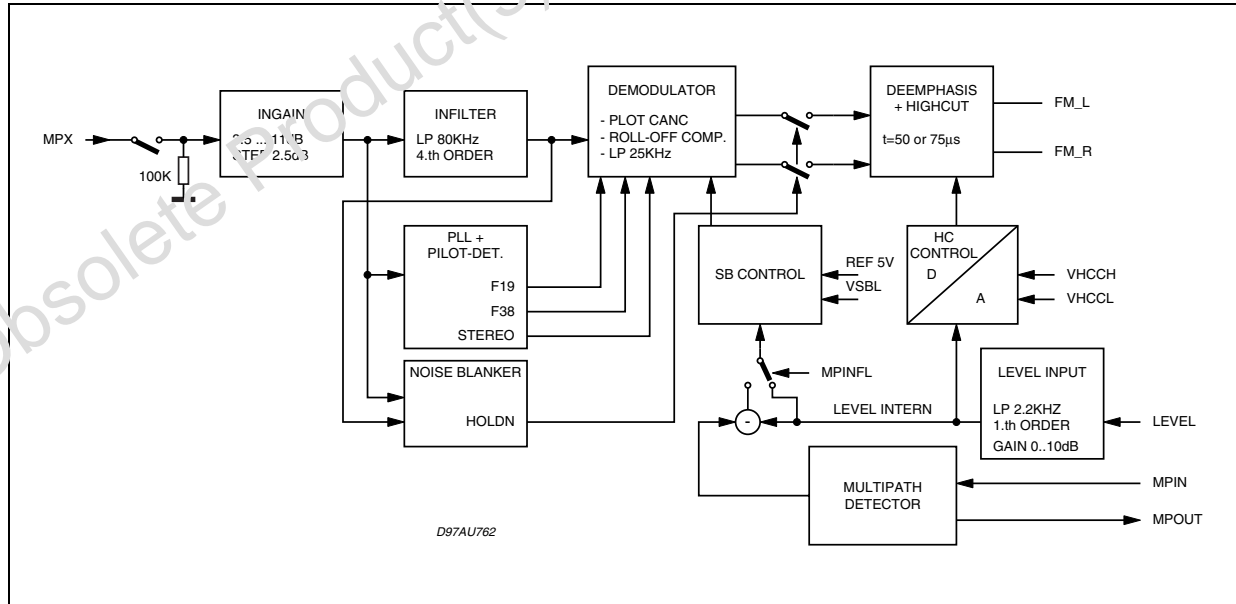
5.4 Multipath detector

- Internal 19 kHz bandpass filter
- Programmable bandpass and rectifier gain
- Two pin solution fully independent usable for external programming
- Selectable internal influence on stereo blend

Table 10. Multipath detector electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f _{CMP}	Center frequency of multipath-bandpass	stereo decoder locked on pilot tone		19		KHz
G _{BPMP}	Bandpass gain	bits D ₂ , D ₁ configuration byte = 00		6		dB
		bits D ₂ , D ₁ configuration byte = 01		16		dB
		bits D ₂ , D ₁ configuration byte = 10		12		dB
		bits D ₂ , D ₁ configuration byte = 11		13		dB
G _{RECTMP}	Rectifier gain	bits D ₇ , D ₆ configuration byte = 00		7.6		dB
		bits D ₇ , D ₆ configuration byte = 01		4.6		dB
		bits D ₇ , D ₆ configuration byte = 10		0		dB
I _{CHMP}	Rectifier charge current			1		μA
I _{DISMP}	Rectifier discharge current			1.5		mA

Figure 20. Block diagram of the stereo decoder

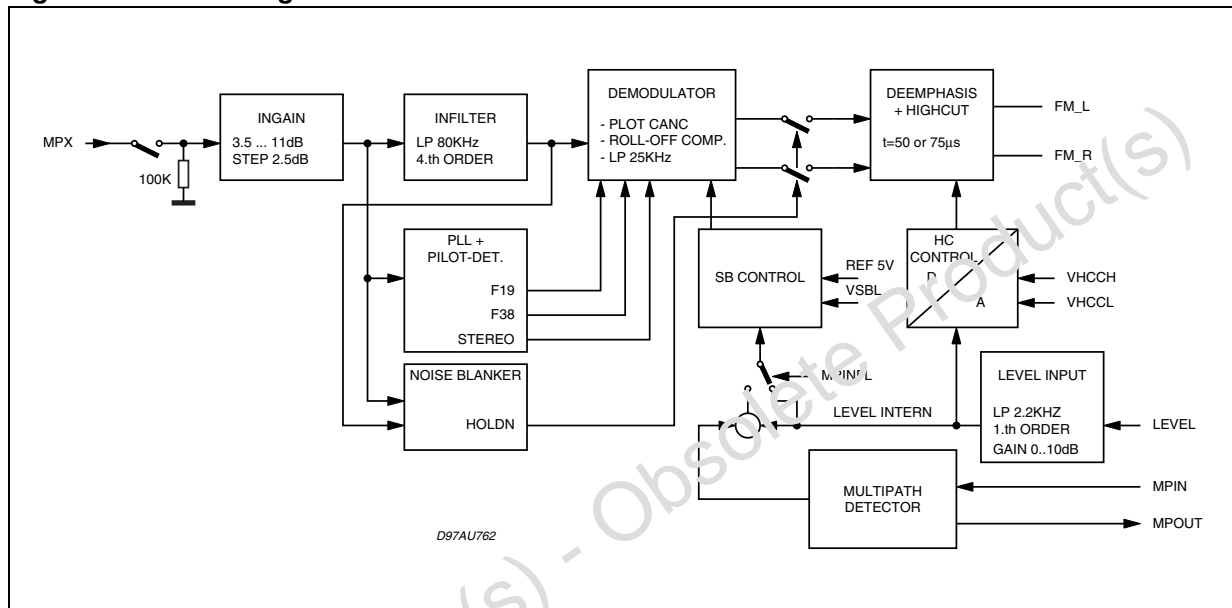


5.5 Description of stereo decoder

The stereo decoder part of the TDA7460ND (see [Figure 20.](#)) contains all functions necessary to demodulate the MPX signal like pilot tone dependent mono/stereo switching as well as "stereo blend" and "high cut" functions.

Adaptations like programmable input gain, roll-off compensation, selectable de-emphasis time constant and a programmable fieldstrength input allow to use different IF devices.

Figure 21. Block diagram of the stereo decoder



5.5.1 Stereo decoder mute

The TDA7460ND has a fast and easy to control RDS mute function which is a combination of the audioprocessor soft mute and the high-ohmic mute of the stereo decoder. If the stereo decoder is selected and a soft mute command is sent (or activated through the SM pin) the stereo decoder will be set automatically to the high-ohmic mute condition after the audio signal has been softmuted.

Hence a checking of alternate frequencies could be performed. To release the system from the mute condition simply the unmute command must be sent: the stereo decoder is unmuted immediately and the audioprocessor is softly unmuted. Fig. 18 shows the output signal V_O as well as the internal stereo decoder mute signal. This influence of Softmute on the stereo decoder mute can be switched off by setting bit 3 of the Softmute byte to "0". A stereo decoder mute command (bit 0, stereo decoder byte set to "1") will set the stereo decoder in any case independently to the high-ohmic mute state.

If any other source than the stereo decoder is selected the decoder remains muted and the MPX pin is connected to V_{ref} to avoid any discharge of the coupling capacitor through leakage currents.

5.5.2 Input stages

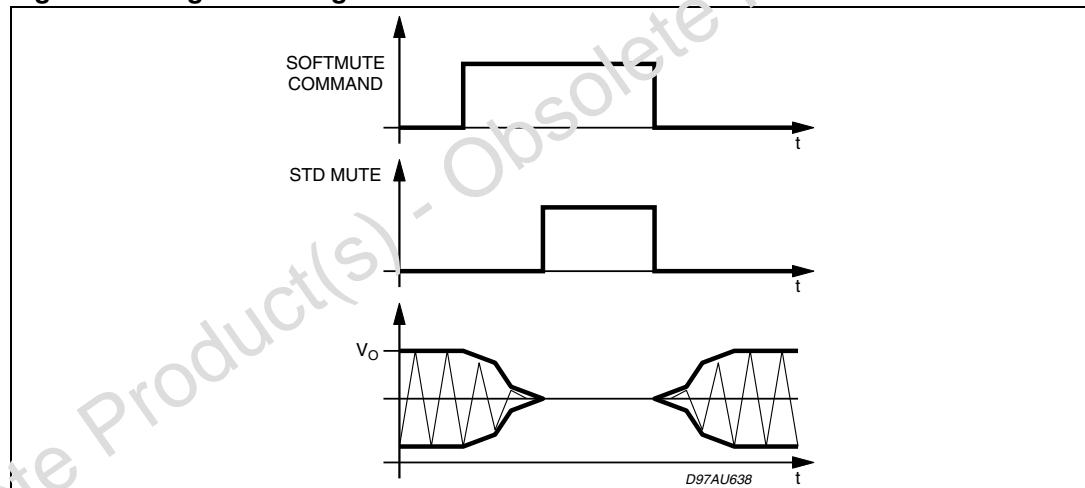
The In gain stage allows to adjust the MPX signal to a magnitude of about 1Vrms internally which is the recommended value. The 4.th order input filter has a corner frequency of 80kHz and is used to attenuate spikes and noise and acts as an anti-aliasing filter for the following switch capacitor filters.

5.5.3 Demodulator

In the demodulator block the left and the right channel are separated from the MPX signal. In this stage also the 19 kHz pilot tone is cancelled. For reaching a high channel separation the TDA7460ND offers an I²C bus programmable roll-off adjustment which is able to compensate the lowpass behavior of the tuner section. If the tuner attenuation at 38kHz is in a range from 20.2% to 31% the TDA7460ND needs no external network before the MPX pin. Within this range an adjustment to obtain at least 40dB channel separation is possible.

The bits for this adjustment are located together with the fieldstrength adjustment in one byte. This gives the possibility to perform an optimization step during the production of the car radio where the channel separation and the fieldstrength control are trimmed.

Figure 22. Signals during stereo decoder's soft mute



5.5.4 De-emphasis and high cut

The lowpass filter for the de-emphasis allows to choose between a time constant of 50ms and 75ms (bit D7, Stereo decoder byte).

The high cut control range will be in both cases $t_{HC} = 2 \cdot t_{Deemp}$. Inside the high cut control range (between VHCH and VHCL) the LEVEL signal is converted into a 5 bit word which controls the lowpass time constant between $t_{Deemp} \dots 3 \cdot t_{Deemp}$. There by the resolution will remain always 5 bits independently of the absolute voltage range between the VHCH and VHCL values.

The high cut function can be switched off by I²C bus (bit D7, Fieldstrength byte set to "0").

5.5.5 PLL and pilot tone detector

The PLL has the task to lock on the 19kHz pilotone during a stereo transmission to allow a correct demodulation. The included detector enables the demodulation if the pilot tone reaches the selected pilotone threshold VPTHST. Two different thresholds are available. The detector output (signal STEREO, see [Figure 1: Block diagram](#)) can be checked by reading the status byte of the TDA7460ND via I²C bus.

5.5.6 Fieldstrength control

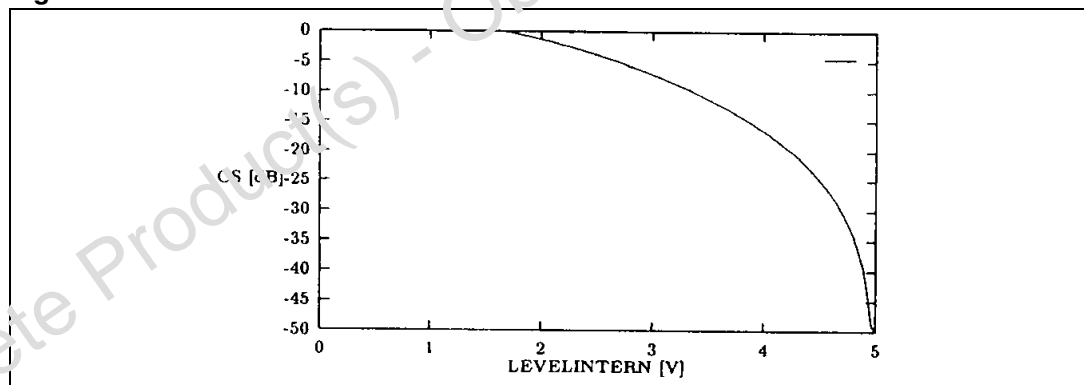
The fieldstrength input is used to control the high cut and the stereo blend function. In addition the signal can be also used to control the noise blanker thresholds.

5.5.7 Level input and gain

To suppress undesired high frequency modulation on the high cut and stereo blend function the LEVEL signal is lowpass filtered firstly. The filter is a combination of a 1st order RC lowpass at 53 kHz (working as anti-aliasing filter) and a 1st-order switched capacitor lowpass at 2.2 kHz. The second stage is a programmable gain stage to adapt the LEVEL signal internally to different IF.

The gain is widely programmable in 16 steps from 0 dB to 10 dB (step = 0.67 dB). These 4 bits are located together with the roll-off bits in the "Stereo decoder Adjustment" byte to simplify a possible adaptation during the production of the carradio.

Figure 23. Internal stereo blend characteristics



5.5.8 Stereo blend control

The stereo blend control block converts the internal LEVEL voltage (LEVEL INTERN) into an demodulator compatible analog signal which is used to control the channel separation between 0dB and the maximum separation. Internally this control range has a fixed upper limit which is the internal reference voltage REF5V. The lower limit can be programmed to be 33%, 42%, 50% or 58% of REF5V (see [Figure 24.](#)).

To adjust the external LEVEL voltage to the internal range two values must be defined: the LEVEL gain L_G and VSBL. To adjust the voltage where the full channel separation is reached (VST) the LEVEL gain L_G has to be defined. The following equation can be used to estimate the gain:

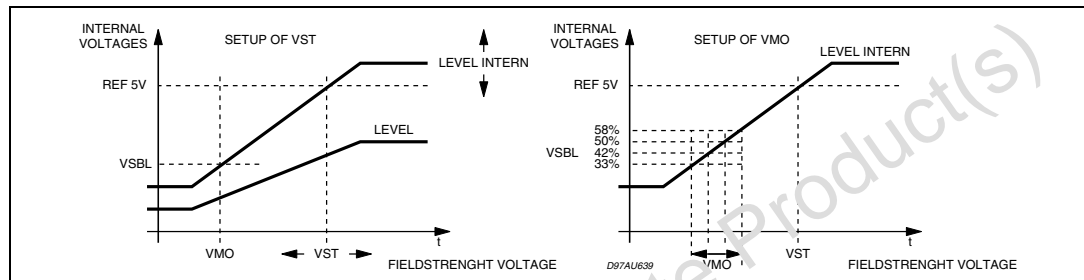
$$\frac{\text{REF5V}}{\text{Field strenght voltage [STE]}}$$

The gain can be programmed through 4 bits in the "Stereo decoder-Adjustment" byte.

The mono voltage VMO (0 dB channel separation) can be chosen selecting 33, 42, 50 or 58 % of REF5V. All necessary internal reference voltages like REF5V are derived from a bandgap circuit. Therefore they have a temperature coefficient near zero. This is useful if the fieldstrength signal is also temperature compensated.

But most if devices apply a level voltage with a TC of 3300 ppm. The TDA7460ND offers this TC for the reference voltages, too. The TC is selectable with bit D7 of the "stereo decoder adjustment" byte.

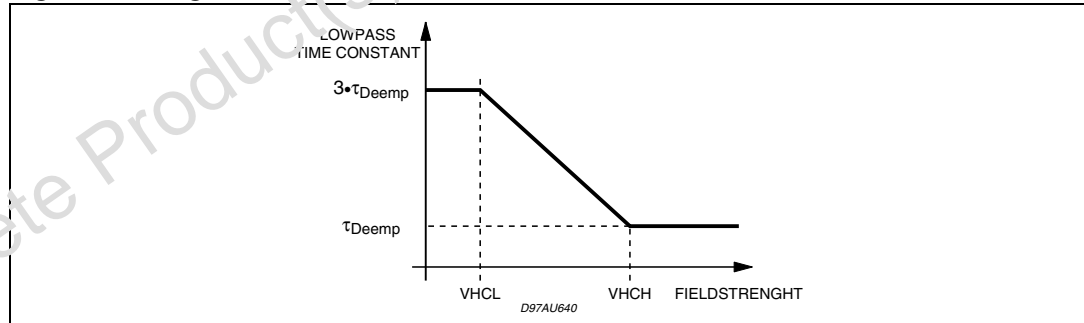
Figure 24. Relation between internal and external LEVEL voltage and setup of stereo blend



5.5.9 High cut control

The high cut control setup is similar to the stereo blend control setup: the starting point VHCH can be set with 2 bits to be 42, 50, 55 or 66% of REF5 V whereas the range can be set to be 17 or 33% of VHCH (see [Figure 25](#)).

Figure 25. High cut characteristics



5.6 Functional description of the noise blanker

In the automotive environment the MPX signal is disturbed by spikes produced by the ignition and for example the wiper motor. The aim of the noise blanker part is to cancel the audible influence of the spikes. Therefore the output of the stereo decoder is held at the actual voltage for 40 μs.

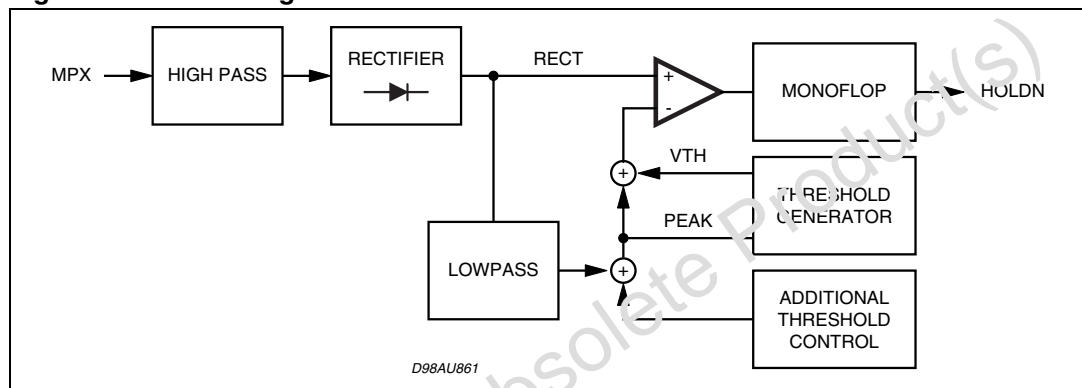
In a first stage the spikes must be detected but to avoid a wrong triggering on high frequency (white) noise a complex trigger control is implemented. Behind the trigger stage a pulse former generates the "blanking" pulse. To avoid any crosstalk to the signal path the noise blanker is supplied by his own biasing circuit.

5.6.1 Trigger path

The incoming MPX signal is highpass filtered, amplified and rectified. This second order highpass-filter has a corner frequency of 140kHz. The rectified signal, RECT, is lowpass filtered to generate a signal called PEAK. Also noise with a frequency 140 kHz increases the PEAK voltage. The PEAK voltage is fed to a threshold generator, which adds to the PEAK voltage a DC dependent threshold VTH. Both signals, RECT and PEAK+VTH are fed to a comparator which triggers a re-triggerable monoflop. The monoflop's output activates the sample-and-hold circuits in the signal path for 40 μ s.

The block diagram of the noise blanker is given in [Figure 26](#).

Figure 26. Block diagram of the noise blanker



5.6.2 Automatic noise controlled threshold adjustment (ATC)

There are mainly two independent possibilities for programming the trigger threshold:

- the low threshold in 8 steps (bits D0 to D2 of the noise blanker byte)
- the noise adjusted threshold in 4 steps (bits D3 and D4 of the noise blanker byte, see [Figure 17](#)).

The low threshold is active in combination with a good MPX signal without any noise; the PEAK voltage is less than 1V. The sensitivity in this operation is high.

If the MPX signal is noisy the PEAK voltage increases due to the higher noise, which is also rectified. With increasing of the PEAK voltage the trigger threshold increases, too. This particular gain is programmable in 4 steps (see [Figure 17](#)).

5.6.3 Automatic threshold control

Besides the noise controlled threshold adjustment there is an additional possibility for influencing the trigger threshold. It is depending on the stereo blend control.

The point where the MPX signal starts to become noisy is fixed by the RF part. Therefore also the starting point of the normal noise-controlled trigger adjustment is fixed (fig. 16). In some cases the behavior of the noise blanker can be improved by increasing the threshold even in a region of higher fieldstrength. Sometimes a wrong triggering occurs for the MPX signal often shows distortion in this range which can be avoided even if using a low threshold.

Because of the overlap of this range and the range of the stereo/mono transition it can be controlled by stereo blend. This threshold increase is programmable in 3 steps or switched off with bits D0 and D1 of the fieldstrength control byte.

5.6.4 Over deviation detector

If the system is tuned to stations with a high deviation the noise blanker can trigger on the higher frequencies of the modulation. To avoid this wrong behavior, which causes noise in the output signal, the noise blanker offers a deviation dependent threshold adjustment.

By rectifying the MPX signal a further signal representing the actual deviation is obtained. It is used to increase the PEAK voltage. Offset and gain of this circuit are programmable in 3 steps with the bits D6 and D7 of the stereo decoder byte (the first step turns off the detector, see [Figure 18.](#)).

5.7 Functional description of the multipath detector

Using the internal detector the audible effects of a multipath condition can be minimized. A multipath condition is detected by rectifying the 19 kHz spectrum in the fieldstrength signal.

Selecting the "internal influence" in the configuration byte, the channel separation is automatically reduced during a multipath condition according to the voltage appearing at the MPOUT pin.

To obtain a optimal performance an adaptation is necessary. Therefore the gain of the 19 kHz bandpass is programmable in four steps as well as the rectifier gain. The attack and decay times can be set by the external capacitor values.

5.8 Test mode

During the test mode which can be activated by setting bit D0 of the testing byte and bit D5 of the subaddress byte to "1" several internal signals are available at the CASSR pin. During this mode the input resistance of 100 kOhm is disconnected from the pin. The internal signals available are shown in the software specification.

Figure 27. Block diagram of the multipath detector

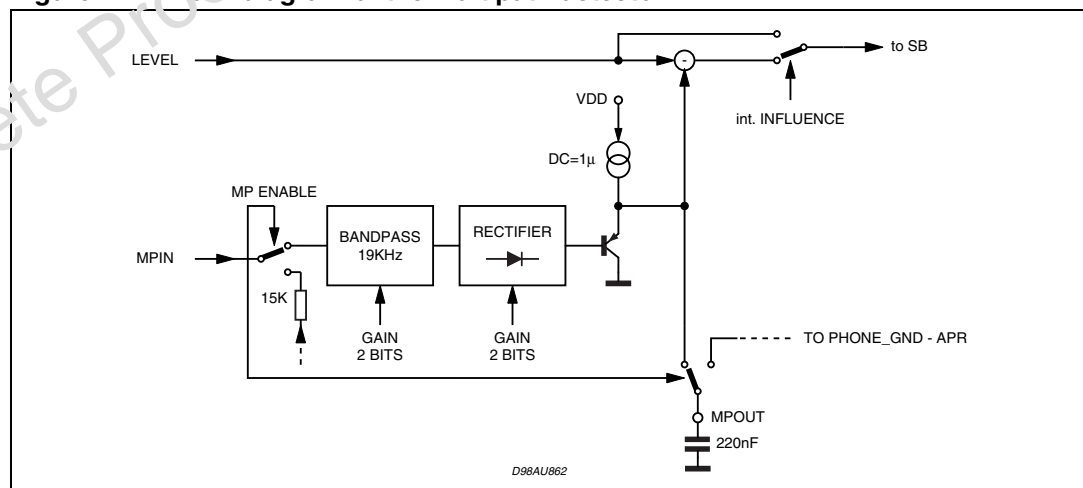


Figure 28. Application example 1 (with phone input)

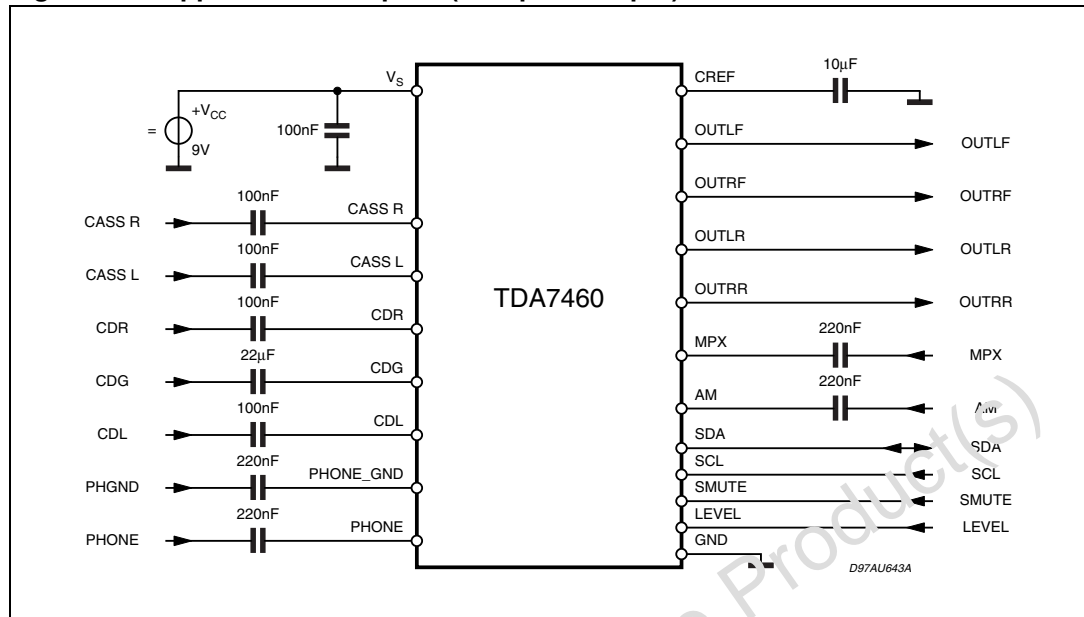
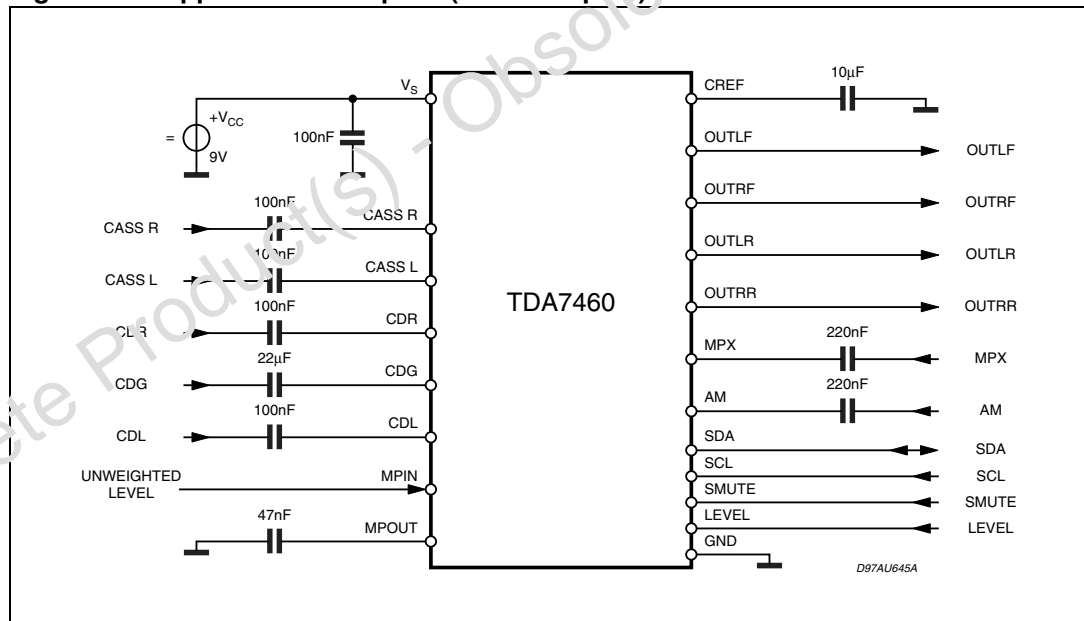


Figure 29. Application example 2 (with multipath)



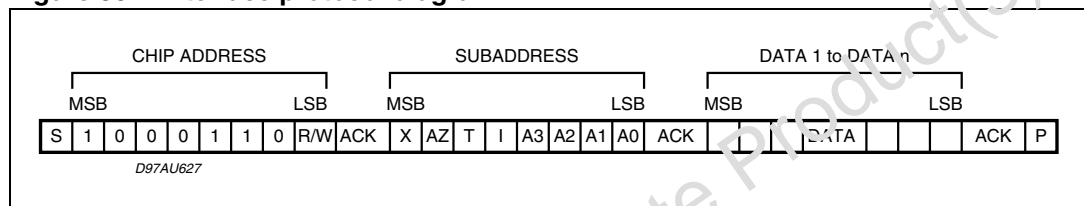
6 I²C bus interface description

6.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB bit determines read / write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)

Figure 30. Interface protocol diagram



- S = Start;
- ACK = Acknowledge;
- AZ = AutoZero-Remain;
- T = Testing;
- I = Auto increment;
- P = Stop;
- Max clock speed is 500 kbits/s.

The transmitted data is automatically updated after each ACK.

Transmission can be repeated without new chip address.

6.2 Auto increment

If bit I in the subaddress byte is set to "1", the auto increment of the subaddress is enabled.

Table 11. Transmitted data (send mode)

MSB				LSB			
X	X	X	X	ST	SM	X	X

SM = Soft Mute activated;

ST = Stereo;

X = not used

Table 12. Subaddress (receive mode)

MSB				LSB				Function
X	AZ	T	I	A3	A2	A1	A0	
				0	0	0	0	Input selector
				0	0	0	1	Loudness / auto-zero
				0	0	1	0	Volume
				0	0	1	1	Soft mute / beep
				0	1	0	0	Bass / treble attenuator
				0	1	0	1	Bass / treble configuration
				0	1	1	0	Speaker attenuator LF
				0	1	1	1	Speaker attenuator LR
				1	0	0	0	Speaker attenuator RF
				1	0	0	1	Speaker attenuator RR / blank time adjust
				1	0	1	0	Stereo decoder
				1	0	1	1	Noise blanker
				1	1	0	0	Fieldstrength control
				1	1	0	1	Configuration
				1	1	1	0	Stereo decoder adjustment
				1	1	1	1	Testing

T = Testmode

I = Auto increment

AZ = Auto Zero Remain

X = not used

7 Data byte specification

Table 13. Input selector

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
					0	0	0	Source selector
					0	0	1	CD
					0	1	0	Cassette
					0	1	1	Phone
					1	0	0	AM
					1	0	1	Stereo decoder
					1	1	0	Input FM
					1	1	1	Mute
					1	1	1	AC inputs
				0				CD mode
				1				CD full-differential
								CD quasi-diff
			1		0	1	1	AM/FM mode
			0		0	1	1	AM mono
			0		1	0	0	AM stereo
			0		1	0	0	AM through Stereo decoder
			1		1	0	0	FM- Stereo decoder
0	0	0						In-gain
0	0	1						14dB
:	:	:						12dB
1	1	0						:
1	1	1						2 dB
								0 dB

For example to select the CD input in quasi-differential mode with gain of 8dB the data byte is: 0/01111000

Table 14. Loudness

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
				0	0	0	0	Attenuation 0 dB
				0	0	0	1	-1 dB
				:	:	:	:	:
				1	1	1	0	-14 dB
				1	1	1	1	-15 dB
			0					Filter on
			1					off (flat)
		0						Center frequency 200 Hz
		1						400 Hz
	0							Loudness G low (1 st order)
	1							normal (2 nd order)
1								must be "1"

Note: The attenuation is specified at high frequencies. Around the center frequency the value is different depending on the programmed attenuation (see [Loudness frequency response](#)).

Table 15. Mute, beep and mixing

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
							0	Mute Enable soft mute
							1	Disable soft mute
					0	0		Mute time =0.48 ms
					0	1		Mute time =0.96 ms
					1	0		Mute time =40.4 ms
					1	1		Mute time =324 ms
			0					Stereo decoder soft mute Influence = off
			1					stereo decoder soft mute influence = on
			0					Beep Beep frequency = 600 Hz
			1					Beep frequency = 1.2 kHz
		0						Mixing Mix-source = beep
		1						Mix-source = phone
0	0							Full mix signal
0	1							Source -12 dB + mix-signal -2.5 dB
1	0							Source -6 dB + mix-signal -6 dB
1	1							Full source

Note: for more information to the stereo decoder-soft mute-influence please refer to the Stereo decoder Description.

Table 16. Volume

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	Gain/attenuation +32 dB
	0	0	0	0	0	0	1	+31 dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	0	0	+20 dB
	0	0	0	1	1	0	1	+19 dB
	0	0	0	1	1	1	0	+18 dB
	:	:	:	:	:	:	:	:
	0	0	1	1	1	1	1	+1 dB
	0	1	0	0	0	0	0	0 dB
	0	1	0	0	0	0	1	- 1 dB
	:	:	:	:	:	:	:	:
	1	1	0	1	1	1	0	-78 dB
	1	1	0	1	1	1	1	-79 dB
								Soft step
0								Soft step volume = off
1								Soft step volume = on

Note: It is not recommended to use a gain more than 20dB for system performance reason. In general, the max. gain should be limited by software to the maximum value, which is needed for the system.

Table 17. Bass and treble attenuation

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
				0	0	0	0	Treble steps -14 dB	
				0	0	0	1	-12 dB	
				:	:	:	:	:	
				0	1	1	0	-2 dB	
				0	1	1	1	0 dB	
				1	1	1	1	0 dB	
				1	1	1	0	+2 dB	
				:	:	:	:	:	
				1	0	0	1	+12 dB	
				1	0	0	0	+14 dB	
0	0	0	0					Bass steps -14 dB	
0	0	0	1					-12 dB	
:	:	:	:					:	
0	1	1	0					-2 dB	
0	1	1	1					0 dB	
1	1	1	1					0 dB	
1	1	1	0					+2 dB	
:	:	:	:					:	
1	0	0	1					+12 dB	
1	0	0	0					+14 dB	

For example 12 dB Treble and -8 dB Bass give the following DATA BYTE: 0 0 1 1 1 0 0 1.

Table 18. Bass and treble filter characteristics

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
						0	0	Treble Center frequency = 10 KHz
						0	1	Center frequency = 12.5 KHz
						1	0	Center frequency = 15 KHz
						1	1	Center frequency = 17.5 KHz
				0	0			Bass Center frequency = 60 Hz
				0	1			Center frequency = 7 Hz
				1	0			Center frequency = 80 Hz
				1	1			Center frequency = 100 Hz
		1	1	1	1			Center frequency = 150 Hz
		0	0					Quality factor = 1
		0	1					Quality factor = 1.25
		1	0					Quality factor = 1.5
		1	1					Quality factor = 2
	0							DC-gain = 0 dB
	1							DC-gain = ±4.4 dB
1								must be "1"

For example Treble center frequency = 15 KHz, Bass center frequency = 100 Hz, Bass Q = 1 and DC = 0 dB give the following DATA BYTE: 1 0 0 0 1 1 1 0

Table 19. Speaker attenuation (LF, LR, RF, RR)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
		0	0	0	0	0	0	Attenuation 0 dB
		0	0	0	0	0	1	-1 dB
		:	:	:	:	:	:	:
		0	1	0	1	1	1	-23 dB
		0	1	1	0	0	0	-24.5 dB
		0	1	1	0	0	1	-26 dB
		0	1	1	0	1	0	-28 dB
		0	1	1	0	1	1	-30 dB
		0	1	1	1	0	0	-32 dB
		0	1	1	1	0	1	-35 dB
		0	1	1	1	1	0	-40 dB
		0	1	1	1	1	1	-50 dB
1	1	1						Speaker mute Must be "1" (except RR speaker; see below)
0	0							Attack Time adj. (only at RR speaker) 38µs
0	1							25.5µs
1	0							32µs
1	1							22µs
0	0	0	0					Bass Steps -14 dB
0	0	0	1					-12 dB
:	:	:	:					:
0	1	1	0					-2 dB
0	1	1	1					0 dB
1	1	1	1					0 dB
1	1	1	0					+2 dB
:	:	:	:					:
1	0	0	1					+12 dB
1	0	0	0					+14 dB

For example 12dB Treble and -8dB Bass give the following DATA BYTE: 0 0 1 1 1 0 0 1.

Table 20. Stereo decoder

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	STD unmuted STD muted
					0 0 1 1	0 1 0 1		IN-Gain 11 dB IN-Gain 8.5 dB IN-Gain 6 dB IN-Gain 3.5 dB
				1				must be "1"
		1 1	0 1					Forced mono Mono/stereo switch automatically
	0 1							Pilot threshold high Pilot threshold low
0 1								De-emphasis 50 μ s De-emphasis 75 μ s

Table 21. Noise blanker

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
					0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	Low threshold 65 mV Low threshold 60 mV Low threshold 55 mV Low threshold 50 mV Low threshold 45 mV Low threshold 40 mV Low threshold 35 mV Low threshold 30 mV
			0 0 1 1	0 1 0 1				Noise controlled threshold 320 mV Noise controlled threshold 260 mV Noise controlled threshold 200 mV Noise controlled threshold 140 mV
		0 1						Noise blanker off Noise blanker on
0 0 1 1	0 1 0 1							Over deviation adjust 2.8 V Over deviation adjust 2.0 V Over deviation adjust 1.2 V Over deviation detector off

Table 22. Field strength control

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
						0	0	Noiseblanker field strength adj 2.3 V	
						0	1	Noiseblanker field strength adj 1.8 V	
						1	0	Noiseblanker field strength adj 1.3 V	
						1	1	Noiseblanker field strength adj off	
				0	0			VSBL at 33 % REF 5 V	
				0	1			VSBL at 42 % REF 5 V	
				1	0			VSBL at 50 % REF 5 V	
				1	1			VSBL at 58 % REF 5 V	
		0	0					VHCH at 42 % REF 5 V	
		0	1					VHCH at 50 % REF 5 V	
		1	0					VHCH at 58 % REF 5 V	
		1	1					VHCH at 66 % REF 5 V	
	1							VHCL at 17 % VHCH	
	0							VHCL at 33 % VHCH	
0								High cut off	
1								High cut on	

Table 23. Configuration

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
						0	0	Noise rectifier discharge resistor R = infinite R = 56 kΩ R = 33 kΩ R = 18 kΩ	
						0	1		
						1	0		
						1	1		
				0	0			Multipath detector bandpass gain 6 dB 16 dB 12 dB 18 dB	
				0	1				
				1	0				
				1	1				
			0					Multipath detector internal influence on off	
			1						
		0						Multipath/function selected (MPIN, MPOUT) Additional input selected (phone)	
		1							
0	0							Multipath detector reflection gain Gain = 7.6 dB Gain = 4.6 dB Gain = 0 dB Off	
0	1								
1	0								
1	1								

Table 24. Stereo decoder adjustment

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
					0	0	0	Roll-off compensation not allowed	
					0	0	1	20.2%	
					0	1	0	21.9%	
					:	:	:	:	
					1	0	0	25.5%	
					:	:	:	:	
					1	1	1	31.0%	
	0	0	0	0				Level gain 0dB	
	0	0	0	1				0.66dB	
	0	0	1	0				1.33dB	
	:	:	:	:				:	
	1	1	1	1				10dB	
0								Temperature compensation at LEVEL input TC = 0	
1								TC = 16.7mV/K (3300ppm)	

Obsolete Product(s) - Obsolete Product(s)

Table 25. Testing

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
							0	Stereo decoder test signals Off	
							1	Test signals enabled if bit D5 of the subaddress (test mode bit) is set to "1", too	
						0		External clock	
						1		Internal clock	
		0	0	0	0			Test signals at CASS_R VHCCH	
		0	0	0	1			Level intern	
		0	0	1	0			Pilot magnitude	
		0	0	1	1			VCOCON, VCC Control Voltage	
		0	1	0	0			Pilot threshold	
		0	1	0	1			HOLDN	
		0	1	1	0			NB threshold	
		0	1	1	1			F228	
		1	0	0	0			VHCCL	
		1	0	0	1			VSBL	
		1	0	1	0			not used	
		1	0	1	1			not used	
		1	1	0	0			PEAK	
		1	1	0	1			not used	
		1	1	1	0			REF5V	
		1	1	1	1			not used	
	0							VCO Off	
	1							On	
0								Audioprocessor test mode only if bit D5 of the subaddress (test mode bit) is set to "1"	
1								Off	

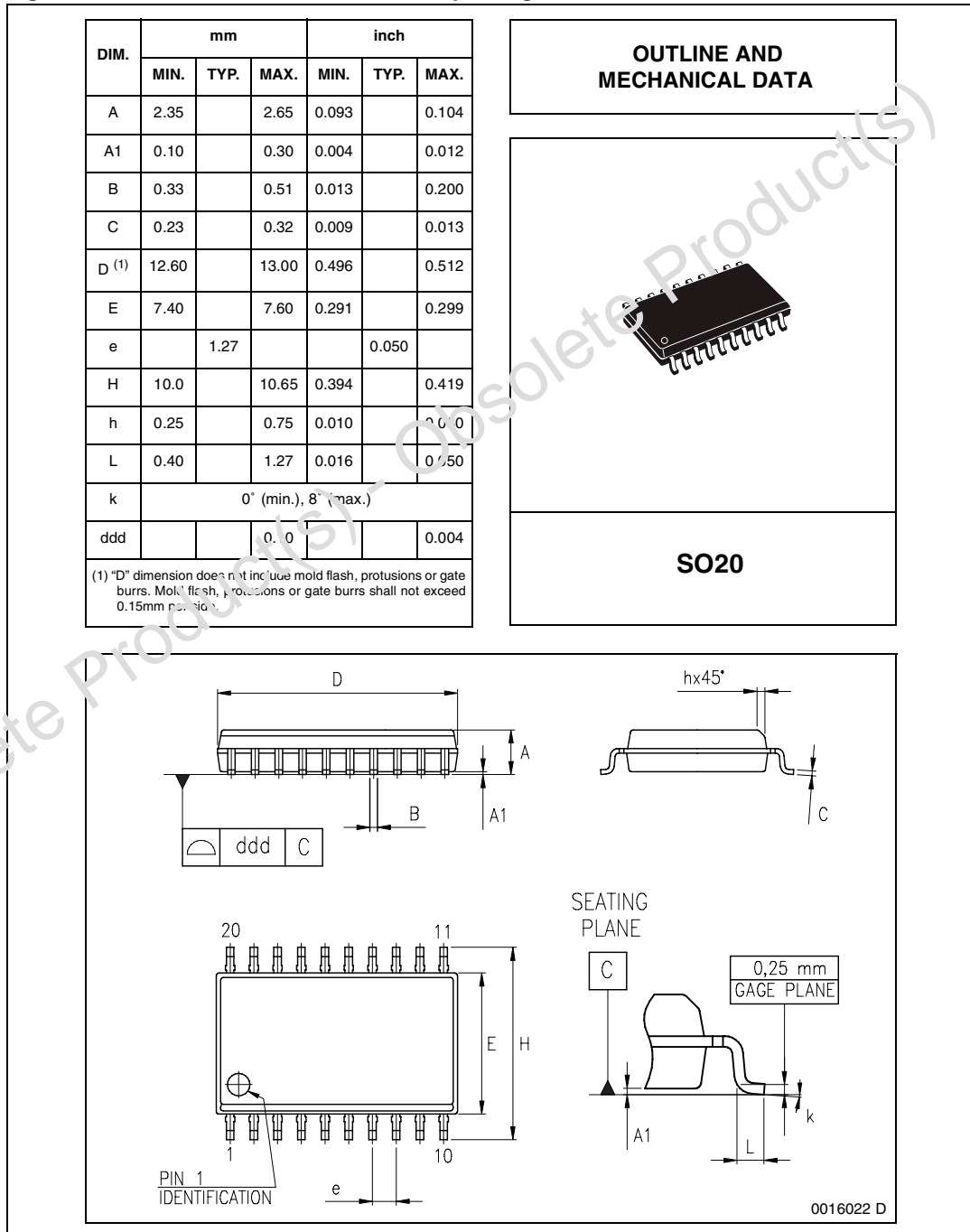
Note: This byte is used for testing or evaluation purposes only and must not be set to other values than the default "11111110" in the application!

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Figure 31. SO20 mechanical data and package dimensions



9 Revision history

Table 26. Document revision history

Date	Revision	Changes
24-Jun-2000	3	Initial release.
06-Mar-2009	4	Document reformatted. Document status changed from datasheet to not for new design. Added Table 1: Device summary on page 1 . Updated Section 8: Package information on page 47 .

Obsolete Product(s) - Obsolete Product(s)

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2009 STMicroelectronics - All rights reserved



STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America



www.st.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View TDA7460NDTR](#) on WIN SOURCE
-  [STMicroelectronics](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management