



THE DATASHEET OF TL103WAID



TL103W Dual Operational Amplifiers With Internal Reference

1 Features

- Operational Amplifier
 - Low Offset Voltage Max of:
 - TL103WA...3 mV (25°C) and 5 mV (Full Temperature)
 - TL103W...4 mV (25°C) and 5 mV (Full Temperature)
 - Low Supply Current...350 μ A/Channel (Typ)
 - Unity Gain Bandwidth...0.9 MHz (Typ)
 - Input Common-Mode Range Includes GND
 - Large Output-Voltage Swing... 0 V to $V_{CC} - 1.5$ V
 - Wide Supply-Voltage Range...3 V to 32 V
 - 2.5-kV ESD Protection (HBM)
- Voltage Reference
 - Fixed 2.5-V Reference
 - Tight Tolerance Max of:
 - TL103WA...0.4% (25°C) and 0.8% (Full Temperature)
 - TL103W . . . 0.7% (25°C) and 1.4% (Full Temperature)
 - Low Temperature Drift...7 mV (Typ) Over Operating Temperature Range
 - Wide Sink-Current Range . . . 0.5 mA (Typ) to 100 mA
 - Output Impedance...0.2 Ω (Typ)

2 Applications

- Battery Chargers
- Switch-Mode Power Supplies
- Linear Voltage Regulation
- Data-Acquisition Systems

3 Description

The TL103W and TL103WA combine the building blocks of a dual operational amplifier and a fixed voltage reference – both of which often are used in the control circuitry of both switch-mode and linear power supplies. OP AMP1 has its noninverting input internally tied to a fixed 2.5-V reference, while OP AMP2 is independent, with both inputs uncommitted.

For the A grade, especially tight voltage regulation can be achieved through low offset voltages for both operational amplifiers (typically 0.5 mV) and tight tolerances for the voltage reference (0.4% at 25°C and 0.8% over operating temperature range).

The TL103W and TL103WA are characterized for operation from -40°C to 105°C .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL103W	SOIC (8)	4.90 mm x 3.91 mm
TL103WA	WSON (8)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

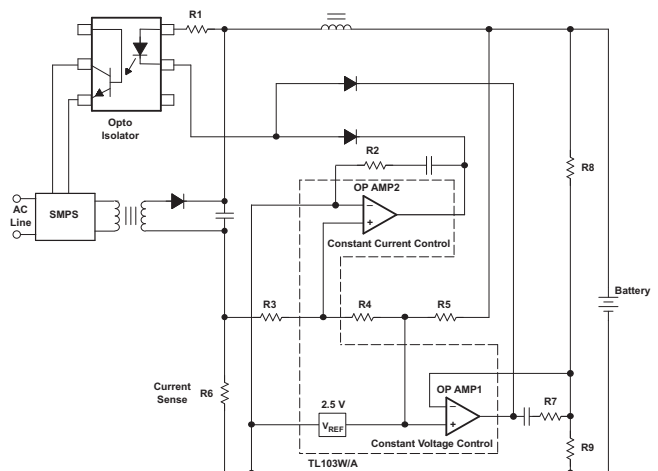


Figure 1. TL103W/A in a Constant-Current and Constant-Voltage Battery Charger



Table of Contents

1 Features	1	6.6 OP AMP2, Independent Operational Amplifier, Electrical Characteristics.....	6
2 Applications	1	6.7 Voltage Reference, Electrical Characteristics.....	7
3 Description	1	6.8 Total Device, Electrical Characteristics.....	7
4 Revision History	2	7 Device and Documentation Support	8
5 Pin Configuration and Functions	3	7.1 Related Links	8
6 Specifications	4	7.2 Receiving Notification of Documentation Updates....	8
6.1 Absolute Maximum Ratings	4	7.3 Community Resources.....	8
6.2 ESD Ratings	4	7.4 Trademarks	8
6.3 Recommended Operating Conditions.....	4	7.5 Electrostatic Discharge Caution.....	8
6.4 Thermal Information	4	7.6 Glossary	8
6.5 OP AMP1, Operational Amplifier With Noninverting Input Connected to the Internal V_{REF} Electrical Characteristics.....	5	8 Mechanical, Packaging, and Orderable Information	8

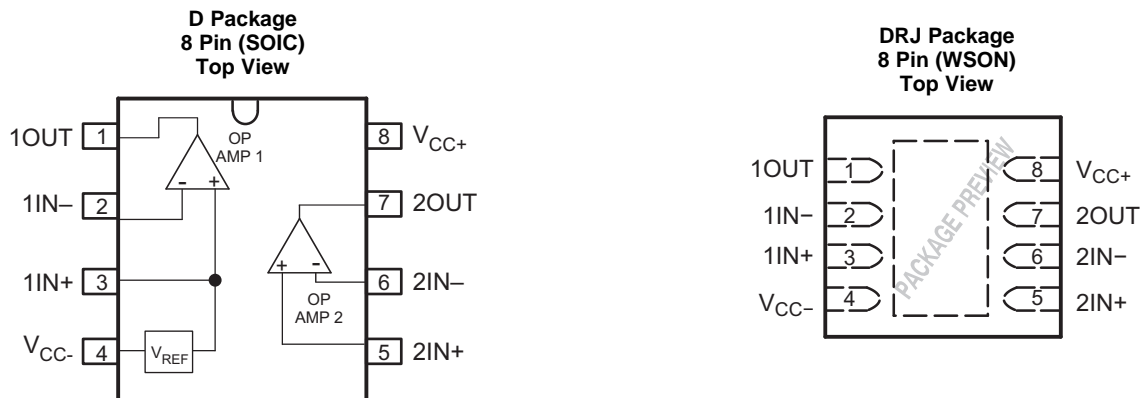
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (February 2016) to Revision M	Page
• Changed positive and negative terminals OP AMP 2 in the D Package image of Pin Configuration and Functions	3

Changes from Revision K (October 2010) to Revision L	Page
• Added the <i>Device Information</i> table, <i>Pin Configuration and Functions</i> , <i>ESD Ratings</i> , <i>Thermal Information</i> , <i>Device and Documentation Support</i> , and <i>Mechanical, Packaging, and Orderable Information</i> sections	1
• Changed Features From: 2 kV ESD Protection (HBM) To: 2.5-kV ESD Protection (HBM)	1
• Changed the Zener diode component to V_{REF} in the <i>Typical Application Circuit</i>	1
• Changed the Zener diode component to V_{REF} in the D Package of Pin Configuration and Functions	3

5 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	D	DRJ		
1OUT	1	1	O	Opamp 1 output
1IN-	2	2	I	Opamp 1 inverting input
1IN+	3	3	I	Opamp 1 non-inverting input and Shunt reference cathode terminal
V _{CC-}	4	4	I	Negative Supply Voltage
2IN+	5	5	O	Opamp 2 output
2IN-	6	6	I	Opamp 2 inverting input
2OUT	7	7	I	Opamp 2 non-inverting input
V _{CC+}	8	8	I	Positive Supply Voltage

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V _{CC} Supply voltage		36	V
V _{ID} Operational amplifier input differential voltage		36	V
V _I Operational amplifier input voltage range	–0.3	36	V
I _{KA} Voltage reference cathode current		100	mA
T _J Maximum junction temperature		150	°C
T _{stg} Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

6.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V _{IN} Supply voltage	3	32	V
I _K Cathode current	1	100	mA
T _A Operating free-air temperature	–40	105	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TL103W / TL103W	UNIT
	D (SOIC)	
	8 PINS	
R _{θJA} Junction-to-ambient thermal resistance	97	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 OP AMP1, Operational Amplifier With Noninverting Input Connected to the Internal V_{REF} Electrical Characteristics

 $V_{CC+} = 5\text{ V}$, $V_{CC} = \text{GND}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{icm} = 0\text{ V}$	25°C		1	4	mV
			Full range			5	
	TL103WA	$V_{icm} = 0\text{ V}$	25°C		0.5	3	
			Full range			5	
αV_{IO}	Input offset-voltage drift		25°C		7	$\mu\text{V}/^\circ\text{C}$	
I_{IB}	Input bias current (negative input)		25°C		20	nA	
A_{VD}	Large-signal voltage gain	$V_{CC+} = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_{icm} = 0\text{ V}$	25°C		100		V/mV
k_{SVR}	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V}$ to 30 V , $V_{icm} = 0\text{ V}$	25°C	65	100		dB
$I_{O(\text{source})}$	Output source current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = 1\text{ V}$	25°C	20	40		mA
I_{SC}	Short circuit to GND	$V_{CC+} = 15\text{ V}$	25°C		40	60	mA
$I_{O(\text{sink})}$	Output sink current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = -1\text{ V}$	25°C	10	12		mA
		$V_{CC+} = 15\text{ V}$, $V_O = 0.2\text{ V}$, $V_{id} = -1\text{ V}$		12	50		μA
V_{OH}	High-level output voltage	$V_{CC} = 30\text{ V}$, $R_L = 2\text{ k}\Omega$	25°C	26	27		V
			Full range	26			
		$V_{CC} = 30\text{ V}$, $R_L = 10\text{ k}\Omega$	25°C	27	28		
			Full range	27			
V_{OL}	Low-level output voltage	$R_L = 10\text{ k}\Omega$	25°C		5	20	mV
			Full range			20	
SR	Slew rate at unity gain	$V_{CC+} = 15\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $V_I = 0.5\text{ V}$ to 2 V , unity gain	25°C	0.2	0.4		V/ μs
GBW	Gain bandwidth product	$V_{CC+} = 30\text{ V}$, $V_I = 10\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 100\text{ kHz}$	25°C	0.5	0.9		MHz
THD	Total harmonic distortion	$V_{CC+} = 30\text{ V}$, $V_O = 2\text{ V}_{pp}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $A_V = 20\text{ dB}$	25°C		0.02%		

6.6 OP AMP2, Independent Operational Amplifier, Electrical Characteristics

$V_{CC+} = 5\text{ V}$, $V_{CC} = \text{GND}$, $V_O = 1.4\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{icm} = 0\text{ V}$	25°C	1		4	mV
			Full range			5	
	TL103WA	$V_{icm} = 0\text{ V}$	25°C	0.5		3	
			Full range			5	
αV_{IO}	Input offset voltage drift		25°C	7			$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current		25°C	2		75	nA
			Full range			150	
I_{IB}	Input bias current		25°C	20		150	nA
			Full range			200	
A_{VD}	Large-signal voltage gain	$V_{CC+} = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_O = 1.4\text{ V}$ to 11.4 V	25°C	50	100		V/mV
			Full range	25			
k_{SVR}	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V}$ to 30 V	25°C	65	100		dB
V_{ICR}	Input common-mode voltage range	$V_{CC+} = 30\text{ V}^{(1)}$	25°C	0	$V_{CC+} - 1.5$		V
			Full range	0	$V_{CC+} - 2$		
CMRR	Common-mode rejection ratio		25°C	70	85		dB
			Full range	60			
$I_{O(\text{source})}$	Output source current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = 1\text{ V}$	25°C	20	40		mA
I_{SC}	Short circuit to GND	$V_{CC+} = 15\text{ V}$	25°C	40		60	mA
$I_{O(\text{sink})}$	Output sink current	$V_{CC+} = 15\text{ V}$, $V_O = 2\text{ V}$, $V_{id} = -1\text{ V}$	25°C	10	12		mA
		$V_{CC+} = 15\text{ V}$, $V_O = 0.2\text{ V}$, $V_{id} = -1\text{ V}$		12	50		μA
V_{OH}	High-level output voltage	$V_{CC} = 30\text{ V}$, $R_L = 2\text{ k}\Omega$	25°C	26	27		V
			Full range	26			
		$V_{CC} = 30\text{ V}$, $R_L = 10\text{ k}\Omega$	25°C	27	28		
			Full range	27			
V_{OL}	Low-level output voltage	$R_L = 10\text{ k}\Omega$	25°C	5		20	mV
			Full range			20	
SR	Slew rate at unity gain	$V_{CC+} = 15\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $V_I = 0.5\text{ V}$ to 3 V , unity gain	25°C	0.2	0.4		V/ μs
GBW	Gain bandwidth product	$V_{CC+} = 30\text{ V}$, $V_I = 10\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 100\text{ kHz}$	25°C	0.5	0.9		MHz
THD	Total harmonic distortion	$V_{CC+} = 30\text{ V}$, $V_O = 2\text{ V}_{pp}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $A_V = 20\text{ dB}$	25°C	0.02%			
V_n	Equivalent input noise voltage	$V_{CC} = 30\text{ V}$, $R_S = 100\ \Omega$, $f = 1\text{ kHz}$	25°C	50			nV/ $\sqrt{\text{Hz}}$

(1) The input common-mode voltage of either input should not be allowed to go below -0.3 V . The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$, but either input can go to $V_{CC+} + 0.3\text{ V}$ (but $\leq 36\text{ V}$) without damage.

6.7 Voltage Reference, Electrical Characteristics

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT	
V _{REF}	Reference voltage	TL103W	I _K = 10 mA	25°C	2.482	2.5	2.518	V
				Full range	2.465		2.535	
		TL103WA	I _K = 10 mA	25°C	2.49	2.5	2.51	
				Full range	2.48		2.52	
ΔV _{REF}	Reference input voltage deviation over temperature range	V _{KA} = V _{REF} , I _K = 10 mA	Full range		7	30	mV	
I _{min}	Minimum cathode current for regulation	V _{KA} = V _{REF}	25°C		0.5	1	mA	
z _{ka}	Dynamic impedance ⁽¹⁾	V _{KA} = V _{REF} , ΔI _K = 1 mA to 100 mA, f < 1 kHz	25°C		0.2	0.5	Ω	

(1) The dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$.

6.8 Total Device, Electrical Characteristics

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
I _{CC}	Total supply current, excluding cathode-current reference	V _{CC+} = 5 V, No load	Full range		0.7	1.2	mA
		V _{CC+} = 30 V, No load				2	

7 Device and Documentation Support

7.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL103W	Click here	Click here	Click here	Click here	Click here
TL103WA	Click here	Click here	Click here	Click here	Click here

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

7.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

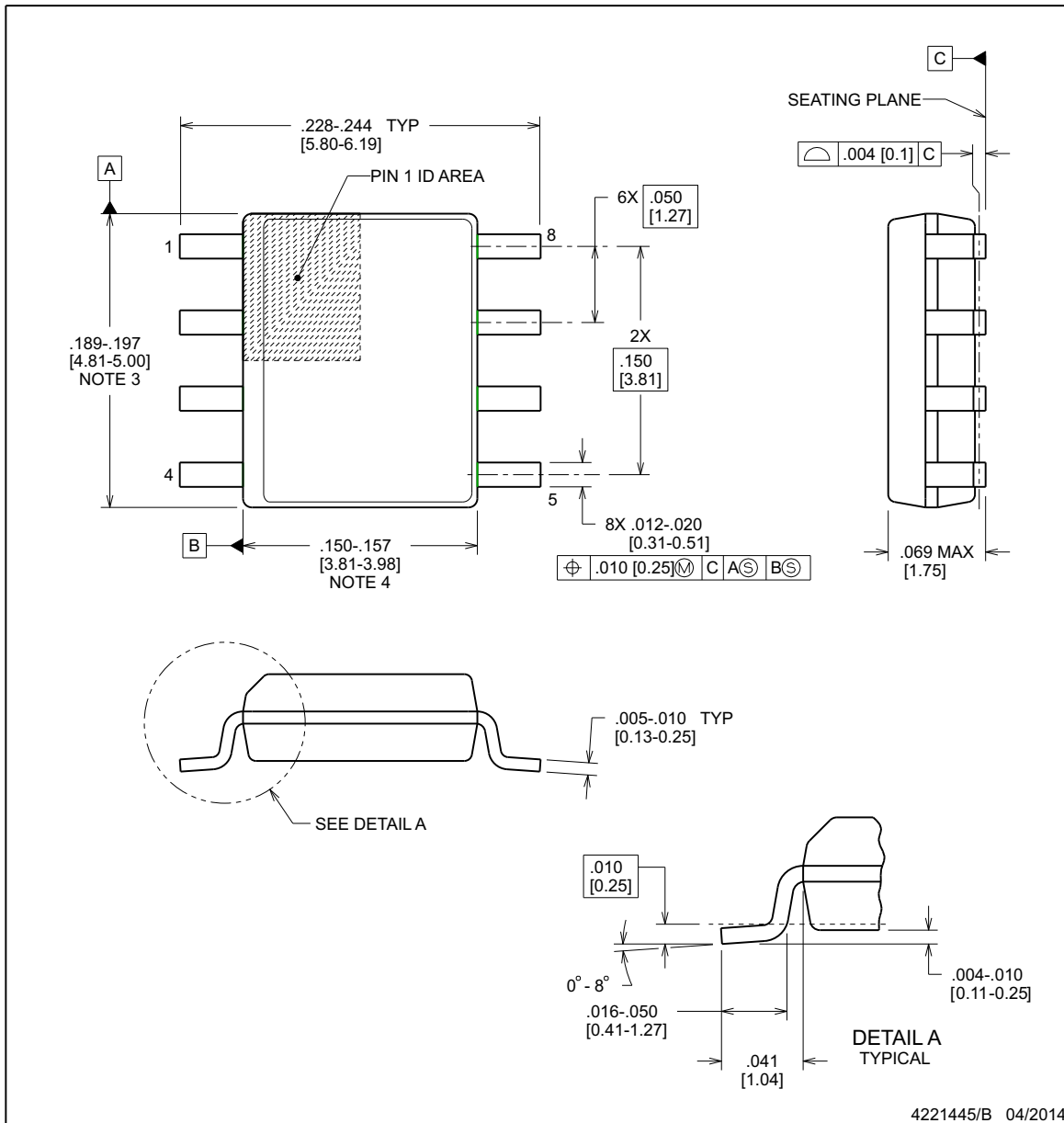
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



D0008B

PACKAGE OUTLINE
SOIC - 1.75 mm max height

SOIC



NOTES:

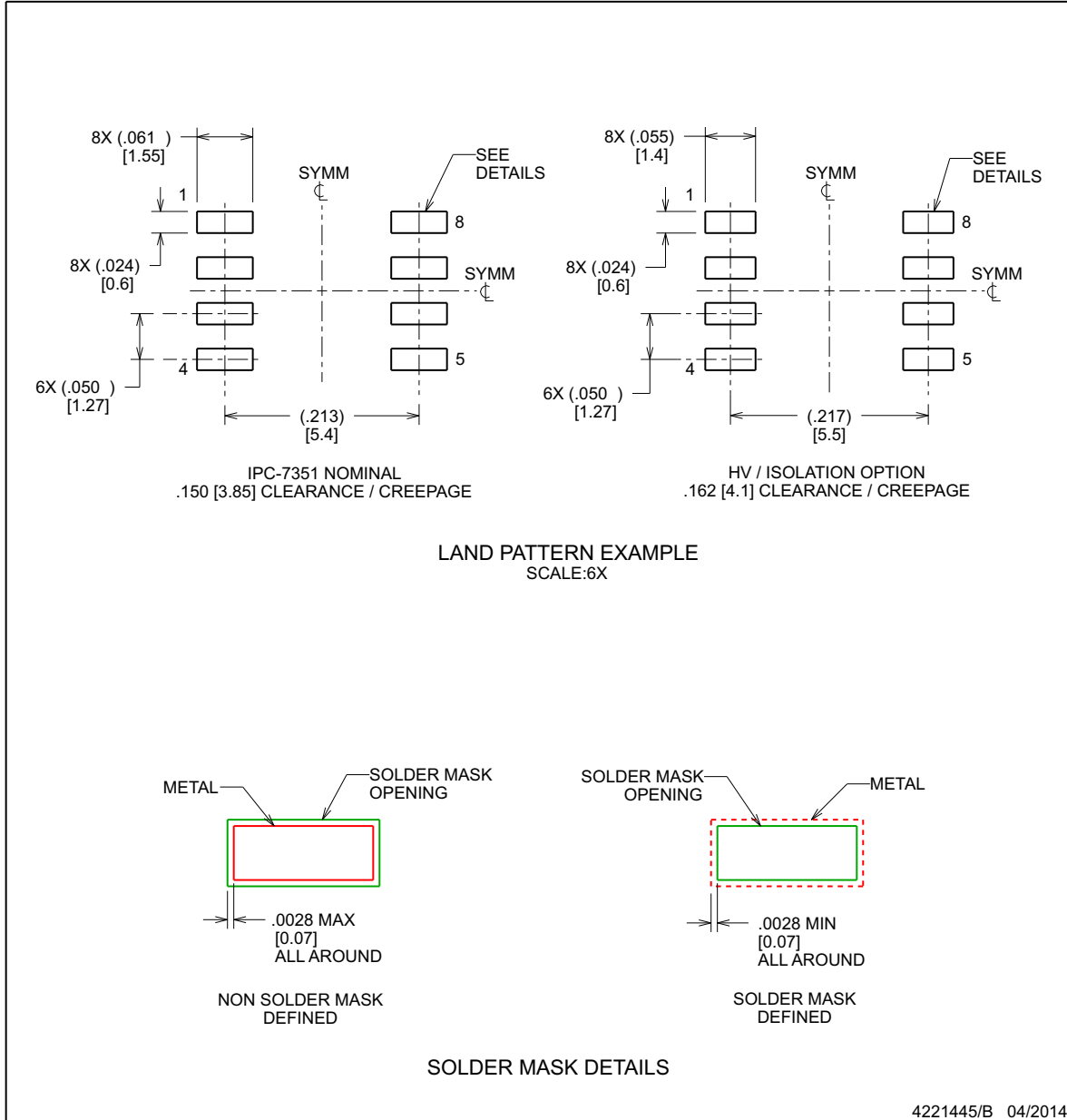
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

SOIC



NOTES: (continued)

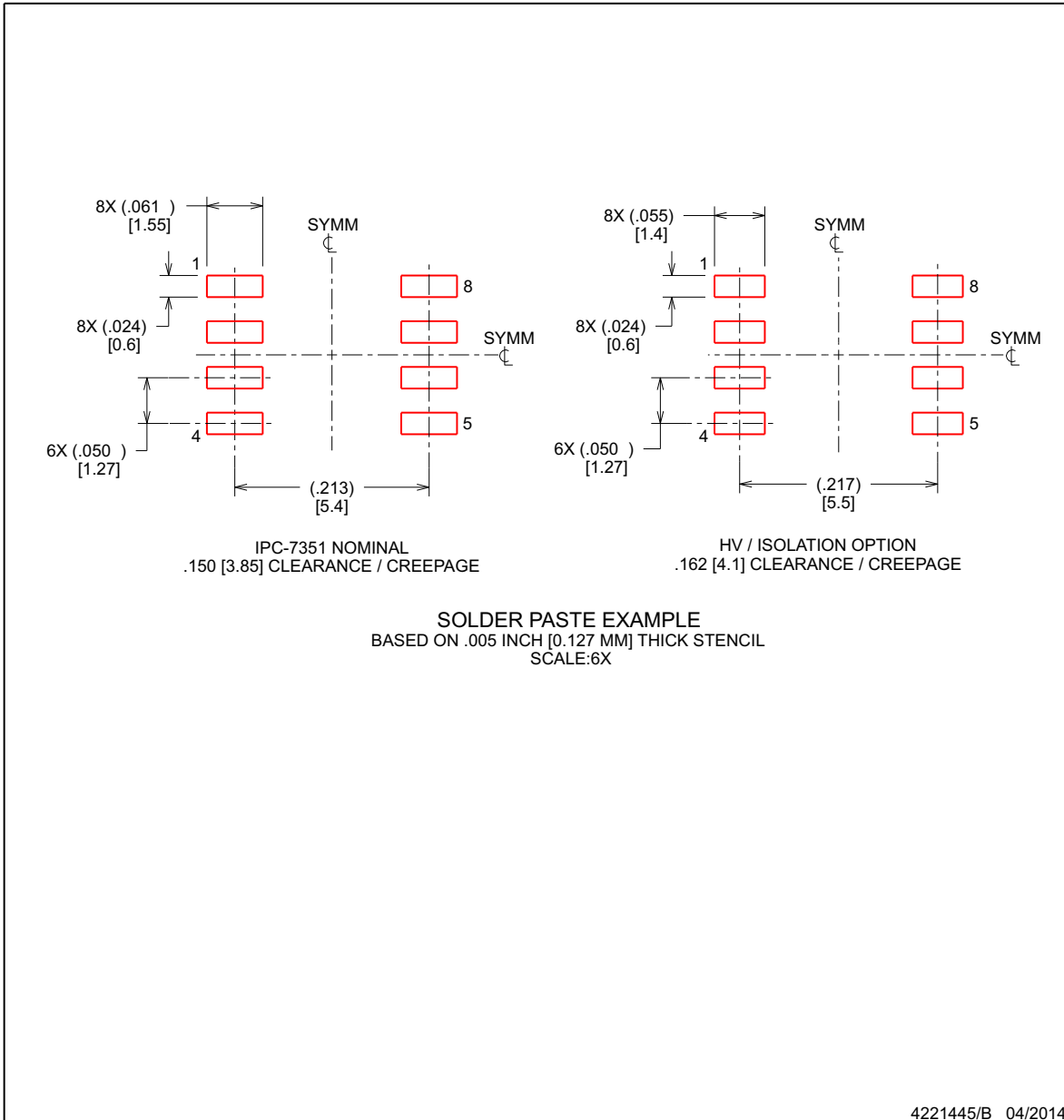
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B

SOIC - 1.75 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL103WAID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	Samples
TL103WAIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	Samples
TL103WID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples
TL103WIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples
TL103WIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples
TL103WIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL103WAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL103WAIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL103WIDR	SOIC	D	8	2500	340.5	338.1	20.6

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View TL103WAID](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management