THE DATASHEET OF

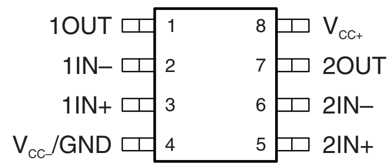
TL3472QDRQ1

HIGH-SLEW-RATE SINGLE-SUPPLY OPERATIONAL AMPLIFIER

FEATURES

- **Qualified for Automotive Applications**
- **Wide Gain-Bandwidth Product: 4 MHz**
- **High Slew Rate: 13 V/μs**
- **Fast Settling Time: 1.1 μs to 0.1%**
- **Wide-Range Single-Supply Operation: 4 V to 36 V**
- **Wide Input Common-Mode Range Includes Ground (V_{CC-})**
- **Low Total Harmonic Distortion: 0.02%**
- **Large-Capacitance Drive Capability: 10,000 pF**
- **Output Short-Circuit Protection**

D PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

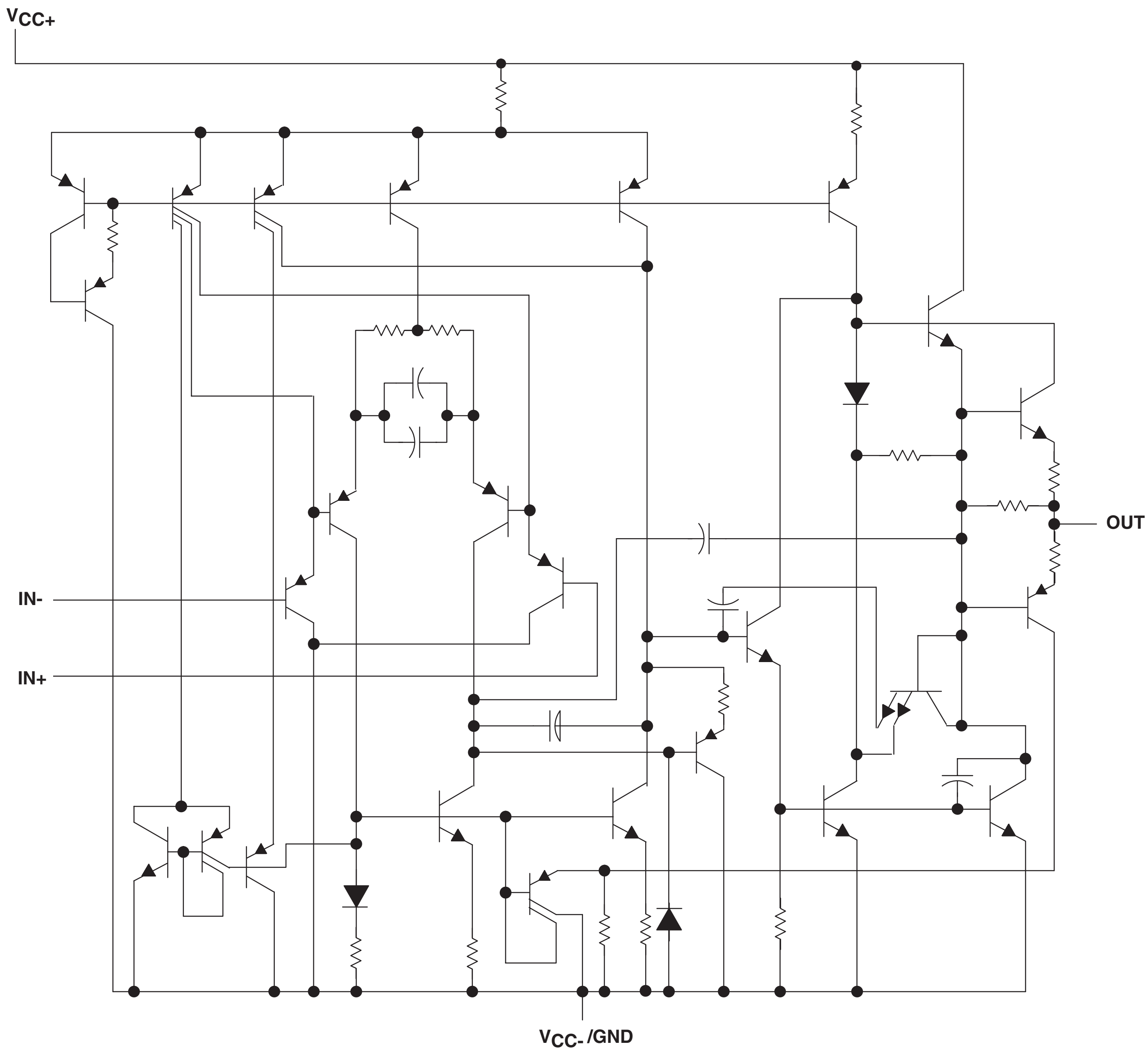
Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, 13-V/μs slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential (V_{CC-}). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	TL3472QDRQ1	T3472Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

SCHEMATIC (EACH AMPLIFIER)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{CC+}	Supply voltage(2)	18 V
V_{CC-}		–18 V
V_{ID}	Differential input voltage	±36 V
V_I	Input voltage (any input)	$V_{CC\pm}$
I_I	Input current (each input)	±1 mA
I_O	Output current	±80 mA
	Total current into V_{CC+}	80 mA
	Total current out of V_{CC-}	80 mA
	Duration of short-circuit current at (or below) 25°C(3)	Unlimited
θ_{JA}	Package thermal impedance(4)(5)	97°C/W
T_J	Operating virtual junction temperature	150°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
(4) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		4	36	V
V_{IC}	Common-mode input voltage	V_{CC} = 5 V	0	2.8	V
		$V_{CC\pm}$ = ±15 V	–15	12.8	
T_A	Operating free-air temperature		–40	125	°C

TEXAS INSTRUMENTS
www.ti.com

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

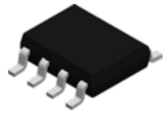
PARAMETER		TEST CONDITIONS		T_A(1)	MIN	TYP(2)	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	V_{CC} = 5 V	25°C		1.5	16	mV
			V_{CC} = ±15 V	25°C		1	17	
				Full range			22	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	V_{CC} = ±15 V	Full range		10		µV/°C
I_{IO}	Input offset current	V_{IC} = 0, V_O = 0, R_S = 50 Ω	V_{CC} = ±15 V	25°C		6	75	nA
				Full range			300	
I_{IB}	Input bias current	V_{IC} = 0, V_O = 0, R_S = 50 Ω	V_{CC} = ±15 V	25°C		100	500	nA
				Full range			700	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C		–15 to 12.8		V
				Full range		–15 to 12.8		
V_{OH}	High-level output voltage	V_{CC+} = 5 V, V_{CC-} = 0, R_L = 2 kΩ		25°C	3.7	4		V
		R_L = 10 kΩ		25°C	13.6	14		
		R_L = 2 kΩ		Full range	13.4			
V_{OL}	Low-level output voltage	V_{CC+} = 5 V, V_{CC-} = 0, R_L = 2 kΩ		25°C		0.1	0.3	V
		R_L = 10 kΩ		25°C		–14.7	–14.3	
		R_L = 2 kΩ		Full range			–13.5	
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		25°C	25	100		V/mV
				Full range	20			
I_{OS}	Short-circuit output current	Source: VID = 1 V, V_O = 0		25°C	–10	–34		mA
		Sink: VID = –1 V, V_O = 0			20	27		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min), R_S = 50 Ω		25°C	65	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±13.5 V to ±16.5 V, R_S = 100 Ω		25°C	70	97		dB
I_{CC}	Supply current (per channel)	V_O = 0, No load		25°C		3.5	4.5	mA
				Full range		4.5	5.5	
		V_{CC+} = 5 V, V_O = 2.5 V, V_{CC-} = 0, No load		25°C		3.5	4.5	

(1) Full range T_A = –40°C to 125°C
(2) All typical values are at T_A = 25°C.

OPERATING CHARACTERISTICS

$V_{CC\pm}$ = ±15 V, T_A = 25°C

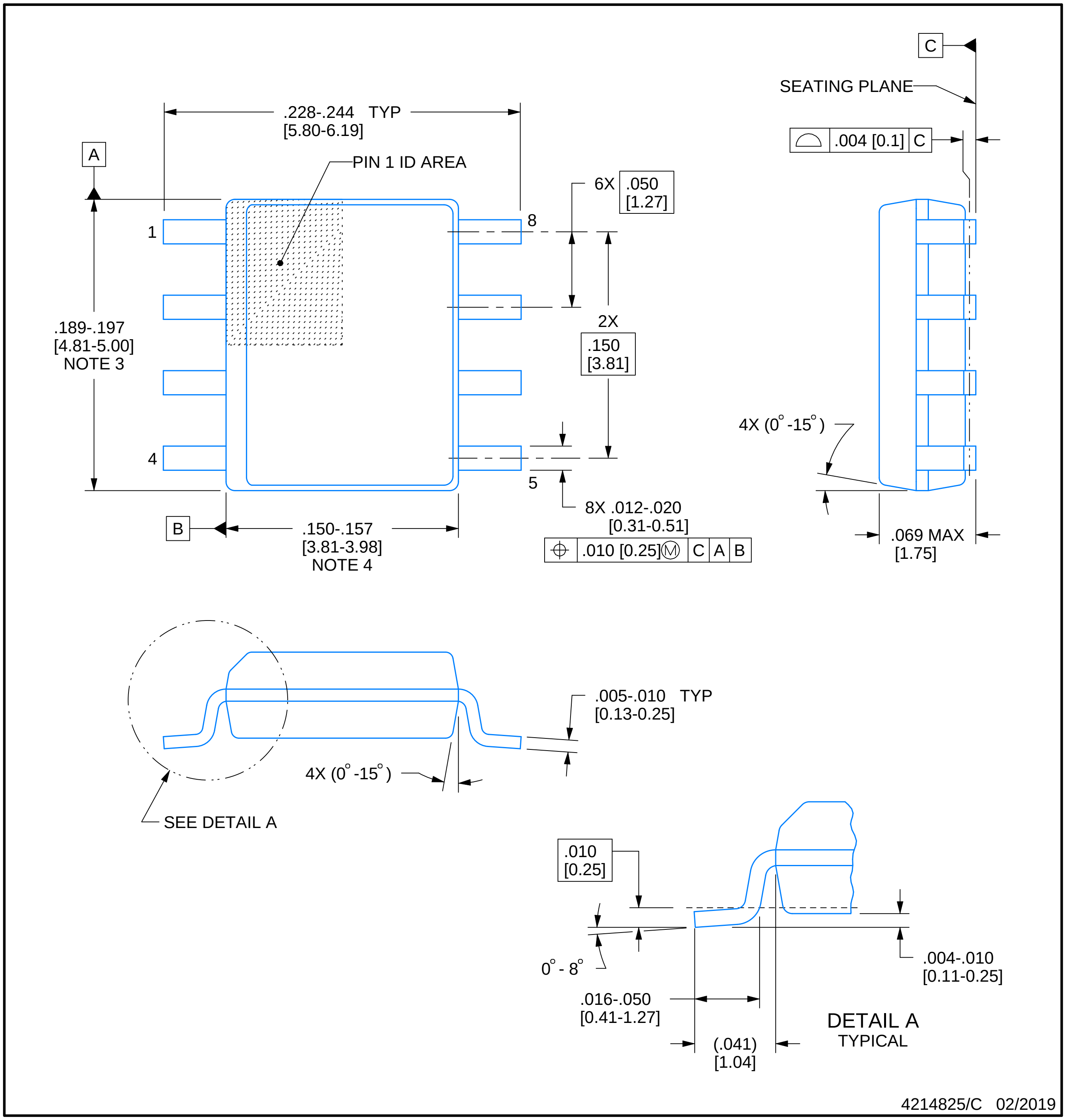
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	V_I = –10 V to 10 V, R_L = 2 kΩ, C_L = 300 pF	A_V = 1	8	10		V/µs
SR–	Negative slew rate	V_I = –10 V to 10 V, R_L = 2 kΩ, C_L = 300 pF	A_V = –1		13		V/µs
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		1.1		µs
			To 0.01%		2.2		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω			49		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.22		pA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V to 20 V, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz			0.02		%
GBW	Gain-bandwidth product	f =100 kHz		3	4		MHz
BW	Power bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 1, THD = 5.0%			160		kHz
ϕ_m	Phase margin	R_L = 2 kΩ	C_L = 0		70		deg
			C_L = 300 pF		50		
	Gain margin	R_L = 2 kΩ	C_L = 0		12		dB
			C_L = 300 pF		4		
r_i	Differential input resistance	V_{IC} = 0			150		MΩ
C_i	Input capacitance	V_{IC} = 0			2.5		pF
	Channel separation	f = 10 kHz			101		dB
z_o	Open-loop output impedance	f = 1 MHz, A_V = 1			20		Ω



PACKAGE OUTLINE

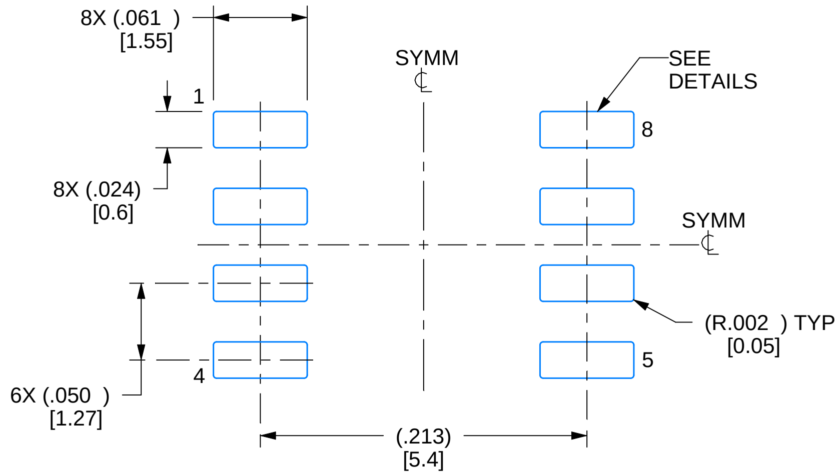
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

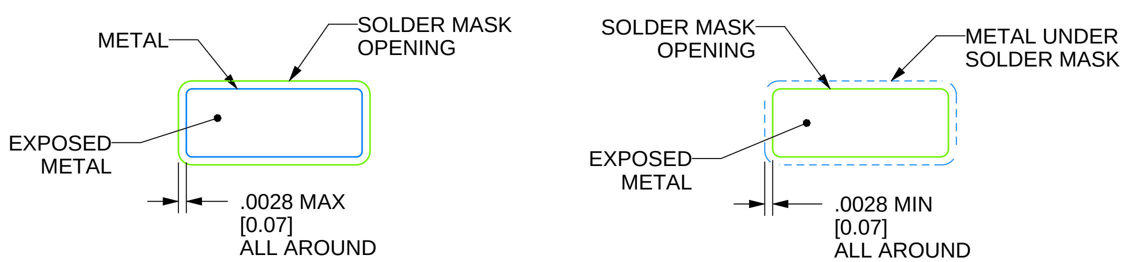


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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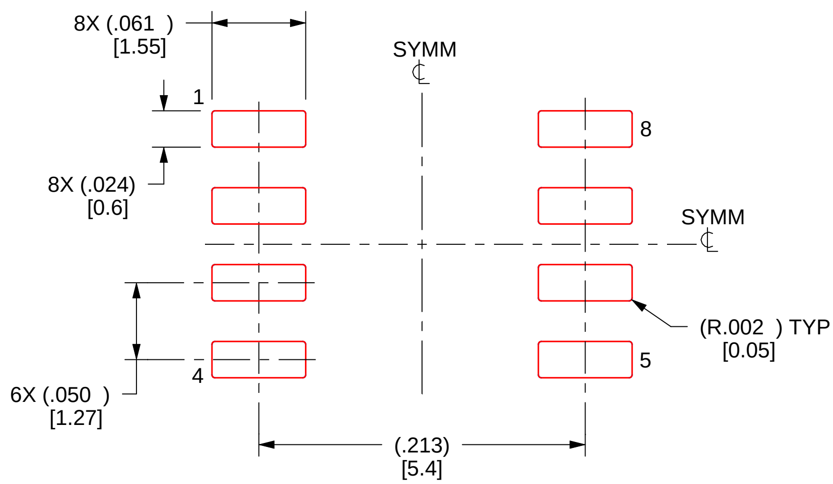
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.