WINSOURCE ELECTRONICS

THE DATASHEET OF

TLC1543CN

10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

FEATURES

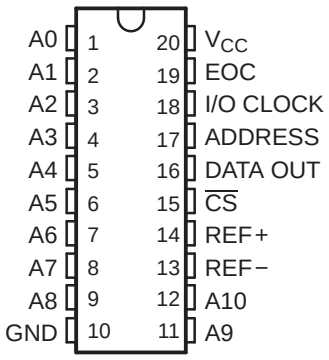
- **10-Bit Resolution A/D Converter**
- **11 Analog Input Channels**
- **Three Built-In Self-Test Modes**
- **Inherent Sample-and-Hold Function**
- **Total Unadjusted Error: ±1LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion (EOC) Output**
- **Terminal Compatible With TLC542**
- **CMOS Technology**

DESCRIPTION

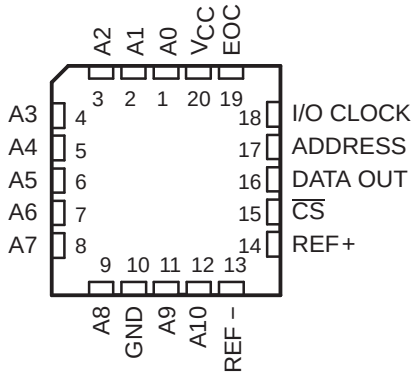
The TLC1542C, TLC1542I, TLC1542M, TLC1542Q, TLC1543C, TLC1543I, and TLC1543Q are CMOS 10-bit switched-capacitor successive-approximation analog-to-digital converters. These devices have three inputs and a 3-state output [chip select ($\overline{CS}$), input-output clock (I/O CLOCK), address input (ADDRESS), and data output (DATA OUT)] that provide a direct 4-wire interface to the serial port of a host processor. These devices allow high-speed data transfers from the host.

In addition to a high-speed A/D converter and versatile control capability, these devices have an on-chip 14-channel multiplexer that can select any one of 11 analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of A/D conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

DB, DW, J, OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)

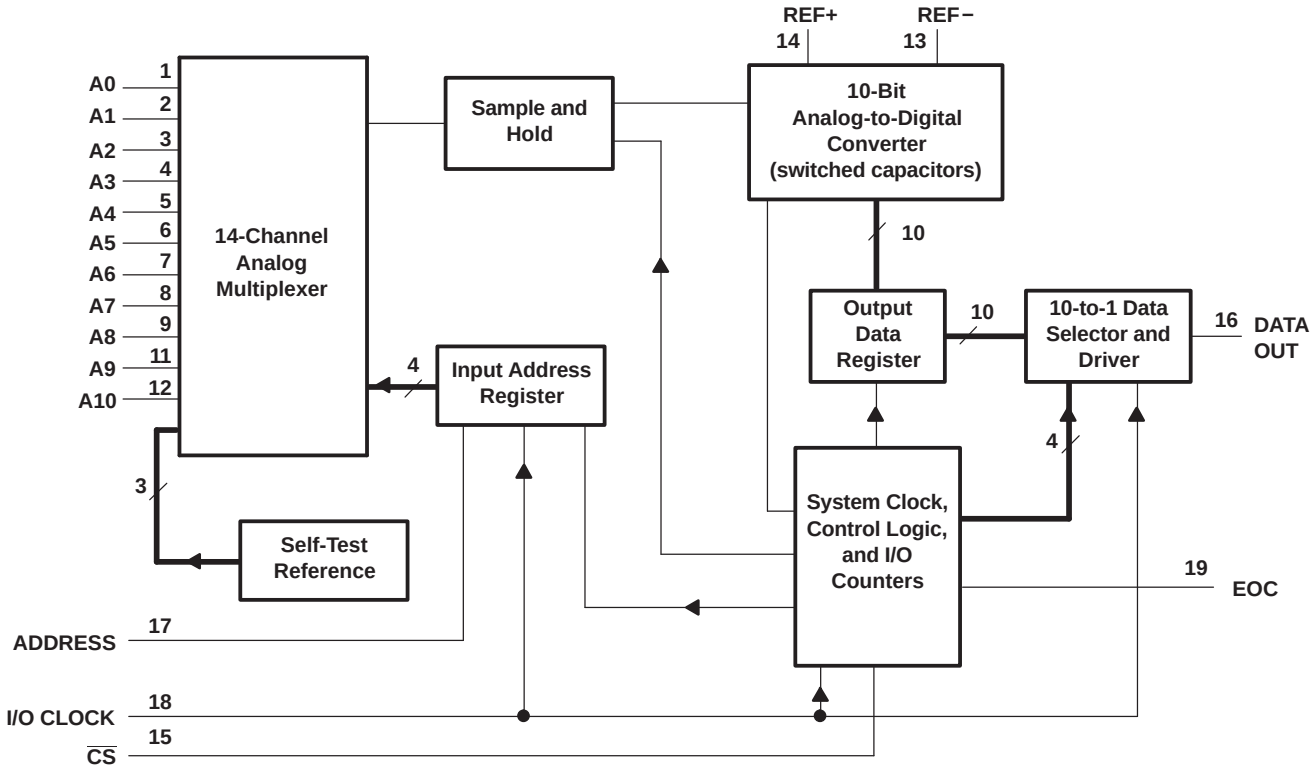


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

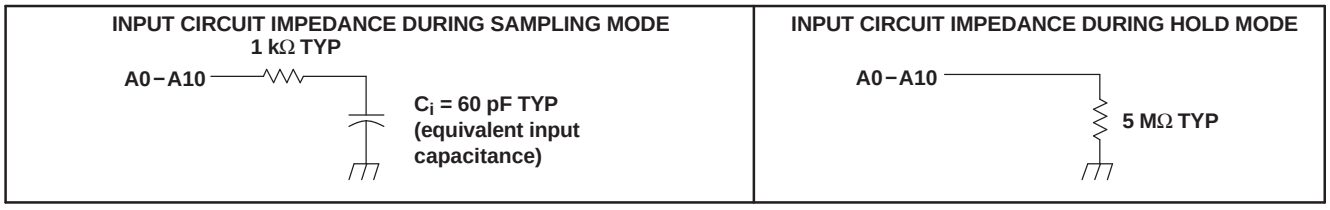
AVAILABLE OPTIONS

T_A	PACKAGE					
	SMALL OUTLINE (DB)	SMALL OUTLINE (DW)	CHIP CARRIER (FN)	PLASTIC DIP (N)	CHIP CARRIER (FK)	CERAMIC DIP (J)
0°C to 70°C		TLC1542CDW	TLC1542CFN	TLC1542CN		
	TLC1543CDB	TLC1543CDW	TLC1543CFN	TLC1543CN		
-40°C to 85°C		TLC1542IDW	TLC1542IFN	TLC1542IN		
	TLC1543IDB	TLC1543IDW	TLC1543IFN	TLC1543IN		
-40°C to 125°C			TLC1542QFN			
	TLC1543QDB	TLC1543QDW	TLC1543QFN			
-55°C to 125°C					TLC1542MFK	TLC1542MJ

FUNCTIONAL BLOCK DIAGRAM



TYPICAL EQUIVALENT INPUTS



TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDRESS	17	I	Serial address input. A 4-bit serial address selects the desired analog input or test voltage that is to be converted next. The address data is presented with the MSB first and shifts in on the first four rising edges of I/O CLOCK. After the four address bits have been read into the address register, this input is ignored for the remainder of the current conversion period.
A0-A10	1-9, 11, 12	I	Analog signal inputs. The 11 analog inputs are applied to these terminals and are internally multiplexed. The driving source impedance should be less than or equal to 1 kΩ.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on this input resets the internal counters and controls and enables DATA OUT, ADDRESS, and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables ADDRESS and I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. This output is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives this output to the logic level corresponding to the next most significant bit, and the remaining bits shift out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
EOC	19	O	End of conversion. This output goes from a high to a low logic level on the trailing edge of the tenth I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10	I	The ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to this terminal.
I/O CLOCK	18	I	Input/output clock. This terminal receives the serial I/O CLOCK input and performs the following four functions: 1) It clocks the four input address bits into the address register on the first four rising edges of the I/O CLOCK with the multiplex address available after the fourth rising edge. 2) On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 3) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 4) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF+	14	I	The upper reference voltage value (nominally V_{CC}) is applied to this terminal. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF- terminal.
REF-	13	I	The lower reference voltage value (nominally ground) is applied to this terminal.
V_{CC}	20	I	Positive supply voltage

DETAILED DESCRIPTION

With chip select ($\overline{CS}$) inactive (high), the ADDRESS and I/O CLOCK inputs are initially disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{CS}$ active (low), the conversion sequence begins with the enabling of I/O CLOCK and ADDRESS and the removal of DATA OUT from the high-impedance state. The serial interface then provides the 4-bit channel address to ADDRESS and the I/O CLOCK sequence to I/O CLOCK. During this transfer, the serial interface also receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first four I/O clocks load the address register with the 4-bit address on ADDRESS, selecting the desired analog channel, and the next six clocks providing the control timing for sampling the analog input.

There are six basic serial-interface timing modes that can be used with the device. These modes are determined by the speed of I/O CLOCK and the operation of $\overline{CS}$ as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, (2) a fast mode with a 10-clock transfer and $\overline{CS}$ active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, (4) a fast mode with a 16-clock transfer and $\overline{CS}$ active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and $\overline{CS}$ inactive (high) between conversion cycles, and (6) a slow mode with a 16-clock transfer and $\overline{CS}$ active (low) continuously.

The MSB of the previous conversion appears at DATA OUT on the falling edge of $\overline{CS}$ in mode 1, mode 3, and mode 5, on the rising edge of EOC in mode 2 and mode 4, and following the sixteenth clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host-serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the EOC output goes low and returns to the high logic level when conversion is complete and the result can be read by the host. Also, on the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero when the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of $\overline{CS}$, the number of I/O serial transfer clocks that can be used, and the timing edge on which the MSB of the previous conversion appears at the output.

Table 1. MODE OPERATION

MODES		$\overline{CS}$	NO. OF 1/O CLOCK	MSB AT DATA OUT(1)	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	$\overline{CS}$ falling edge	Figure 9
	Mode 2	Low continuously	10	EOC rising edge	Figure 10
	Mode 3	High between conversion cycles	11 TO 16(2)	$\overline{CS}$ falling edge	Figure 11
	Mode 4	Low continuously	16(2)	EOC rising edge	Figure 12
Slow Modes	Mode 5	High between conversion cycles	11 to 16(3)	$\overline{CS}$ falling edge	Figure 13
	Mode 6	Low continuously	16(3)	16th clock falling edge	Figure 14

(1) These edges also initiate serial-interface communication.
(2) No more than 16 clocks should be used.
(3) No more than 16 clocks should be used.

FAST MODES

The device is in a fast mode when the serial I/O CLOCK data transfer is completed before the conversion is completed. With a 10-clock serial transfer, the device can only run in a fast mode since a conversion does not begin until the falling edge of the tenth I/O CLOCK.

MODE 1: FAST MODE, $\overline{CS}$ INACTIVE (HIGH) BETWEEN CONVERSION CYCLES, 10-CLOCK TRANSFER

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

MODE 2: FAST MODE, $\overline{CS}$ ACTIVE (LOW) CONTINUOUSLY, 10-CLOCK TRANSFER

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

MODE 3: FAST MODE, $\overline{CS}$ INACTIVE (HIGH) BETWEEN CONVERSION CYCLES, 11- to 16-CLOCK TRANSFER

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers, and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

MODE 4: FAST MODE, $\overline{CS}$ ACTIVE (LOW) CONTINUOUSLY, 16-CLOCK TRANSFER

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions; the rising edge of EOC then begins each sequence by removing DATA OUT from the low logic level, allowing the MSB of the previous conversion to appear immediately on this output.

SLOW MODES

In a slow mode, the conversion is completed before the serial I/O CLOCK data transfer is completed. A slow mode requires a minimum 11-clock transfer into I/O CLOCK, and the rising edge of the eleventh clock must occur before the conversion period is complete; otherwise, the device loses synchronization with the host-serial interface and $\overline{CS}$ has to be toggled to initialize the system. The eleventh rising edge of the I/O CLOCK must occur within 9.5 μs after the tenth I/O clock falling edge.

MODE 5: SLOW MODE, $\overline{CS}$ INACTIVE (HIGH) BETWEEN CONVERSION CYCLES, 11- to 16-CLOCK TRANSFER

In this mode, $\overline{CS}$ is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of $\overline{CS}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{CS}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{CS}$ disables the I/O CLOCK and ADDRESS terminals within a setup time plus two falling edges of the internal system clock.

MODE 6: SLOW MODE, $\overline{CS}$ ACTIVE (LOW) CONTINUOUSLY, 16-CLOCK TRANSFER

In this mode, $\overline{CS}$ is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle, $\overline{CS}$ is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16-clock transfer initiated by the serial interface.

ADDRESS BITS

The 4-bit analog channel-select address for the next conversion cycle is presented to the ADDRESS terminal (MSB first) and is clocked into the address register on the first four leading edges of I/O CLOCK. This address selects one of 14 inputs (11 analog inputs or three internal test inputs).

ANALOG INPUTS AND TEST MODES

The 11 analog inputs and the three internal test inputs are selected by the 14-channel multiplexer according to the input address as shown in Tables 2 and 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK, and sampling continues for six I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK. The three test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs.

Table 2. ANALOG-CHANNEL-SELECT ADDRESS

ANALOG INPUT SELECTED	VALUE SHIFTED INTO ADDRESS INPUT	
	BINARY	HEX
A0	0000	0
A1	0001	1
A2	0010	2
A3	0011	3
A4	0100	4
A5	0101	5
A6	0110	6
A7	0111	7
A8	1000	8
A9	1001	9
A10	1010	A

Table 3. TEST-MODE-SELECT ADDRESS

INTERNAL SELF-TEST VOLTAGE SELECTED(1)	VALUE SHIFTED INTO ADDRESS INPUT		OUTPUT RESULT (HEX)(2)
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

(1) V_{ref+} is the voltage applied to the REF+ input, and V_{ref-} is the voltage applied to the REF- input.
(2) The output results shown are the ideal values and vary with the reference stability and with internal offsets.

CONVERTER AND ANALOG INPUT

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF-) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF-. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a 0 bit is placed in the output register and the 512-weight capacitor is switched to REF-. If the voltage at the summing node is less than the trip point of the threshold detector, a 1 bit is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

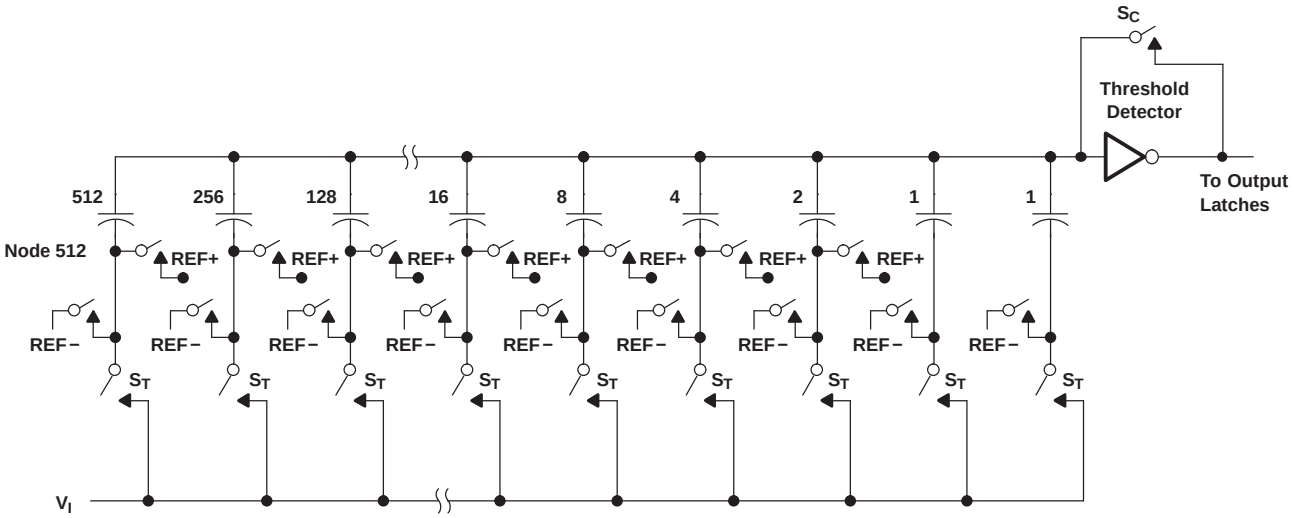


Figure 1. Simplified Model of the Successive-Approximation System

CHIP-SELECT OPERATION

The trailing edge of $\overline{CS}$ starts all modes of operation, and $\overline{CS}$ can abort a conversion sequence in any mode. A high-to-low transition on $\overline{CS}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Exercise care to prevent $\overline{CS}$ from being taken low close to completion of conversion because the output data can be corrupted.

REFERENCE VOLTAGE INPUTS

There are two reference inputs used with the device: REF+ and REF-. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading respectively. The values of REF+, REF-, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF-.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC}, see (2)	Supply voltage range		-0.5 V to 6.5 V
V_I	Input voltage range		-0.3 V to V_{CC} + 0.3 V
V_O	Output voltage range		-0.3 V to V_{CC} + 0.3 V
V_{ref+}	Positive reference voltage		V_{CC} + 0.1 V
V_{ref-}	Negative reference voltage		-0.1 V
	Peak input current (any input)		±20 mA
	Peak total input current (all inputs)		±30 mA
T_A	Operating free-air temperature range	TLC1542C, TLC1543C	0°C to 70°C
		TLC1542I, TLC1543I	-40°C to 85°C
		TLC1542Q, TLC1543Q	-40°C to 125°C
		TLC1542M	-55°C to 125°C
T_{stg}	Storage temperature range,		-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds		260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to digital ground with REF- and GND wired together (unless otherwise noted).

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{ref+}, see (1)	Positive reference voltage			V_{CC}		V
V_{ref-}, see (1)	Negative reference voltage			0		V
V_{ref+}-V_{ref-}, see (1)	Differential reference voltage		2.5	V_{CC}	V_{CC}+0.2	V
	Analog input voltage ,see (1)		0		V_{CC}	V
V_{IH}	High-level control input voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level control input voltage	V_{CC} = 4.5 V to 5.5 V			0.8	V
$t_{su(A)}$, see Figure 4	Setup time, address bits at data input before I/O CLOCK↑		100			ns
$t_{h(A)}$, see Figure 4	Hold time, address bits after I/O CLOCK↑		0			ns
$t_{h(CS)}$, see Figure 5	Hold time, $\overline{CS}$ low after last I/O CLOCK↓		0			ns
$t_{su(CS)}$, see (2) and Figure 5	Setup time, $\overline{CS}$ low before clocking in first address bit		1.425			µs
	Clock frequency at I/O CLOCK, see (3)		0		2.1	MHz
$t_{wH(I/O)}$	Pulse duration, I/O CLOCK high,		190			ns
$t_{wL(I/O)}$	Pulse duration, I/O CLOCK low,		190			ns
$t_{t(I/O)}$, see (4) and Figure 6	Transition time, I/O CLOCK,				1	µs
$t_{t(CS)}$	Transition time, ADDRESS and $\overline{CS}$,				10	µs

(1) Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V (V_{ref+} - V_{ref-}); however, the electrical specifications are no longer applicable.
(2) To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}$↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.
(3) For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge (≤ 2 V) at least 1 I/O CLOCK rising edge (≥ 2 V) must occur within 9.5 µs.
(4) This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

RECOMMENDED OPERATING CONDITIONS (continued)

			MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature,	TLC1542C, TLC1543C	0		70	°C
		TLC1542I, TLC1543I	-40		85	
		TLC1542Q, TLC1543Q	-40		125	
		TLC1542M	-55		125	

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = V_{ref+} = 4.5 V to 5.5 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_{OH} = -1.6 mA	2.4			V
			V_{CC} = 4.5 V to 5.5 V,	I_{OH} = -20 µA	V_{CC}-0.1			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 20 µA			0.1	
I_{OZ}	Off-state (high-impedance-state) output current		V_O = V_{CC},	$\overline{CS}$ at V_{CC}			10	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}			-10	
I_{IH}	High-level input current		V_I = V_{CC}			0.005	2.5	µA
I_{IL}	Low-level input current		V_I = 0			0.005	-2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			0.8	2.5	mA
	Selected channel leakage current TLC1542/TLC1543 C, I, or Q		Selected channel at V_{CC},	Unselected channel at 0 V			1	µA
			Selected channel at 0 V,	Unselected channel at V_{CC}			-1	
	Selected channel leakage current TLC1542M		Selected channel at V_{CC}, T_A= 25°C	Unselected channel at 0 V,			1	µA
			Selected channel at 0 V, T_A = 25°C	Unselected channel at V_{CC},			-1	
			Selected channel at V_{CC},	Unselected channel at 0 V			2.5	
			Selected channel at 0 V,	Unselected channel at V_{CC}			-2.5	
	Maximum static analog reference current into REF+		V_{ref+} = V_{CC},	V_{ref-} = GND			10	µA
C_i	Input capacitance	Analog inputs				7		pF
		Control inputs				5		

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

OPERATING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = V_{ref+} = 4.5 V to 5.5 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
E_L	Linearity error, see (2)	TLC1542C, I, or Q			±0.5	LSB
		TLC1543C, I, or Q			±1	LSB
		TLC1542M			±1	LSB

(1) All typical values are at T_A = 25°C.
(2) Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.

OPERATING CHARACTERISTICS (continued)

over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 4.5$ V to 5.5 V, I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)

			TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
E_{ZS}	Zero-scale error, see (3)	TLC1542C, I, or Q	See (4)			±1	LSB
		TLC1543C, I, or Q	See (4)			±1	LSB
		TLC1542M	See (4)			±1	LSB
E_{FS}	Full-scale error, see (3)	TLC1542C, I, or Q	See (4)			±1	LSB
		TLC1543C, I, or Q	See (4)			±1	LSB
		TLC1542M	See (4)			±1	LSB
	Total unadjusted error, see (5)	TLC1542C, I, or Q				±1	LSB
		TLC1543C, I, or Q				±1	LSB
		TLC1542M				±1	LSB
	Self-test output code, see Table 3 and (6)		ADDRESS = 1011		512		
			ADDRESS = 1100		0		
			ADDRESS = 1101		1023		
t_{conv}	Conversion time		See timing diagrams			21	µs
t_c	Total cycle time (access, sample, and conversion)		See timing diagrams and (7)			21 +10 I/O CLOCK periods	µs
t_{acq}	Channel acquisition time (sample)		See timing diagrams and (7)			6	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓		See Figure 6	10			ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid		See Figure 6			240	ns
$t_{d(I/O-EOC)}$	Delay time, tenth I/O CLOCK↓ to EOC↓		See Figure 7		70	240	ns
$t_{d(EOC-DATA)}$	Delay time, EOC↑ to DATA OUT (MSB)		See Figure 8			100	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB driven)		See Figure 3			1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)		See Figure 3			150	ns
$t_{r(EOC)}$	Rise time, EOC		See Figure 8			300	ns
$t_{f(EOC)}$	Fall time, EOC		See Figure 7			300	ns
$t_{r(DATA)}$	Rise time, data bus		See Figure 6			300	ns
$t_{f(DATA)}$	Fall time, data bus		See Figure 6			300	ns
$t_{d(I/O-CS)}$	Delay time, tenth I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note (8))					9	µs

(3) Zero-scale error is the difference between 0000000000 and the converted output for zero input voltage; full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
(4) Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V (V_{ref+}-V_{ref-}); however, the electrical specifications are no longer applicable.
(5) Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
(6) Both the input address and the output codes are expressed in positive logic.
(7) I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 6)
(8) Any transitions of $\overline{CS}$ are recognized as valid only if the level is maintained for a setup time plus two falling edges of the internal clock (1.425 µs) after the transition.

PARAMETER MEASUREMENT INFORMATION

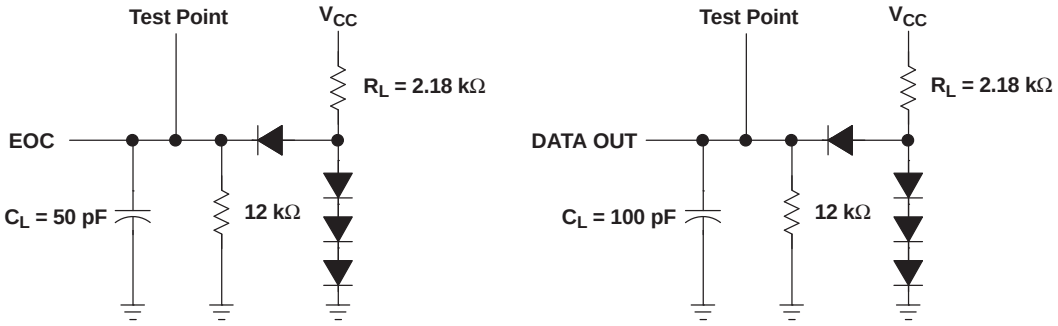


Figure 2. Load Circuits

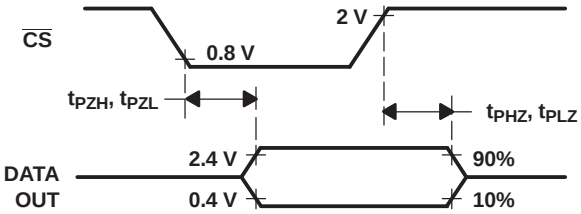


Figure 3. DATA OUT Enable and Disable Voltage Waveforms

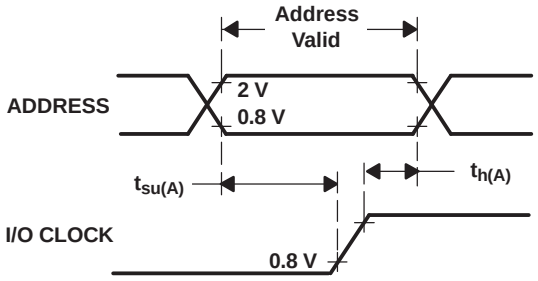


Figure 4. ADDRESS Setup and Hold Time Voltage Waveforms

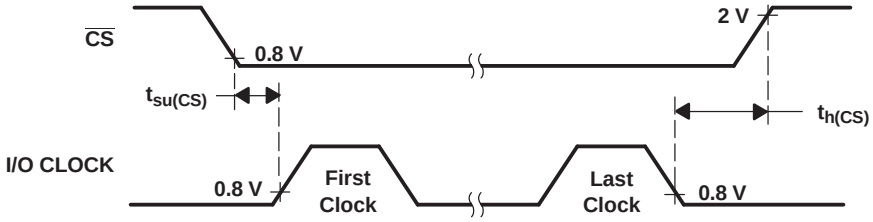


Figure 5. I/O CLOCK Setup and Hold Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

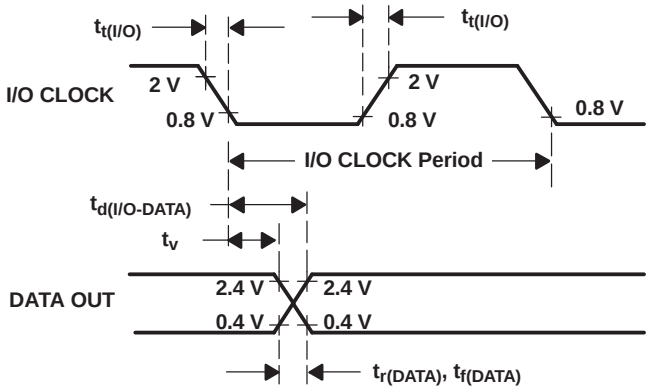


Figure 6. I/O CLOCK and DATA OUT Voltage Waveforms

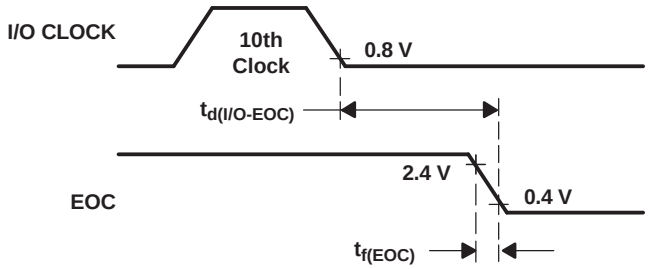


Figure 7. I/O CLOCK and EOC Voltage Waveforms

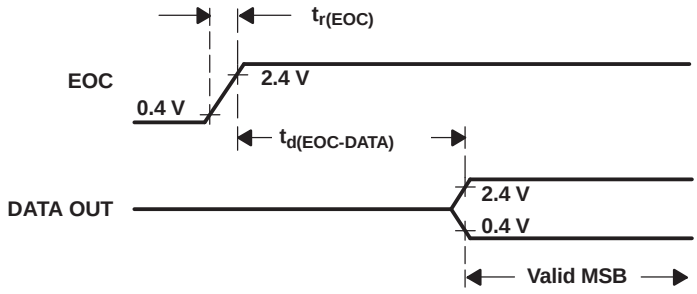
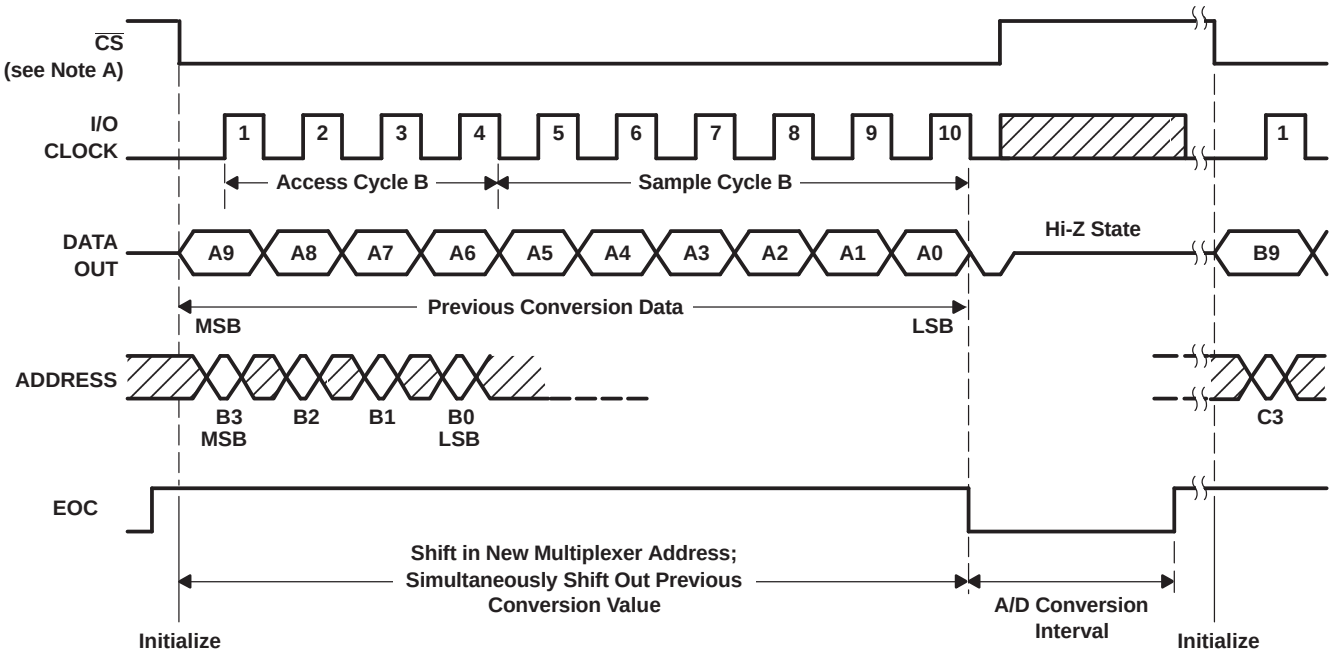


Figure 8. EOC and DATA OUT Voltage Waveforms

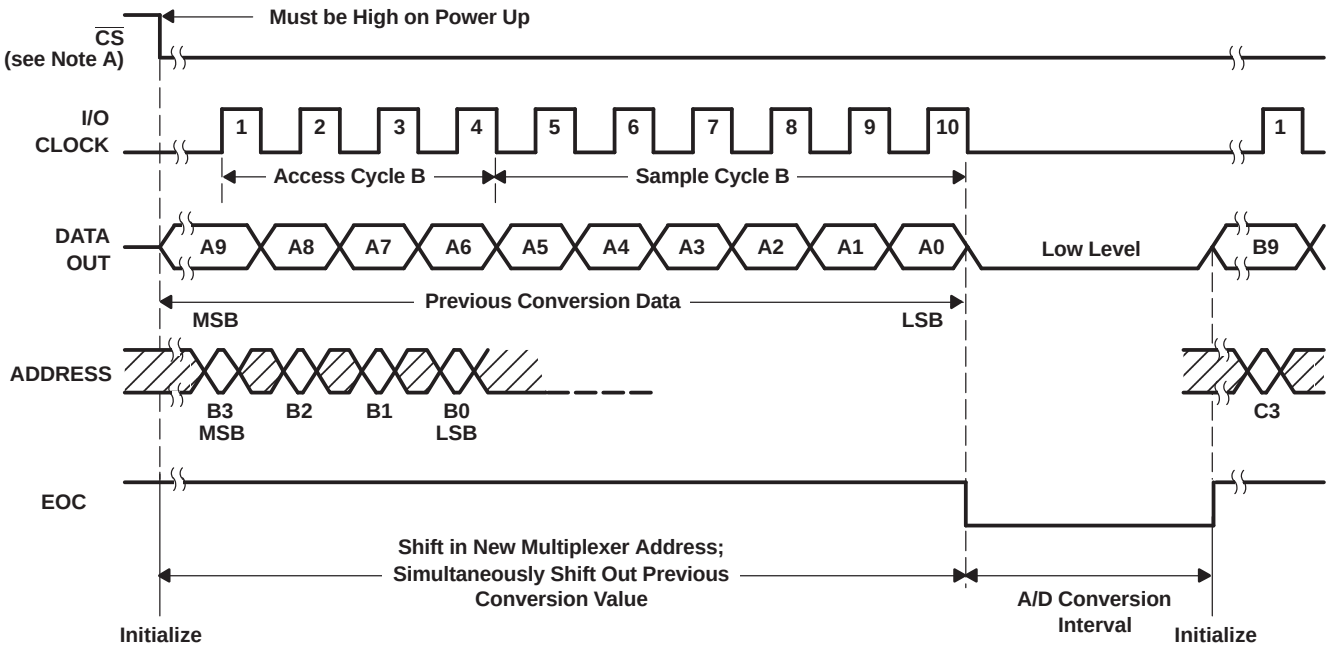
PARAMETER MEASUREMENT INFORMATION (continued)

TIMING DIAGRAMS



A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

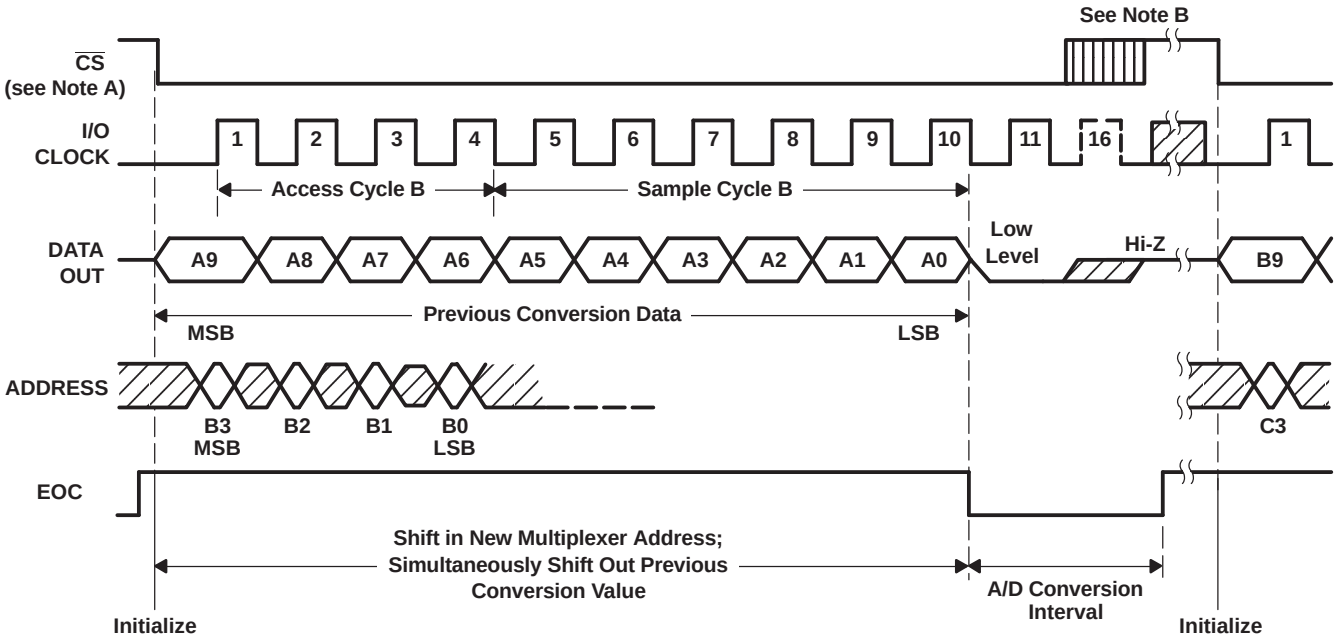
Figure 9. Timing for 10-Clock Transfer Using $\overline{CS}$



A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 10. Timing for 10-Clock Transfer Not Using $\overline{CS}$

PARAMETER MEASUREMENT INFORMATION (continued)

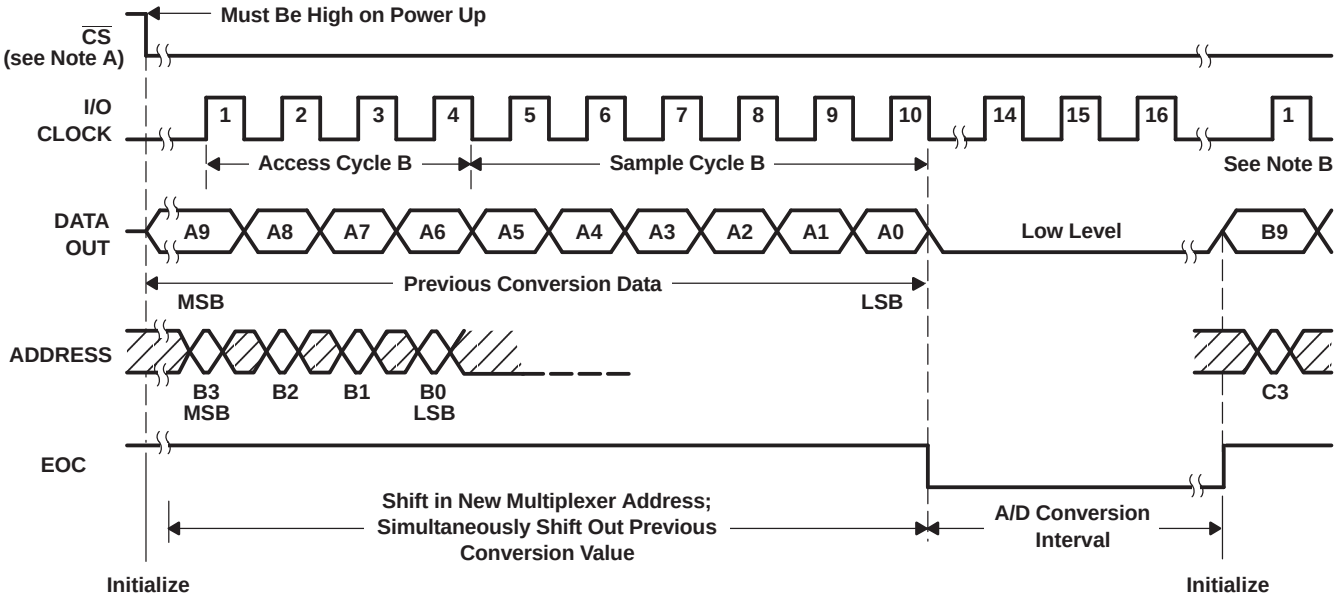


A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. A low-to-high transition of $\overline{CS}$ disables ADDRESS and the I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.

Figure 11. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

PARAMETER MEASUREMENT INFORMATION (continued)

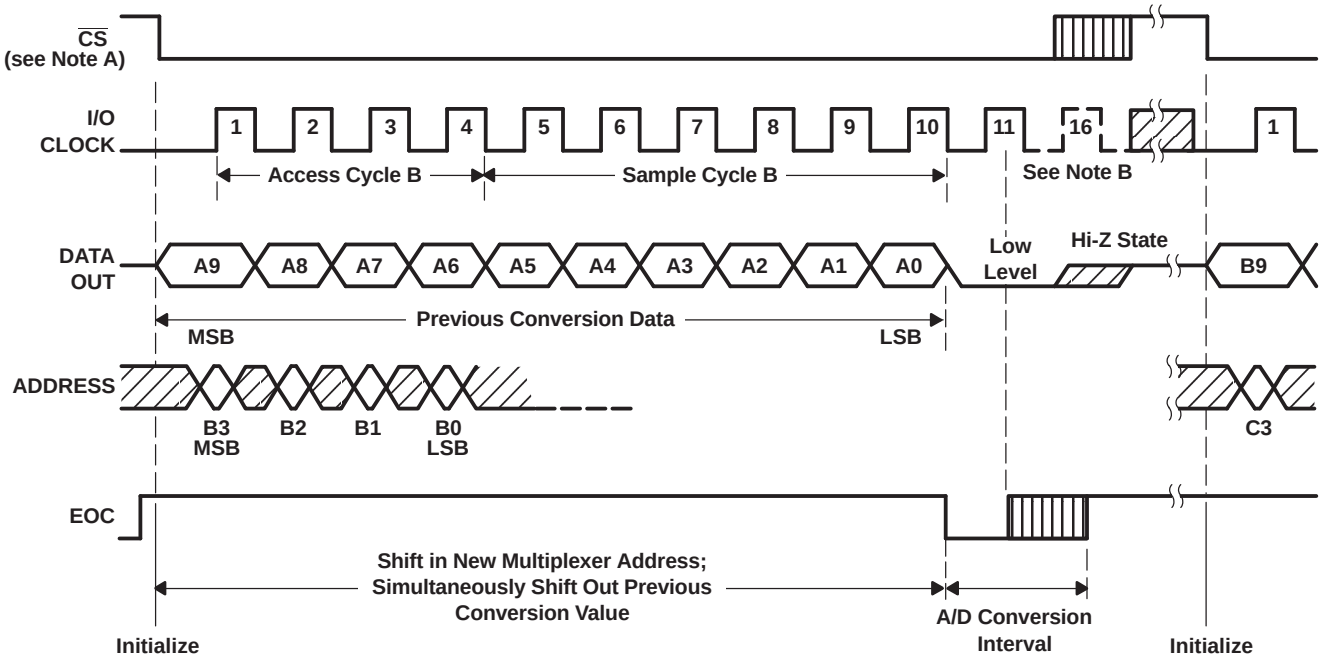


A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The first I/O CLOCK must occur after the rising edge of EOC.

Figure 12. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Shorter Than Conversion)

PARAMETER MEASUREMENT INFORMATION (continued)

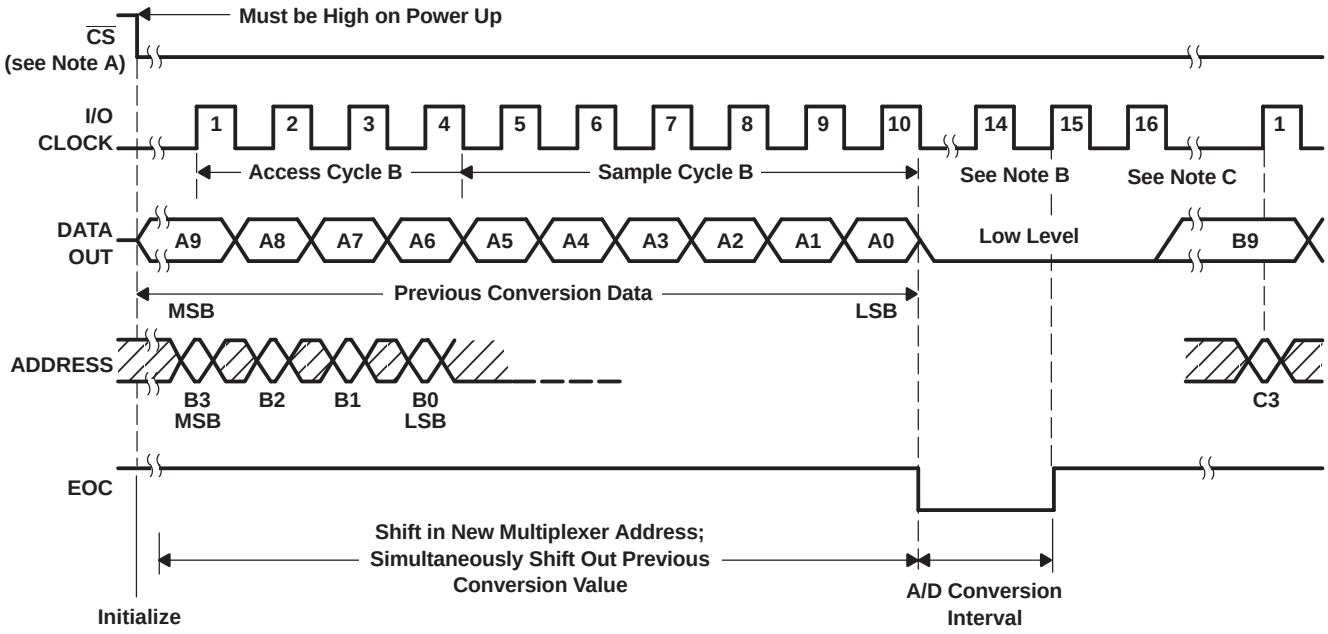


A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

Figure 13. Timing for 11- to 16-Clock Transfer Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

PARAMETER MEASUREMENT INFORMATION (continued)



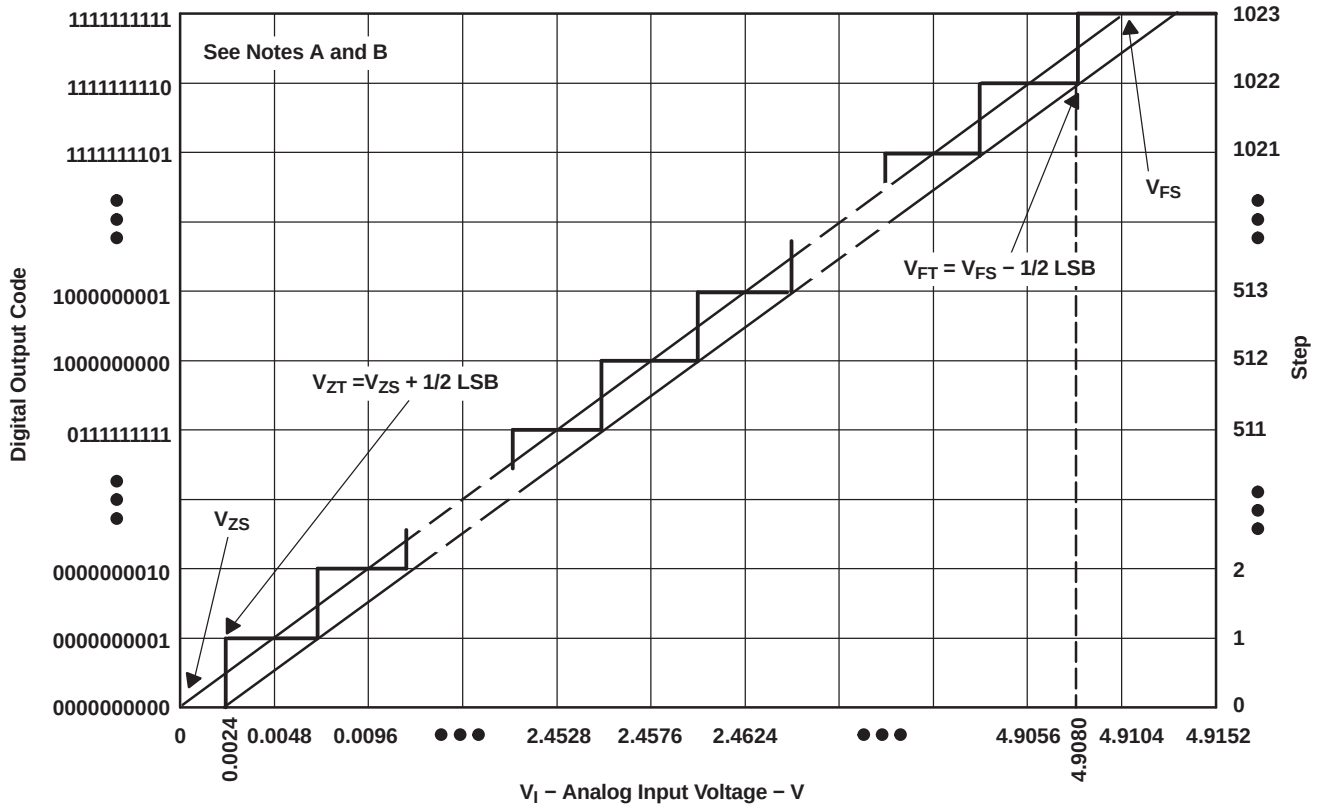
A. A. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal system clock after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

B. The 11th rising edge of the I/O CLOCK sequence must occur before the conversion is complete to prevent losing serial interface synchronization.

C. C. The I/O CLOCK sequence is exactly 16 clock pulses long.

Figure 14. Timing for 16-Clock Transfer Not Using $\overline{CS}$ (Serial Transfer Interval Longer Than Conversion)

APPLICATION INFORMATION



A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0024 V and the transition to full scale (V_{FT}) is 4.908 V. 1 LSB = 4.8 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 15. Ideal Conversion Characteristics

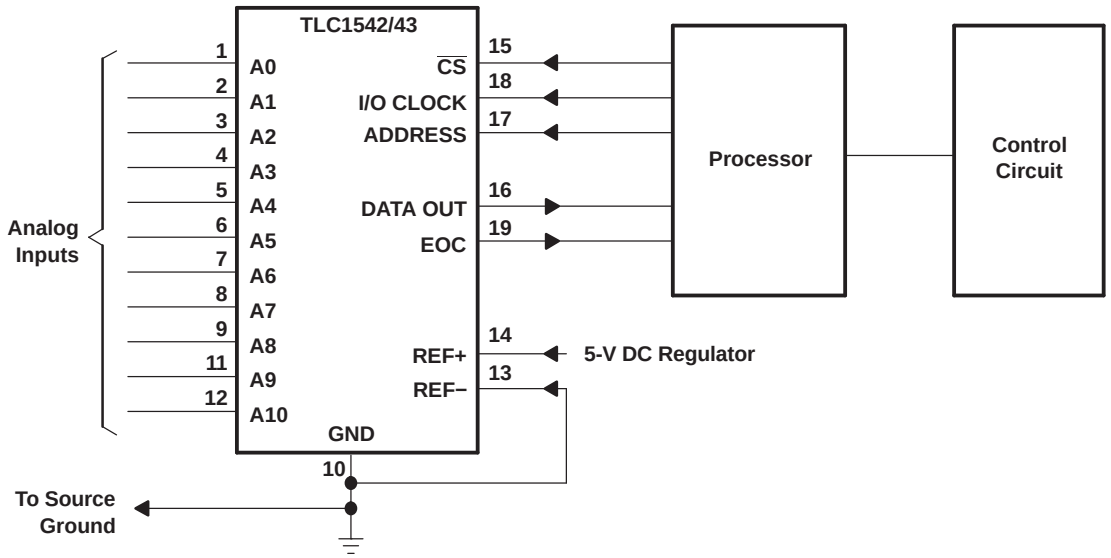


Figure 16. Serial Interface

APPLICATION INFORMATION (continued)

SIMPLIFIED ANALOG INPUT ANALYSIS

Using the equivalent circuit in Figure 17Figure 17, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_tC_i}\right)$$

where

$$R_t = R_s + r_i \tag{1}$$

The final voltage to 1/2 LSB is given by

$$V_C \text{ (1/2 LSB)} = V_S - (V_S/2048) \tag{2}$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - (V_S/2048) = V_S \left(1 - e^{-t_c/R_tC_i}\right)$$

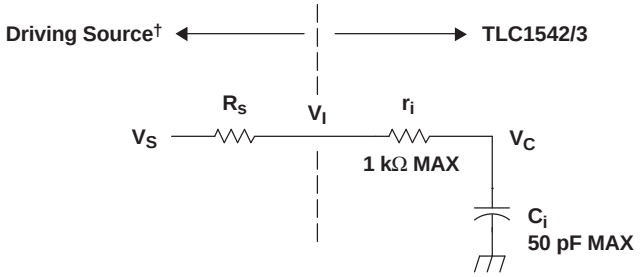
and

$$t_c \text{ (1/2 LSB)} = R_t \times C_i \times \ln(2048) \tag{3}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c \text{ (1/2 LSB)} = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(2048) \tag{4}$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at A0 – A10
V_S = External Driving Source Voltage
R_s = Source Resistance
r_i = Input Resistance
C_i = Equivalent Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 17. Equivalent Input Circuit Including the Driving Source

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC1542CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1542C	Samples
TLC1542CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1542C	Samples
TLC1542CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC1542C	Samples
TLC1542CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		TLC1542C	Samples
TLC1542CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC1542CN	Samples
TLC1542IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1542I	Samples
TLC1542IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1542I	Samples
TLC1542IN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC1542IN	Samples
TLC1543CDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P1543	Samples
TLC1543CDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P1543	Samples
TLC1543CDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P1543	Samples
TLC1543CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1543C	Samples
TLC1543CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1543C	Samples
TLC1543CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1543C	Samples
TLC1543CDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1543C	Samples
TLC1543CFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		TLC1543C	Samples
TLC1543CFNR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	TLC1543C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC1543CFNRG3	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	TLC1543C	Samples
TLC1543CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC1543CN	Samples
TLC1543IDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y1543	Samples
TLC1543IDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y1543	Samples
TLC1543IDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y1543	Samples
TLC1543IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1543I	Samples
TLC1543IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1543I	Samples
TLC1543IDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1543I	Samples
TLC1543IFN	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		TLC1543I	Samples
TLC1543IFNG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		TLC1543I	Samples
TLC1543IN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC1543IN	Samples
TLC1543INE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC1543IN	Samples
TLC1543QDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1543Q	Samples
TLC1543QDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1543Q	Samples
TLC1543QDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1543Q	Samples
TLC1543QDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1543Q	Samples
TLC1543QDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC1543Q	Samples
TLC1543QDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC1543Q	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC1543QDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC1543Q	Samples
TLC1543QDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC1543Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLC1543 :

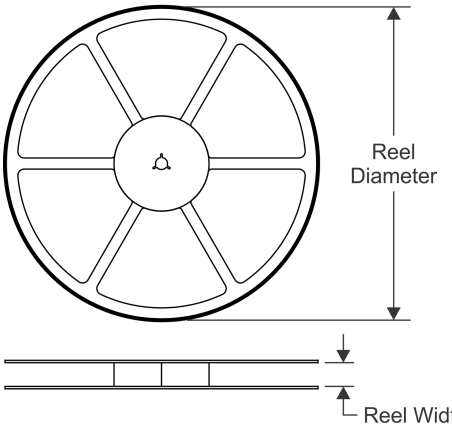
- Enhanced Product: TLC1543-EP

NOTE: Qualified Version Definitions:

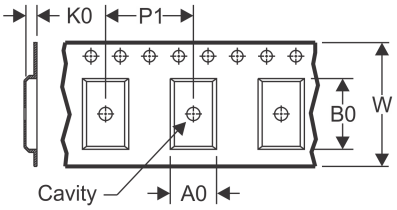
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

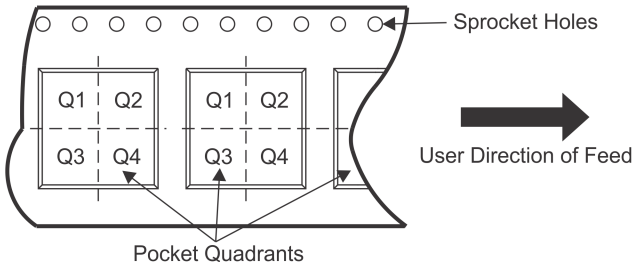


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

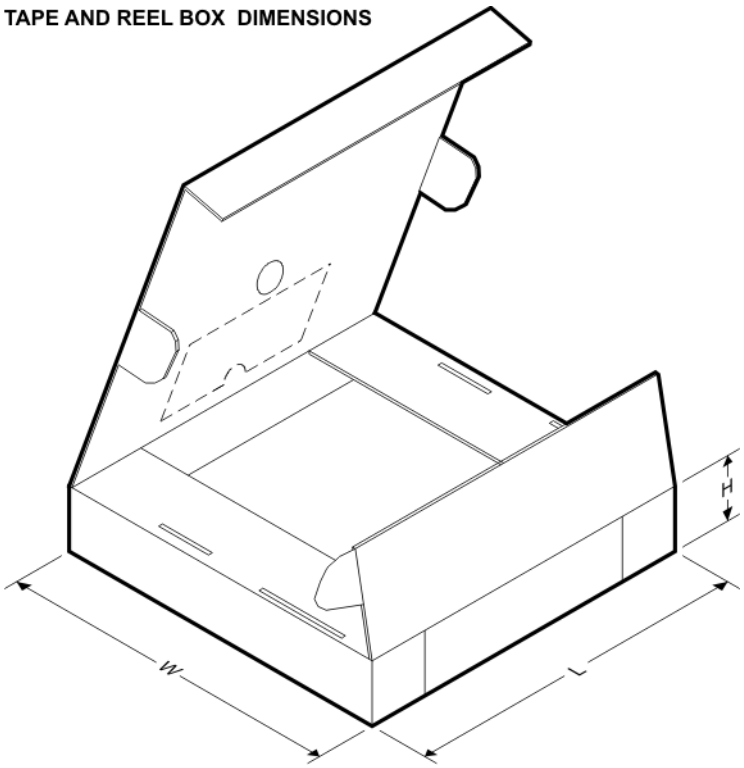
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC1542CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLC1542IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLC1543CDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TLC1543IDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TLC1543QDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TLC1543QDBRG4	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TLC1543QDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



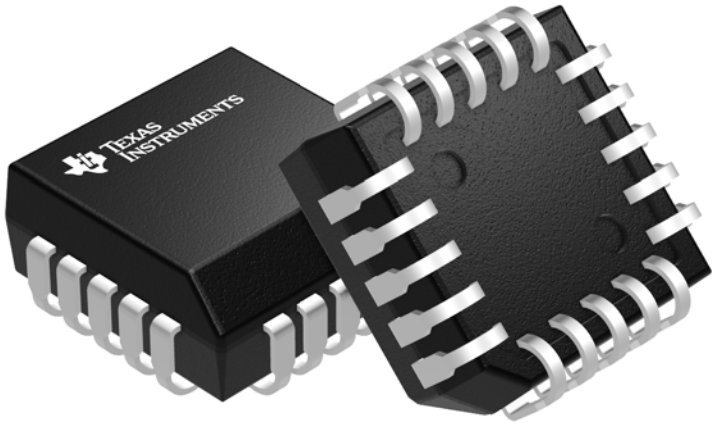
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC1542CDWR	SOIC	DW	20	2000	350.0	350.0	43.0
TLC1542IDWR	SOIC	DW	20	2000	350.0	350.0	43.0
TLC1543CDBR	SSOP	DB	20	2000	350.0	350.0	43.0
TLC1543IDBR	SSOP	DB	20	2000	350.0	350.0	43.0
TLC1543QDBR	SSOP	DB	20	2000	350.0	350.0	43.0
TLC1543QDBRG4	SSOP	DB	20	2000	350.0	350.0	43.0
TLC1543QDWR	SOIC	DW	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

FN 20 PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

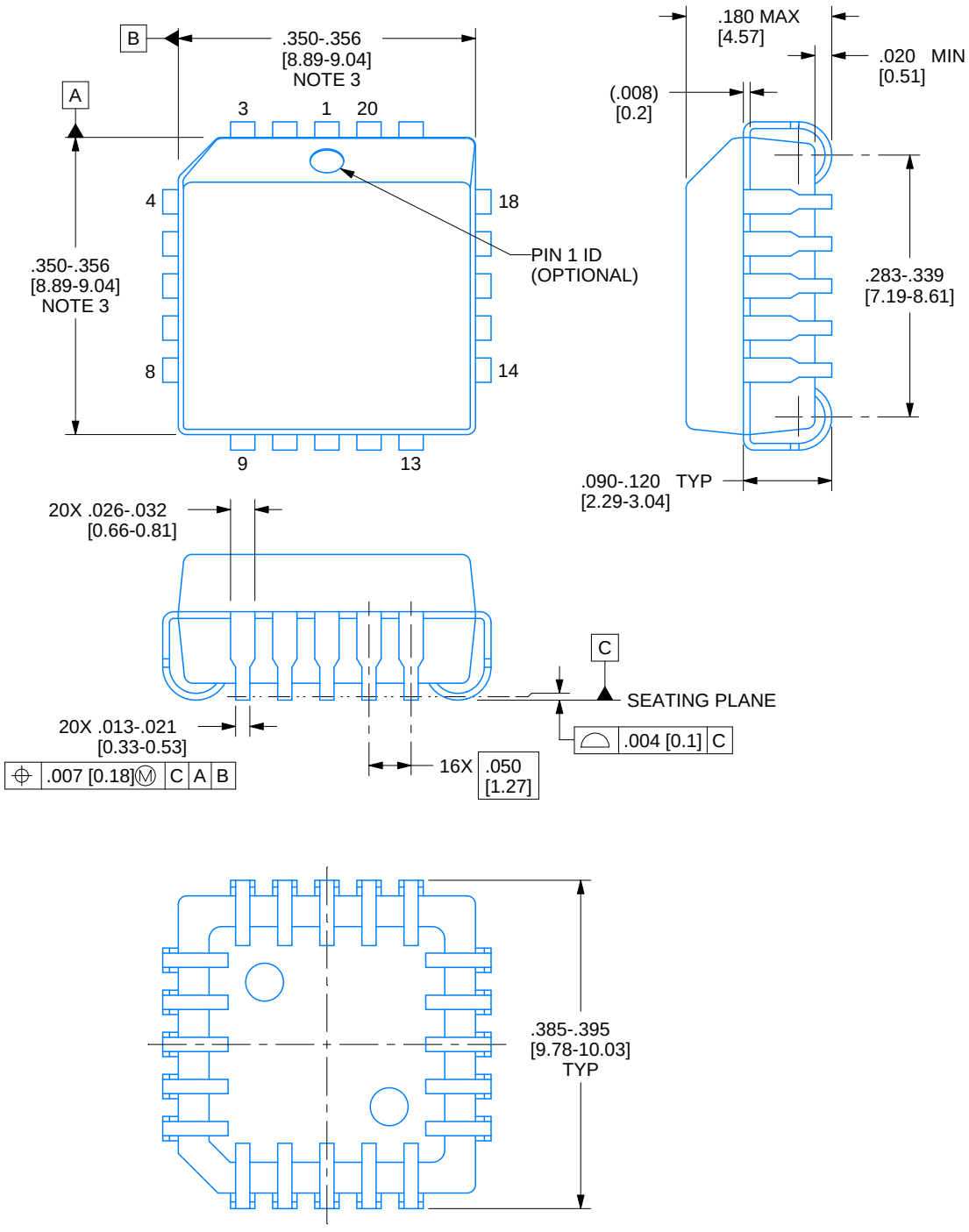
4040005-2/C

PACKAGE OUTLINE

FN0020A

PLCC - 4.57 mm max height

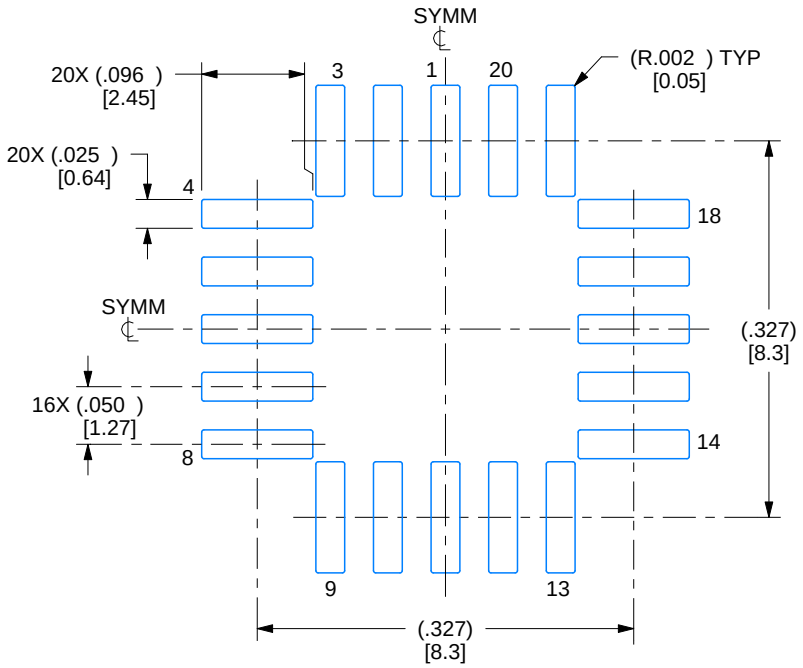
PLASTIC CHIP CARRIER



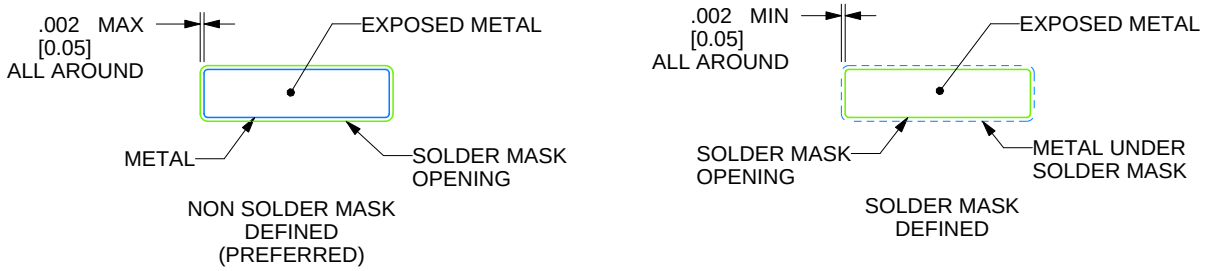
4215152/B 04/2017

NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

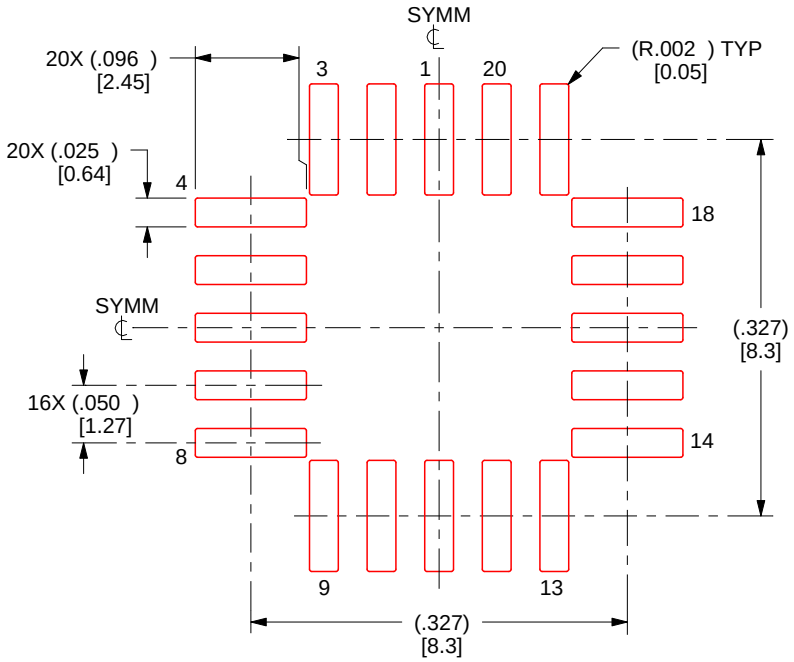


SOLDER MASK DETAILS

4215152/B 04/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215152/B 04/2017

NOTES: (continued)

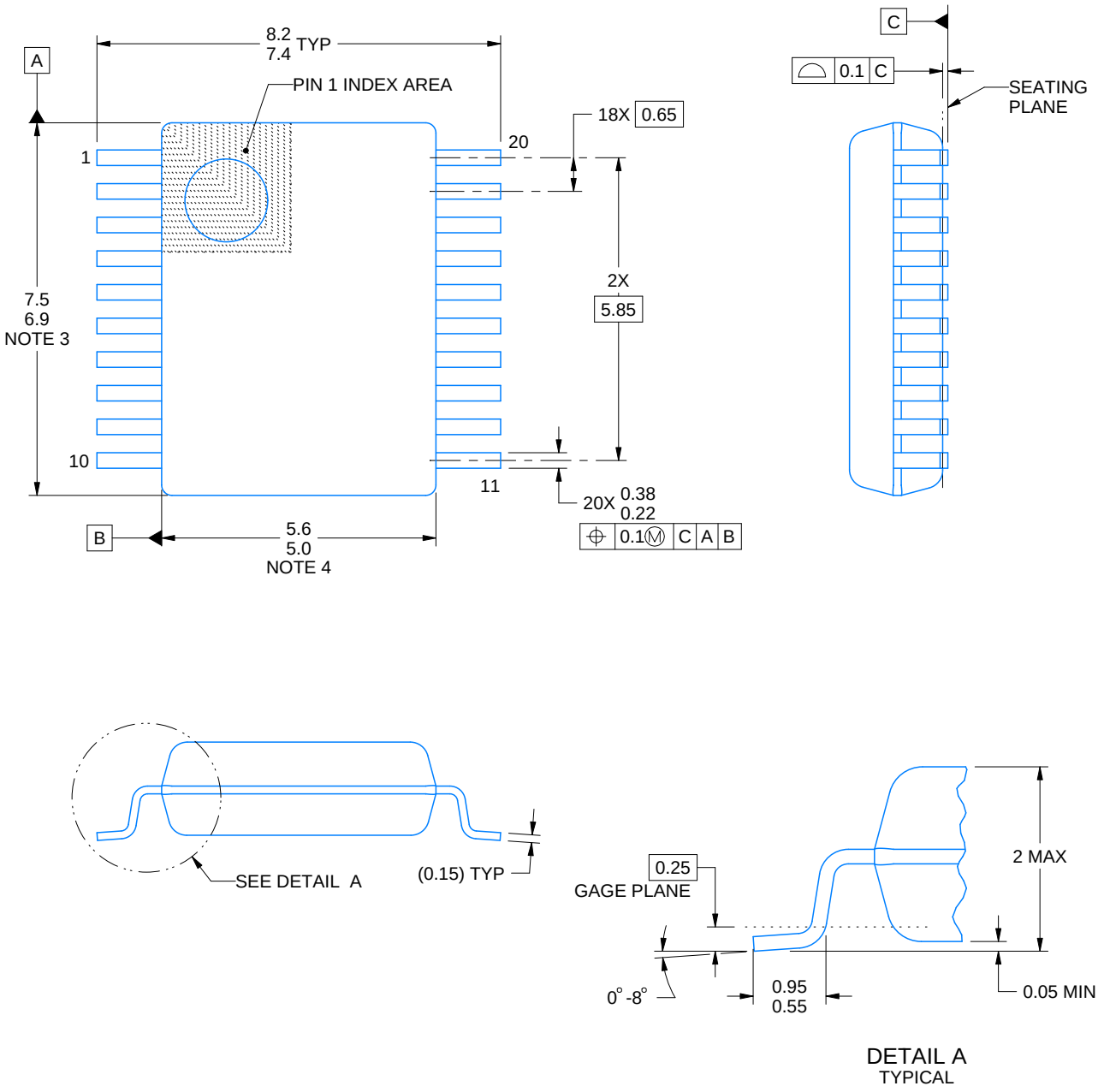
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0020A

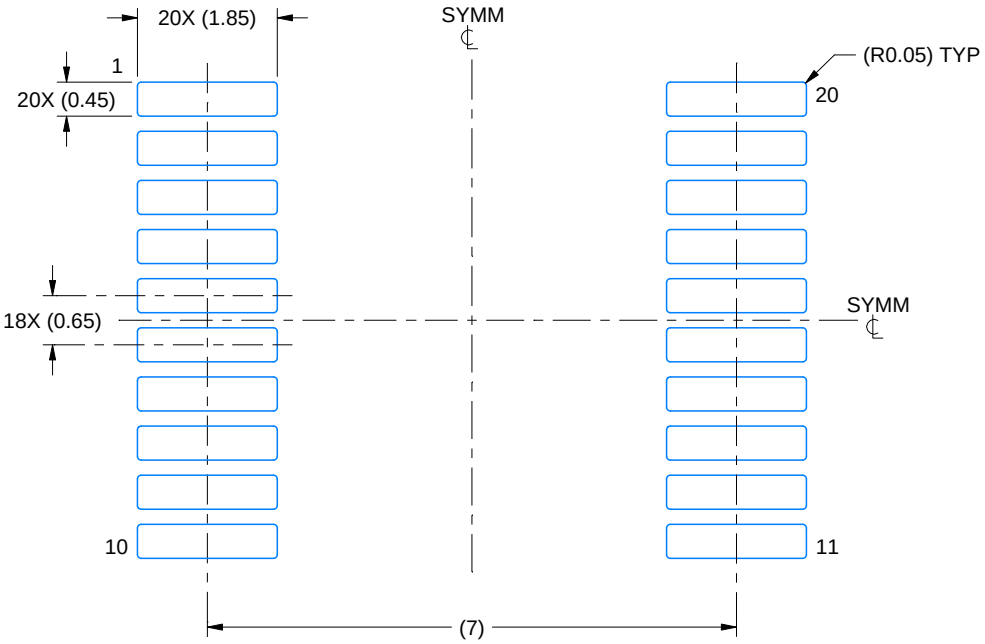
TSSOP - 2 mm max height

SMALL OUTLINE PACKAGE

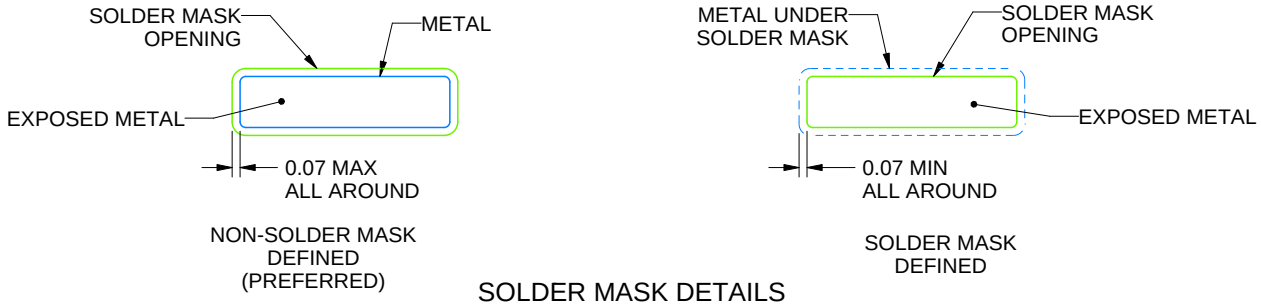


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

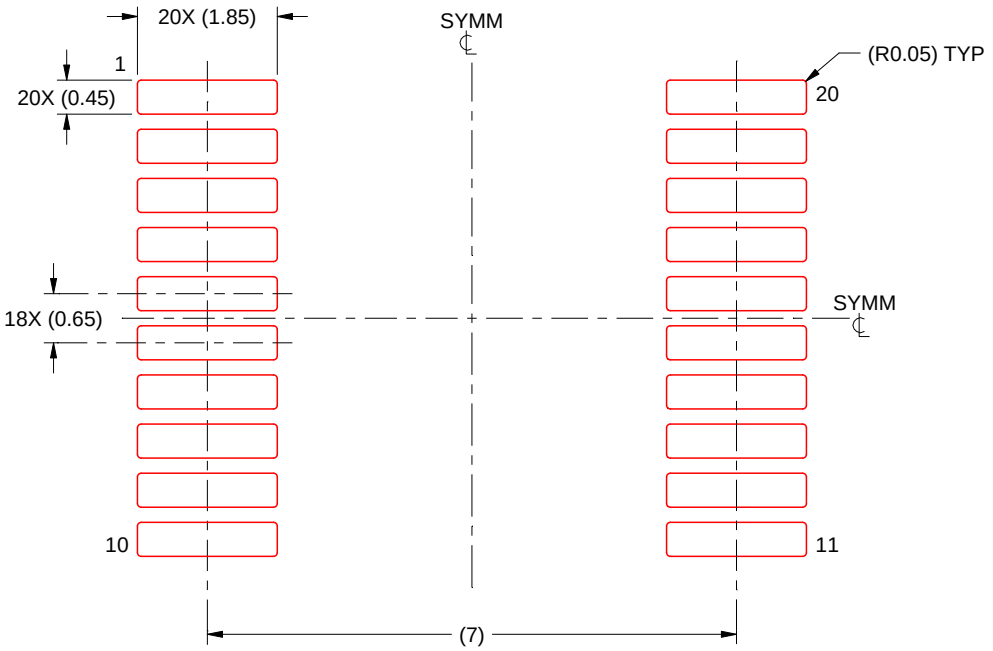


SOLDER MASK DETAILS

4214851/A 12/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/A 12/2017

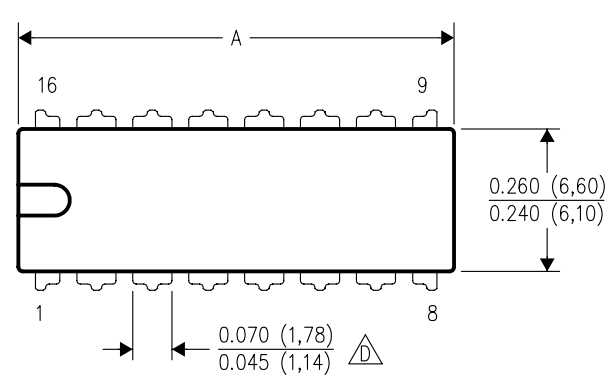
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

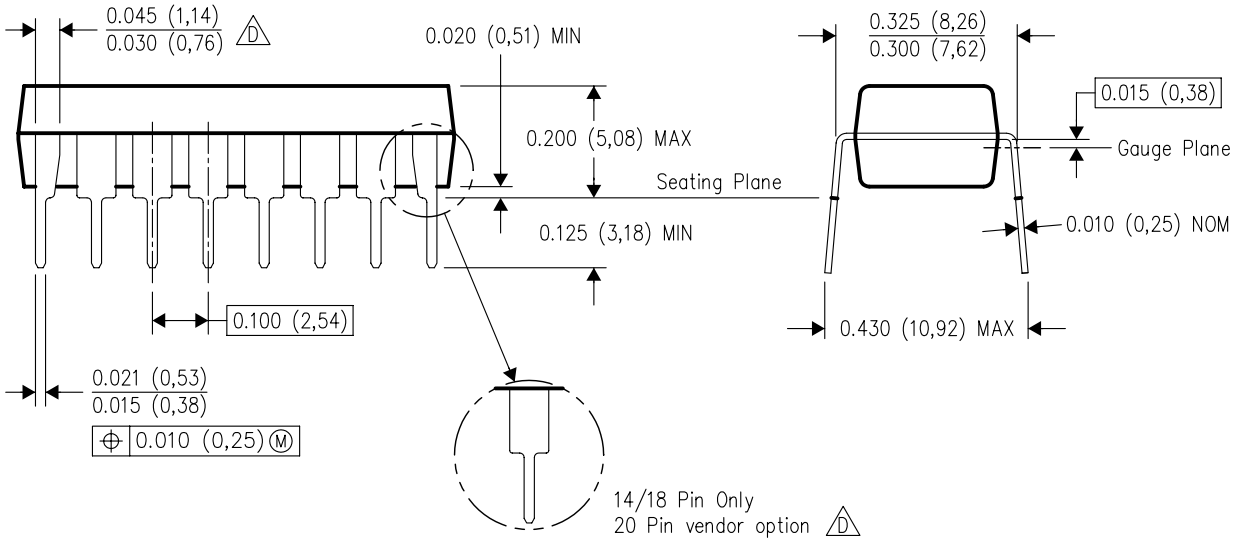
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

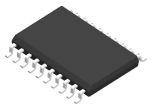


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

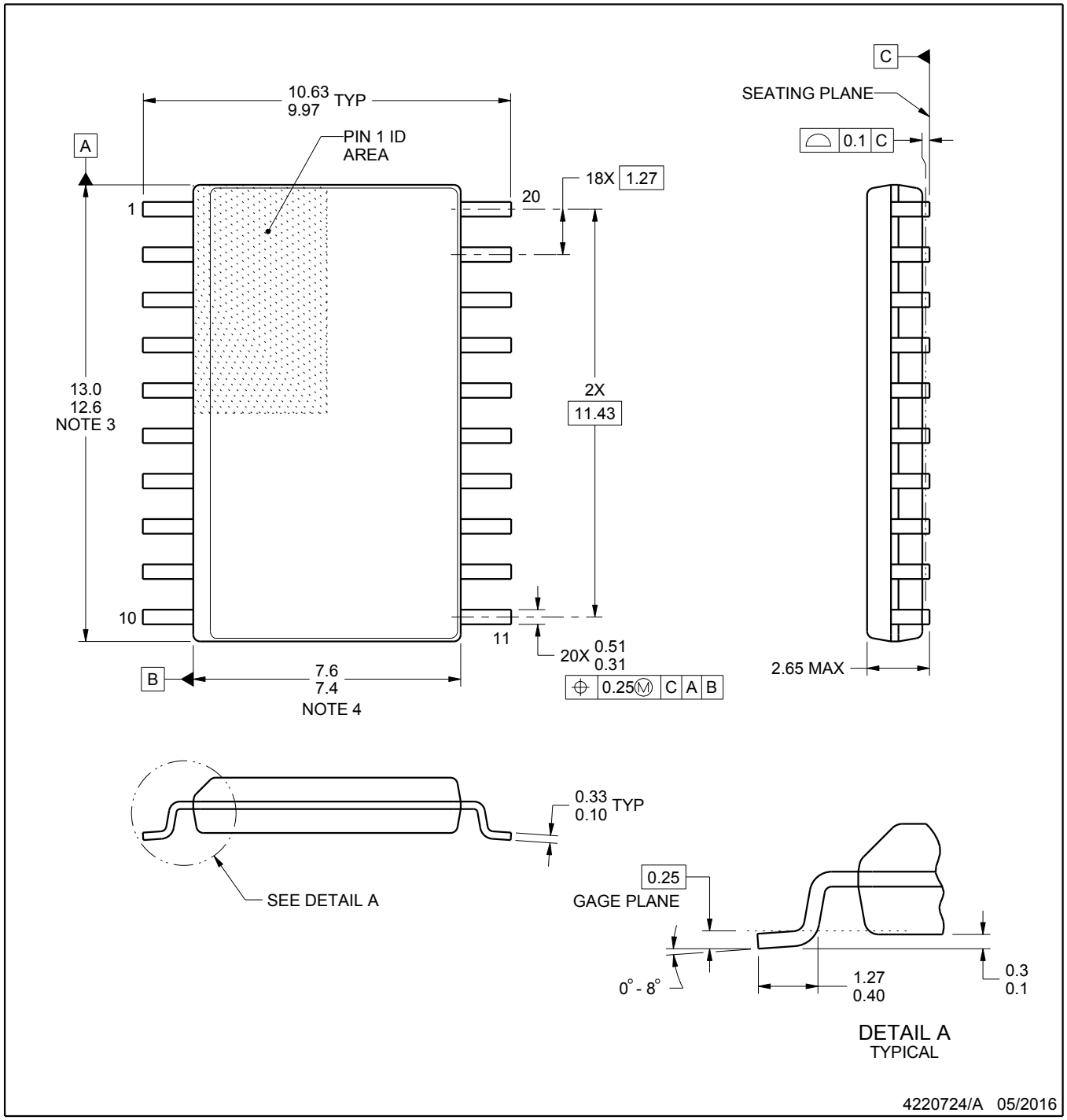


PACKAGE OUTLINE

DW0020A

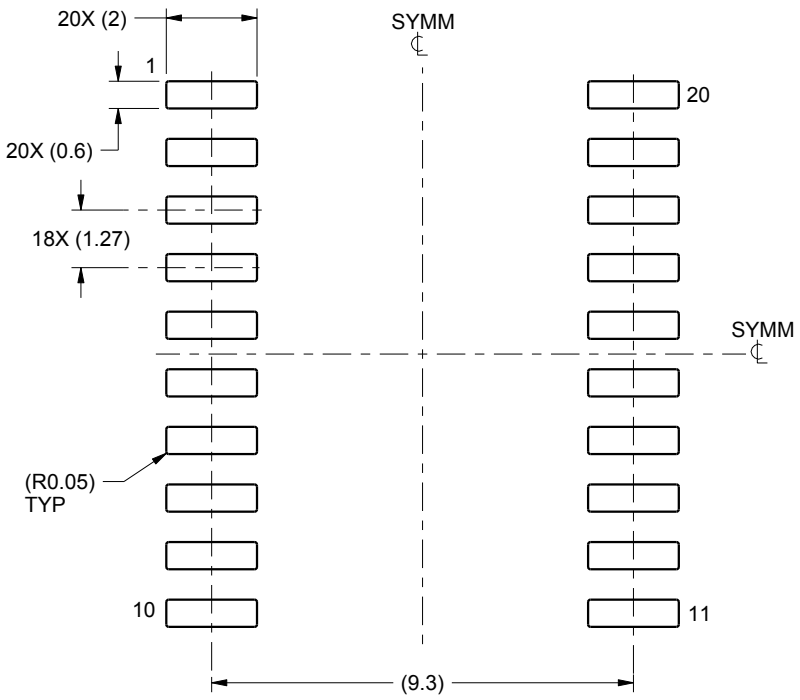
SOIC - 2.65 mm max height

SOIC

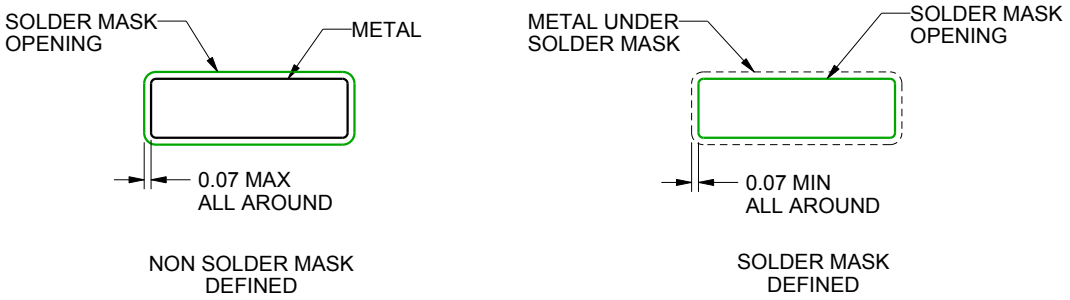


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

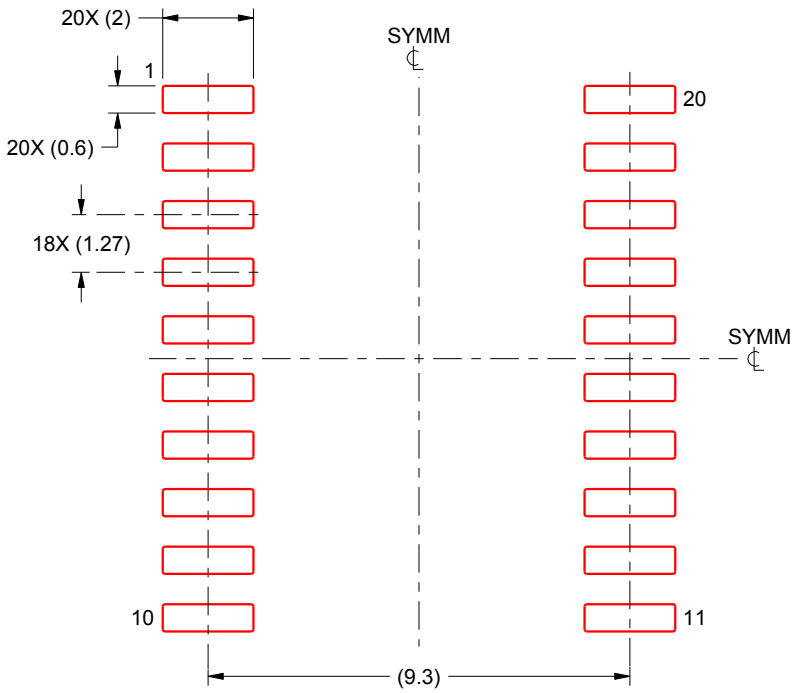


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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