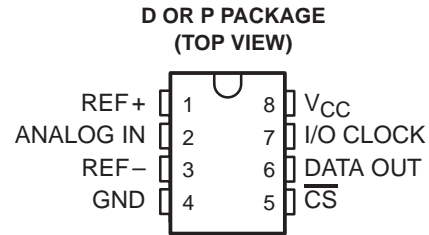




# TLC548C, TLC548I, TLC549C, TLC549I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

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- Microprocessor Peripheral or Standalone Operation
- 8-Bit Resolution A/D Converter
- Differential Reference Input Voltages
- Conversion Time . . . 17  $\mu$ s Max
- Total Access and Conversion Cycles Per Second
  - TLC548 . . . up to 45 500
  - TLC549 . . . up to 40 000
- On-Chip Software-Controllable Sample-and-Hold Function
- Total Unadjusted Error . . .  $\pm 0.5$  LSB Max
- 4-MHz Typical Internal System Clock
- Wide Supply Range . . . 3 V to 6 V
- Low Power Consumption . . . 15 mW Max
- Ideal for Cost-Effective, High-Performance Applications including Battery-Operated Portable Instrumentation
- Pinout and Control Signals Compatible With the TLC540 and TLC545 8-Bit A/D Converters and with the TLC1540 10-Bit A/D Converter
- CMOS Technology



## description

The TLC548 and TLC549 are CMOS analog-to-digital converter (ADC) integrated circuits built around an 8-bit switched-capacitor successive-approximation ADC. These devices are designed for serial interface with a microprocessor or peripheral through a 3-state data output and an analog input. The TLC548 and TLC549 use only the input/output clock (I/O CLOCK) input along with the chip select ( $\overline{CS}$ ) input for data control. The maximum I/O CLOCK input frequency of the TLC548 is 2.048 MHz, and the I/O CLOCK input frequency of the TLC549 is specified up to 1.1 MHz.

### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	TLC548CD TLC549CD	TLC548CP TLC549CP
–40°C to 85°C	TLC548ID TLC549ID	TLC548IP TLC549IP



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# TLC548C, TLC548I, TLC549C, TLC549I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

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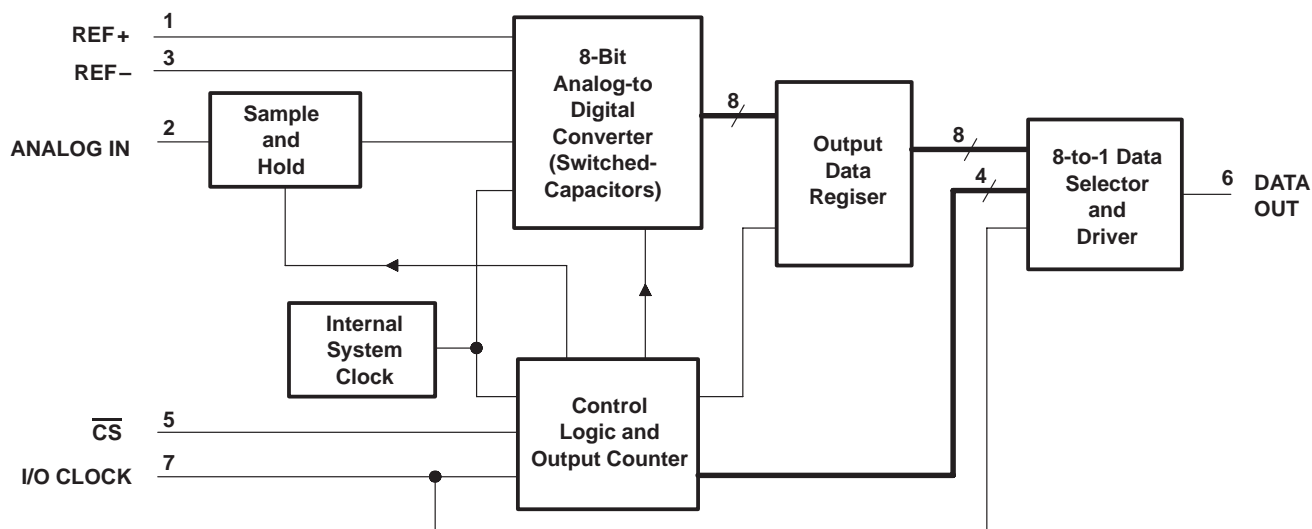
## description (continued)

Operation of the TLC548 and the TLC549 is very similar to that of the more complex TLC540 and TLC541 devices; however, the TLC548 and TLC549 provide an on-chip system clock that operates typically at 4 MHz and requires no external components. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing and permits manipulation of the TLC548 and TLC549 as desired for a wide range of software and hardware requirements. The I/O CLOCK together with the internal system clock allow high-speed data transfer and conversion rates of 45 500 conversions per second for the TLC548, and 40 000 conversions per second for the TLC549.

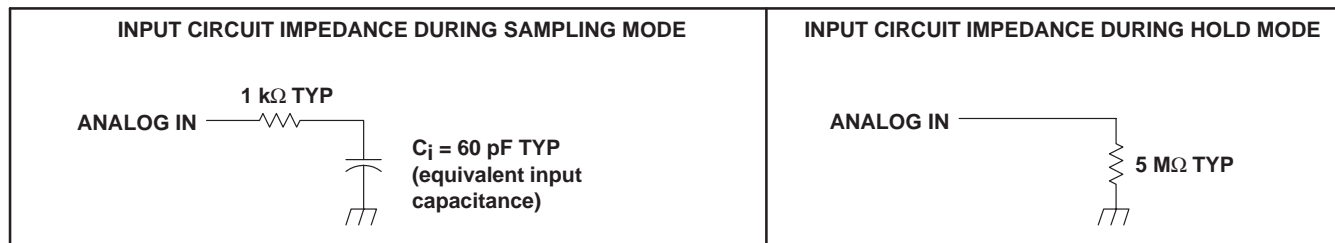
Additional TLC548 and TLC549 features include versatile control logic, an on-chip sample-and-hold circuit that can operate automatically or under microprocessor control, and a high-speed converter with differential high-impedance reference voltage inputs that ease ratiometric conversion, scaling, and circuit isolation from logic and supply noises. Design of the totally switched-capacitor successive-approximation converter circuit allows conversion with a maximum total error of  $\pm 0.5$  least significant bit (LSB) in less than 17  $\mu$ s.

The TLC548C and TLC549C are characterized for operation from 0°C to 70°C. The TLC548I and TLC549I are characterized for operation from -40°C to 85°C.

## functional block diagram



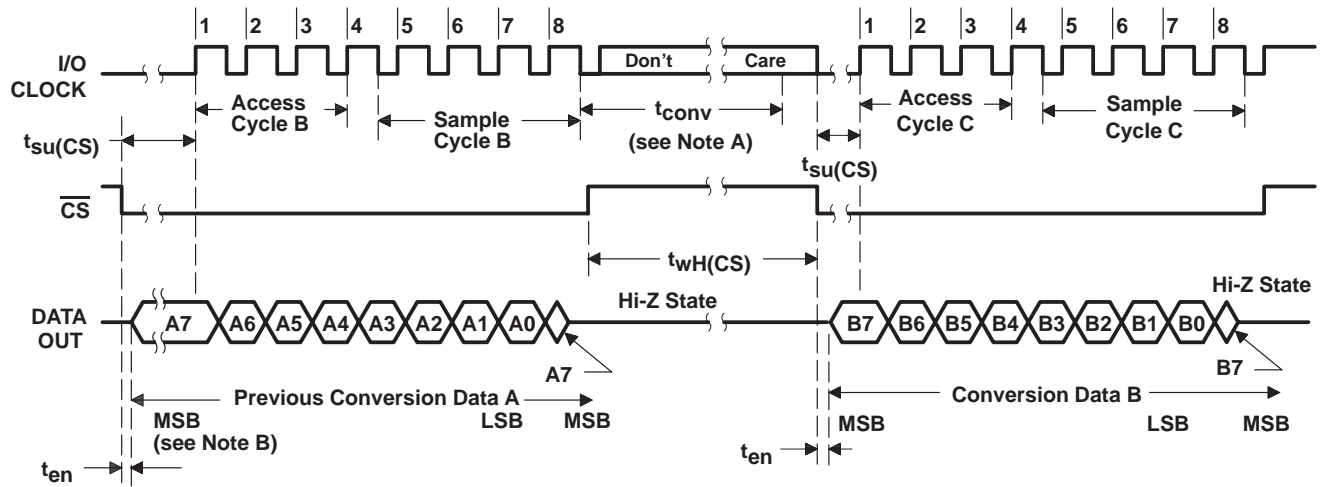
## typical equivalent inputs



# TLC548C, TLC548I, TLC549C, TLC549I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

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## operating sequence



- NOTES: A. The conversion cycle, which requires 36 internal system clock periods (17  $\mu$ s maximum), is initiated with the eighth I/O clock pulse trailing edge after  $\overline{CS}$  goes low for the channel whose address exists in memory at the time.
- B. The most significant bit (A7) is automatically placed on the DATA OUT bus after  $\overline{CS}$  is brought low. The remaining seven bits (A6–A0) are clocked out on the first seven I/O clock falling edges. B7–B0 follows in the same manner.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	6.5 V
Input voltage range at any input	–0.3 V to $V_{CC} + 0.3$ V
Output voltage range	–0.3 V to $V_{CC} + 0.3$ V
Peak input current range (any input)	$\pm 10$ mA
Peak total input current range (all inputs)	$\pm 30$ mA
Operating free-air temperature range, $T_A$ (see Note 2):	
TLC548C, TLC549C	0°C to 70°C
TLC548I, TLC549I	–40°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- NOTES: 1. All voltage values are with respect to the network ground terminal with the REF– and GND terminals connected together, unless otherwise noted.
2. The D package is not recommended below –40°C.



# TLC548C, TLC548I, TLC549C, TLC549I

## 8-BIT ANALOG-TO-DIGITAL CONVERTERS

### WITH SERIAL CONTROL

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#### recommended operating conditions

	TLC548			TLC549			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	3	5	6	3	5	6	V
Positive reference voltage, $V_{ref+}$ (see Note 3)	2.5	$V_{CC}$	$V_{CC}+0.1$	2.5	$V_{CC}$	$V_{CC}+0.1$	V
Negative reference voltage, $V_{ref-}$ (see Note 3)	-0.1	0	2.5	-0.1	0	2.5	V
Differential reference voltage, $V_{ref+}$ , $V_{ref-}$ (see Note 3)	1	$V_{CC}$	$V_{CC}+0.2$	1	$V_{CC}$	$V_{CC}+0.2$	V
Analog input voltage (see Note 3)	0		$V_{CC}$	0		$V_{CC}$	V
High-level control input voltage, $V_{IH}$ (for $V_{CC} = 4.75$ V to 5.5 V)	2			2			V
Low-level control input voltage, $V_{IL}$ (for $V_{CC} = 4.75$ V to 5.5 V)			0.8			0.8	V
Input/output clock frequency, $f_{clock(I/O)}$ (for $V_{CC} = 4.75$ V to 5.5 V)	0		2.048	0		1.1	MHz
Input/output clock high, $t_{wH(I/O)}$ (for $V_{CC} = 4.75$ V to 5.5 V)	200			404			ns
Input/output clock low, $t_{wL(I/O)}$ (for $V_{CC} = 4.75$ V to 5.5 V)	200			404			ns
Input/output clock transition time, $t_t(I/O)$ (for $V_{CC} = 4.75$ V to 5.5 V) (see Note 4 and Operating Sequence)			100			100	ns
Duration of $\overline{CS}$ input high state during conversion, $t_{wH(CS)}$ (for $V_{CC} = 4.75$ V to 5.5 V) (see Operating Sequence)	17			17			$\mu$ s
Setup time, $\overline{CS}$ low before first I/O CLOCK, $t_{su(CS)}$ (for $V_{CC} = 4.75$ V to 5.5 V) (see Note 5)	1.4			1.4			$\mu$ s
TLC548C, TLC549C	0		70	0		70	$^{\circ}$ C
TLC548I, TLC549I	-40		85	-40		85	

- NOTES:
3. Analog input voltages greater than that applied to REF+ convert to all ones (11111111), while input voltages less than that applied to REF- convert to all zeros (00000000). For proper operation, the positive reference voltage  $V_{ref+}$ , must be at least 1 V greater than the negative reference voltage,  $V_{ref-}$ . In addition, unadjusted errors may increase as the differential reference voltage,  $V_{ref+} - V_{ref-}$ , falls below 4.75 V.
  4. This is the time required for the I/O CLOCK input signal to fall from  $V_{IH}$  min to  $V_{IL}$  max or to rise from  $V_{IL}$  max to  $V_{IH}$  min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2  $\mu$ s for remote data acquisition applications in which the sensor and the ADC are placed several feet away from the controlling microprocessor.
  5. To minimize errors caused by noise at the  $\overline{CS}$  input, the internal circuitry waits for two rising edges and one falling edge of internal system clock after  $\overline{CS}\downarrow$  before responding to control input signals. This  $\overline{CS}$  setup time is given by the  $t_{en}$  and  $t_{su(CS)}$  specifications.



**TLC548C, TLC548I, TLC549C, TLC549I**  
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**WITH SERIAL CONTROL**

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**electrical characteristics over recommended operating free-air temperature range,**  
 **$V_{CC} = V_{ref+} = 4.75\text{ V to }5.5\text{ V}$ ,  $f_{clock(I/O)} = 2.048\text{ MHz}$  for TLC548 or  $1.1\text{ MHz}$  for TLC549**  
**(unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OH}$	High-level output voltage	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -360\text{ }\mu\text{A}$	2.4			V
$V_{OL}$	Low-level output voltage	$V_{CC} = 4.75\text{ V}$ , $I_{OL} = 3.2\text{ mA}$			0.4	V
$I_{OZ}$	High-impedance off-state output current	$V_O = V_{CC}$ , $\overline{CS}$ at $V_{CC}$			10	$\mu\text{A}$
		$V_O = 0$ , $\overline{CS}$ at $V_{CC}$			-10	
$I_{IH}$	High-level input current, control inputs	$V_I = V_{CC}$		0.005	2.5	$\mu\text{A}$
$I_{IL}$	Low-level input current, control inputs	$V_I = 0$		-0.005	-2.5	$\mu\text{A}$
$I_{I(on)}$	Analog channel on-state input current during sample cycle	Analog input at $V_{CC}$		0.4	1	$\mu\text{A}$
		Analog input at 0 V		-0.4	-1	
$I_{CC}$	Operating supply current	$\overline{CS}$ at 0 V		1.8	2.5	mA
$I_{CC} + I_{ref}$	Supply and reference current	$V_{ref+} = V_{CC}$		1.9	3	mA
$C_i$	Input capacitance	Analog inputs		7	55	pF
		Control inputs		5	15	

**operating characteristics over recommended operating free-air temperature range,**  
 **$V_{CC} = V_{ref+} = 4.75\text{ V to }5.5\text{ V}$ ,  $f_{clock(I/O)} = 2.048\text{ MHz}$  for TLC548 or  $1.1\text{ MHz}$  for TLC549**  
**(unless otherwise noted)**

PARAMETER	TEST CONDITIONS	TLC548			TLC549			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$E_L$	Linearity error	See Note 6		$\pm 0.5$	$\pm 0.5$		LSB	
$E_{ZS}$	Zero-scale error	See Note 7		$\pm 0.5$	$\pm 0.5$		LSB	
$E_{FS}$	Full-scale error	See Note 7		$\pm 0.5$	$\pm 0.5$		LSB	
	Total unadjusted error	See Note 8		$\pm 0.5$	$\pm 0.5$		LSB	
$t_{conv}$	Conversion time	See Operating Sequence		8	17	12	17	$\mu\text{s}$
	Total access and conversion time	See Operating Sequence		12	22	19	25	$\mu\text{s}$
$t_a$	Channel acquisition time (sample cycle)	See Operating Sequence		4		4		I/O clock cycles
$t_v$	Time output data remains valid after I/O CLOCK↓			10	10		ns	
$t_d$	Delay time to data output valid	I/O CLOCK↓		200		400		ns
$t_{en}$	Output enable time			1.4		1.4		$\mu\text{s}$
$t_{dis}$	Output disable time			150		150		ns
$t_r(\text{bus})$	Data bus rise time	See Figure 1		300		300		ns
$t_f(\text{bus})$	Data bus fall time			300		300		ns

† All typicals are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

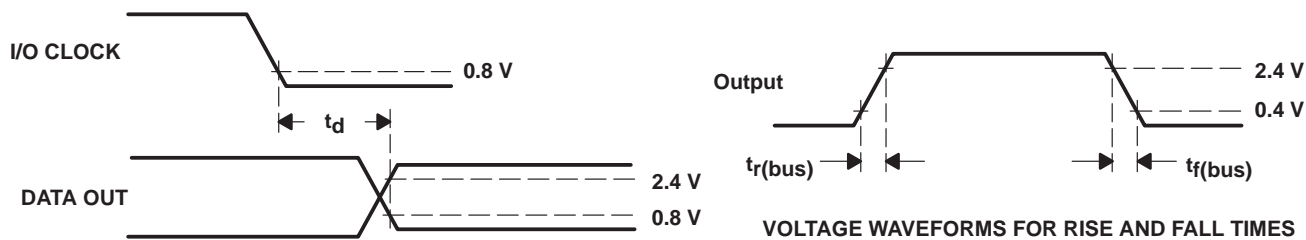
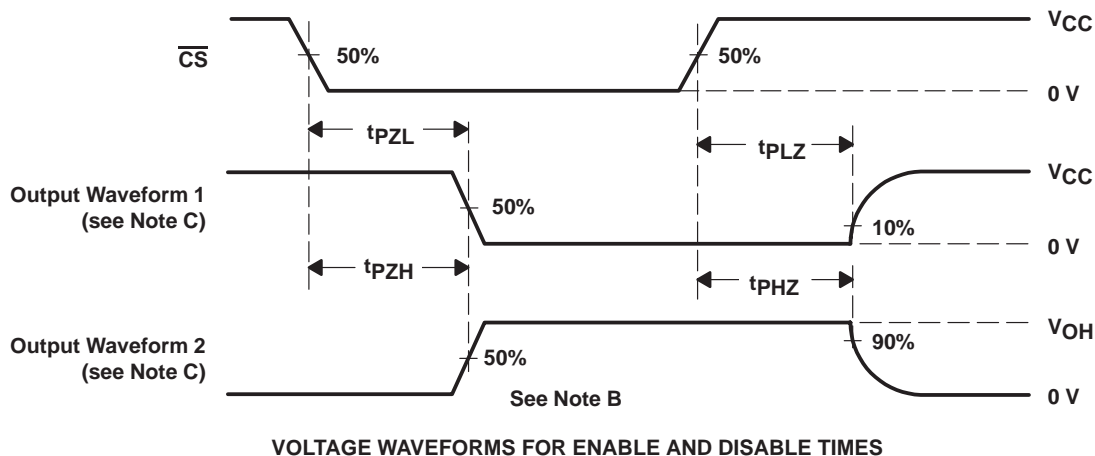
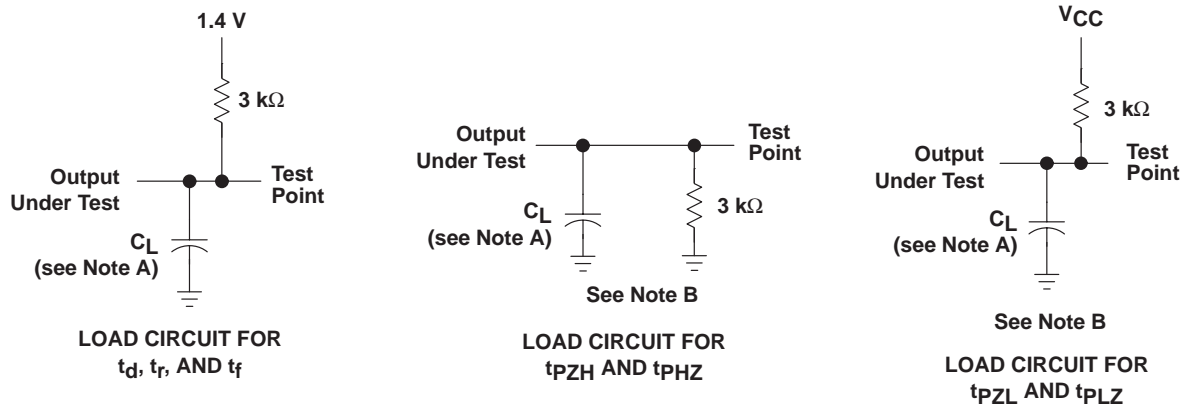
- NOTES: 6. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.  
7. Zero-scale error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.  
8. Total unadjusted error is the sum of linearity, zero-scale, and full-scale errors.



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L = 50 \text{ pF}$  for TLC548 and  $100 \text{ pF}$  for TLC549;  $C_L$  includes jig capacitance.  
 B.  $t_{en} = t_{pZH}$  or  $t_{pZL}$ ,  $t_{dis} = t_{pHZ}$  or  $t_{pLZ}$ .  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuits and Voltage Waveforms

## APPLICATIONS INFORMATION

### simplified analog input analysis

Using the equivalent circuit in Figure 2, the time required to charge the analog input capacitance from 0 to  $V_S$  within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (1)$$

where

$$R_t = R_s + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S/512) \quad (2)$$

Equating equation 1 to equation 2 and solving for time  $t_c$  gives

$$V_S - (V_S/512) = V_S \left(1 - e^{-t_c/R_t C_i}\right) \quad (3)$$

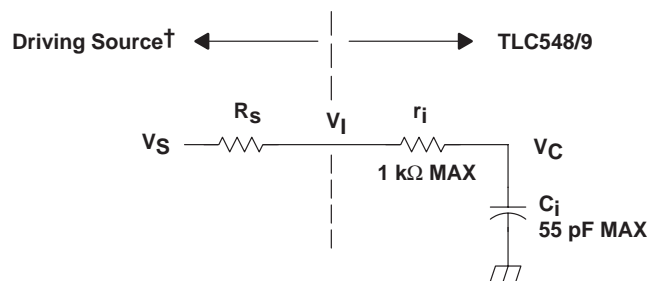
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(512) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_s + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(512) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



$V_I$  = Input Voltage at ANALOG IN  
 $V_S$  = External Driving Source Voltage  
 $R_S$  = Source Resistance  
 $r_i$  = Input Resistance  
 $C_i$  = Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- $R_S$  must be real at the input frequency.

**Figure 2. Equivalent Input Circuit Including the Driving Source**

# TLC548C, TLC548I, TLC549C, TLC549I

## 8-BIT ANALOG-TO-DIGITAL CONVERTERS

### WITH SERIAL CONTROL

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## PRINCIPLES OF OPERATION

The TLC548 and TLC549 are each complete data acquisition systems on a single chip. Each contains an internal system clock, sample-and-hold function, 8-bit A/D converter, data register, and control logic circuitry. For flexibility and access speed, there are two control inputs: I/O CLOCK and chip select ( $\overline{CS}$ ). These control inputs and a TTL-compatible 3-state output facilitate serial communications with a microprocessor or minicomputer. A conversion can be completed in 17  $\mu$ s or less, while complete input-conversion-output cycles can be repeated in 22  $\mu$ s for the TLC548 and in 25  $\mu$ s for the TLC549.

The internal system clock and I/O CLOCK are used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Due to this independence and the internal generation of the system clock, the control hardware and software need only be concerned with reading the previous conversion result and starting the conversion by using the I/O clock. In this manner, the internal system clock drives the “conversion crunching” circuitry so that the control hardware and software need not be concerned with this task.

When  $\overline{CS}$  is high, DATA OUT is in a high-impedance condition and I/O CLOCK is disabled. This  $\overline{CS}$  control function allows I/O CLOCK to share the same control logic point with its counterpart terminal when additional TLC548 and TLC549 devices are used. This also serves to minimize the required control logic terminals when using multiple TLC548 and TLC549 devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1.  $\overline{CS}$  is brought low. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for two rising edges and then a falling edge of the internal system clock after a  $\overline{CS}\downarrow$  before the transition is recognized. However, upon a  $\overline{CS}$  rising edge, DATA OUT goes to a high-impedance state within the specified  $t_{dis}$  even though the rest of the integrated circuitry does not recognize the transition until the specified  $t_{su}(CS)$  has elapsed. This technique protects the device against noise when used in a noisy environment. The most significant bit (MSB) of the previous conversion result initially appears on DATA OUT when  $\overline{CS}$  goes low.
2. The falling edges of the first four I/O CLOCK cycles shift out the second, third, fourth, and fifth most significant bits of the previous conversion result. The on-chip sample-and-hold function begins sampling the analog input after the fourth high-to-low transition of I/O CLOCK. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three more I/O CLOCK cycles are then applied to the I/O CLOCK terminal and the sixth, seventh, and eighth conversion bits are shifted out on the falling edges of these clock cycles.
4. The final (the eighth) clock cycle is applied to I/O CLOCK. The on-chip sample-and-hold function begins the hold operation upon the high-to-low transition of this clock cycle. The hold function continues for the next four internal system clock cycles, after which the holding function terminates and the conversion is performed during the next 32 system clock cycles, giving a total of 36 cycles. After the eighth I/O CLOCK cycle,  $\overline{CS}$  must go high or the I/O clock must remain low for at least 36 internal system clock cycles to allow for the completion of the hold and conversion functions.  $\overline{CS}$  can be kept low during periods of multiple conversion. When keeping  $\overline{CS}$  low during periods of multiple conversion, special care must be exercised to prevent noise glitches on the I/O CLOCK line. If glitches occur on I/O CLOCK, the I/O sequence between the microprocessor/controller and the device loses synchronization. When  $\overline{CS}$  is taken high, it must remain high until the end of conversion. Otherwise, a valid high-to-low transition of  $\overline{CS}$  causes a reset condition, which aborts the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 internal system clock cycles occur. Such action yields the conversion result of the previous conversion and not the ongoing conversion.



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## PRINCIPLES OF OPERATION

For certain applications, such as strobing applications, it is necessary to start conversion at a specific point in time. This device accommodates these applications. Although the on-chip sample-and-hold function begins sampling upon the high-to-low transition of the fourth I/O CLOCK cycle, the hold function does not begin until the high-to-low transition of the eighth I/O CLOCK cycle, which should occur at the moment when the analog signal must be converted. The TLC548 and TLC549 continue sampling the analog input until the high-to-low transition of the eighth I/O CLOCK pulse. The control circuitry or software then immediately lowers I/O CLOCK and starts the holding function to hold the analog signal at the desired point in time and starts the conversion.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC548CD	LIFEBUY	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC548C	
TLC548CDR	LIFEBUY	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LC548C	
TLC548CP	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLC548CP	
TLC548ID	LIFEBUY	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LC548I	
TLC548IDR	LIFEBUY	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LC548I	
TLC548IP	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLC548IP	
TLC549CD	LIFEBUY	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC549C	
TLC549CDG4	LIFEBUY	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC549C	
TLC549CDR	LIFEBUY	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LC549C	
TLC549CDRG4	LIFEBUY	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LC549C	
TLC549CP	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLC549CP	
TLC549ID	LIFEBUY	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LC549I	
TLC549IDG4	LIFEBUY	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LC549I	
TLC549IDR	LIFEBUY	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LC549I	
TLC549IDRG4	LIFEBUY	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LC549I	
TLC549IP	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLC549IP	
TLC549IPS	LIFEBUY	SO	PS	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y549	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC549IPSR	LIFEBUY	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y549	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC548CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC548IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC549CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC549IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC549IPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC548CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC548IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC549CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC549IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC549IPSR	SO	PS	8	2000	367.0	367.0	38.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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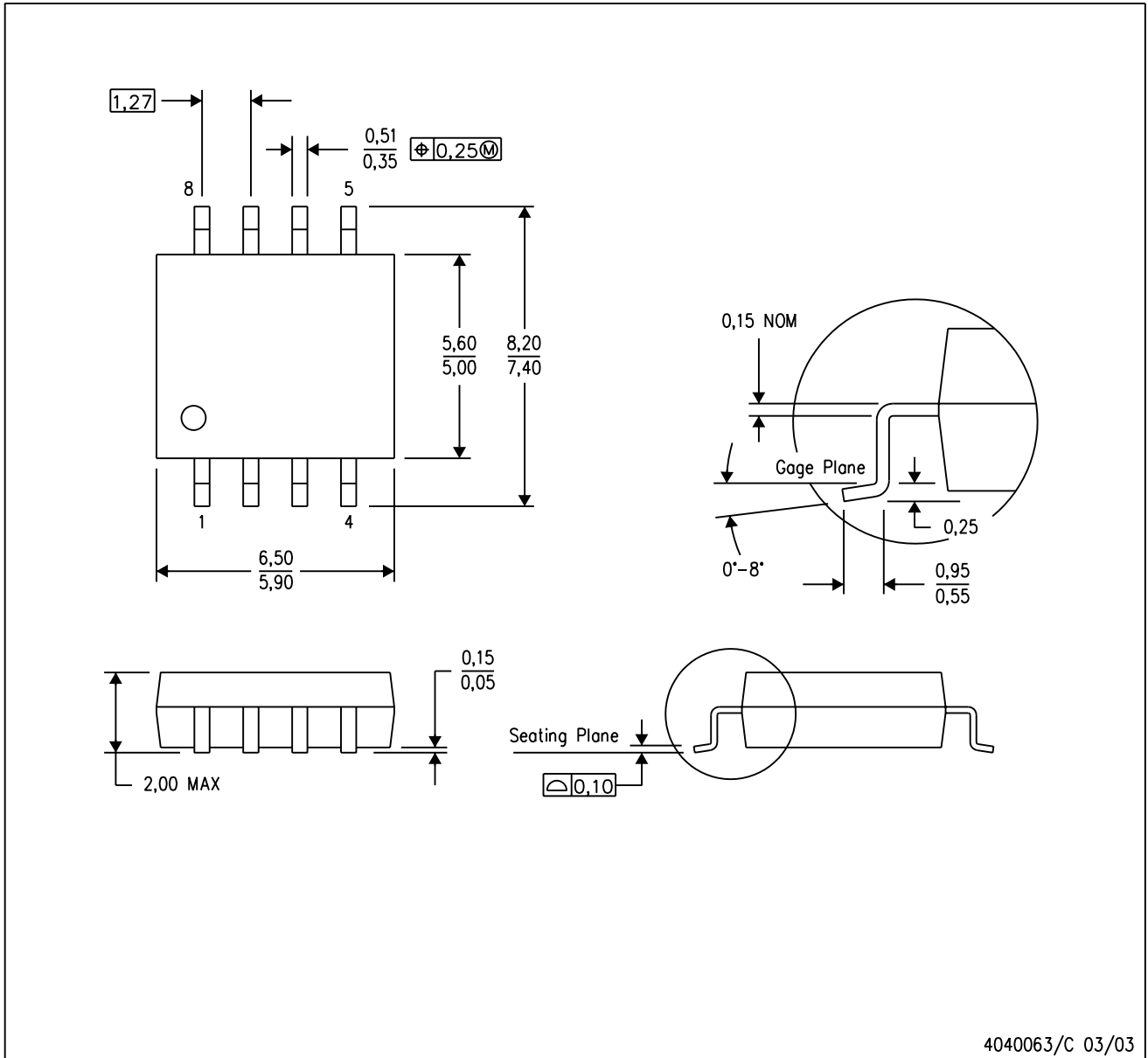
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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