



# THE DATASHEET OF TLE2022CP



# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

SLOS191D – FEBRUARY 1997 – REVISED NOVEMBER 2010

- Supply Current . . . 300  $\mu$ A Max
- High Unity-Gain Bandwidth . . . 2 MHz Typ
- High Slew Rate . . . 0.45 V/ $\mu$ s Min
- Supply-Current Change Over Military Temp Range . . . 10  $\mu$ A Typ at  $V_{CC} \pm = \pm 15$  V
- Specified for Both 5-V Single-Supply and  $\pm 15$ -V Operation
- Phase-Reversal Protection
- High Open-Loop Gain . . . 6.5 V/ $\mu$ V (136 dB) Typ
- Low Offset Voltage . . . 100  $\mu$ V Max
- Offset Voltage Drift With Time 0.005  $\mu$ V/mo Typ
- Low Input Bias Current . . . 50 nA Max
- Low Noise Voltage . . . 19 nV/ $\sqrt{\text{Hz}}$  Typ

## description

The TLE202x, TLE202xA, and TLE202xB devices are precision, high-speed, low-power operational amplifiers using a new Texas Instruments Excalibur process. These devices combine the best features of the OP21 with highly improved slew rate and unity-gain bandwidth.

The complementary bipolar Excalibur process utilizes isolated vertical pnp transistors that yield dramatic improvement in unity-gain bandwidth and slew rate over similar devices.

The addition of a bias circuit in conjunction with this process results in extremely stable parameters with both time and temperature. This means that a precision device remains a precision device even with changes in temperature and over years of use.

This combination of excellent dc performance with a common-mode input voltage range that includes the negative rail makes these devices the ideal choice for low-level signal conditioning applications in either single-supply or split-supply configurations. In addition, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs goes below the negative supply rail.

A variety of available options includes small-outline and chip-carrier versions for high-density systems applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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## TLE2021 AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES						CHIP FORM <sup>§</sup> (Y)
		SMALL OUTLINE <sup>†</sup> (D)	SSOP <sup>‡</sup> (DB)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP <sup>‡</sup> (PW)	
0°C to 70°C	200 μV 500 μV	TLE2021ACD TLE2021CD	TLE2021CDBLE	—	—	TLE2021ACP TLE2021CP	— TLE2021CPWLE	— TLE2021Y
-40°C to 85°C	200 μV 500 μV	TLE2021AID TLE2021ID	—	—	—	TLE2021AIP TLE2021IP	—	—
-55°C to 125°C	100 μV 500 μV	— TLE2021MD	—	TLE2021BMFK TLE2021MFK	TLE2021BMJG TLE2021MJG	— TLE2021MP	—	—

<sup>†</sup> The D packages are available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TLE2021CDR).

<sup>‡</sup> The DB and PW packages are only available left-end taped and reeled.

<sup>§</sup> Chip forms are tested at 25°C only.

## TLE2022 AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES						CHIP FORM <sup>§</sup> (Y)
		SMALL OUTLINE <sup>†</sup> (D)	SSOP <sup>‡</sup> (DB)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP <sup>‡</sup> (PW)	
0°C to 70°C	150 μV 300 μV 500 μV	TLE2022BCD TLE2022ACD TLE2022CD	— — TLE2022CDBLE	—	—	— TLE2022ACP TLE2022CP	— — TLE2022CPWLE	— — TLE2022Y
-40°C to 85°C	150 μV 300 μV 500 μV	TLE2022BID TLE2022AID TLE2022ID	—	—	—	— TLE2022AIP TLE2022IP	—	—
-55°C to 125°C	150 μV 300 μV 500 μV	— TLE2022AMD TLE2022MD	—	— TLE2022AMFK TLE2022MFK	TLE2022BMJG TLE2022AMJG TLE2022MJG	— TLE2022AMP TLE2022MP	—	—

<sup>†</sup> The D packages are available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TLE2022CDR).

<sup>‡</sup> The DB and PW packages are only available left-end taped and reeled.

<sup>§</sup> Chip forms are tested at 25°C only.

## TLE2024 AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGED DEVICES				CHIP FORM <sup>§</sup> (Y)
		SMALL OUTLINE (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	500 μV 750 μV 1000 μV	TLE2024BCDW TLE2024ACDW TLE2024CDW	—	—	TLE2024BCN TLE2024ACN TLE2024CN	— — TLE2024Y
-40°C to 85°C	500 μV 750 μV 1000 μV	TLE2024BIDW TLE2024AIDW TLE2024IDW	—	—	TLE2024BIN TLE2024AIN TLE2024IN	—
-55°C to 125°C	500 μV 750 μV 1000 μV	TLE2024BMDW TLE2024AMDW TLE2024MDW	TLE2024BMFK TLE2024AMFK TLE2024MFK	TLE2024BMJ TLE2024AMJ TLE2024MJ	TLE2024BMN TLE2024AMN TLE2024MN	—

<sup>§</sup> Chip forms are tested at 25°C only.



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**TLE2021**  
D, DB, JG, P, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

**TLE2021**  
FK PACKAGE  
(TOP VIEW)

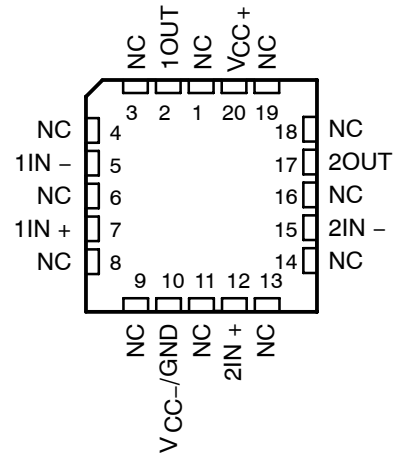


**D, DB, JG, P, OR PW PACKAGE**  
(TOP VIEW)



NC – No internal connection

**FK PACKAGE**  
(TOP VIEW)



**DW PACKAGE**  
(TOP VIEW)



**FK PACKAGE**  
(TOP VIEW)



**J OR N PACKAGE**  
(TOP VIEW)



NC – No internal connection

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TLE2021Y chip information

This chip, when properly assembled, display characteristics similar to the TLE2021. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.



# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TLE2022Y chip information

This chip, when properly assembled, displays characteristics similar to TLE2022. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.



# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TLE2024Y chip information

This chip, when properly assembled, displays characteristics similar to the TLE2024. Thermal compression or ultrasonic bonding may be used on the doped aluminum-bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.



# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT			
COMPONENT	TLE2021	TLE2022	TLE2024
Transistors	40	80	160
Resistors	7	14	28
Diodes	4	8	16
Capacitors	4	8	16

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC+}$ (see Note 1)	20 V
Supply voltage, $V_{CC-}$ (see Note 1)	-20 V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm 0.6$ V
Input voltage range, $V_I$ (any input, see Note 1)	$\pm V_{CC}$
Input current, $I_I$ (each input)	$\pm 1$ mA
Output current, $I_O$ (each output):	
TLE2021	$\pm 20$ mA
TLE2022	$\pm 30$ mA
TLE2024	$\pm 40$ mA
Total current into $V_{CC+}$	80 mA
Total current out of $V_{CC-}$	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : C suffix	0°C to 70°C
I suffix	-40°C to 85°C
M suffix	-55°C to 125°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Case temperature for 60 seconds, $T_C$ : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DP, P, or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  - Differential voltages are at  $IN+$  with respect to  $IN-$ . Excessive current flows if a differential input voltage in excess of approximately  $\pm 600$  mV is applied between the inputs unless some limiting resistance is used.
  - The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D-8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DB-8	525 mW	4.2 mW/°C	336 mW	—	—
DW-16	1025 mW	8.2 mW/°C	656 mW	533 mW	205 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J-14	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG-8	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N-14	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P-8	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW-8	525 mW	4.2 mW/°C	336 mW	—	—

## recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC}$		$\pm 2$	$\pm 20$	$\pm 2$	$\pm 20$	$\pm 2$	$\pm 20$	V
Common-mode input voltage, $V_{IC}$	$V_{CC} = \pm 5$ V	0	3.5	0	3.2	0	3.2	V
	$V_{CC\pm} = \pm 15$ V	-15	13.5	-15	13.2	-15	13.2	
Operating free-air temperature, $T_A$		0	70	-40	85	-55	125	°C



**TLE2021 electrical characteristics at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2021C			TLE2021AC			TLE2021BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage		25°C	120	600		100	300		80	200	$\mu\text{V}$	
		Full range		850		600		300				
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		Full range	2			2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	0.005			0.005			0.005			$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C	0.2	6		0.2	6		0.2	6	nA	
	Full range	10			10			10				
$I_{IB}$ Input bias current		25°C	25	70		25	70		25	70	nA	
		Full range	90			90			90			
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4		0 to 3.5	-0.3 to 4		0 to 3.5	-0.3 to 4	V	
		Full range	0 to 3.5			0 to 3.5			0 to 3.5			
$V_{OH}$ High-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	4	4.3		4	4.3		4	4.3	V	
		Full range	3.9			3.9			3.9			
$V_{OL}$ Low-level output voltage		25°C	0.7		0.8	0.7		0.8	0.7		0.8	V
		Full range	0.85			0.85			0.85			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.4\text{ V to }4\text{ V}, R_L = 10\ \text{k}\Omega$	25°C	0.3	1.5		0.3	1.5		0.3	1.5		$\text{V}/\mu\text{V}$
		Full range	0.3			0.3			0.3			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\text{min}}, R_S = 50\ \Omega$	25°C	85	110		85	110		85	110		dB
		Full range	80			80			80			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC} = 5\text{ V to }30\text{ V}$	25°C	105	120		105	120		105	120		dB
		Full range	100			100			100			
$I_{CC}$ Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C	200		300	200		300	200		300	$\mu\text{A}$
		Full range	300			300			300			
$\Delta I_{CC}$ Supply-current change over operating temperature range		Full range	5			5			5			$\mu\text{A}$

$^\dagger$  Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2021 electrical characteristics at specified free-air temperature,  $V_{CC} = \pm 15\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2021C			TLE2021AC			TLE2021BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		120	500		80	200		40	100	$\mu\text{V}$
		Full range			750			500			200	
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C		0.2	6		0.2	6		0.2	6	nA
		Full range			10			10			10	
$I_{IB}$ Input bias current	25°C		25	70		25	70		25	70	nA	
	Full range			90			90			90		
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14	V	
		Full range	-15 to 13.5			-15 to 13.5			-15 to 13.5			
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	14	14.3		14	14.3		14	14.3	V	
		Full range	13.9			13.9			13.9			
$V_{OM-}$ Maximum negative peak output voltage swing		25°C	-13.7	-14.1		-13.7	-14.1		-13.7	-14.1	V	
		Full range	-13.7			-13.7			-13.7			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	1	6.5		1	6.5		1	6.5	$\text{V}/\mu\text{V}$	
		Full range	1			1			1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\ \text{min}, R_S = 50\ \Omega$	25°C	100	115		100	115		100	115	dB	
		Full range	96			96			96			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5\ \text{V}$ to $\pm 15\ \text{V}$	25°C	105	120		105	120		105	120	dB	
		Full range	100			100			100			
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$	25°C		240	350		240	350		240	350	$\mu\text{A}$
		Full range			350			350			350	
$\Delta I_{CC}$ Supply-current change over operating temperature range		Full range		6			6			6		$\mu\text{A}$

$^\dagger$  Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2022 electrical characteristics at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2022C			TLE2022AC			TLE2022BC			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$V_{IO}$ Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	600			400			250			$\mu\text{V}$	
		Full range	800			550			400				
$^\circ V_{IO}$ Temperature coefficient of input offset voltage		Full range	2			2			2			$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			0.005			$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C	0.5	6		0.4	6		0.3	6		nA	
		Full range	10			10			10				
$I_{IB}$ Input bias current	25°C	35	70		33	70		30	70		nA		
	Full range	90			90			90					
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4	V		
		Full range	0 to 3.5		0 to 3.5		0 to 3.5		0 to 3.5				
$V_{OH}$ High-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	4	4.3		4	4.3		4	4.3		V	
Full range		3.9			3.9			3.9					
$V_{OL}$ Low-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	0.7		0.8		0.7	0.8		0.7	0.8		V
		Full range	0.85			0.85			0.85				
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.4\ \text{V to } 4\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	0.3	1.5		0.4	1.5		0.5	1.5		$\text{V}/\mu\text{V}$	
		Full range	0.3			0.4			0.5				
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50\ \Omega$	25°C	85	100		87	102		90	105		dB	
		Full range	80			82			85				
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC} \pm / \Delta V_{IO}$ )	$V_{CC} = 5\ \text{V to } 30\ \text{V}$	25°C	100	115		103	118		105	120		dB	
		Full range	95			98			100				
$I_{CC}$ Supply current	$V_O = 2.5\ \text{V}, \text{ No load}$	25°C	450	600		450	600		450	600		$\mu\text{A}$	
		Full range	600			600			600				
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range	7			7			7			$\mu\text{A}$	

$^\dagger$  Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2022 electrical characteristics at specified free-air temperature,  $V_{CC} = \pm 15\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2022C			TLE2022AC			TLE2022BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		150	500		120	300		70	150	$\mu\text{V}$
		Full range			700			450			300	
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C		0.5	6		0.4	6		0.3	6	nA
		Full range			10			10			10	
$I_{IB}$ Input bias current	25°C		35	70		33	70		30	70	nA	
	Full range			90			90			90		
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14	V	
		Full range	-15 to 13.5			-15 to 13.5			-15 to 13.5			
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	14	14.3		14	14.3		14	14.3	V	
		Full range	13.9			13.9			13.9			
$V_{OM-}$ Maximum negative peak output voltage swing		25°C	-13.7	-14.1		-13.7	-14.1		-13.7	-14.1	V	
		Full range	-13.7			-13.7			-13.7			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	0.8	4		1	7		1.5	10	$\text{V}/\mu\text{V}$	
		Full range	0.8			1			1.5			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50\ \Omega$	25°C	95	106		97	109		100	112	dB	
		Full range	91			93			96			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}$	25°C	100	115		103	118		105	120	dB	
		Full range	95			98			100			
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$	25°C		550	700		550	700		550	700	$\mu\text{A}$
		Full range			700			700			700	
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range		9			9			9		$\mu\text{A}$

$^\dagger$  Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2024 electrical characteristics at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLE2024C			TLE2024AC			TLE2024BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0,$ $R_S = 50\ \Omega$	25°C	1100			850			600			$\mu\text{V}$
		Full range	1300			1050			800			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range	2			2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			0.005			$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C	0.6	6		0.5	6		0.4	6		nA
		Full range	10			10			10			
$I_{IB}$ Input bias current	25°C	45	70		40	70		35	70		nA	
	Full range	90			90			90				
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4	V	
		Full range	0 to 3.5		0 to 3.5		0 to 3.5		0 to 3.5			
$V_{OH}$ High-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	3.9	4.2		3.9	4.2		4	4.3		V
		Full range	3.7			3.7			3.8			
$V_{OL}$ Low-level output voltage		25°C	0.7		0.8		0.7		0.8		V	
		Full range	0.95			0.95			0.95			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.4\ \text{V to } 4\ \text{V},$ $R_L = 10\ \text{k}\Omega$	25°C	0.2	1.5		0.3	1.5		0.4	1.5		$\text{V}/\mu\text{V}$
		Full range	0.1			0.1			0.1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin},$ $R_S = 50\ \Omega$	25°C	80	90		82	92		85	95		dB
		Full range	80			82			85			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC} = 5\ \text{V to } 30\ \text{V}$	25°C	98	112		100	115		103	117		dB
		Full range	93			95			98			
$I_{CC}$ Supply current	$V_O = 2.5\ \text{V},$ No load	25°C	800	1200		800	1200		800	1200		$\mu\text{A}$
		Full range	1200			1200			1200			
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range	15			15			15			$\mu\text{A}$

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2024 electrical characteristics at specified free-air temperature,  $V_{CC} = \pm 15\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2024C			TLE2024AC			TLE2024BC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	1000			750			500			$\mu\text{V}$
		Full range	1200			950			700			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range	2			2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.006			0.006			0.006			$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C	0.6	6		0.5	6		0.4	6	nA	
		Full range	10			10			10			
$I_{IB}$ Input bias current	25°C	50	70		45	70		40	70	nA		
	Full range	90			90			90				
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14	V	
		Full range	-15 to 13.5			-15 to 13.5			-15 to 13.5			
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	13.8	14.1		13.9	14.2		14	14.3	V	
		Full range	13.7			13.8			13.9			
$V_{OM-}$ Maximum negative peak output voltage swing		25°C	-13.7	-14.1		-13.7	-14.1		-13.7	-14.1	V	
		Full range	-13.6			-13.6			-13.6			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	0.4	2		0.8	4		1	7	$\text{V}/\mu\text{V}$	
		Full range	0.4			0.8			1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50\ \Omega$	25°C	92	102		94	105		97	108	dB	
		Full range	88			90			93			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}$	25°C	98	112		100	115		103	117	dB	
		Full range	93			95			98			
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$	25°C	1050	1400		1050	1400		1050	1400	$\mu\text{A}$	
		Full range	1400			1400			1400			
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range	20			20			20			$\mu\text{A}$

$^\dagger$  Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2021 electrical characteristics at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLE2021I			TLE2021AI			TLE2021BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage		25°C		120	600		100	300		80	200	$\mu\text{V}$
		Full range			950			600			300	
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range		2			2			2	$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		0.005			0.005			0.005	$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C		0.2	6		0.2	6		0.2	6	nA
		Full range			10			10			10	
$I_{IB}$ Input bias current		25°C		25	70		25	70		25	70	nA
	Full range			90			90			90		
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4		0 to 3.5	-0.3 to 4		0 to 3.5	-0.3 to 4	V	
		Full range	0 to 3.2			0 to 3.2			0 to 3.2			
$V_{OH}$ High-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	4	4.3		4	4.3		4	4.3	V	
		Full range	3.9			3.9			3.9			
$V_{OL}$ Low-level output voltage		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
		Full range			0.9			0.9			0.9	
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.4\text{ V to }4\text{ V}, R_L = 10\ \text{k}\Omega$	25°C	0.3	1.5		0.3	1.5		0.3	1.5	$\text{V}/\mu\text{V}$	
		Full range	0.25			0.25			0.25			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\ \text{min}, R_S = 50\ \Omega$	25°C	85	110		85	110		85	110	dB	
		Full range	80			80			80			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC} = 5\text{ V to }30\text{ V}$	25°C	105	120		105	120		105	120	dB	
		Full range	100			100			100			
$I_{CC}$ Supply current	$V_O = 2.5\text{ V},$ No load	25°C		200	300		200	300		200	300	$\mu\text{A}$
		Full range			300			300			300	
$\Delta I_{CC}$ Supply-current change over operating temperature range		Full range		6			6			6	$\mu\text{A}$	

† Full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2021 electrical characteristics at specified free-air temperature,  $V_{CC} = \pm 15\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2021I			TLE2021AI			TLE2021BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage		25°C		120	500		80	200		40	100	$\mu\text{V}$
		Full range			850			500			200	
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range		2			2			2	$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		0.006			0.006			0.006	$\mu\text{V}/\text{mo}$	
$I_{IO}$ Input offset current		25°C		0.2	6		0.2	6		0.2	6	nA
	Full range			10			10			10		
$I_{IB}$ Input bias current		25°C		25	70		25	70		25	70	nA
		Full range			90			90			90	
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14	V	
		Full range	-15 to 13.2			-15 to 13.2			-15 to 13.2			
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	14	14.3		14	14.3		14	14.3	V	
		Full range	13.9			13.9			13.9			
$V_{OM-}$ Maximum negative peak output voltage swing		25°C	-13.7	-14.1		-13.7	-14.1		-13.7	-14.1	V	
		Full range	-13.6			-13.6			-13.6			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 10\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	1	6.5		1	6.5		1	6.5	$\text{V}/\mu\text{V}$	
		Full range	0.75			0.75			0.75			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\ \text{min}}, R_S = 50\ \Omega$	25°C	100	115		100	115		100	115	dB	
		Full range	96			96			96			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5\ \text{V}$ to $\pm 15\ \text{V}$	25°C	105	120		105	120		105	120	dB	
		Full range	100			100			100			
$I_{CC}$ Supply current	$V_O = 0\ \text{V}, \text{No load}$	25°C		240	350		240	350		240	350	$\mu\text{A}$
		Full range			350			350			350	
$\Delta I_{CC}$ Supply-current change over operating temperature range		Full range		7			7			7	$\mu\text{A}$	

$^\dagger$  Full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2022 electrical characteristics at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2022I			TLE2022AI			TLE2022BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	600			400			250			$\mu\text{V}$
		Full range	800			550			400			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range	2			2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			0.005			$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C	0.5	6		0.4	6		0.3	6		nA
		Full range	10			10			10			
$I_{IB}$ Input bias current		25°C	35	70		33	70		30	70		nA
		Full range	90			90			90			
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4		0 to 3.5	-0.3 to 4		0 to 3.5	-0.3 to 4	V	
		Full range	0 to 3.2			0 to 3.2			0 to 3.2			
$V_{OH}$ High-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	4	4.3		4	4.3		4	4.3	V	
		Full range	3.9			3.9			3.9			
$V_{OL}$ Low-level output voltage		25°C		0.7	0.8		0.7	0.8		0.7	0.8	V
		Full range	0.9			0.9			0.9			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.4\ \text{V to } 4\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	0.3	1.5		0.4	1.5		0.5	1.5	$\text{V}/\mu\text{V}$	
		Full range	0.2			0.2			0.2			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\text{min}}, R_S = 50\ \Omega$	25°C	85	100		87	102		90	105	dB	
		Full range	80			82			85			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = 5\ \text{V to } 30\ \text{V}$	25°C	100	115		103	118		105	120	dB	
		Full range	95			98			100			
$I_{CC}$ Supply current	$V_O = 2.5\ \text{V}, \text{ No load}$	25°C		450	600		450	600		450	600	$\mu\text{A}$
		Full range	600			600			600			
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range	15			15			15			$\mu\text{A}$

$^\dagger$  Full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2022 electrical characteristics at specified free-air temperature,  $V_{CC} = \pm 15\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2022I			TLE2022AI			TLE2022BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C		150	500		120	300		70	150	$\mu\text{V}$
		Full range			700			450			300	
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C		0.5	6		0.4	6		0.3	6	nA
		Full range			10			10			10	
$I_{IB}$ Input bias current	25°C		35	70		33	70		30	70	nA	
	Full range			90			90			90		
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14	V	
		Full range	-15 to 13.2			-15 to 13.2			-15 to 13.2			
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	14	14.3		14	14.3		14	14.3	V	
		Full range	13.9			13.9			13.9			
$V_{OM-}$ Maximum negative peak output voltage swing		25°C	-13.7	-14.1		-13.7	-14.1		-13.7	-14.1	V	
		Full range	-13.6			-13.6			-13.6			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	0.8	4		1	7		1.5	10	$\text{V}/\mu\text{V}$	
		Full range	0.8			1			1.5			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50\ \Omega$	25°C	95	106		97	109		100	112	dB	
		Full range	91			93			96			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 2.5\ \text{V to } \pm 15\ \text{V}$	25°C	100	115		103	118		105	120	dB	
		Full range	95			98			100			
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$	25°C		550	700		550	700		550	700	$\mu\text{A}$
		Full range			700			700			700	
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range		30			30			30		$\mu\text{A}$

$^\dagger$  Full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2024 electrical characteristics at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2024I			TLE2024AI			TLE2024BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage		25°C	1100			850			600			$\mu\text{V}$
		Full range	1300			1050			800			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range	2			2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0,$ $R_S = 50\ \Omega$	25°C	0.005			0.005			0.005			$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C	0.6	6	0.5	6	0.4	6				nA
	Full range	10			10			10				
$I_{IB}$ Input bias current		25°C	45	70	40	70	35	70			nA	
		Full range	90			90			90			
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4			V	
		Full range	0 to 3.2		0 to 3.2		0 to 3.2					
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	3.9	4.2	3.9	4.2	4	4.3			V	
		Full range	3.7			3.7			3.8			
$V_{OM-}$ Maximum negative peak output voltage swing		25°C	0.7		0.8		0.7		0.8		V	
		Full range	0.95			0.95			0.95			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.4\ \text{V to } 4\ \text{V},$ $R_L = 10\ \text{k}\Omega$	25°C	0.2	1.5	0.3	1.5	0.4	1.5			$\text{V}/\mu\text{V}$	
		Full range	0.1			0.1			0.1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\text{min}},$ $R_S = 50\ \Omega$	25°C	80	90	82	92	85	95			dB	
		Full range	80			82			85			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}$	25°C	98	112	100	115	103	117			dB	
		Full range	93			95			98			
$I_{CC}$ Supply current	$V_O = 0,$ No load	25°C	800	1200	800	1200	800	1200			$\mu\text{A}$	
		Full range	1200			1200			1200			
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range	30			30			30			$\mu\text{A}$

$^\dagger$  Full range is  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2024 electrical characteristics at specified free-air temperature,  $V_{CC} = \pm 15$  V (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2024I			TLE2024AI			TLE2024BI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, R_S = 50 \Omega$	25°C	1000			750			500			$\mu V$
		Full range	1200			950			700			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range	2			2			2			$\mu V/^\circ C$
Input offset voltage long-term drift (see Note 4)		25°C	0.006			0.006			0.006			$\mu V/mo$
$I_{IO}$ Input offset current		25°C	0.6	6	0.5	6	0.4	6				nA
		Full range	10			10			10			
$I_{IB}$ Input bias current	25°C	50	70	45	70	40	70				nA	
	Full range	90			90			90				
$V_{ICR}$ Common-mode input voltage range	$R_S = 50 \Omega$	25°C	-15 to 13.5	-15.3 to 14	-15 to 13.5	-15.3 to 14	-15 to 13.5	-15.3 to 14			V	
		Full range	-15 to 13.2		-15 to 13.2		-15 to 13.2					
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10 k\Omega$	25°C	13.8	14.1	13.9	14.2	14	14.3			V	
		Full range	13.7			13.7			13.8			
$V_{OM-}$ Maximum negative peak output voltage swing		25°C	-13.7	-14.1	-13.7	-14.1	-13.7	-14.1			V	
		Full range	-13.6			-13.6			-13.6			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10 k\Omega$	25°C	0.4	2	0.8	4	1	7			V/ $\mu V$	
		Full range	0.4			0.8			1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50 \Omega$	25°C	92	102	94	105	97	108			dB	
		Full range	88			90			93			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5$ V to $\pm 15$ V	25°C	98	112	100	115	103	117			dB	
		Full range	93			95			98			
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$	25°C	1050	1400	1050	1400	1050	1400			$\mu A$	
		Full range	1400			1400			1400			
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range	50			50			50			$\mu A$

$^\dagger$  Full range is  $-40^\circ C$  to  $85^\circ C$ .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ C$  extrapolated to  $T_A = 25^\circ C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2021 electrical characteristics at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLE2021M			TLE2021BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	$V_{IC} = 0,$ $R_S = 50\ \Omega$	25°C	120	600		80	200	$\mu\text{V}$	
			Full range		1100		300			
$\alpha_{VIO}$	Temperature coefficient of input offset voltage		Full range	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)			25°C	0.005			0.005		$\mu\text{V}/\text{mo}$	
$I_{IO}$	Input offset current		25°C	0.2	6		0.2	6	nA	
			Full range		10		10			
$I_{IB}$	Input bias current		25°C	25	70		25	70	nA	
			Full range		90		90			
$V_{ICR}$	Common-mode input voltage range		$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4		0 to 3.5	-0.3 to 4	V
				Full range	0 to 3.2			0 to 3.2		
$V_{OH}$	High-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	4	4.3		4	4.3	V	
			Full range	3.8			3.8			
$V_{OL}$	Low-level output voltage		25°C		0.7	0.8		0.7	0.8	V
			Full range		0.95		0.95			
$A_{VD}$	Large-signal differential voltage amplification		$V_O = 1.4\ \text{V to } 4\ \text{V},$ $R_L = 10\ \text{k}\Omega$	25°C	0.3	1.5		0.3	1.5	$\text{V}/\mu\text{V}$
				Full range	0.1			0.1		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin},$ $R_S = 50\ \Omega$	25°C	85	110		85	110	dB	
			Full range	80			80			
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = 5\ \text{V to } 30\ \text{V}$	25°C	105	120		105	120	dB	
			Full range	100			100			
$I_{CC}$	Supply current	$V_O = 2.5\ \text{V},$ No load	25°C	170	230		170	230	$\mu\text{A}$	
			Full range		230		230			
$\Delta I_{CC}$	Supply current change over operating temperature range		Full range		9		9		$\mu\text{A}$	

$^\dagger$  Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2021 electrical characteristics at specified free-air temperature,  $V_{CC} = \pm 15$  V (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLE2021M			TLE2021BM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, R_S = 50 \Omega$	25°C		120	500		40	100	$\mu$ V
		Full range			1000			200	
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range		2			2		$\mu$ V/°C
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006		$\mu$ V/mo
$I_{IO}$ Input offset current		25°C		0.2	6		0.2	6	nA
		Full range			10			10	
$I_{IB}$ Input bias current	25°C		25	70		25	70	nA	
	Full range			90			90		
$V_{ICR}$ Common-mode input voltage range	$R_S = 50 \Omega$	25°C	-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14	V	
		Full range	-15 to 13.2			-15 to 13.2			
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10 k\Omega$	25°C	14	14.3		14	14.3	V	
		Full range	13.8			13.8			
$V_{OM-}$ Maximum negative peak output voltage swing		25°C	-13.7	-14.1		-13.7	-14.1	V	
		Full range	-13.6			-13.6			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10 k\Omega$	25°C	1	6.5		1	6.5	V/ $\mu$ V	
		Full range	0.5			0.5			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50 \Omega$	25°C	100	115		100	115	dB	
		Full range	96			96			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5$ V to $\pm 15$ V	25°C	105	120		105	120	dB	
		Full range	100			100			
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$	25°C		200	300		200	300	$\mu$ A
		Full range			300			300	
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range		10			10		$\mu$ A

† Full range is -55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2022 electrical characteristics at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2022M			TLE2022AM			TLE2022BM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	600			400			250			$\mu\text{V}$
		Full range	800			550			400			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range	2			2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			0.005			$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C	0.5	6		0.4	6		0.3	6		nA
		Full range	10			10			10			
$I_{IB}$ Input bias current	25°C	35	70		33	70		30	70		nA	
	Full range	90			90			90				
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4		0 to 3.5	-0.3 to 4		0 to 3.5	-0.3 to 4	V	
		Full range	0 to 3.2			0 to 3.2			0 to 3.2			
$V_{OH}$ High-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	4	4.3		4	4.3		4	4.3	V	
		Full range	3.8			3.8			3.8			
$V_{OL}$ Low-level output voltage		25°C	0.7	0.8		0.7	0.8		0.7	0.8	V	
		Full range	0.95			0.95			0.95			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.4\ \text{V to } 4\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	0.3	1.5		0.4	1.5		0.5	1.5	$\text{V}/\mu\text{V}$	
		Full range	0.1			0.1			0.1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50\ \Omega$	25°C	85	100		87	102		90	105	dB	
		Full range	80			82			85			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = 5\ \text{V to } 30\ \text{V}$	25°C	100	115		103	118		105	120	dB	
		Full range	95			98			100			
$I_{CC}$ Supply current	$V_O = 2.5\ \text{V}, \text{ No load}$	25°C	450	600		450	600		450	600	$\mu\text{A}$	
		Full range	600			600			600			
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range	37			37			37			$\mu\text{A}$

$^\dagger$  Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2022 electrical characteristics at specified free-air temperature,  $V_{CC} = \pm 15$  V (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2022M			TLE2022AM			TLE2022BM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, R_S = 50 \Omega$	25°C		150	500		120	300		70	150	$\mu V$
		Full range			700			450			300	
$^{\circ}V_{IO}$ Temperature coefficient of input offset voltage		Full range		2			2			2		$\mu V/^{\circ}C$
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006			0.006		$\mu V/mo$
$I_{IO}$ Input offset current		25°C		0.5	6		0.4	6		0.3	6	nA
		Full range			10			10			10	
$I_{IB}$ Input bias current	25°C		35	70		33	70		30	70	nA	
	Full range			90			90			90		
$V_{ICR}$ Common-mode input voltage range	$R_S = 50 \Omega$	25°C	-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14	V	
		Full range	-15 to 13.2			-15 to 13.2			-15 to 13.2			
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10 k\Omega$	25°C	14	14.3		14	14.3		14	14.3	V	
		Full range	13.9			13.9			13.9			
$V_{OM-}$ Maximum negative peak output voltage swing		25°C	-13.7	-14.1		-13.7	-14.1		-13.7	-14.1	V	
		Full range	-13.6			-13.6			-13.6			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10 k\Omega$	25°C	0.8	4		1	7		1.5	10	$V/\mu V$	
		Full range	0.8			1			1.5			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50 \Omega$	25°C	95	106		97	109		100	112	dB	
		Full range	91			93			96			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5$ V to $\pm 15$ V	25°C	100	115		103	118		105	120	dB	
		Full range	95			98			100			
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$	25°C		550	700		550	700		550	700	$\mu A$
		Full range			700			700			700	
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range		60			60			60		$\mu A$

$^\dagger$  Full range is  $-55^{\circ}C$  to  $125^{\circ}C$ .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^{\circ}C$  extrapolated to  $T_A = 25^{\circ}C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2024 electrical characteristics at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2024M			TLE2024AM			TLE2024BM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage		25°C	1100			850			600			$\mu\text{V}$
		Full range	1300			1050			800			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range	2			2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0,$ $R_S = 50\ \Omega$	25°C	0.005			0.005			0.005			$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current		25°C	0.6	6	0.5	6	0.4	6				nA
	Full range	10			10			10				
$I_{IB}$ Input bias current		25°C	45	70	40	70	35	70				nA
		Full range	90			90			90			
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4				V
		Full range	0 to 3.2		0 to 3.2		0 to 3.2					
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	3.9	4.2	3.9	4.2	4	4.3				V
		Full range	3.7		3.7		3.8					
$V_{OM-}$ Maximum negative peak output voltage swing		25°C	0.7 0.8		0.7 0.8		0.7 0.8					V
		Full range	0.95			0.95			0.95			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.4\ \text{V to } 4\ \text{V},$ $R_L = 10\ \text{k}\Omega$	25°C	0.2	1.5	0.3	1.5	0.4	1.5				$\text{V}/\mu\text{V}$
		Full range	0.1		0.1		0.1					
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\text{min}},$ $R_S = 50\ \Omega$	25°C	80	90	82	92	85	95				dB
		Full range	80		82		85					
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}$	25°C	98	112	100	115	103	117				dB
		Full range	93		95		98					
$I_{CC}$ Supply current	$V_O = 0,$ No load	25°C	800	1200	800	1200	800	1200				$\mu\text{A}$
		Full range	1200			1200			1200			
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range	50			50			50			$\mu\text{A}$

$^\dagger$  Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2024 electrical characteristics at specified free-air temperature,  $V_{CC} = \pm 15$  V (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLE2024M			TLE2024AM			TLE2024BM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage		25°C	1000			750			500			$\mu$ V
		Full range	1200			950			700			
$\alpha_{VIO}$ Temperature coefficient of input offset voltage	$V_{IC} = 0, R_S = 50 \Omega$	Full range	2			2			2			$\mu$ V/°C
Input offset voltage long-term drift (see Note 4)		25°C	0.006			0.006			0.006			$\mu$ V/mo
$I_{IO}$ Input offset current		25°C	0.6	6	0.5	6	0.4	6	nA			
		Full range	10			10						
$I_{IB}$ Input bias current		25°C	50	70	45	70	40	70	nA			
		Full range	90			90						
$V_{ICR}$ Common-mode input voltage range	$R_S = 50 \Omega$	25°C	-15 to 13.5	-15.3 to 14	-15 to 13.5	-15.3 to 14	-15 to 13.5	-15.3 to 14	V			
		Full range	-15 to 13.2		-15 to 13.2		-15 to 13.2					
$V_{OM+}$ Maximum positive peak output voltage swing	$R_L = 10 \text{ k}\Omega$	25°C	13.8	14.1	13.9	14.2	14	14.3	V			
		Full range	13.7			13.8						
$V_{OM-}$ Maximum negative peak output voltage swing		25°C	-13.7	-14.1	-13.7	-14.1	-13.7	-14.1	V			
		Full range	-13.6			-13.6						
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 10 \text{ k}\Omega$	25°C	0.4	2	0.8	4	1	7	V/ $\mu$ V			
		Full range	0.4			0.8						
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50 \Omega$	25°C	92	102	94	105	97	108	dB			
		Full range	88			90						
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5$ V to $\pm 15$ V	25°C	98	112	100	115	103	117	dB			
		Full range	93			95						
$I_{CC}$ Supply current	$V_O = 0, \text{ No load}$	25°C	1050	1400	1050	1400	1050	1400	$\mu$ A			
		Full range	1400			1400						
$\Delta I_{CC}$ Supply current change over operating temperature range		Full range	85			85			$\mu$ A			

$^\dagger$  Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLE2021 operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	$T_A$	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$ , See Figure 1	25°C			0.5			0.5			V/ $\mu\text{s}$
$V_n$	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C			21 50			21 50			nV/Hz
		f = 1 kHz	25°C			17 30			17 30			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C			0.16			0.16			$\mu\text{V}$
		f = 0.1 to 10 Hz	25°C			0.47			0.47			
$I_n$	Equivalent input noise current		25°C			0.09			0.09			pA/Hz
$B_1$	Unity-gain bandwidth	See Figure 3	25°C			1.2			1.2			MHz
$\phi_m$	Phase margin at unity gain	See Figure 3	25°C			42°			42°			

**TLE2021 operating characteristics at specified free-air temperature,  $V_{CC} = \pm 15\text{ V}$**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$ , See Figure 1	25°C			0.45 0.65			0.45 0.65			V/ $\mu\text{s}$
			Full range			0.45			0.42			
$V_n$	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C			19 50			19 50			nV/Hz
		f = 1 kHz	25°C			15 30			15 30			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C			0.16			0.16			$\mu\text{V}$
		f = 0.1 to 10 Hz	25°C			0.47			0.47			
$I_n$	Equivalent input noise current		25°C			0.09			0.09			pA/Hz
$B_1$	Unity-gain bandwidth	See Figure 3	25°C			2			2			MHz
$\phi_m$	Phase margin at unity gain	See Figure 3	25°C			46°			46°			

<sup>†</sup> Full range is 0°C to 70°C for the C-suffix devices, –40°C to 85°C for the I-suffix devices, and –55°C to 125°C for the M-suffix devices.

**TLE2022 operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$** 

PARAMETER	TEST CONDITIONS	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$ , See Figure 1			0.5			0.5			$\text{V}/\mu\text{s}$
$V_n$	Equivalent input noise voltage (see Figure 2)	f = 10 Hz			21			21			$\text{nV}/\sqrt{\text{Hz}}$
		f = 1 kHz			17			17			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz			0.16			0.16			$\mu\text{V}$
		f = 0.1 to 10 Hz			0.47			0.47			
$I_n$	Equivalent input noise current	0.1			0.1			0.1			$\text{pA}/\sqrt{\text{Hz}}$
$B_1$	Unity-gain bandwidth	See Figure 3			1.7			1.7			MHz
$\phi_m$	Phase margin at unity gain	See Figure 3			47°			47°			

**TLE2022 operating characteristics at specified free-air temperature,  $V_{CC} = \pm 15\text{ V}$** 

PARAMETER	TEST CONDITIONS	$T_A$	C SUFFIX†			I SUFFIX†			M SUFFIX†			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 10\text{ V}$ , See Figure 1	25°C			0.45			0.45			$\text{V}/\mu\text{s}$
			Full range			0.45			0.42			
$V_n$	Equivalent input noise voltage (see Figure 2)	25°C	f = 10 Hz			19			19			$\text{nV}/\sqrt{\text{Hz}}$
			f = 1 kHz			15			15			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	25°C	f = 0.1 to 1 Hz			0.16			0.16			$\mu\text{V}$
			f = 0.1 to 10 Hz			0.47			0.47			
$I_n$	Equivalent input noise current	25°C	0.1			0.1			0.1			$\text{pA}/\sqrt{\text{Hz}}$
$B_1$	Unity-gain bandwidth	25°C	See Figure 3			2.8			2.8			MHz
$\phi_m$	Phase margin at unity gain	25°C	See Figure 3			52°			52°			

† Full range is 0°C to 70°C for the C-suffix devices, -40°C to 85°C for the I suffix devices and -55°C to 125°C for the I-suffix devices.

**TLE2024 operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	C SUFFIX			I SUFFIX			M SUFFIX			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$ , See Figure 1			0.5			0.5			$\text{V}/\mu\text{s}$
$V_n$	Equivalent input noise voltage (see Figure 2)	f = 10 Hz			21 50			21 50			$\text{nV}/\sqrt{\text{Hz}}$
		f = 1 kHz			17 30			17 30			
$V_{N(\text{PP})}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz			0.16			0.16			$\mu\text{V}$
		f = 0.1 to 10 Hz			0.47			0.47			
$I_n$	Equivalent input noise current				0.1			0.1			$\text{pA}/\sqrt{\text{Hz}}$
$B_1$	Unity-gain bandwidth	See Figure 3			1.7			1.7			MHz
$\phi_m$	Phase margin at unity gain	See Figure 3			47°			47°			

**TLE2024 operating characteristics at specified free-air temperature,  $V_{CC} = \pm 15\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$	C SUFFIX†			I SUFFIX†			M SUFFIX†			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$25^\circ\text{C}$	0.45	0.7		0.45	0.7		0.45	0.7		$\text{V}/\mu\text{s}$
		Full range	0.45			0.42			0.4			
$V_n$	Equivalent input noise voltage (see Figure 2)	$25^\circ\text{C}$		19	50		19	50		19		$\text{nV}/\sqrt{\text{Hz}}$
		$25^\circ\text{C}$		15	30		15	30		15		
$V_{N(\text{PP})}$	Peak-to-peak equivalent input noise voltage	$25^\circ\text{C}$		0.16			0.16			0.16		$\mu\text{V}$
		$25^\circ\text{C}$		0.47			0.47			0.47		
$I_n$	Equivalent input noise current	$25^\circ\text{C}$		0.1			0.1			0.1	$\text{pA}/\sqrt{\text{Hz}}$	
$B_1$	Unity-gain bandwidth	$25^\circ\text{C}$		2.8			2.8			2.8	MHz	
$\phi_m$	Phase margin at unity gain	$25^\circ\text{C}$		52°			52°			52°		

† Full range is  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the C-suffix devices,  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  for the I suffix devices and  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for the I-suffix devices.

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TLE2021Y electrical characteristics at $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLE2021Y			UNIT
		MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0$ , $R_S = 50\ \Omega$		150		$\mu\text{V}$
Input offset voltage long-term drift (see Note 4)			0.005		$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current			0.5		nA
$I_{IB}$ Input bias current			35		nA
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$		- 0.3 to 4		V
$V_{OH}$ Maximum high-level output voltage	$R_L = 10\ \text{k}\Omega$		4.3		V
$V_{OL}$ Maximum low-level output voltage			0.7		V
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.4\ \text{to}\ 4\ \text{V}$ , $R_L = 10\ \text{k}\Omega$		1.5		$\text{V}/\mu\text{V}$
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\ \text{min}$ , $R_S = 50\ \Omega$		100		dB
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = 5\ \text{V}\ \text{to}\ 30\ \text{V}$		115		dB
$I_{CC}$ Supply current	$V_O = 2.5\ \text{V}$ , No load		400		$\mu\text{A}$

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

## TLE2021Y operating characteristics at $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLE2021Y			UNIT
		MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1\ \text{V}\ \text{to}\ 3\ \text{V}$		0.5		$\text{V}/\mu\text{s}$
$V_n$ Equivalent input noise voltage	$f = 10\ \text{Hz}$		21		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\ \text{kHz}$		17		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\ \text{to}\ 1\ \text{Hz}$		0.16		$\mu\text{V}$
	$f = 0.1\ \text{to}\ 10\ \text{Hz}$		0.47		
$I_n$ Equivalent input noise current			0.1		$\text{pA}/\sqrt{\text{Hz}}$
$B_1$ Unity-gain bandwidth			1.7		MHz
$\phi_m$ Phase margin at unity gain			47°		



# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TLE2022Y electrical characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLE2022Y			UNIT
		MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0$ , $R_S = 50\ \Omega$		150	600	$\mu\text{V}$
Input offset voltage long-term drift (see Note 4)			0.005		$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current			0.5		nA
$I_{IB}$ Input bias current			35		nA
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$		- 0.3 to 4		V
$V_{OH}$ Maximum high-level output voltage	$R_L = 10\ \text{k}\Omega$		4.3		V
$V_{OL}$ Maximum low-level output voltage			0.7		V
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.4\text{ to }4\ \text{V}$ , $R_L = 10\ \text{k}\Omega$		1.5		$\text{V}/\mu\text{V}$
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\ \text{min}$ , $R_S = 50\ \Omega$		100		dB
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm} / \Delta V_{IO}$ )	$V_{CC} = 5\ \text{V to }30\ \text{V}$		115		dB
$I_{CC}$ Supply current	$V_O = 2.5\ \text{V}$ , No load		450		$\mu\text{A}$

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

## TLE2022Y operating characteristics, $V_{CC} = 5\ \text{V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLE2022Y			UNIT
		MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1\ \text{V to }3\ \text{V}$ , See Figure 1		0.5		$\text{V}/\mu\text{s}$
$V_n$ Equivalent input noise voltage (see Figure 2)	$f = 10\ \text{Hz}$		21		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\ \text{kHz}$		17		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\ \text{to }1\ \text{Hz}$		0.16		$\mu\text{V}$
	$f = 0.1\ \text{to }10\ \text{Hz}$		0.47		
$I_n$ Equivalent input noise current			0.1		$\text{pA}/\sqrt{\text{Hz}}$
$B_1$ Unity-gain bandwidth	See Figure 3		1.7		MHz
$\phi_m$ Phase margin at unity gain	See Figure 3		47°		



# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TLE2024Y electrical characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLE2024Y			UNIT
		MIN	TYP	MAX	
Input offset voltage long-term drift (see Note 4)			0.005		$\mu\text{V}/\text{mo}$
$I_{IO}$ Input offset current	$V_{IC} = 0$ , $R_S = 50\ \Omega$		0.6		nA
$I_{IB}$ Input bias current			45		nA
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$		-0.3 to 4		V
$V_{OH}$ High-level output voltage	$R_L = 10\ \text{k}\Omega$		4.2		V
$V_{OL}$ Low-level output voltage			0.7		V
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.4\text{ V to }4\text{ V}$ , $R_L = 10\ \text{k}\Omega$		1.5		$\text{V}/\mu\text{V}$
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$ , $R_S = 50\ \Omega$		90		dB
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )	$V_{CC} = 5\text{ V to }30\text{ V}$		112		dB
$I_{CC}$ Supply current	$V_O = 2.5\text{ V}$ , No load		800		$\mu\text{A}$

NOTE 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

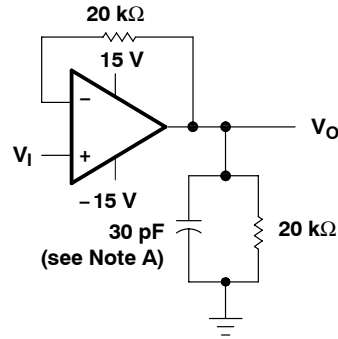
## TLE2024Y operating characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLE2024Y			UNIT
		MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$ , See Figure 1		0.5		$\text{V}/\mu\text{s}$
$V_n$ Equivalent input noise voltage (see Figure 2)	$f = 10\text{ Hz}$		21		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$		17		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$		0.16		$\mu\text{V}$
	$f = 0.1\text{ to }10\text{ Hz}$		0.47		
$I_n$ Equivalent input noise current			0.1		$\text{pA}/\sqrt{\text{Hz}}$
$B_1$ Unity-gain bandwidth	See Figure 3		1.7		MHz
$\phi_m$ Phase margin at unity gain	See Figure 3		47°		

PARAMETER MEASUREMENT INFORMATION



(a) SINGLE SUPPLY



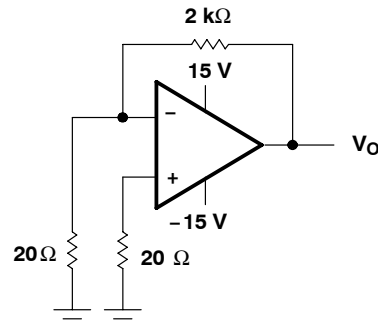
(b) SPLIT SUPPLY

NOTE A:  $C_L$  includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit



(a) SINGLE SUPPLY

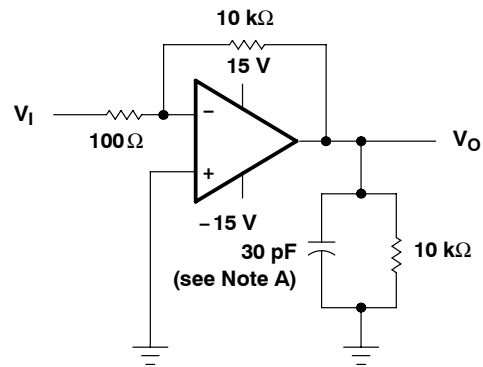


(b) SPLIT SUPPLY

Figure 2. Noise-Voltage Test Circuit



(a) SINGLE SUPPLY



(b) SPLIT SUPPLY

NOTE A:  $C_L$  includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

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## PARAMETER MEASUREMENT INFORMATION



NOTE A:  $C_L$  includes fixture capacitance.

Figure 4. Small-Signal Pulse-Response Test Circuit

### typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

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## TYPICAL CHARACTERISTICS

**Table of Graphs**

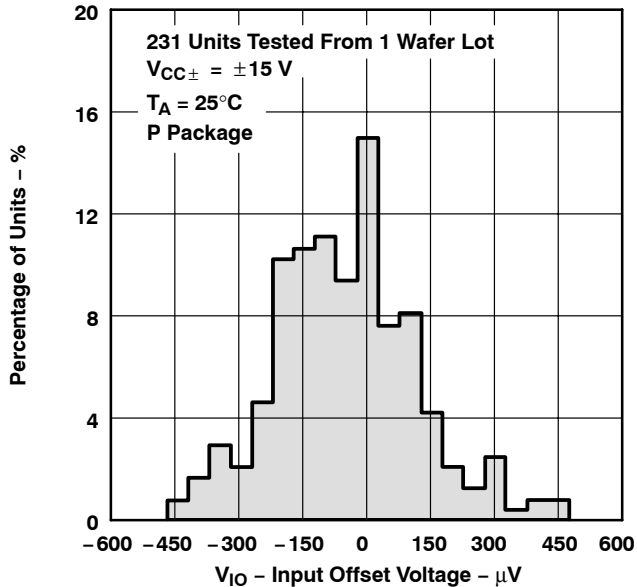
		<b>FIGURE</b>	
$V_{IO}$	Input offset voltage	Distribution	5, 6, 7
$I_{IB}$	Input bias current	vs Common-mode input voltage vs Free-air temperature	8, 9, 10 11, 12, 13
$I_I$	Input current	vs Differential input voltage	14
$V_{OM}$	Maximum peak output voltage	vs Output current vs Free-air temperature	15, 16, 17 18
$V_{OH}$	High-level output voltage	vs High-level output current vs Free-air temperature	19, 20 21
$V_{OL}$	Low-level output voltage	vs Low-level output current vs Free-air temperature	22 23
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	24, 25
$A_{VD}$	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	26 27, 28, 29
$I_{OS}$	Short-circuit output current	vs Supply voltage vs Free-air temperature	30 – 33 34 – 37
$I_{CC}$	Supply current	vs Supply voltage vs Free-air temperature	38, 39, 40 41, 42, 43
CMRR	Common-mode rejection ratio	vs Frequency	44, 45, 46
SR	Slew rate	vs Free-air temperature	47, 48, 49
	Voltage-follower small-signal pulse response		50, 51
	Voltage-follower large-signal pulse response		52 – 57
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz 0.1 to 10 Hz	58 59
$V_n$	Equivalent input noise voltage	vs Frequency	60
$B_1$	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	61, 62 63, 64
$\phi_m$	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	65, 66 67, 68 69, 70
	Phase shift	vs Frequency	26

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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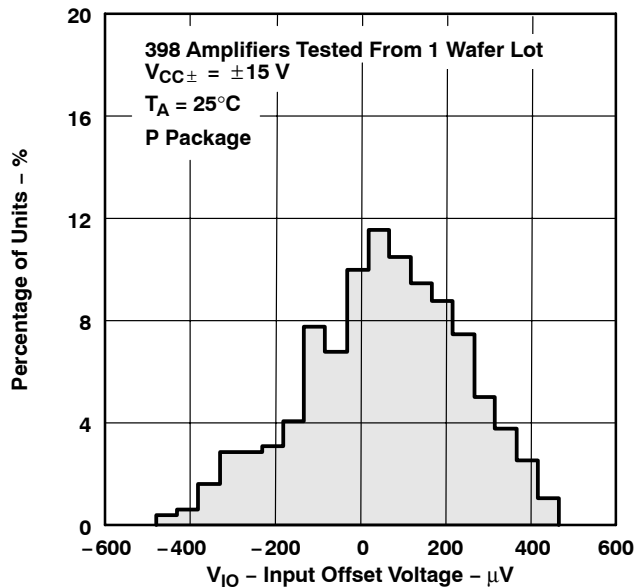
## TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLE2021  
INPUT OFFSET VOLTAGE**



**Figure 5**

**DISTRIBUTION OF TLE2022  
INPUT OFFSET VOLTAGE**



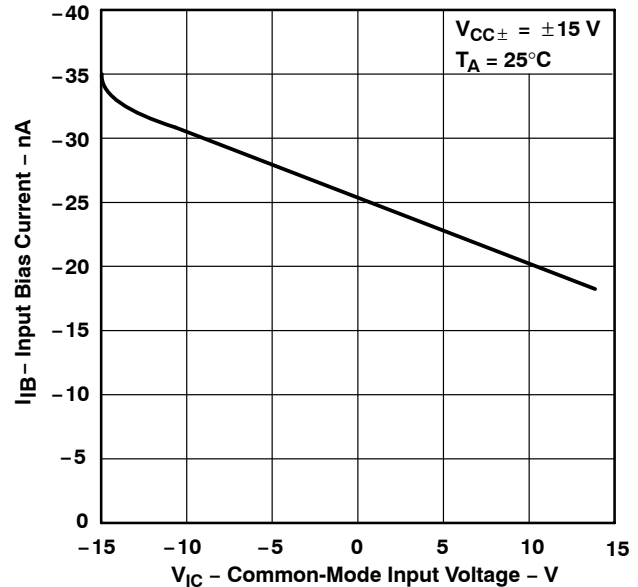
**Figure 6**

**DISTRIBUTION OF TLE2024  
INPUT OFFSET VOLTAGE**



**Figure 7**

**TLE2021  
INPUT BIAS CURRENT  
vs  
COMMON-MODE INPUT VOLTAGE**



**Figure 8**

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS

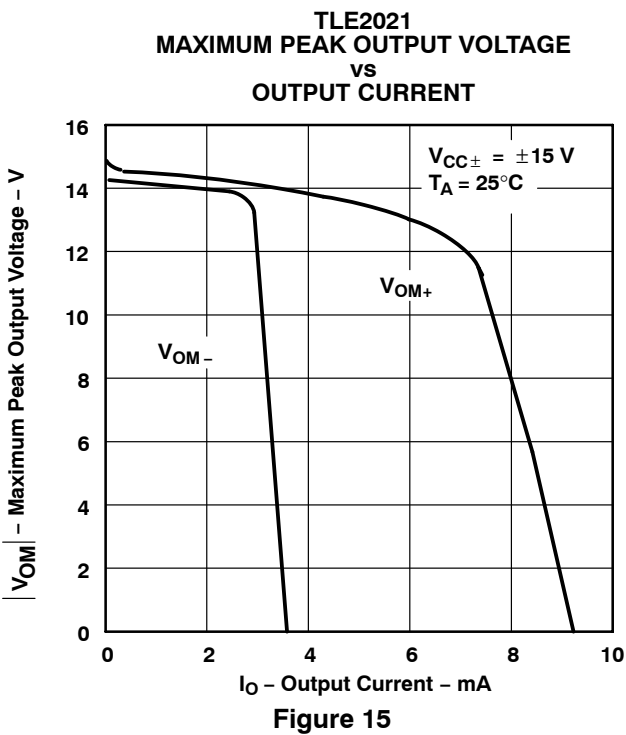
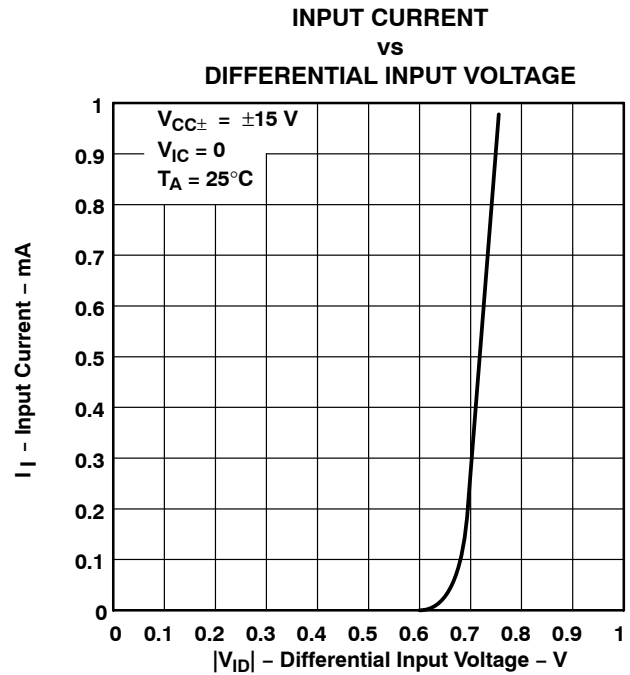
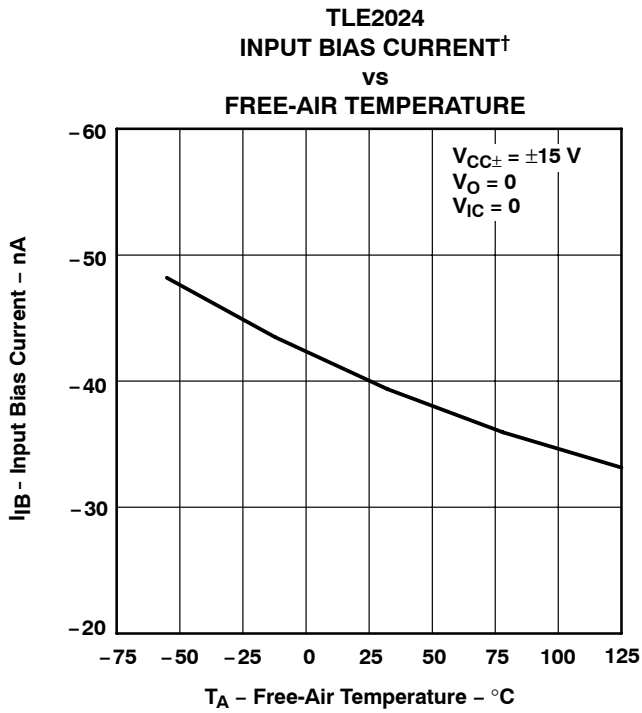


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TLE202x, TLE202xA, TLE202xB, TLE202xY**  
**EXCALIBUR HIGH-SPEED LOW-POWER PRECISION**  
**OPERATIONAL AMPLIFIERS**

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**TYPICAL CHARACTERISTICS**



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS



Figure 21

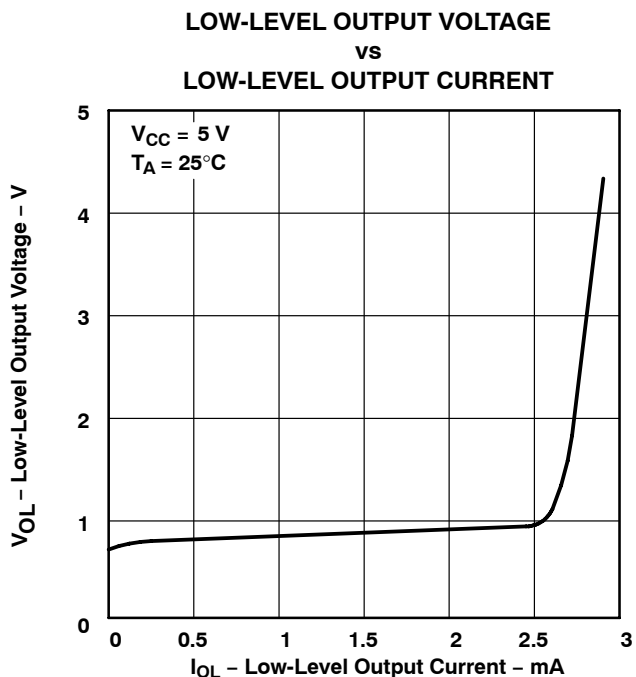


Figure 22

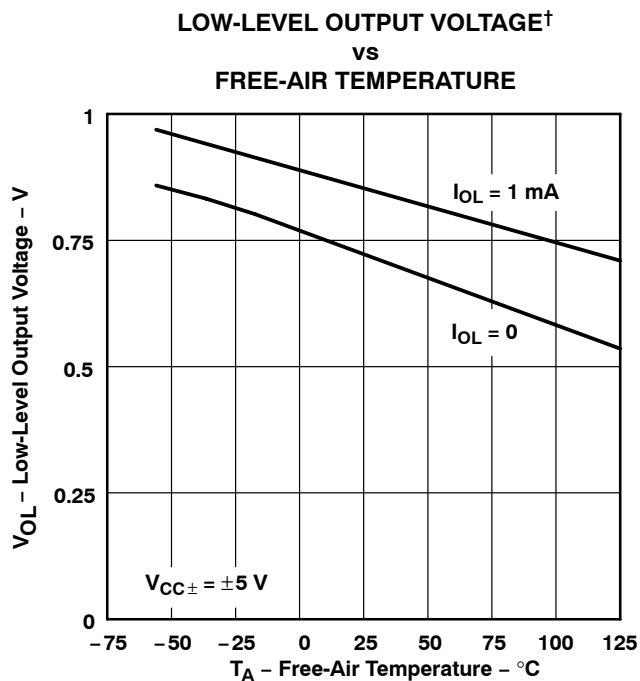


Figure 23

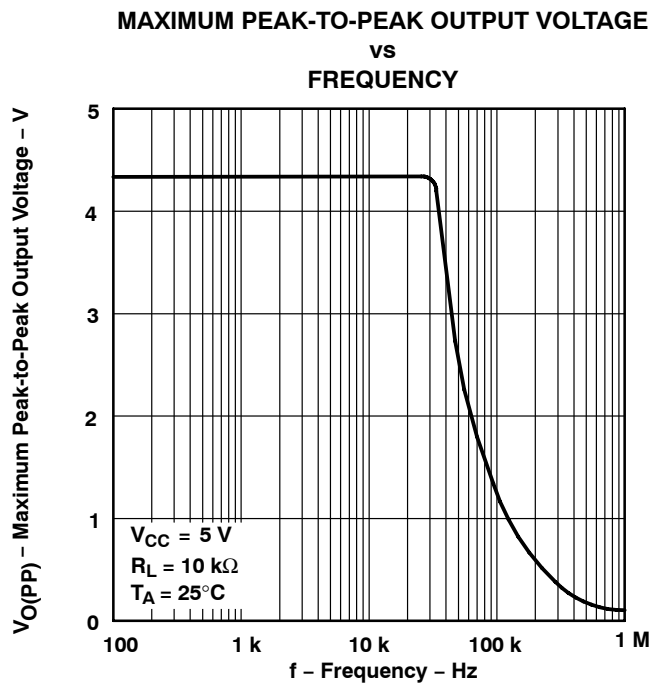


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS

### MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY



Figure 25

### LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY



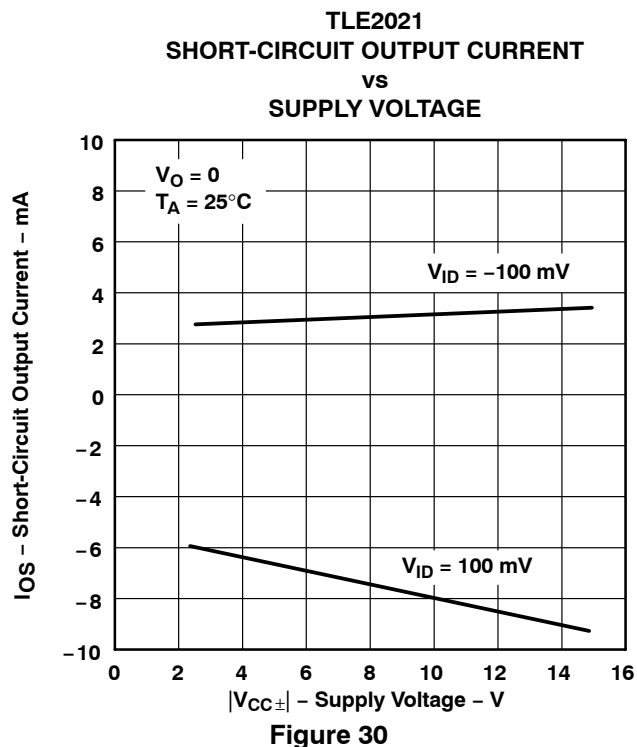
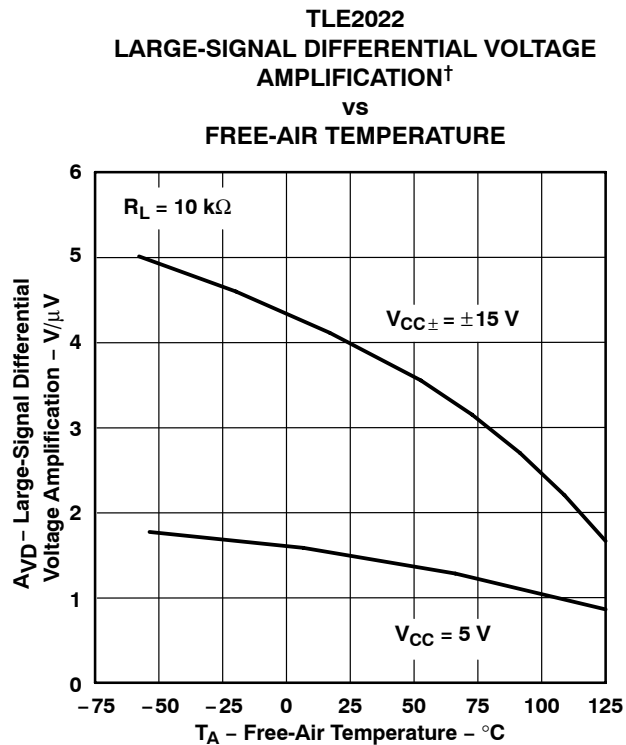
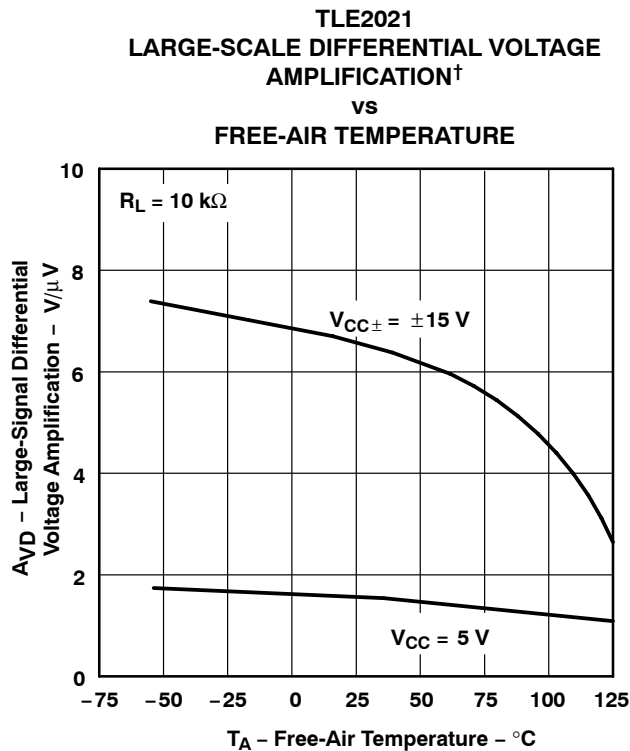
Figure 26



# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS

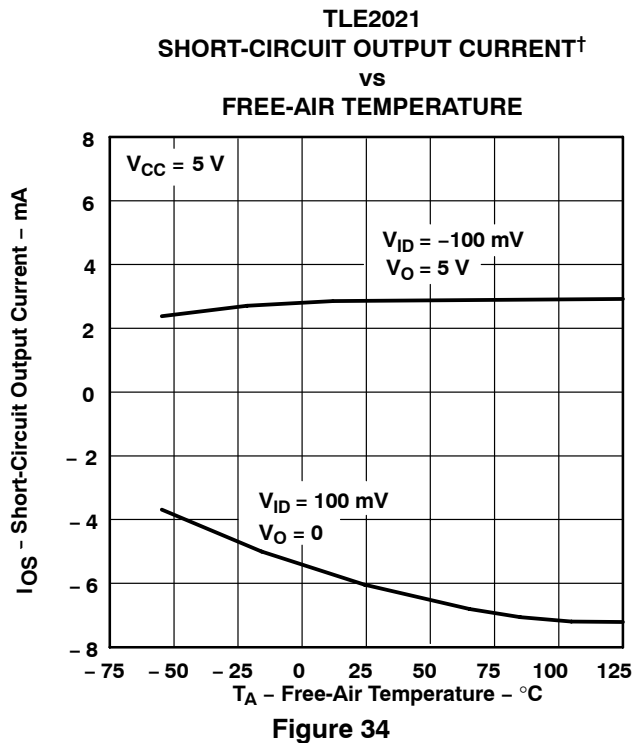
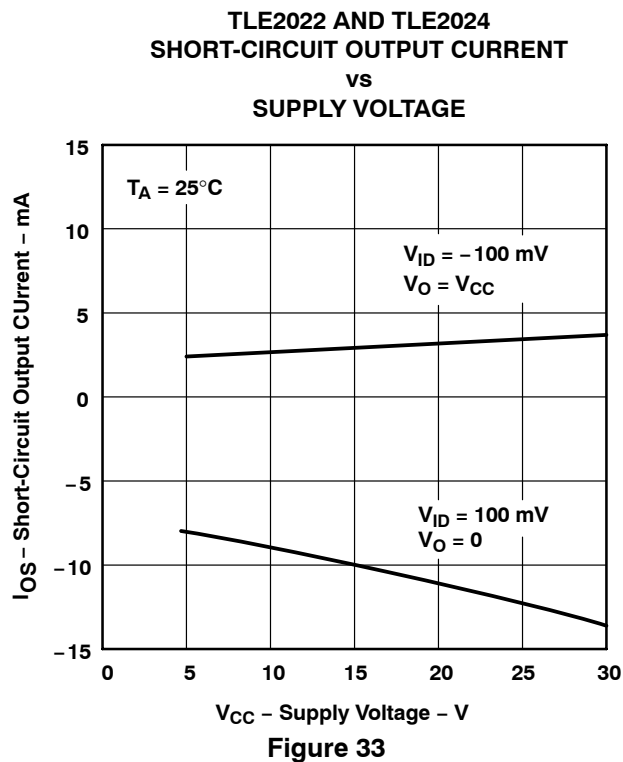
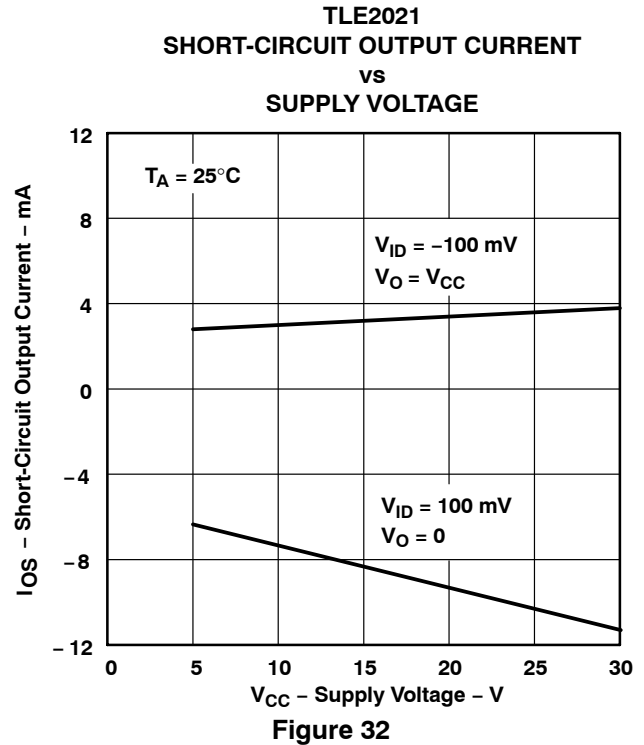
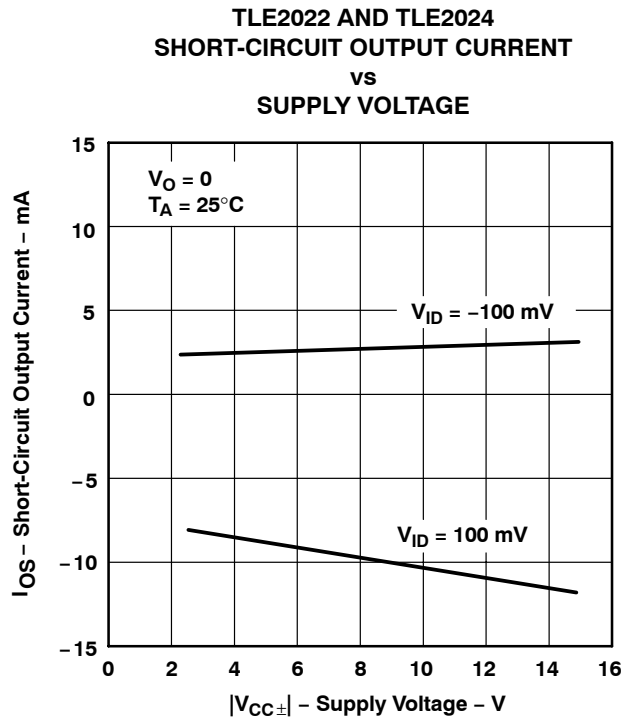


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS

**TLE2022 AND TLE2024  
SHORT-CIRCUIT OUTPUT CURRENT†  
vs  
FREE-AIR TEMPERATURE**



Figure 35

**TLE2021  
SHORT-CIRCUIT OUTPUT CURRENT†  
vs  
FREE-AIR TEMPERATURE**

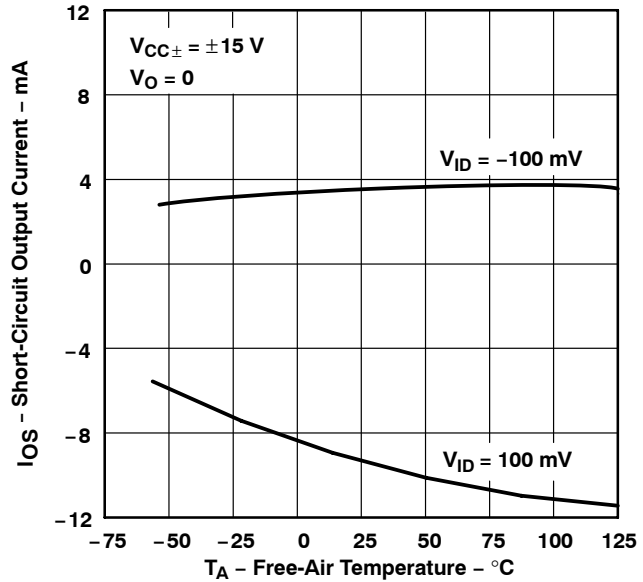


Figure 36

**TLE2022 AND TLE2024  
SHORT-CIRCUIT OUTPUT CURRENT†  
vs  
FREE-AIR TEMPERATURE**



Figure 37

**TLE2021  
SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE**

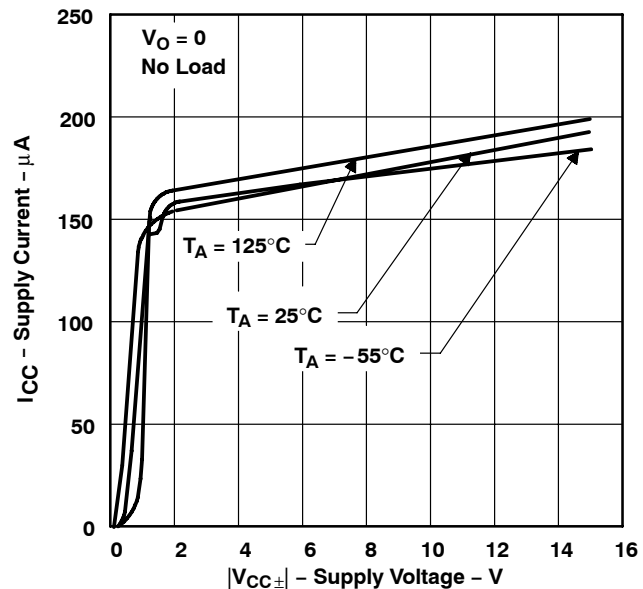


Figure 38

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS



Figure 39

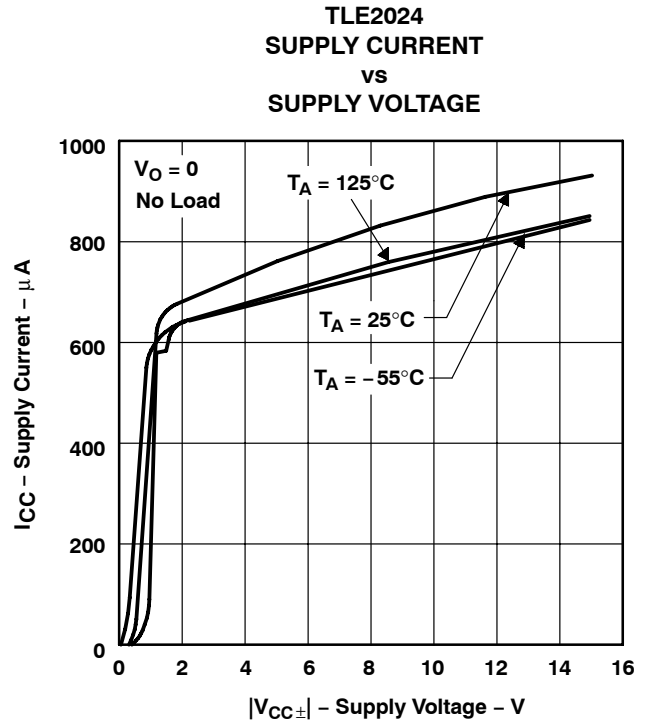


Figure 40

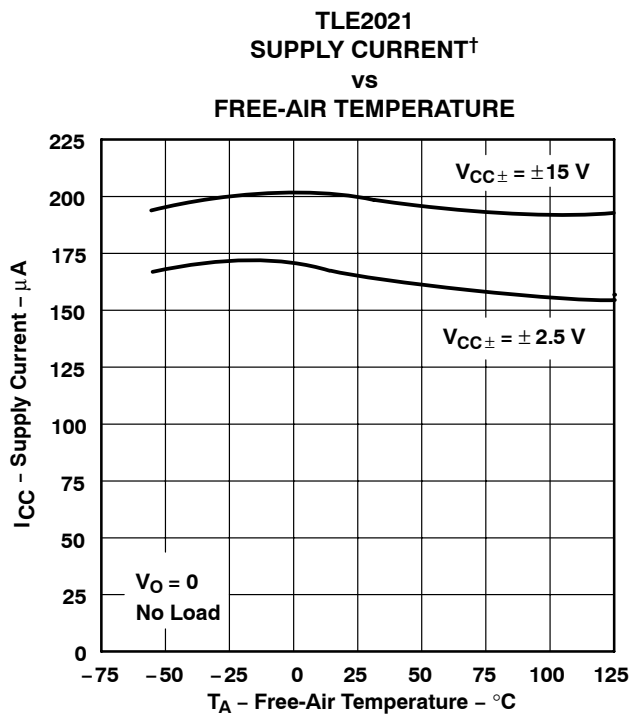


Figure 41

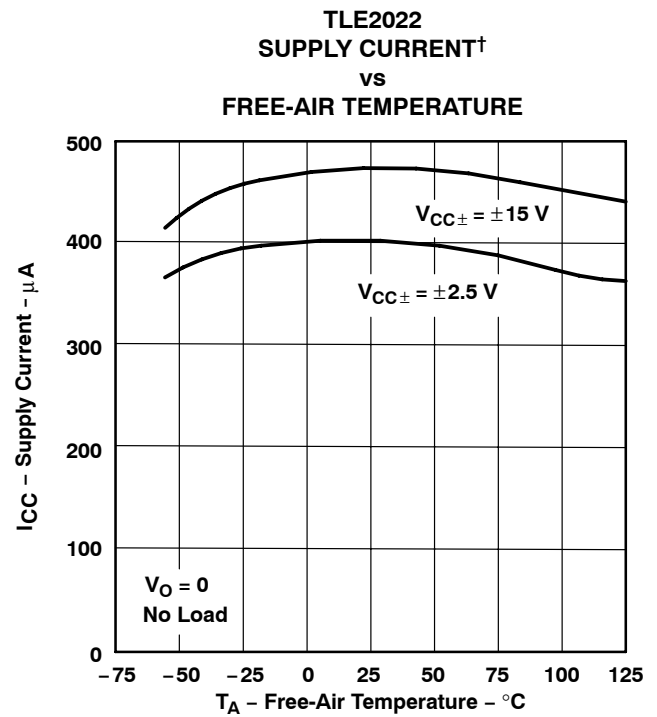


Figure 42

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS



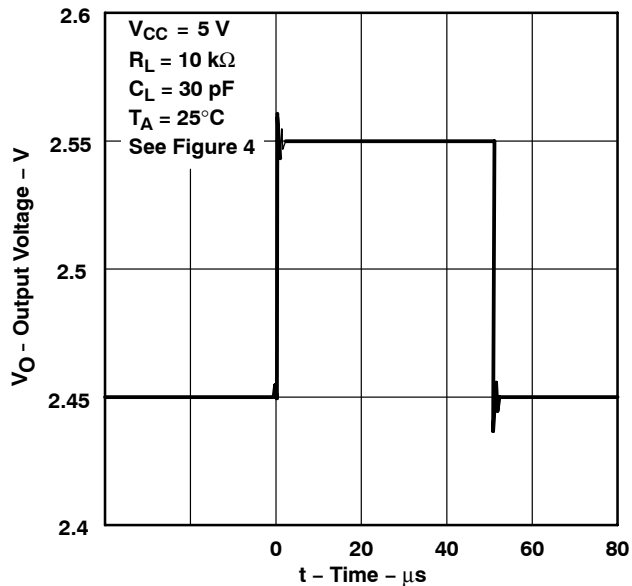
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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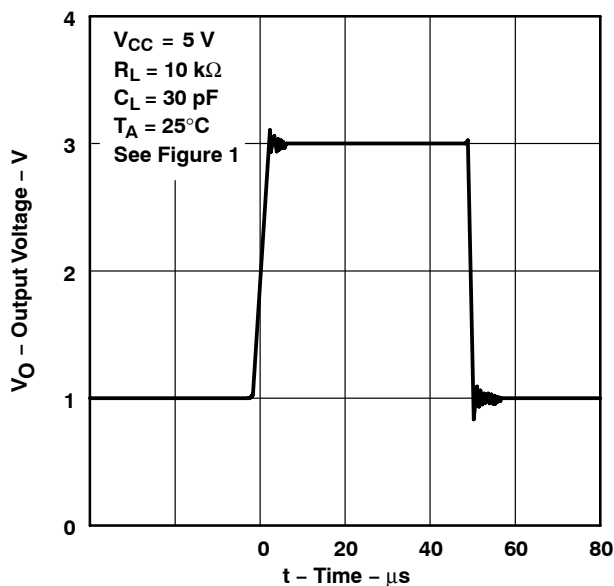
## TYPICAL CHARACTERISTICS

**VOLTAGE-FOLLOWER  
SMALL-SIGNAL  
PULSE RESPONSE**



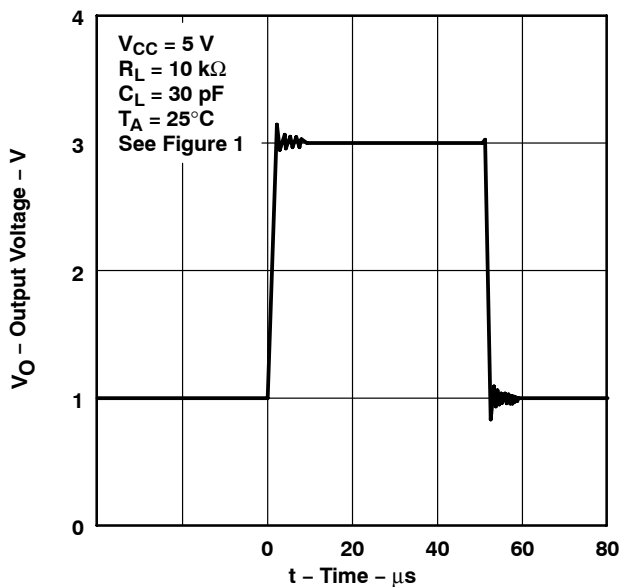
**Figure 51**

**TLE2021  
VOLTAGE-FOLLOWER LARGE-SIGNAL  
PULSE RESPONSE**



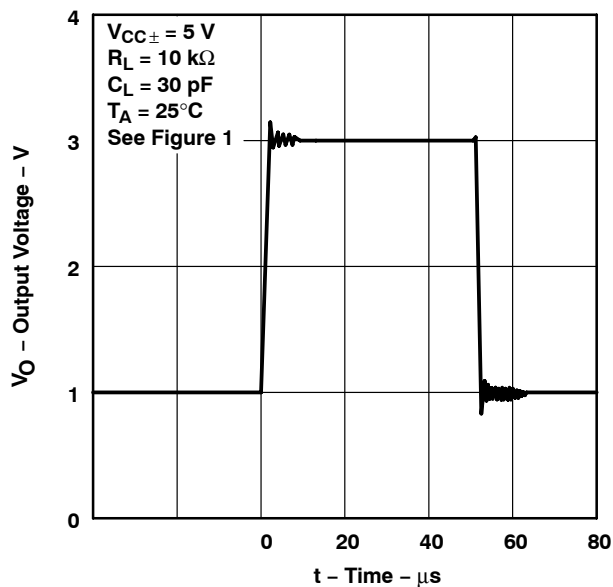
**Figure 52**

**TLE2022  
VOLTAGE-FOLLOWER LARGE-SIGNAL  
PULSE RESPONSE**



**Figure 53**

**TLE2024  
VOLTAGE-FOLLOWER LARGE-SCALE  
PULSE RESPONSE**



**Figure 54**



# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS



Figure 55



Figure 56



Figure 57



Figure 58

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS

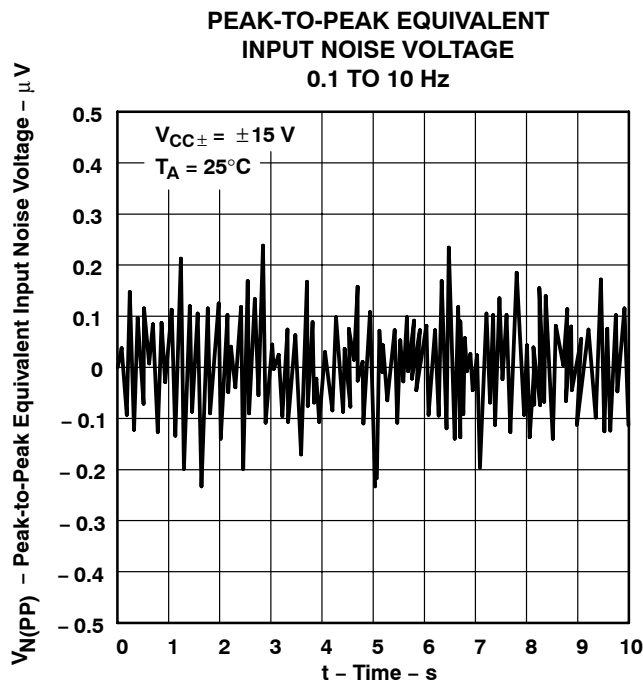


Figure 59

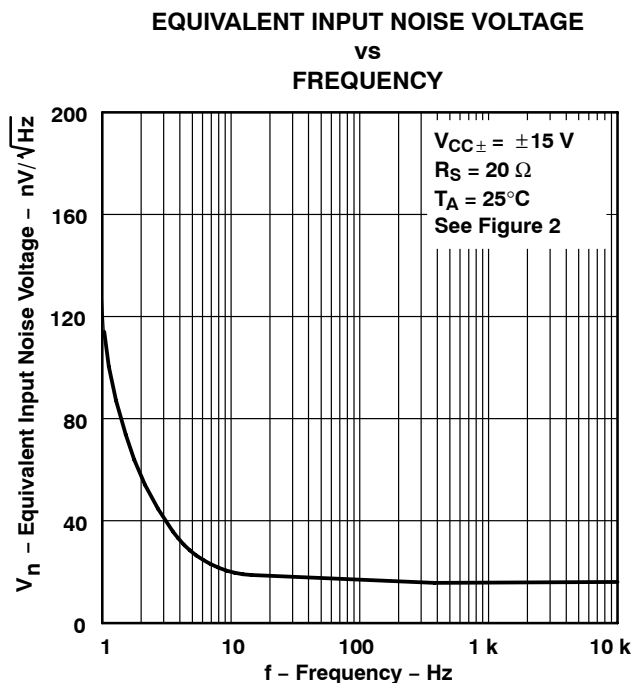


Figure 60



Figure 61

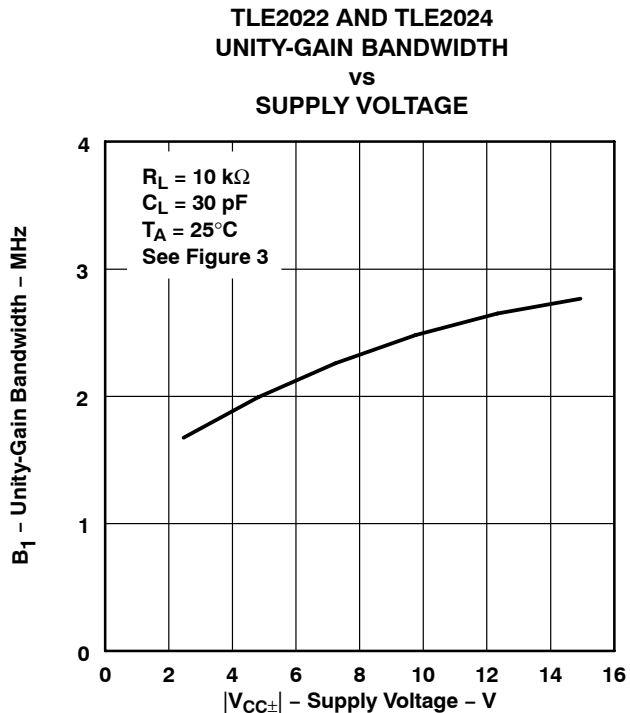


Figure 62

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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## TYPICAL CHARACTERISTICS

**TLE2021  
PHASE MARGIN  
vs  
LOAD CAPACITANCE**



Figure 67

**TLE2022 AND TLE2024  
PHASE MARGIN  
vs  
LOAD CAPACITANCE**



Figure 68

**TLE2021  
PHASE MARGIN†  
vs  
FREE-AIR TEMPERATURE**



Figure 69

**TLE2022 AND TLE2024  
PHASE MARGIN†  
vs  
FREE-AIR TEMPERATURE**



Figure 70

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



## APPLICATION INFORMATION

### voltage-follower applications

The TLE202x circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. This feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 k $\Omega$ , this pole degrades the amplifier phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 71).



**Figure 71. Voltage Follower**

### Input offset voltage nulling

The TLE202x series offers external null pins that further reduce the input offset voltage. The circuit in Figure 72 can be connected as shown if this feature is desired. When external nulling is not needed, the null pins may be left disconnected.



**Figure 72. Input Offset Voltage Null Circuit**

# TLE202x, TLE202xA, TLE202xB, TLE202xY EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 73, Figure 74, and Figure 75 were generated using the TLE202x typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



Figure 73. Boyle Subcircuit

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```
.SUBCKT TLE2021 1 2 3 4 5
*
c1 11 12 6.244E-12
c2 6 7 13.4E-12
c3 87 0 10.64E-9
cpsr 85 86 15.9E-9
dcm+ 81 82 dx
dcm- 83 81 dx
dc 5 53 dx
de 54 5 dx
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
ecmr 84 99 (2 99) 1
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
epsr 85 0 poly(1) (3,4) -60E-6 2.0E-6
ense 89 2 poly(1) (88,0) 120E-6 1
fb 7 99 poly(6) vb vc ve vlp vln vpsr 0 547.3E6
+ -50E7 50E7 50E7 -50E7 547E6
ga 6 0 11 12 188.5E-6
gcm 0 6 10 99 335.2E-12
gpsr 85 86 (85,86) 100E-6
grc1 4 11 (4,11) 1.885E-4
grc2 4 12 (4,12) 1.885E-4
gre1 13 10 (13,10) 6.82E-4
gre2 14 10 (14,10) 6.82E-4
hlim 90 0 vlim 1k

hcmr 80 1 poly(2) vcm+ vcm- 0 1E2 1E2
irp 3 4 185E-6
iee 3 10 dc 15.67E-6
iio 2 0 2E-9
i1 88 0 1E-21
q1 11 89 13 qx
q2 12 80 14 qx
R2 6 9 100.0E3
rcm 84 81 1K
ree 10 99 14.76E6
rn1 87 0 2.55E8
rn2 87 88 11.67E3
ro1 8 5 62
ro2 7 99 63
vcm+ 82 99 13.3
vcm- 83 99 -14.6
vb 9 0 dc 0
vc 3 53 dc 1.300
ve 54 4 dc 1.500
vlim 7 8 dc 0
vlp 91 0 dc 3.600
vln 0 92 dc 3.600
vpsr 0 86 dc 0
.model dx d(is=800.0E-18)
.model qx pnp(is=800.0E-18 bf=270)
.ends
```

**Figure 74. Boyle Macromodel for the TLE2021**

```
.SUBCKT TLE2022 1 2 3 4 5
*
c1 11 12 6.814E-12
c2 6 7 20.00E-12
dc 5 53 dx
de 54 5 dx
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0
+ 45.47E6 -50E6 50E6 50E6 -50E6
ga 6 0 11 12 377.9E-6
gcm 0 6 10 99 7.84E-10
iee 3 10 DC 18.07E-6
hlim 90 0 vlim 1k
q1 11 2 13 qx
q2 12 1 14 qx
r2 6 9 100.0E3

rc1 4 11 2.842E3
rc2 4 12 2.842E3
ge1 13 10 (10,13) 31.299E-3
ge2 14 10 (10,14) 31.299E-3
ree 10 99 11.07E6
ro1 8 5 250
ro2 7 99 250
rp 3 4 137.2E3
vb 9 0 dc 0
vc 3 53 dc 1.300
ve 54 4 dc 1.500
vlim 7 8 dc 0
vlp 91 0 dc 3
vln 0 92 dc 3
.model dx d(is=800.0E-18)
.model qx pnp(is=800.0E-18 bf=257.1)
.ends
```

**Figure 75. Boyle Macromodel for the TLE2022**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9088101MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9088101MPA TLE2021M	<a href="#">Samples</a>
5962-9088102M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9088102M2A TLE2022MFKB	<a href="#">Samples</a>
5962-9088102MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9088102MPA TLE2022M	<a href="#">Samples</a>
5962-9088103M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9088103M2A TLE2024MFKB	<a href="#">Samples</a>
5962-9088103MCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9088103MC A TLE2024MJB	<a href="#">Samples</a>
5962-9088104Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9088104Q2A TLE2021 AMFKB	<a href="#">Samples</a>
5962-9088104QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9088104QPA TLE2021AM	<a href="#">Samples</a>
5962-9088105Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9088105Q2A TLE2022A MFKB	<a href="#">Samples</a>
5962-9088105QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9088105QPA TLE2022AM	<a href="#">Samples</a>
5962-9088106Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9088106Q2A TLE2024A MFKB	<a href="#">Samples</a>
5962-9088106QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9088106QC A TLE2024AMJB	<a href="#">Samples</a>
5962-9088107Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9088107Q2A TLE2021 BMFKB	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9088107QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9088107QPA TLE2021BM	<a href="#">Samples</a>
5962-9088108Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9088108Q2A TLE2022B MFKB	<a href="#">Samples</a>
5962-9088108QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9088108QPA TLE2022BM	<a href="#">Samples</a>
5962-9088109Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9088109Q2A TLE2024 BMFKB	<a href="#">Samples</a>
5962-9088109QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9088109QC A TLE2024BMJB	<a href="#">Samples</a>
TLE2021ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2021AC	<a href="#">Samples</a>
TLE2021ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2021AC	<a href="#">Samples</a>
TLE2021ACP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2021AC	<a href="#">Samples</a>
TLE2021AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021AI	<a href="#">Samples</a>
TLE2021AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2021AI	<a href="#">Samples</a>
TLE2021AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2021AI	<a href="#">Samples</a>
TLE2021AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9088104Q2A TLE2021 AMFKB	<a href="#">Samples</a>
TLE2021AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9088104QPA TLE2021AM	<a href="#">Samples</a>
TLE2021BMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type		5962- 9088107Q2A TLE2021 BMFKB	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2021BMJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLE2021 BMJG	<a href="#">Samples</a>
TLE2021BMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type		9088107QPA TLE2021BM	<a href="#">Samples</a>
TLE2021CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2021C	<a href="#">Samples</a>
TLE2021CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2021C	<a href="#">Samples</a>
TLE2021CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2021C	<a href="#">Samples</a>
TLE2021CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2021CP	<a href="#">Samples</a>
TLE2021CPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2021CP	<a href="#">Samples</a>
TLE2021ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021I	<a href="#">Samples</a>
TLE2021IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021I	<a href="#">Samples</a>
TLE2021IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021I	<a href="#">Samples</a>
TLE2021IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2021I	<a href="#">Samples</a>
TLE2021IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLE2021IP	<a href="#">Samples</a>
TLE2021MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2021M	<a href="#">Samples</a>
TLE2021MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2021M	<a href="#">Samples</a>
TLE2021MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLE2021MJG	<a href="#">Samples</a>
TLE2021MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9088101MPA TLE2021M	<a href="#">Samples</a>
TLE2022ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2022AC	<a href="#">Samples</a>
TLE2022ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2022AC	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2022ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2022AC	<a href="#">Samples</a>
TLE2022ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2022AC	<a href="#">Samples</a>
TLE2022ACP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2022AC	<a href="#">Samples</a>
TLE2022ACPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2022AC	<a href="#">Samples</a>
TLE2022AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022AI	<a href="#">Samples</a>
TLE2022AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022AI	<a href="#">Samples</a>
TLE2022AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2022AI	<a href="#">Samples</a>
TLE2022AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2022AI	<a href="#">Samples</a>
TLE2022AMD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022AM	<a href="#">Samples</a>
TLE2022AMDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2022AM	<a href="#">Samples</a>
TLE2022AMDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022AM	<a href="#">Samples</a>
TLE2022AMDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2022AM	<a href="#">Samples</a>
TLE2022AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9088105Q2A TLE2022A MFKB	<a href="#">Samples</a>
TLE2022AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9088105QPA TLE2022AM	<a href="#">Samples</a>
TLE2022BMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9088108Q2A TLE2022B MFKB	<a href="#">Samples</a>
TLE2022BMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9088108QPA TLE2022BM	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2022CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2022C	<a href="#">Samples</a>
TLE2022CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2022C	<a href="#">Samples</a>
TLE2022CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2022CP	<a href="#">Samples</a>
TLE2022CPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2022CP	<a href="#">Samples</a>
TLE2022ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022I	<a href="#">Samples</a>
TLE2022IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022I	<a href="#">Samples</a>
TLE2022IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2022I	<a href="#">Samples</a>
TLE2022IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2022IP	<a href="#">Samples</a>
TLE2022IPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2022IP	<a href="#">Samples</a>
TLE2022MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022M	<a href="#">Samples</a>
TLE2022MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2022M	<a href="#">Samples</a>
TLE2022MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2022M	<a href="#">Samples</a>
TLE2022MDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2022M	<a href="#">Samples</a>
TLE2022MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9088102M2A TLE2022MFKB	<a href="#">Samples</a>
TLE2022MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLE2022MJG	<a href="#">Samples</a>
TLE2022MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9088102MPA TLE2022M	<a href="#">Samples</a>
TLE2024ACDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLE2024AC	<a href="#">Samples</a>
TLE2024ACDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLE2024AC	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2024ACN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2024ACN	<a href="#">Samples</a>
TLE2024AIDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLE2024AI	<a href="#">Samples</a>
TLE2024AIN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2024AIN	<a href="#">Samples</a>
TLE2024AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9088106Q2A TLE2024A MFKB	<a href="#">Samples</a>
TLE2024AMJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9088106QC A TLE2024AMJB	<a href="#">Samples</a>
TLE2024BMDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2024BM	<a href="#">Samples</a>
TLE2024BMDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLE2024BM	<a href="#">Samples</a>
TLE2024BMDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2024BM	<a href="#">Samples</a>
TLE2024BMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9088109Q2A TLE2024 BMFKB	<a href="#">Samples</a>
TLE2024BMJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLE2024BMJ	<a href="#">Samples</a>
TLE2024BMJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9088109QC A TLE2024BMJB	<a href="#">Samples</a>
TLE2024CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLE2024C	<a href="#">Samples</a>
TLE2024CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLE2024C	<a href="#">Samples</a>
TLE2024CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLE2024C	<a href="#">Samples</a>
TLE2024CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2024CN	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2024CNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2024CN	<a href="#">Samples</a>
TLE2024IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLE2024I	<a href="#">Samples</a>
TLE2024IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2024IN	<a href="#">Samples</a>
TLE2024MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2024M	<a href="#">Samples</a>
TLE2024MDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2024M	<a href="#">Samples</a>
TLE2024MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9088103M2A TLE2024MFKB	<a href="#">Samples</a>
TLE2024MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9088103MCA TLE2024MJB	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

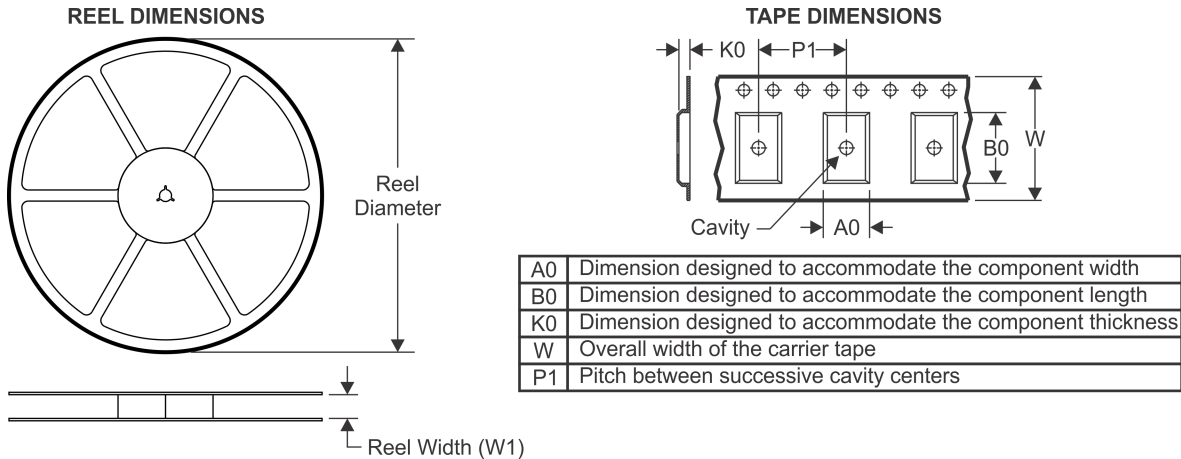
**OTHER QUALIFIED VERSIONS OF TLE2021, TLE2021A, TLE2021AM, TLE2021M, TLE2022, TLE2022A, TLE2022AM, TLE2022M, TLE2024, TLE2024A, TLE2024AM, TLE2024B, TLE2024BM, TLE2024M :**

- Catalog: [TLE2021A](#), [TLE2021](#), [TLE2022A](#), [TLE2022](#), [TLE2024A](#), [TLE2024B](#), [TLE2024](#)
- Automotive: [TLE2021-Q1](#), [TLE2021A-Q1](#), [TLE2021A-Q1](#), [TLE2021-Q1](#), [TLE2022-Q1](#), [TLE2022A-Q1](#), [TLE2022A-Q1](#), [TLE2022-Q1](#), [TLE2024-Q1](#), [TLE2024A-Q1](#), [TLE2024A-Q1](#), [TLE2024-Q1](#)
- Enhanced Product: [TLE2021-EP](#), [TLE2021A-EP](#), [TLE2021A-EP](#), [TLE2021-EP](#), [TLE2022-EP](#), [TLE2022A-EP](#), [TLE2022A-EP](#), [TLE2022-EP](#), [TLE2024-EP](#), [TLE2024A-EP](#), [TLE2024A-EP](#), [TLE2024-EP](#)
- Military: [TLE2021M](#), [TLE2021AM](#), [TLE2022M](#), [TLE2022AM](#), [TLE2024M](#), [TLE2024AM](#), [TLE2024BM](#)

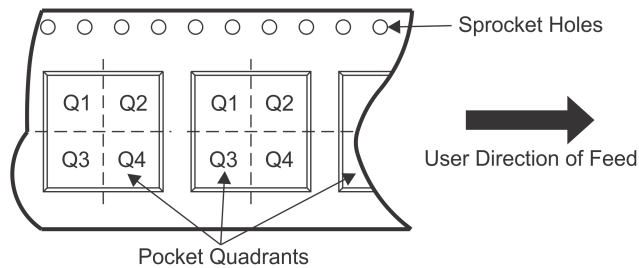
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

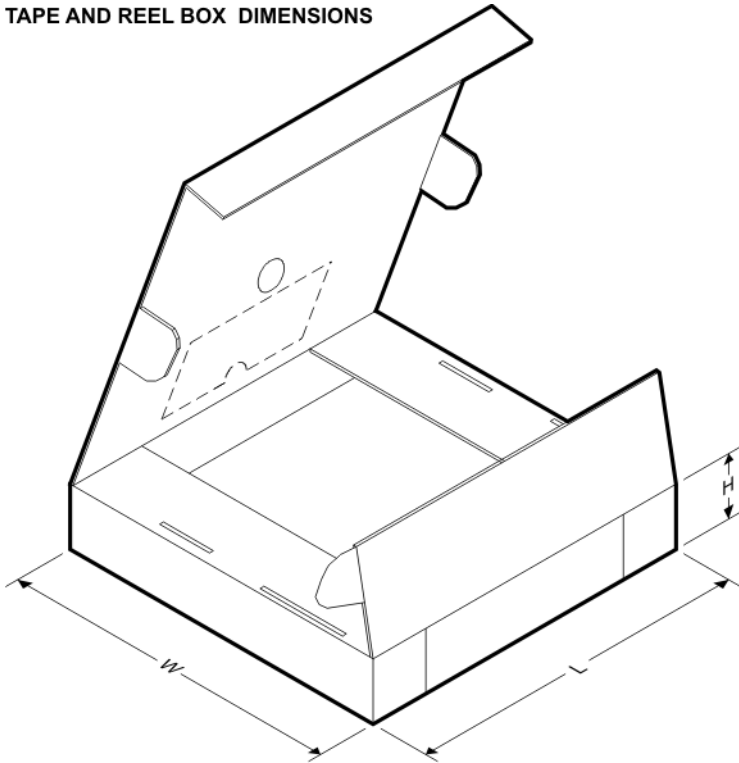


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2021ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2021AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2021CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2021IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022AMDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022AMDRG4	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2024ACDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TLE2024CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


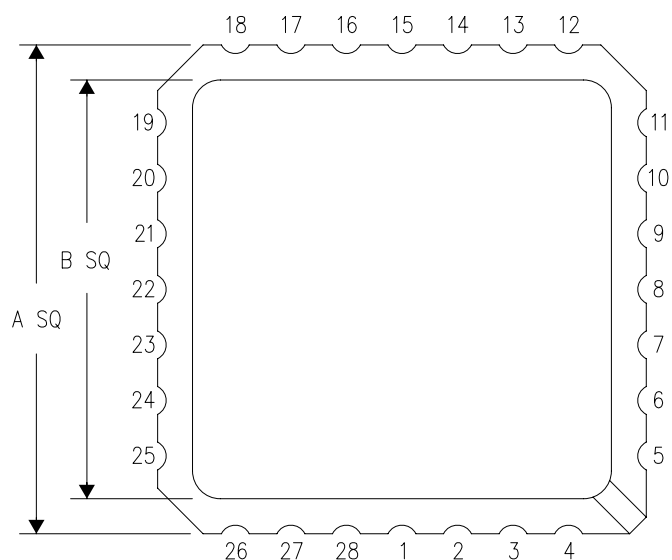
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2021ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2021AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2021CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2021IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2022ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2022AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2022AMDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2022AMDRG4	SOIC	D	8	2500	340.5	338.1	20.6
TLE2022CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2022IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2022MDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2024ACDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TLE2024CDWR	SOIC	DW	16	2000	350.0	350.0	43.0

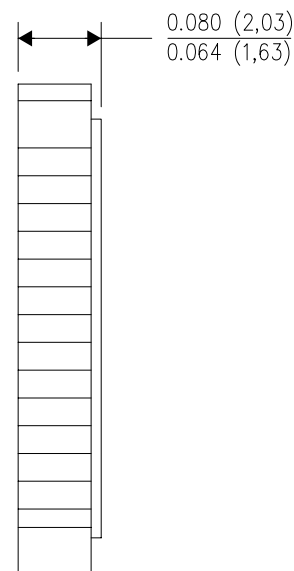
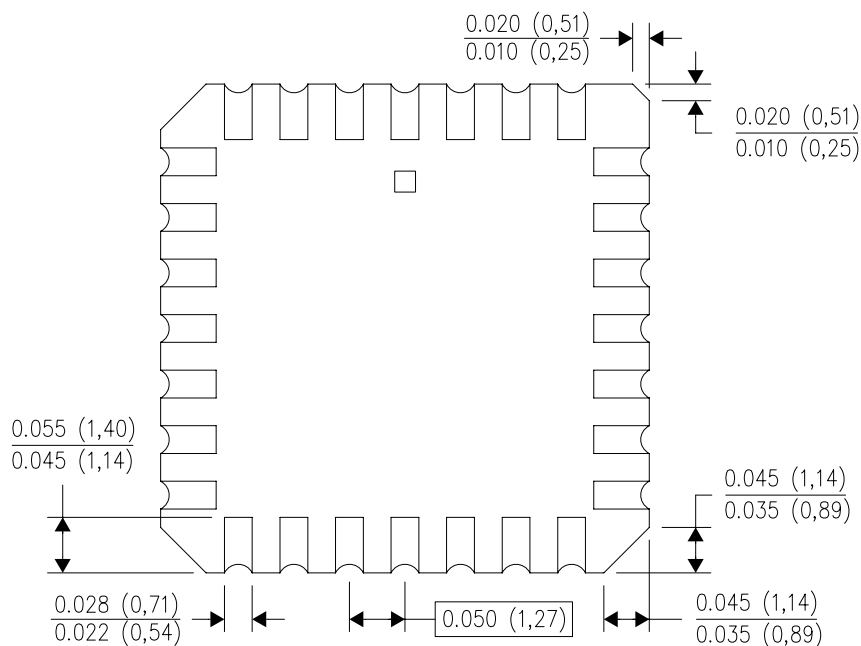
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## GENERIC PACKAGE VIEW

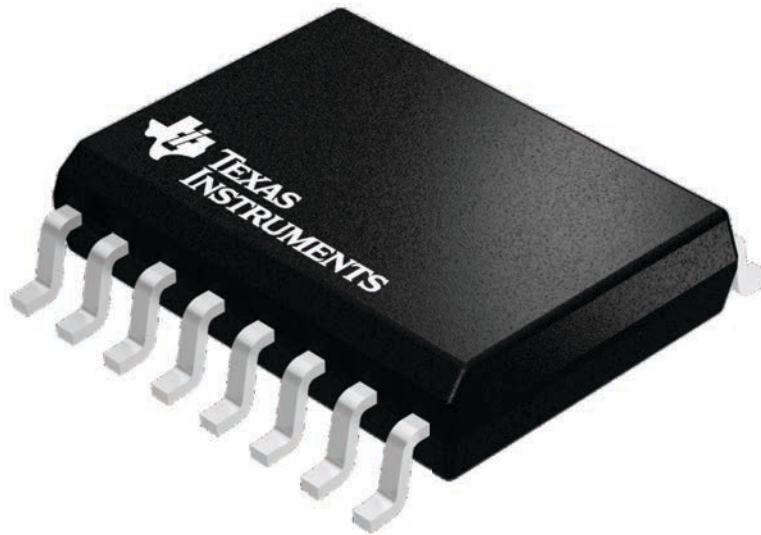
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

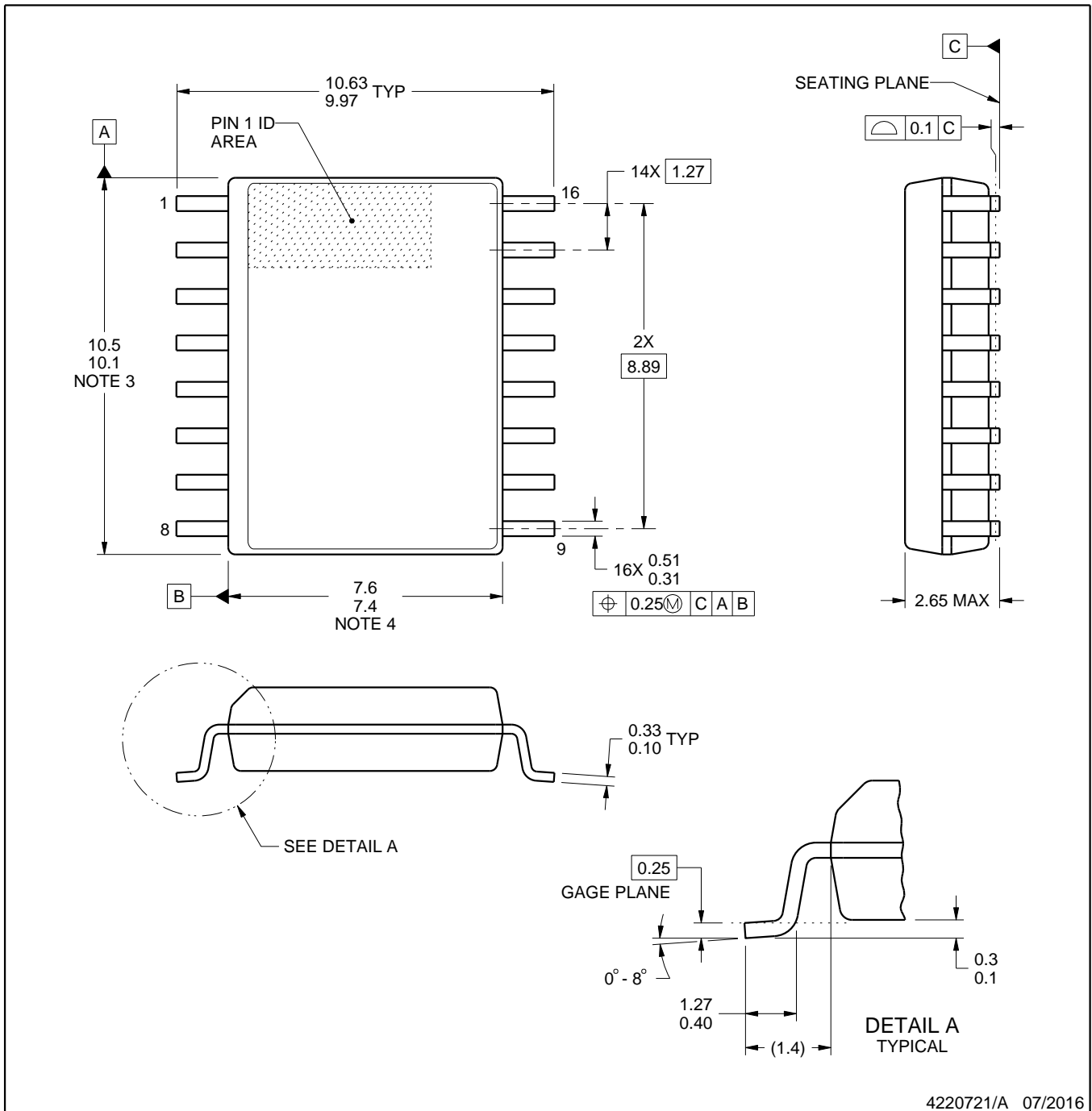


DW0016A

# PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

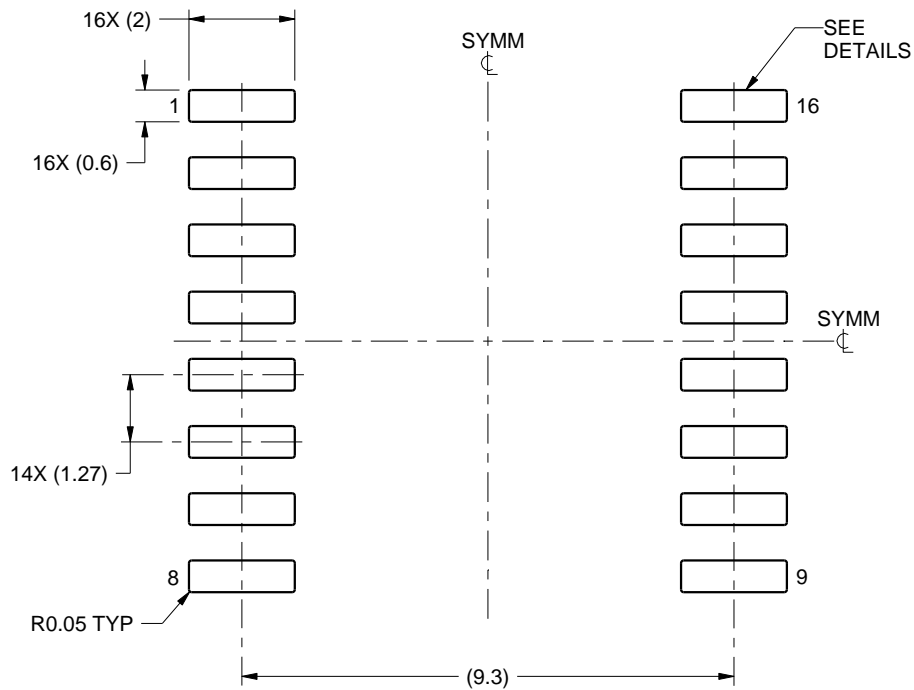
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

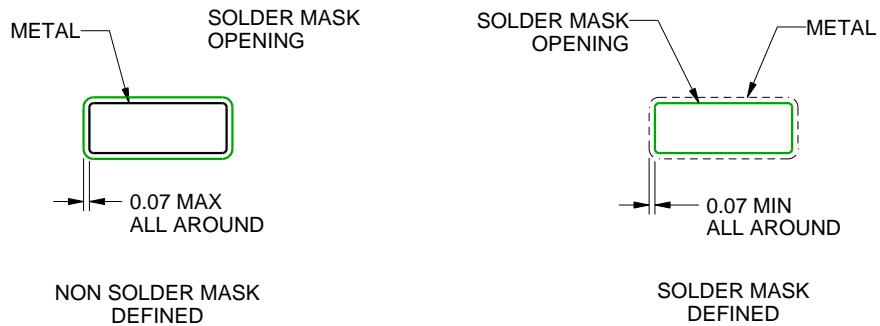
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

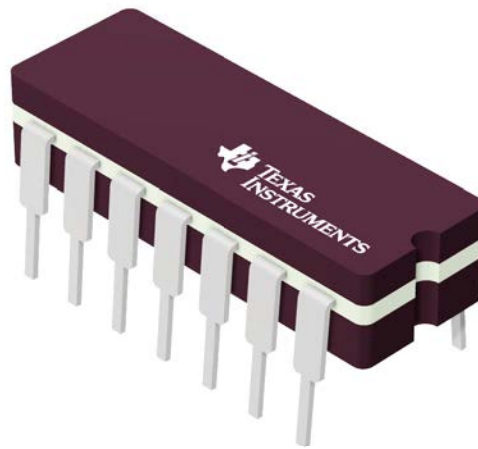
4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J 14

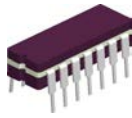
**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

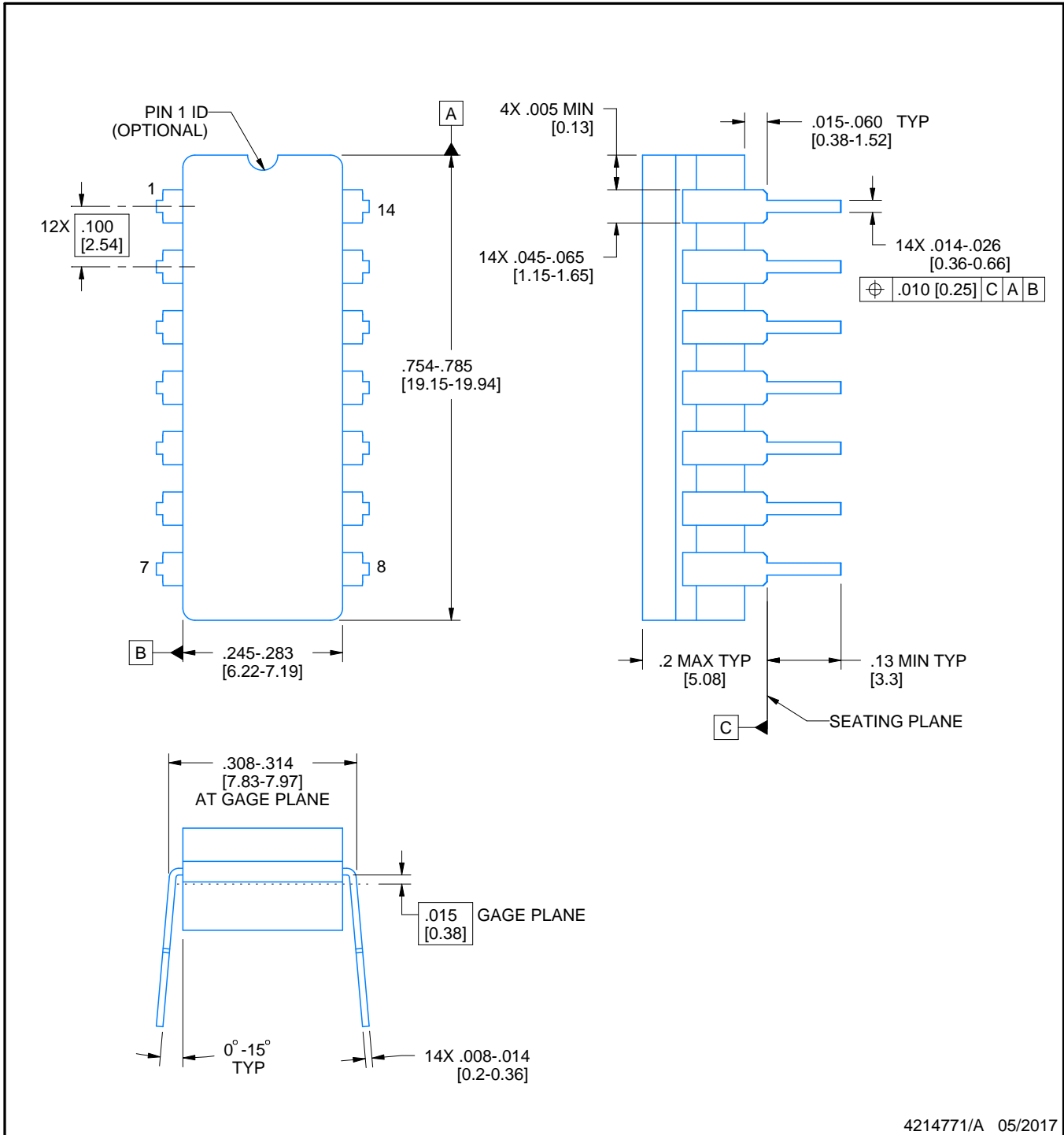
J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

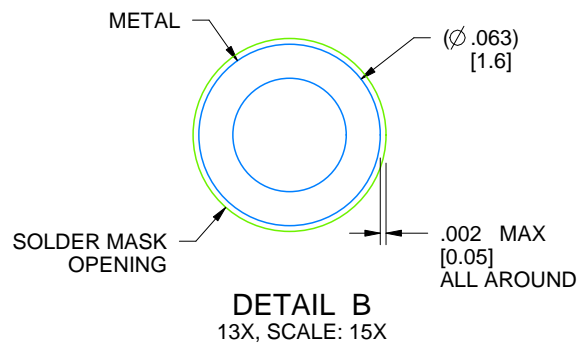
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

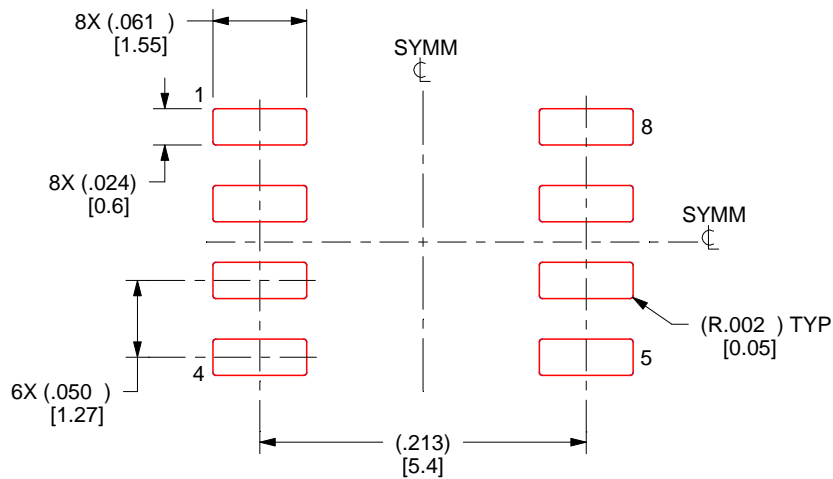
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

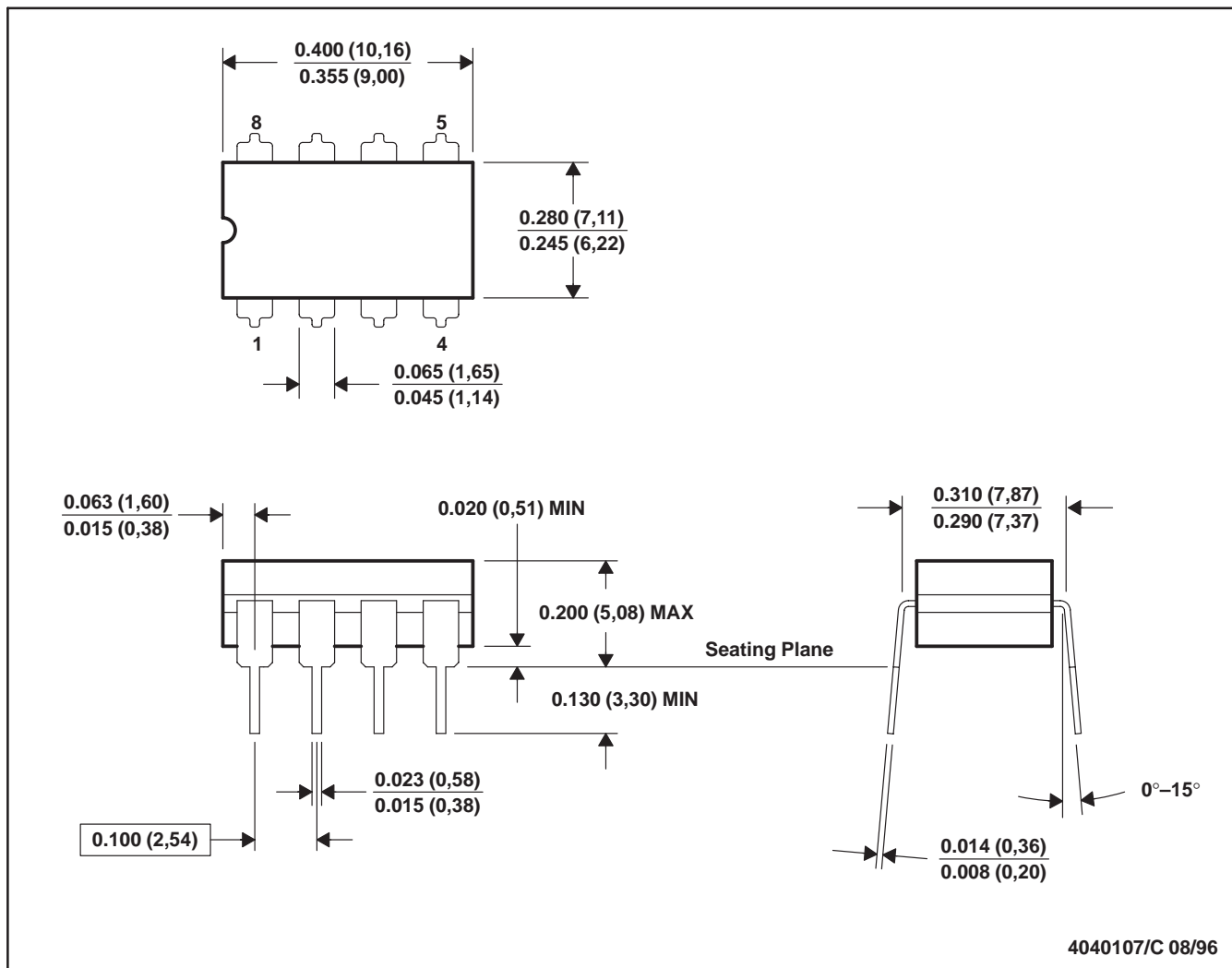
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

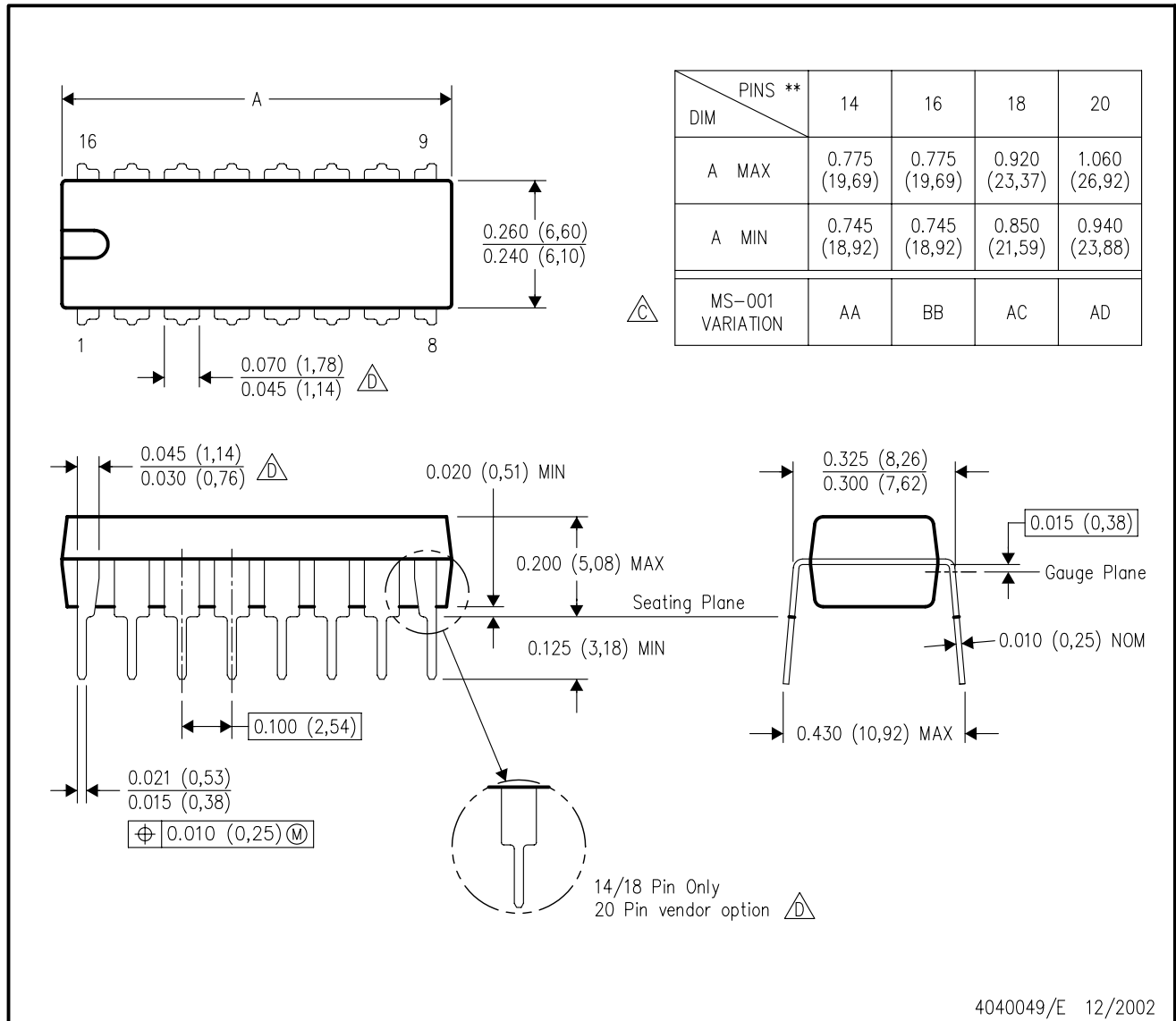


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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