THE DATASHEET OF

TLE2061ACDR

- **2× Bandwidth (2 MHz) of the TL06x and TL03x Operational Amplifiers**
- **Low Supply Current . . . 290 μA/Ch Typ**
- **On-chip Offset Voltage Trimming for Improved DC Performance**
- **High Output Drive, Specified into 100-Ω Loads**
- **Lower Noise Floor Than Earlier Generations of Low-Power BiFETs**

description

The TLE206x series of low-power JFET-input operational amplifiers doubles the bandwidth of the earlier generation TL06x and TL03x BiFET families without significantly increasing power consumption. Texas Instruments Excalibur process also delivers a lower noise floor than the TL06x and TL03x. On-chip zener trimming of offset voltage yields precision grades for dc-coupled applications. The TL206x devices are pin-compatible with other Texas Instruments BiFETs; they can be used to double the bandwidth of TL06x and TL03x circuits or to reduce power consumption of TL05x, TL07x, and TL08x circuits by nearly 90%.

BiFET operational amplifiers offer the inherently-higher input impedance of the JFET-input transistors, without sacrificing the output drive associated with bipolar amplifiers. This makes them better suited for interfacing with high-impedance sensors or low-level ac signals. They also feature inherently better ac response than bipolar or CMOS devices having comparable power consumption. The TLE206x family features a high-output-drive circuit capable of driving 100-Ω loads at supplies as low as ±5 V. This makes them uniquely suited for driving transformer loads in modems and other applications requiring good ac characteristics, low power, and high output drive.

Because BiFET operational amplifiers are designed for use with dual power supplies, care must be taken to observe common-mode input voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required and loads should be terminated to a virtual ground node at mid-supply. Texas Instruments TLE2426 integrated virtual ground generator is useful when operating BiFET amplifiers from single supplies.

The TLE206x are fully specified at ±15 V and ±5 V. For operation in low-voltage and/or single-supply systems, Texas Instruments LinCMOS families of operational amplifiers (TLC- and TLV-prefixes) are recommended. When moving from BiFET to CMOS amplifiers, particular attention should be paid to slew rate and bandwidth requirements and output loading. The Texas Instruments TLV2432 and TLV2442 CMOS operational amplifiers are excellent choices to consider.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TLE2061 AVAILABLE OPTIONS

PACKAGED DEVICES							
T_A	V_{IO}max AT 25°C	SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP‡ (PW)	CERAMIC FLAT PACK (U)
0°C to 70°C	500 μV	—	—	—	—	—	—
	1.5 mV	TLE2061ACD	—	—	TLE2061ACP	—	—
	3 mV	TLE2061CD	—	—	TLE2061CP	TLE2061CPWLE	—
−40°C to 85°C	500 μV	—	—	—	—	—	—
	1.5 mV	TLE2061AID	—	—	TLE2061AIP	—	—
	3 mV	TLE2061ID	—	—	TLE2061IP	—	—
−55°C to 125°C	500 μV	—	—	TLE2061BMJG	—	—	—
	1.5 mV	TLE2061AMD	TLE2061AMFK	TLE2061AMJG	—	—	TLE2061AMU
	3 mV	TLE2061MD	TLE2061MFK	TLE2061MJG	—	—	TLE2061MU

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2061ACDR).Chips are tested at 25°C.
‡ The PW package is available left-end taped and reeled (indicated by the LE suffix on the device type (e.g., TLE2061CPWLE).

TLE2062 AVAILABLE OPTIONS

PACKAGED DEVICES						
T_A	V_{IO}max AT 25°C	SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CERAMIC FLAT PACK (U)
0°C to 70°C	1 mV	TLE2062BCD	—	—	TLE2062BCP	—
	2 mV	TLE2062ACD	—	—	TLE2062ACP	—
	4 mV	TLE2062CD	—	—	TLE2062CP	—
−40°C to 85°C	1 mV	TLE2062BID	—	—	TLE2062BIP	—
	2 mV	TLE2062AID	—	—	TLE2062AIP	—
	4 mV	TLE2062ID	—	—	TLE2062IP	—
−55°C to 125°C	1 mV	TLE2062BMD	—	TLE2062BMJG	—	—
	2 mV	TLE2062AMD	TLE2062AMFK	TLE2062AMJG	—	TLE2062AMU
	4 mV	TLE2062MD	TLE2062MFK	TLE2062MJG	—	TLE2062MU

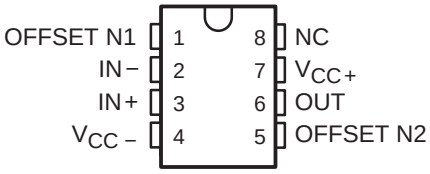
† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2062ACDR).

TLE2064 AVAILABLE OPTIONS

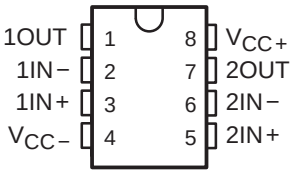
PACKAGED DEVICES						
T_A	V_{IO}max AT 25°C	SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	CERAMIC FLAT PACK (W)
0°C to 70°C	2 mV	—	—	—	TLE2064BCN	—
	4 mV	TLE2064ACD			TLE2064ACN	
	6 mV	TLE2064CD			TLE2064CN	
−40°C to 85°C	2 mV	—	—	—	TLE2064BIN	—
	4 mV	TLE2064AID			TLE2064AIN	
	6 mV	TLE2064ID			TLE2064IN	
−55°C to 125°C	2 mV	—	TLE2064BMFK	TLE2064BMJ	—	—
	4 mV	TLE2064AMD	TLE2064AMFK	TLE2064AMJ		TLE2064AMW
	6 mV	TLE2064MD	TLE2064MFK	TLE2064MJ		TLE2064MW

† The D packages are available taped and reeled. Add R suffix to device type, (e.g., TLE2064ACDR).

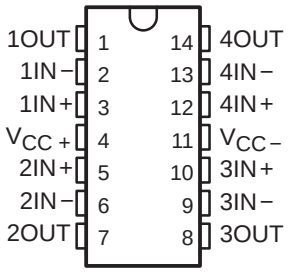
TLE2061, TLE2061A, AND TLE2061B
D, DB, JG, P, OR PW PACKAGE
(TOP VIEW)



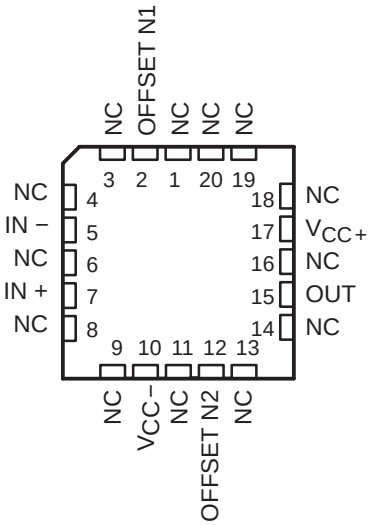
TLE2062, TLE2062A, TLE2062B
D, JG, OR P PACKAGE
(TOP VIEW)



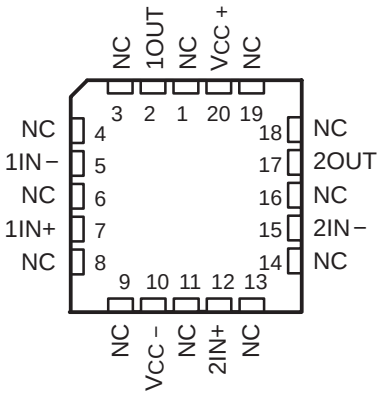
TLE2064, TLE2064A, TLE2064B
D, J, N, OR W PACKAGE
(TOP VIEW)



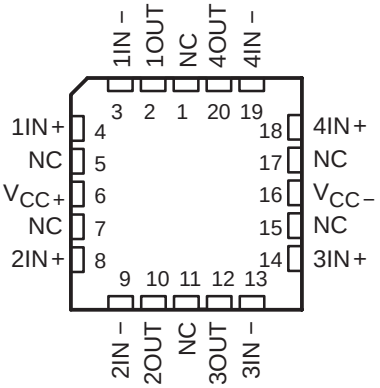
TLE2061M, TLE2061AM, TLE2061BM
FK PACKAGE
(TOP VIEW)



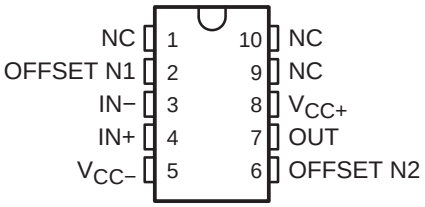
TLE2062M, TLE2062AM, TLE2062BM
FK PACKAGE
(TOP VIEW)



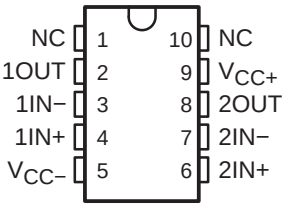
TLE2064M, TLE2064AM, TLE2064BM
FK PACKAGE
(TOP VIEW)



TLE2061 AND TLE2061A
U PACKAGE
(TOP VIEW)

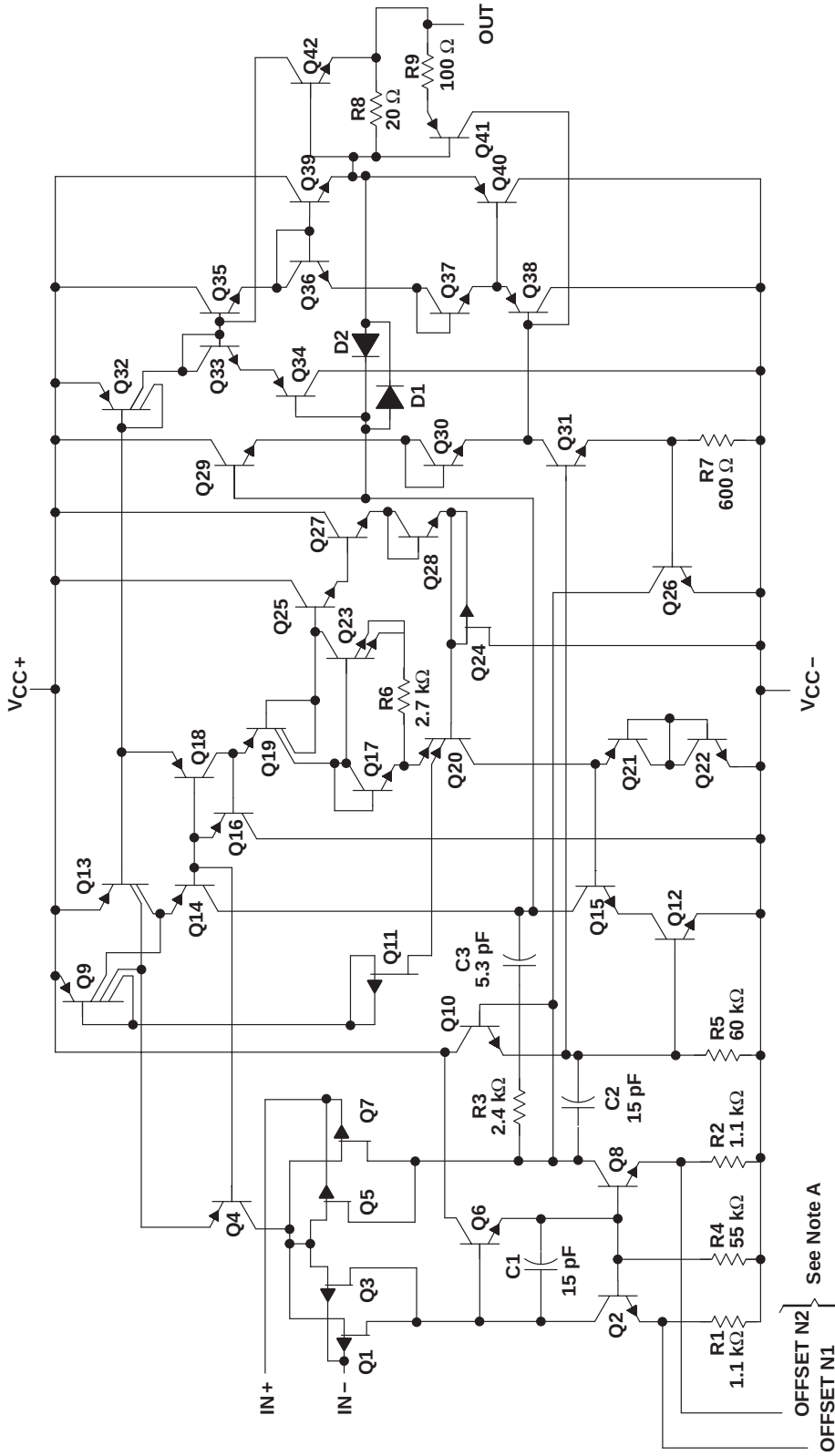


TLE2062 AND TLE2062A
U PACKAGE
(TOP VIEW)



NC − No internal connection

equivalent schematic (each channel)



ACTUAL DEVICE COMPONENT COUNT			
COMPONENT	TLE2061	TLE2062	TLE2064
Transistors	43	42	42
Resistors	9	9	9
Diodes	1	2	2
Capacitors	3	3	3

NOTES: A. OFFSET N1 AND OFFSET N2 are only availiable on the TLE2061x devices.
B. Component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . . 19 V
Supply voltage, V_{CC-} . . . . . −19 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±38 V
Input voltage range, V_I (any input) . . . . . $\pm V_{CC}$
Input current, I_I (each input) . . . . . ±1 mA
Output current, I_O . . . . . ±80 mA
Total current into V_{CC+} . . . . . 80 mA
Total current out of V_{CC-} . . . . . −80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package (8-pin) . . . . . 97.1°C/W
D package (14-pin) . . . . . 86.2°C/W
N package . . . . . 79.7°C/W
P package . . . . . 84.6°C/W
PW package . . . . . 113°C/W
Package thermal impedance, θ_{JC} (see Notes 4 and 5): FK package . . . . . 5.6°C/W
J package . . . . . 15.1°C/W
JG package . . . . . 14.5°C/W
U package . . . . . 14.7°C/W
W package . . . . . 10°C/W
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . −40°C to 85°C
M suffix . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG, U, or W package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7 (plastic) or MIL-STD-883 Method 1012 (ceramic).

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±3.5	±18	±3.5	±18	±3.5	±18	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ±5 V	−1.6	4	−1.6	4	−1.6	4	V
	$V_{CC\pm}$ = ±15 V	−11	13	−11	13	−11	13	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

TLE2061C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061C	V_{IC} = 0, R_S = 50 Ω	25°C		0.8	3.1	mV
				Full range			4	
		TLE2061AC		25°C		0.6	2.6	
				Full range			3.5	
		TLE2061BC		25°C		0.5	1.9	
				Full range			2.4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.3			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.3			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 6: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2061C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		29		μA

† Full range is 0°C to 70°C.

TLE2061C operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ, C_L = 100 pF	25°C	2.2	3.4		V/μs
			Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz, R_S = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, f = 10 kHz, $V_{O(PP)}$ = 2 V, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω, C_L = 100 pF			1.3		
t_s	Settling time	0.1%	25°C		5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1, R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		58°		
		R_L = 100 Ω, C_L = 100 pF			75°		

† Full range is 0°C to 70°C.

TLE2061C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061C	V_{IC} = 0, R_S = 50 kΩ	25°C		0.6	3	mV
				Full range			3.9	
		TLE2061AC		25°C		0.5	1.5	
				Full range			2.5	
		TLE2061BC		25°C		0.3	0.5	
				Full range			1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2061C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		290	350	μA
			Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		34		μA

† Full range is 0°C to 70°C.

TLE2061C operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2061C TLE2061AC TLE2061BC			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ, C_L = 100 pF	25°C	2.6	3.4		V/μs
			Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz, R_S = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, f = 10 kHz, $V_{O(PP)}$ = 2 V, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω, C_L = 100 pF			1.5		
t_s	Settling time	0.1%	25°C		5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1, R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		60°		
		R_L = 600 Ω, C_L = 100 pF			70°		

† Full range is 0°C to 70°C.

TLE2061I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061I, TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061I	V_{IC} = 0, R_S = 50 Ω	25°C		0.8	3.1	mV
				Full range			4.4	
		TLE2061AI		25°C		0.6	2.6	
				Full range			3.9	
		TLE2061BI		25°C		0.5	1.9	
				Full range			2.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.1			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.1			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		V_O = 0, No load	25°C		280	325	μA
				Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		29		μA

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2061I operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/μs
				Full range	1.7			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF			1.3		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF			75°		

† Full range is −40°C to 85°C.

TLE2061I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061I, TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061I	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			4.3	
		TLE2061AI		25°C		0.5	1.5	
				Full range			2.9	
		TLE2061BI		25°C		0.3	0.5	
				Full range			1.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	01			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		V_O = 0, No load	25°C		290	350	μA
				Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		34		μA

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2061I operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061I TLE2061AI TLE2061BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

† Full range is −40°C to 85°C.

TLE2061M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061M TLE2061AM TLE2061BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061M	V_{IC} = 0, R_S = 50 Ω	25°C		0.8	3.1	mV
				Full range			6	
		TLE2061AM		25°C		0.6	2.6	
				Full range			4.6	
		TLE2061BM		25°C		0.5	1.9	
				Full range			3.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3			
			R_L = 600 Ω	25°C	2.5	3.6		
				Full range	2			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.5	−3.9		V
				Full range	−3			
		FK and JG packages	R_L = 600 Ω	25°C	−2.5	−3.5		
				Full range	−2			
		D and P packages	R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
		FK and JG packages	V_O = 0 to 2.5 V, R_L = 600 Ω	25°C	1	65		
				Full range	0.5			
			V_O = 0 to −2.5 V, R_L = 600 Ω	25°C	1	16		
				Full range	0.5			
		D and P packages	V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2061M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061M TLE2061AM TLE2061BM			UNIT
				MIN	TYP	MAX	
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current	V_O = 0, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		39		μA

† Full range is −55°C to 125°C.

TLE2061M operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2061M TLE2061AM TLE2061BM			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF		3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		59		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		1.8		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.3		
t_s	Settling time	0.1%			5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		58°		
		R_L = 600 Ω,	C_L = 100 pF		75°		

TLE2061M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2061M ,TLE2061AM TLE2061BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2061M	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			6	
		TLE2061AM		25°C		0.5	1.5	
				Full range			3.6	
		TLE2061BM		25°C		0.3	0.5	
				Full range			1.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13	13.7		V
				Full range	12.5			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13	−13.7		V
				Full range	−12.5			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	7			
			V_O = 0 to − 8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2061M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continue)

PARAMETER		TEST CONDITIONS	T_A†	TLE2061M ,TLE2061AM TLE2061BM			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		290	350	μA
			Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		46		μA

† Full range is −55°C to 125°C.

TLE2061M operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2061M TLE2061AM TLE2061BM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2	3.4		V/μs
				Full range	1.8			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω	25°C		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
t_s	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Full range is −55°C to 125°C.

TLE2061Y electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2061Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		0.6	3	mV
α_{VIO}	Input offset voltage long-term drift (see Note 4)				0.04		μV/mo
I_{IO}	Input offset current				2		pA
I_{IB}	Input bias current				4		pA
V_{ICR}	Common-mode input voltage range			−11 to 13	−12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		13.2	13.7		V
		R_L = 600 Ω		12.5	13.2		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		−13.2	−13.7		V
		R_L = 600 Ω		−12.5	− 13		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 10 kΩ	30	230		V/mV
		V_O = 0 to 8 V,	R_L = 600 Ω	25	100		
		V_O = 0 to − 8 V,	R_L = 600 Ω	3	25		
r_i	Input resistance				10^{12}		Ω
c_i	Input capacitance				4		pF
z_o	Open-loop output impedance	I_O = 0			280		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω,	V_{IC} = V_{ICR}min	72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω		75	93		dB
I_{CC}	Supply current	V_O = 0,	No load		290	350	μA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2061Y operating characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2061Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	2.6	3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 Hz			1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		2		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.5		
t_s	Settling time	0.1%			5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		60°		
		R_L = 600 Ω,	C_L = 100 pF		70°		

TLE2062C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2062C TLE2062AC TLE2062BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062C	V_{IC} = 0, R_S = 50 Ω	25°C		1	5	mV
				Full range			5.9	
		TLE2062AC		25°C		0.9	4	
				Full range			4.9	
		TLE2062BC		25°C		0.7	3	
				Full range			3.9	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.3			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.3			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2062C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2062C TLE2062AC TLE2062BC			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		560	620	μA
			Full range			635	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		26		μA

† Full range is 0°C to 70°C.

TLE2062C operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2062C TLE2062AC TLE2062BC			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ, C_L = 100 pF	25°C	2.2	3.4		V/μs
			Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz, R_S = 20 Ω	25°C		43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ, A_{VD} = 2, f = 10 kHz	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω, C_L = 100 pF	25°C		1.3		
	Settling time	0.1%	25°C		5		μs
		0.01%	25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1, R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		58°		
		R_L = 100 Ω, C_L = 100 pF	25°C		75°		

† Full range is 0°C to 70°C.

TLE2062C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2062C TLE2062AC TLE2062BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062C	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	4	mV
				Full range			4.9	
		TLE2062AC		25°C		0.8	2	
				Full range			2.9	
		TLE2062BC		25°C		0.5	1	
				Full range			1.9	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2062C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2062C TLE2062AC TLE2062BC			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0 V,	No load	25°C		625	690	μA
				Full range			715	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		36		μA

† Full range is 0°C to 70°C.

TLE2062C operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2062C TLE2062AC TLE2062BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 2,	R_L = 10 kΩ, f = 10 kHz	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 10 0 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Full range is 0°C to 70°C.

TLE2062I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062I	V_{IC} = 0, R_S = 50 Ω	25°C		1	5	mV
				Full range			6.3	
		TLE2062AI		25°C		0.9	4	
				Full range			5.3	
		TLE2062BI		25°C		0.7	3	
				Full range			4.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.1			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.1			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2062I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		560	620	μA
			Full range			640	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		54		μA

† Full range is −40°C to 85°C.

TLE2062I operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ, C_L = 100 pF	25°C	2.2	3.4		V/μs
			Full range	1.7			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz, R_S = 20 Ω	25°C		43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ, A_{VD} = 2, f = 10 kHz	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω, C_L = 100 pF	25°C		1.3		
	Settling time	0.1%	25°C		5		μs
		0.01%	25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1, R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		58°		
		R_L = 100 Ω, C_L = 100 pF	25°C		75°		

† Full range is −40°C to 85°C.

TLE2062I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062I	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	4	mV
				Full range			5.3	
		TLE2062AI		25°C		0.8	2	
				Full range			3.3	
		TLE2062BI		25°C		0.5	1	
				Full range			2.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2062I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
				MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0, No load	25°C		625	690	μA
			Full range			720	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		74		μA

† Full range is −40°C to 85°C.

TLE2062I operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	T_A†	TLE2062I TLE2062AI TLE2062BI			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ, C_L = 100 pF	25°C	2.6	3.4		V/μs
			Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz, R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz, R_S = 20 Ω	25°C		40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ, A_{VD} = 2, f = 10 kHz	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω, C_L = 100 pF	25°C		1.5		
	Settling time	0.1%	25°C		5		μs
		0.01%	25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1, R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ, C_L = 100 pF	25°C		60°		
		R_L = 600 Ω, C_L = 100 pF	25°C		70°		

† Full range is −40°C to 85°C.

TLE2062M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER			TEST CONDITIONS	T_A†	TLE2062M TLE2062AM TLE2062BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062M	V_{IC} = 0, R_S = 50 Ω	25°C		1	5	mV
				Full range			7	
		TLE2062AM		25°C		0.9	4	
				Full range			6	
		TLE2062BM		25°C		0.7	3	
				Full range			5	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3			
		FK and JG packages	R_L = 600 Ω	25°C	2.5	3.6		
				Full range	2			
		D and P packages	R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.5	−3.9		V
				Full range	−3			
		FK and JG packages	R_L = 600 Ω	25°C	−2.5	−3.5		
				Full range	−2			
		D and P packages	R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
		FK and JG packages	V_O = 0 to 2.5 V, R_L = 600 Ω	25°C	1	65		
				Full range	0.5			
			V_O = 0 to −2.5 V, R_L = 600 Ω	25°C	1	16		
				Full range	0.5			
		D and P packages	V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.25			

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2062M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2062M TLE2062AM TLE2062BM			UNIT
				MIN	TYP	MAX	
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω,	25°C	65	82		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current (two amplifiers)	V_O = 0, No load	25°C		560	620	μA
			Full range			650	
ΔI_{CC}	Supply-current change over operating temperature range (two amplifiers)	V_O = 0, No load	Full range		72		μA

† Full range is −55°C to 125°C.

TLE2062M operating characteristics at specified free-air temperature, T_A = 25°C, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		TLE2062M TLE2062AM TLE2062BM			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF		3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		59		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 2,	R_L = 10 kΩ, f = 10 kHz		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		1.8		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.3		
	Settling time	0.1%			5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		58°		
		R_L = 600 Ω,	C_L = 100 pF		75°		

TLE2062M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2062M TLE2062AM TLE2062BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2062M	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	4	mV
				Full range			6	
		TLE2062AM		25°C		0.8	2	
				Full range			4	
		TLE2062BM		25°C		0.5	1	
				Full range			3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13	13.7		V
				Full range	12.5			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	11			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13	−13.7		V
				Full range	−12.5			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−11			
A_{VD}	Large-signal differential voltage amplification		V_O = ± 10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	7			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ± 5 V to ± 15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2062M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2062M TLE2062AM TLE2062BM			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current	V_O = 0,	No load	25°C		625	690	μA
				Full range			730	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		97		μA

† Full range is −55°C to 125°C.

TLE2062M operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2062M TLE2062AM TLE2062BM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2	3.4		V/μs
				Full range	1.8			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω	25°C		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 2,	R_L = 10 kΩ, f = 10 kHz	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF	25°C		1.5		
	Settling time	0.1%		25°C		5		μs
		0.01%		25°C		10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF	25°C		70°		

† Full range is −55°C to 125°C.

TLE2062Y electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2062Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		0.9	4	mV
α_{VIO}	Input offset voltage long-term drift (see Note 4)				0.04		μV/mo
I_{IO}	Input offset current				2		pA
I_{IB}	Input bias current				4		pA
V_{ICR}	Common-mode input voltage range			−11 to 13	−12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		13.2	13.7		V
		R_L = 600 Ω		12.5	13.2		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		−13.2	−13.7		V
		R_L = 600 Ω		−12.5	−13		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 10 kΩ	30	230		V/mV
		V_O = 0 to 8 V,	R_L = 600 Ω	25	100		
		V_O = 0 to −8 V,	R_L = 600 Ω	3	25		
r_i	Input resistance				10^{12}		Ω
c_i	Input capacitance				4		pF
z_o	Open-loop output impedance	I_O = 0			560		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω		75	93		dB
I_{CC}	Supply current	V_O = 0,	No load		625	690	μA

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2062Y operating characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2062Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	2.6	3.4	4	V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 Hz			1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 2,	R_L = 10 kΩ, f = 10 kHz		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		2		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.5		
	Settling time	0.1%			5		μs
		0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		60°		
		R_L = 600 Ω,	C_L = 100 pF		70°		

TLE2064C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064C	V_{IC} = 0, R_S = 50 Ω	25°C		1.2	7	mV
				Full range			7.9	
		TLE2064AC		25°C		1.2	6	
				Full range			6.9	
		TLE2064BC		25°C		0.8	3.5	
				Full range			4.4	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.3			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.3			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.15			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2064C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		1.12	1.3	mA
				Full range			1.3	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		52		μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

† Full range is 0°C to 70°C.

TLE2064C operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF			1.3		
t_s	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF			75°		

† Full range is 0°C to 70°C.

TLE2064C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064C	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	6	mV
				Full range			6.9	
		TLE2064AC		25°C		0.9	4	
				Full range			4.9	
		TLE2064BC		25°C		0.7	2	
				Full range			4	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	75			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2064C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		1.25	1.4	mA
				Full range			1.5	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		72		μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

† Full range is 0°C to 70°C.

TLE2064C operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2064C TLE2064AC TLE2064BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.5			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
t_s	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		50°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

† Full range is 0°C to 70°C.

TLE2064I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064I	V_{IC} = 0, R_S = 50 Ω	25°C		1.2	7	mV
				Full range			8.3	
		TLE2064AI		25°C		1.2	6	
				Full range			7.3	
		TLE2064BI		25°C		0.8	3.5	
				Full range			4.8	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3.1			
			R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.7	−3.9		V
				Full range	−3.1			
			R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
			V_O = 0 to 2 V, R_L = 100 Ω	25°C	0.75	45		
				Full range	0.5			
			V_O = 0 to −2 V, R_L = 100 Ω	25°C	0.5	3		
				Full range	0.15			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is −40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2064I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		1.12	1.3	mA
				Full range			1.3	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		108		μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

† Full range is −40°C to 85°C.

TLE2064I operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.2	3.4		V/μs
				Full range	1.7			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		59	100	nV/√Hz
		f = 1 kHz,	f = 1 kHz,			43	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		1.8		MHz
		R_L = 100 Ω,	C_L = 100 pF			1.3		
t_s	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		58°		
		R_L = 100 Ω,	C_L = 100 pF			75°		

† Full range is − 40°C to 85°C.

TLE2064I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064I	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	6	mV
				Full range			7.3	
		TLE2064AI		25°C		0.9	4	
				Full range			5.3	
		TLE2064BI		25°C		0.7	2	
				Full range			3.3	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13.2	−13.7		V
				Full range	−13			
			R_L = 600 Ω	25°C	−12.5	−13		
				Full range	−12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is − 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2064I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		1.25	1.4	mA
				Full range			1.5	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		148		μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

† Full range is − 40°C to 85°C.

TLE2064I operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2064I TLE2064AI TLE2064BI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	2.1			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω,	25°C		70	100	nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			40	60	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, R_L = 10 kΩ	f = 10 kHz, $V_{O(PP)}$ = 2 V,	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
t_s	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

† Full range is − 40°C to 85°C.

TLE2064M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064M TLE2064AM TLE2064BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064M	V_{IC} = 0, R_S = 50 Ω	25°C		1.2	7	mV
				Full range			9	
		TLE2064AM		25°C		1.2	6	
				Full range			8	
		TLE2064BM		25°C		0.8	3.5	
				Full range			5.5	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.6 to 4	−2 to 6		V
				Full range	−1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	3.5	3.7		V
				Full range	3			
		FK and J packages	R_L = 600 Ω	25°C	2.5	3.6		
				Full range	2			
		D and N packages	R_L = 100 Ω	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−3.5	−3.9		V
				Full range	−3			
		FK and J packages	R_L = 600 Ω	25°C	−2.5	−3.5		
				Full range	−2			
		D and N packages	R_L = 100 Ω	25°C	−2.5	−2.7		
				Full range	−2			
A_{VD}	Large-signal differential voltage amplification		V_O = ±2.8 V, R_L = 10 kΩ	25°C	15	80		V/mV
				Full range	2			
		FK and J packages	V_O = 0 to 2.5 V, R_L = 600 Ω	25°C	1	65		
				Full range	0.5			
			V_O = 0 to −2.5 V, R_L = 600 Ω	25°C	1	16		
				Full range	0.5			

† Full range is − 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2064M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V (unless otherwise noted) continued)

PARAMETER			TEST CONDITIONS		T_A†	TLE2064M TLE2064AM TLE2064BM			UNIT
						MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	D and N packages	V_O = 0 to 2 V,	R_L = 100 Ω	25°C	0.75	45		V/mV
					Full range	0.25			
			V_O = 0 to −2 V,	R_L = 100 Ω	25°C	0.4	3		
					Full range	0.15			
r_i	Input resistance				25°C		10^{12}		Ω
c_i	Input capacitance				25°C		4		pF
z_o	Open-loop output impedance		I_O = 0		25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	65	82		dB
					Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω		25°C	75	93		dB
					Full range	65			
I_{CC}	Supply current (four amplifiers)		V_O = 0,	No load	25°C		1.12	1.3	mA
					Full range			1.3	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)				Full range		144		μA
V_{O1}/V_{O2}	Crosstalk attenuation		A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

† Full range is −55°C to 125°C.

TLE2064M operating characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2064M TLE2064AM TLE2064BM			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF		3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		59		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		43		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		1.8		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.3		
t_s	Settling time	ε = 0.1%			5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		140		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		58°		
		R_L = 600 Ω,	C_L = 100 pF		75°		

TLE2064M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2064M TLE2064AM TLE2064BM			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2064M	V_{IC} = 0, R_S = 50 Ω	25°C		0.9	6	mV
				Full range			8	
		TLE2064AM		25°C		0.9	4	
				Full range			6	
		TLE2064BM		25°C		0.7	2	
				Full range			4	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			Full range		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	−11 to 13	−12 to 16		V
				Full range	−11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13	13.7		V
				Full range	12.5			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	−13	−13.7		V
				Full range	−12.5			
			R_L = 600 Ω	25°C	−13	−13		
				Full range	−12.5			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	7			
			V_O = 0 to −8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		560		Ω
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω	25°C	75	93		dB
				Full range	65			

† Full range is − 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2064M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLE2064M TLE2064AM TLE2064BM			UNIT
					MIN	TYP	MAX	
I_{CC}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		1.25	1.4	mA
				Full range			1.5	
ΔI_{CC}	Supply-current change over operating temperature range (four amplifiers)			Full range		194		μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz	25°C		120		dB

† Full range is − 55°C to 125°C.

TLE2064M operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS		T_A†	TLE2064M TLE2064AM TLE2064BM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	25°C	2.6	3.4		V/μs
				Full range	1.8			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω	25°C		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω			40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		2		MHz
		R_L = 600 Ω,	C_L = 100 pF			1.5		
t_s	Settling time	ε = 0.1%		25°C		5		μs
		ε = 0.01%				10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ	25°C		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF	25°C		60°		
		R_L = 600 Ω,	C_L = 100 pF			70°		

† Full range is − 55°C to 125°C.

TLE2064Y electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

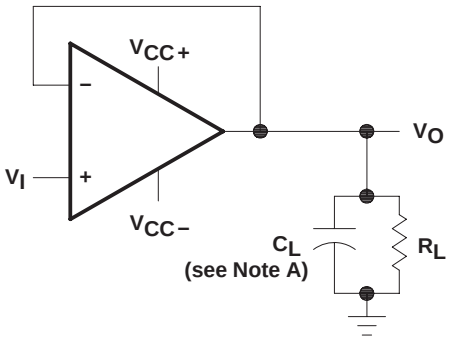
PARAMETER		TEST CONDITIONS		TLE2064Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω		0.9	6	mV
$\propto V_{IO}$	Input offset voltage long-term drift (see Note 4)				0.04		μV/mo
I_{IO}	Input offset current				2		pA
I_{IB}	Input bias current				4		pA
V_{ICR}	Common-mode input voltage range			−11 to 13	−12 to 16		V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		13.2	13.7		V
		R_L = 600 Ω		12.5	13.2		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		−13.2	−13.7		V
		R_L = 600 Ω		12.5	13		V
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 10 kΩ	30	230		V/mV
		V_O = 0 to 8 V,	R_L = 600 Ω	25	100		
		V_O = 0 to −8 V,	R_L = 600 Ω	3	25		
r_i	Input resistance				10^{12}		Ω
c_i	Input capacitance				4		pF
z_o	Open-loop output impedance	I_O = 0			560		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω, V_{IC} = V_{ICR}min,		72	90		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, R_S = 50 Ω		75	93		dB
I_{CC}	Supply current	V_O = 0,	No load		1.25	1.4	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 1000,	f = 1 kHz		120		dB

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLE2064Y operating characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2064Y			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain (see Figure 1)	R_L = 10 kΩ,	C_L = 100 pF	2.6	3.4		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz,	R_S = 20 Ω		70		nV/√Hz
		f = 1 kHz,	R_S = 20 Ω		40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			1.1		μV
I_n	Equivalent input noise current	f = 1 kHz			1.1		fA/√Hz
THD	Total harmonic distortion	A_{VD} = 2, $V_{O(PP)}$ = 2 V,	f = 10 kHz, R_L = 10 kΩ		0.025%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		2		MHz
		R_L = 600 Ω,	C_L = 100 pF		1.5		
t_s	Settling time	ε = 0.1%			5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 1,	R_L = 10 kΩ		40		kHz
ϕ_m	Phase margin at unity gain (see Figure 3)	R_L = 10 kΩ,	C_L = 100 pF		60°		
		R_L = 600 Ω,	C_L = 100 pF		70°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

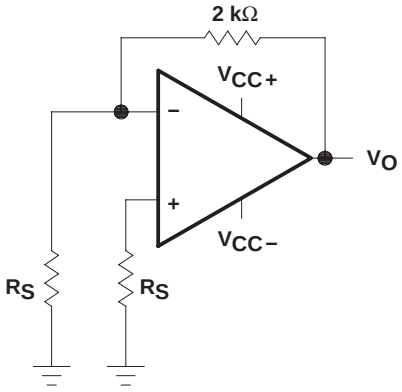
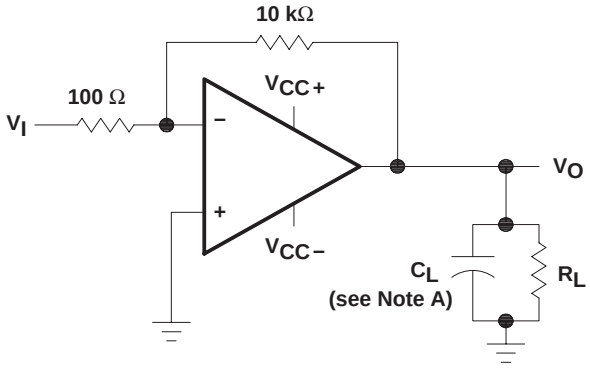


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias current level typical of the TLE206x, TLE2064xA, and TLE206xB, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4, 5, 6
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	7 8
I_{IO}	Input offset current	vs Free-air temperature	8
V_{ICR}	Common-mode input voltage	vs Free-air temperature	9
V_{OM}	Maximum peak output voltage	vs Output current vs Supply voltage	10, 11 12, 13, 14
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency vs Load resistance	15, 16 17
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	18 19
I_{OS}	Short-circuit output current	vs Elasped time vs Free-air temperature	20 21
z_o	Output impedance	vs Frequency	22, 23
CMRR	Common-mode rejection ratio	vs Frequency	24
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	25, 26, 27 28, 29, 30
	Voltage-follower small-signal pulse response	vs Time	31, 32
	Voltage-follower large-signal pulse response	vs Time	33, 34
	Noise voltage (referred to input)	0.1 to 10 Hz	35
V_n	Equivalent input noise voltage	vs Frequency	36
THD	Total harmonic distortion	vs Frequency	37, 38
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	39 40
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	41 42 43
	Phase shift	vs Frequency	18

TYPICAL CHARACTERISTICS

**TLE2061
DISTRIBUTION OF
INPUT OFFSET VOLTAGE**

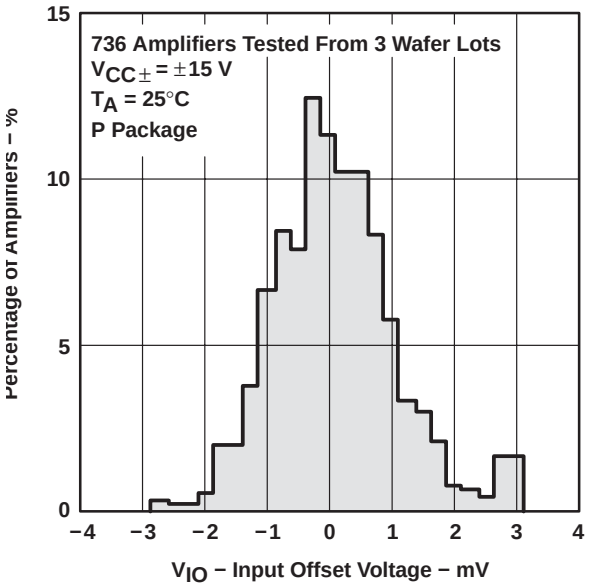


Figure 4

**TLE2062
DISTRIBUTION OF
INPUT OFFSET VOLTAGE**

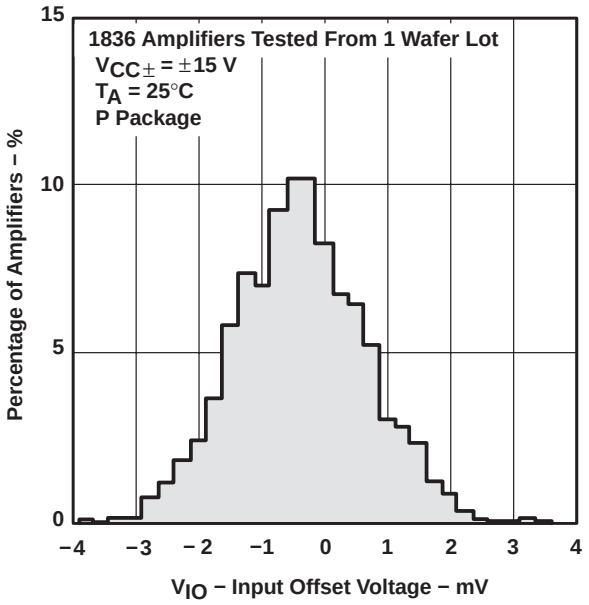


Figure 5

**TLE2064
DISTRIBUTION OF
INPUT OFFSET VOLTAGE**

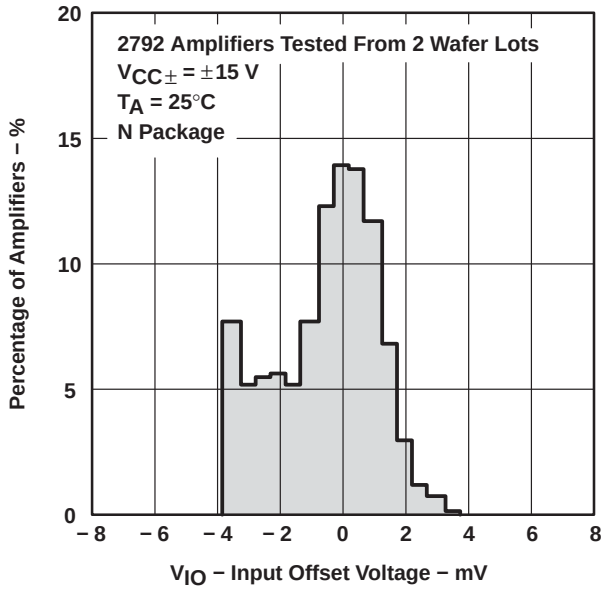


Figure 6

**INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE**

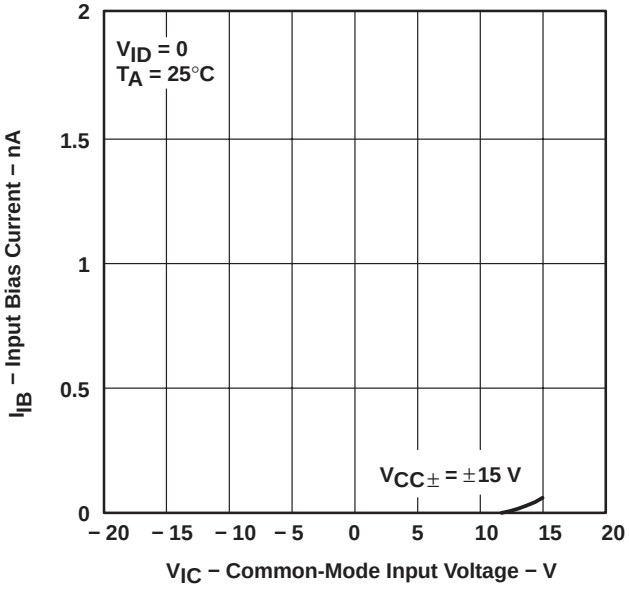


Figure 7

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

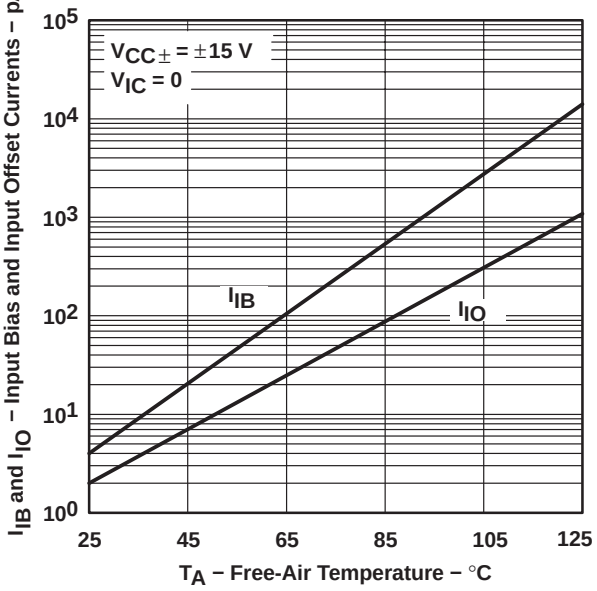


Figure 8

COMMON-MODE INPUT VOLTAGE vs FREE-AIR TEMPERATURE

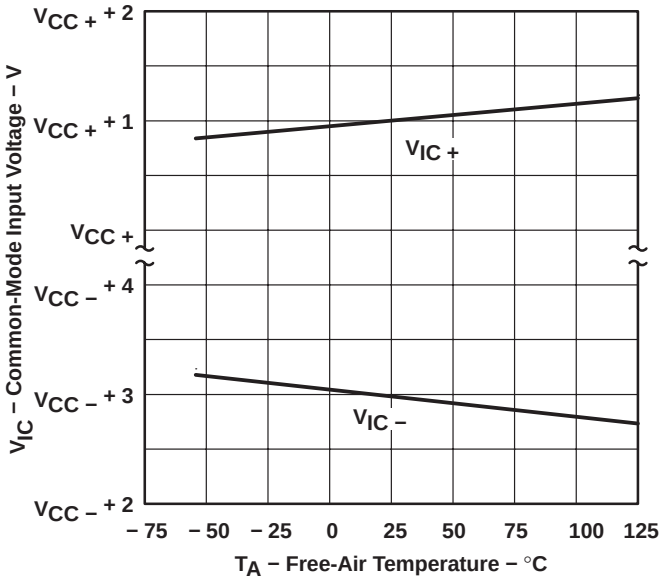


Figure 9

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

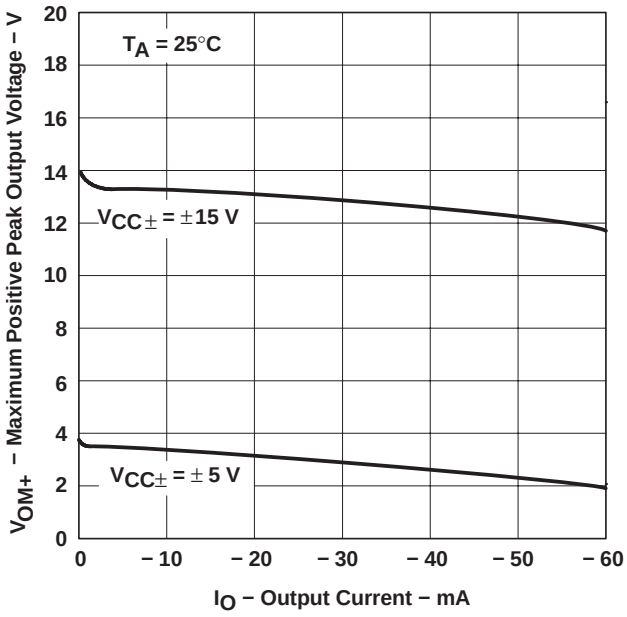


Figure 10

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

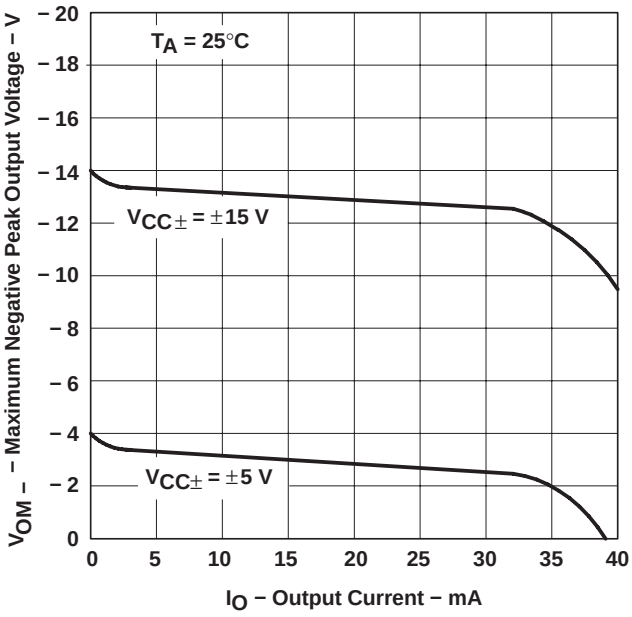


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

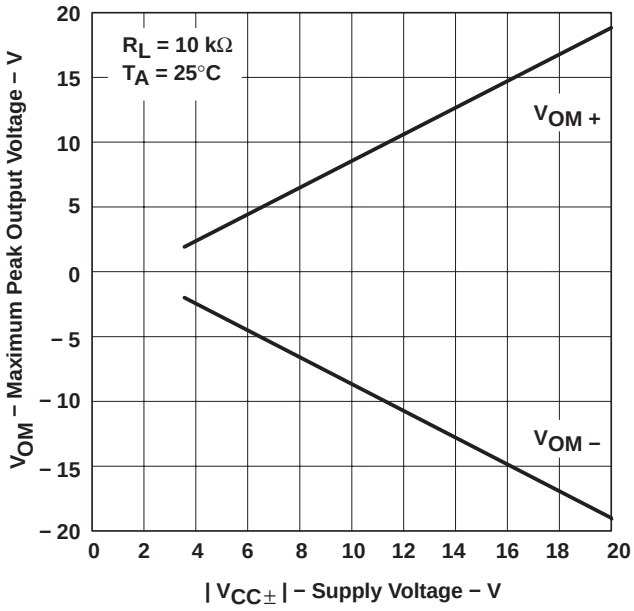


Figure 12

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

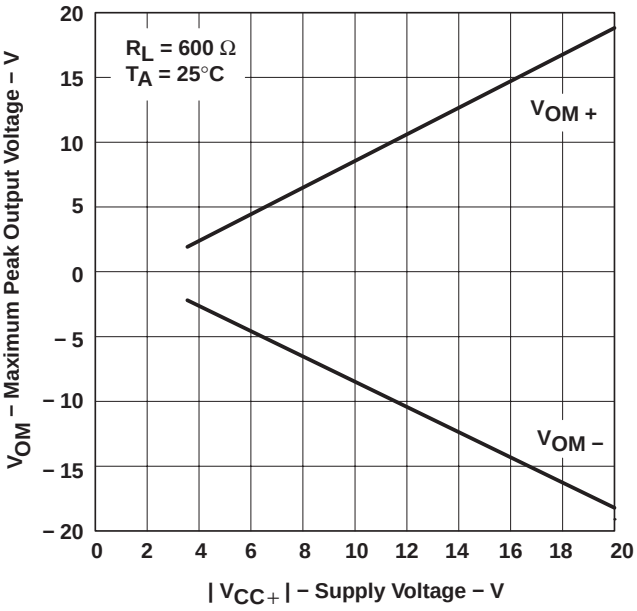


Figure 13

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

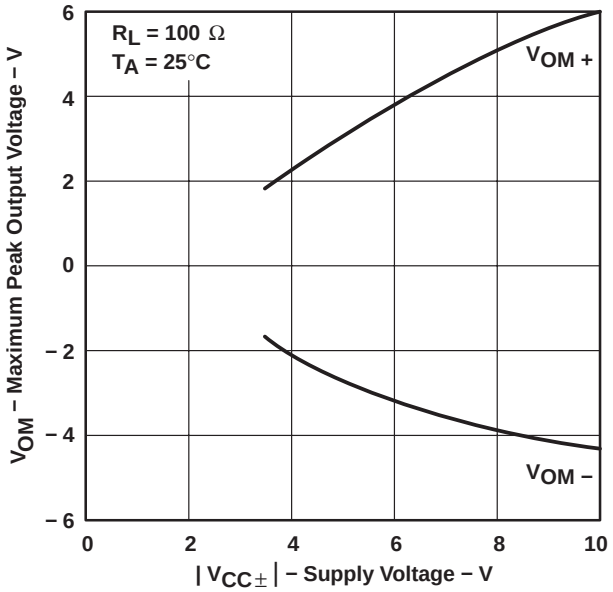


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

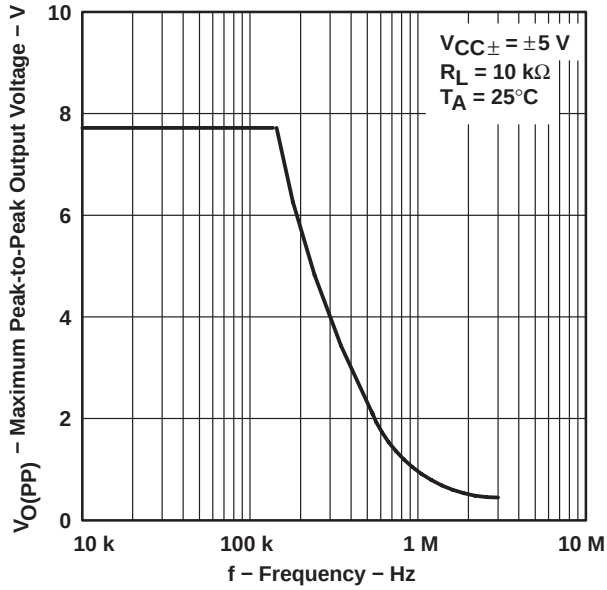


Figure 15

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

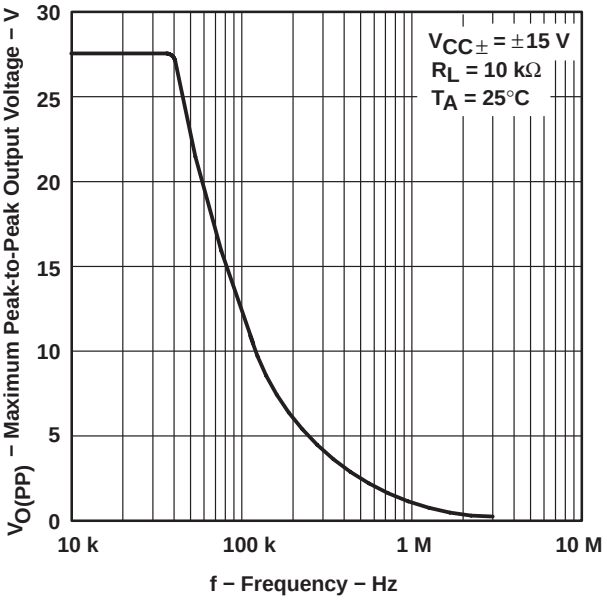


Figure 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

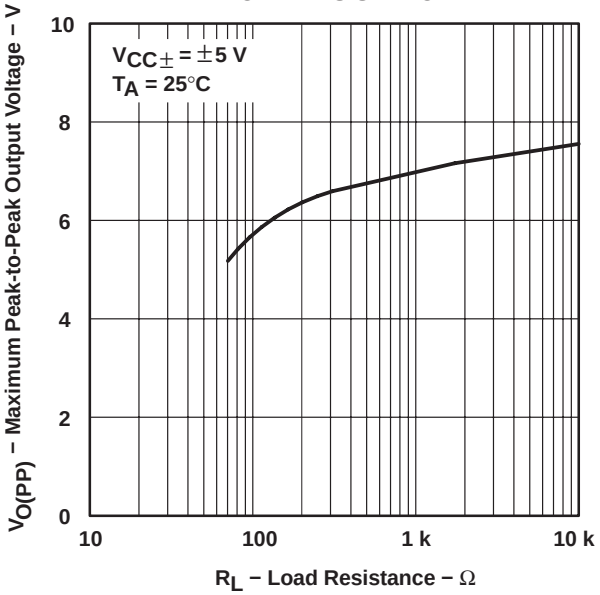


Figure 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

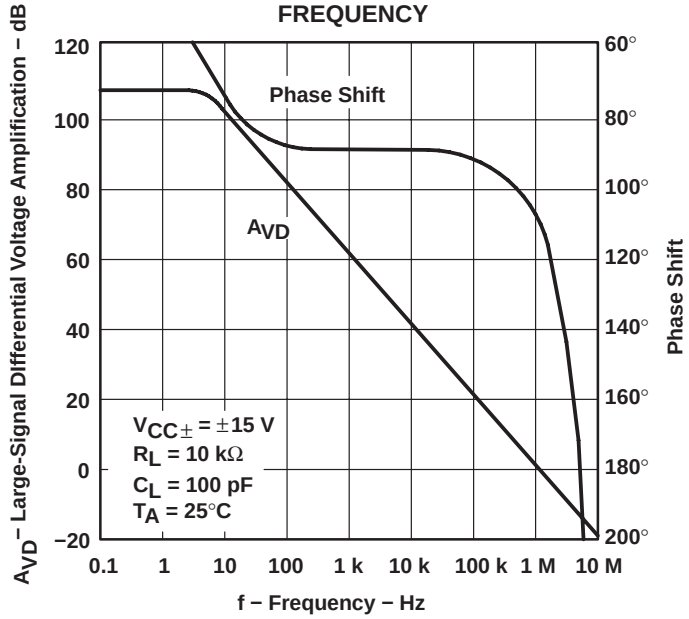


Figure 18

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

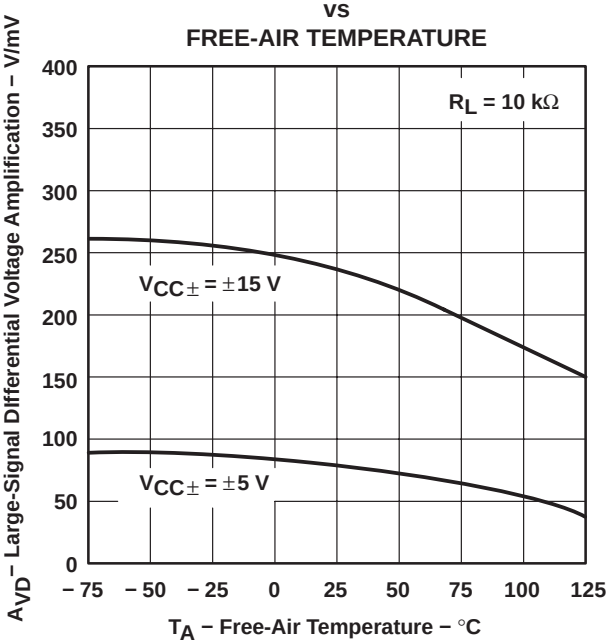


Figure 19

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

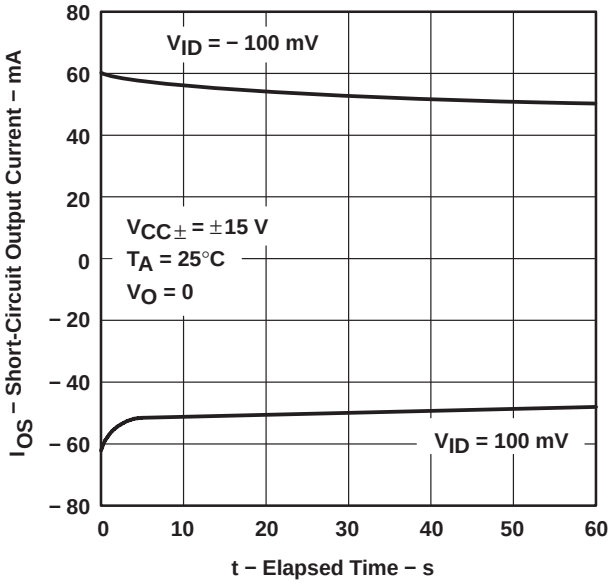


Figure 20

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

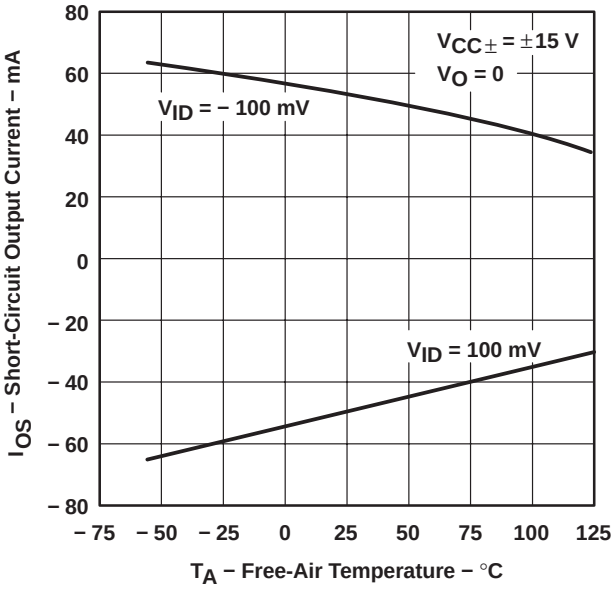


Figure 21

TLE2061 OUTPUT IMPEDANCE vs FREQUENCY

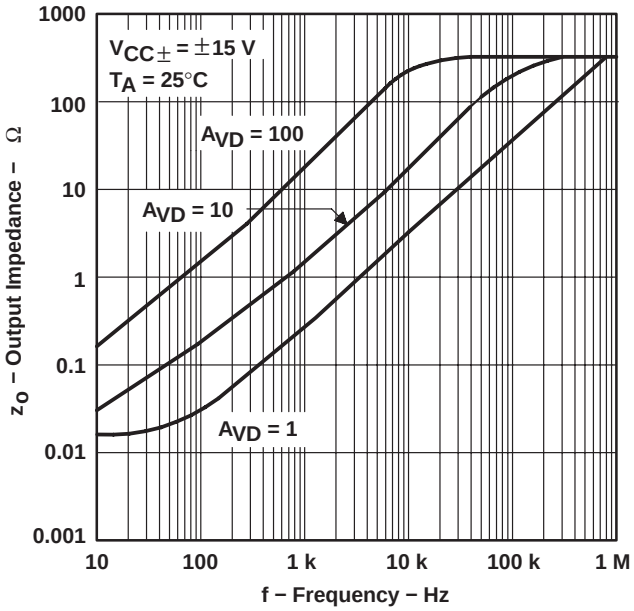


Figure 22

TLE2062 AND TLE2064 OUTPUT IMPEDANCE vs FREQUENCY

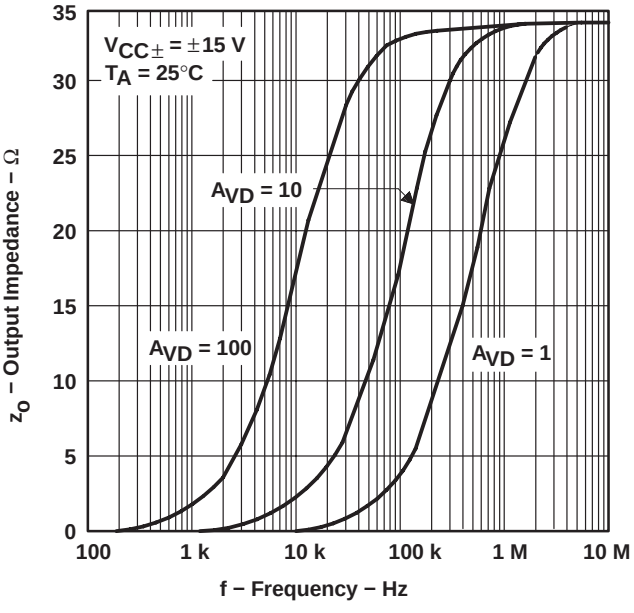


Figure 23

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO vs FREQUENCY

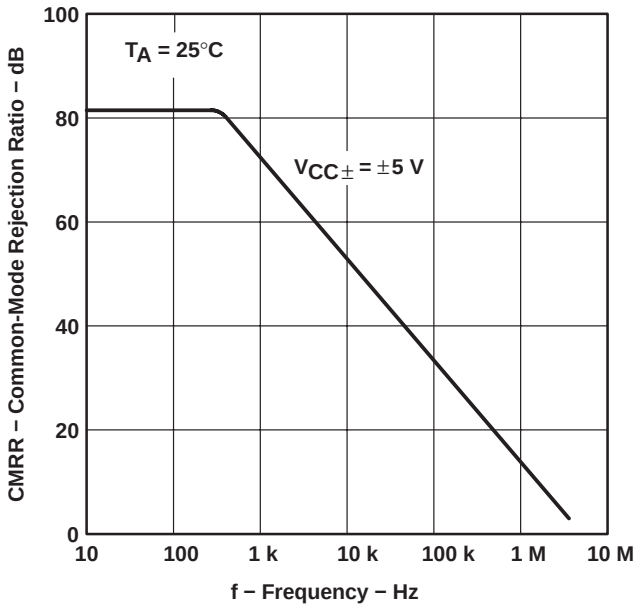


Figure 24

TLE2061 SUPPLY CURRENT vs SUPPLY VOLTAGE

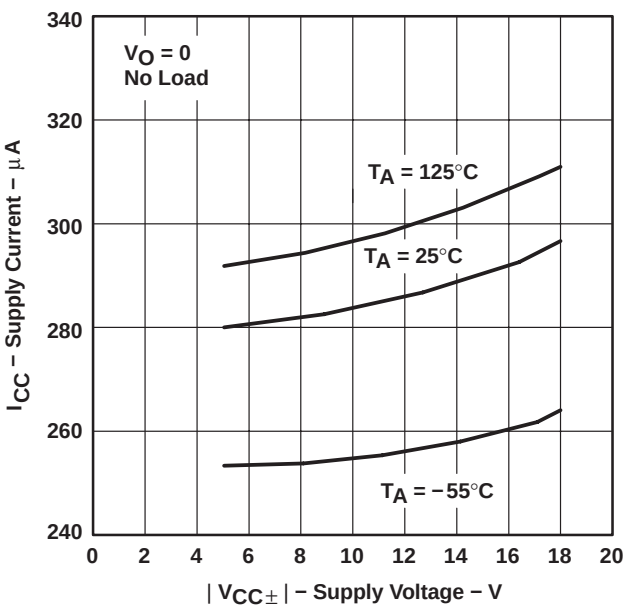


Figure 25

TLE2062 SUPPLY CURRENT vs SUPPLY VOLTAGE

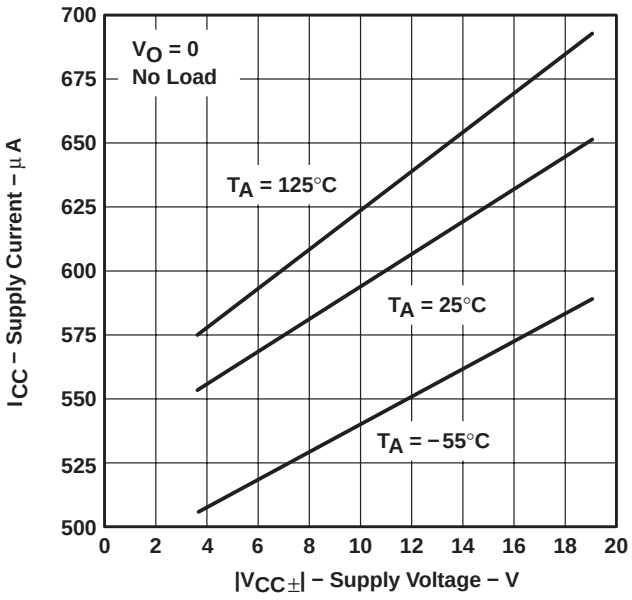


Figure 26

TLE2064 SUPPLY CURRENT vs SUPPLY VOLTAGE

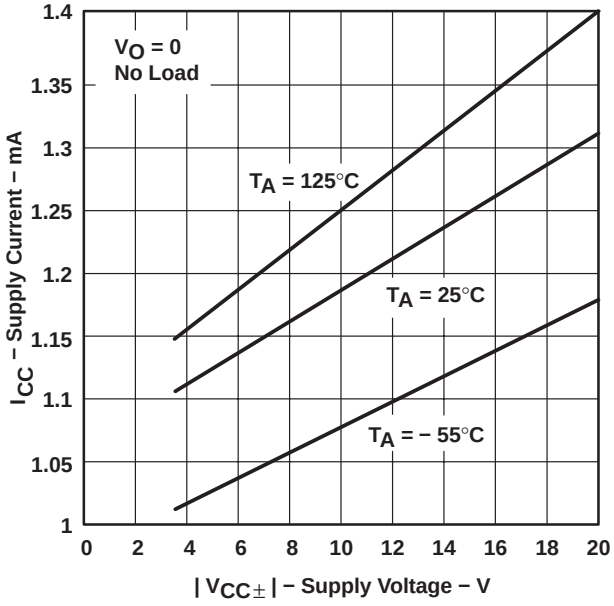


Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

**TLE2061
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

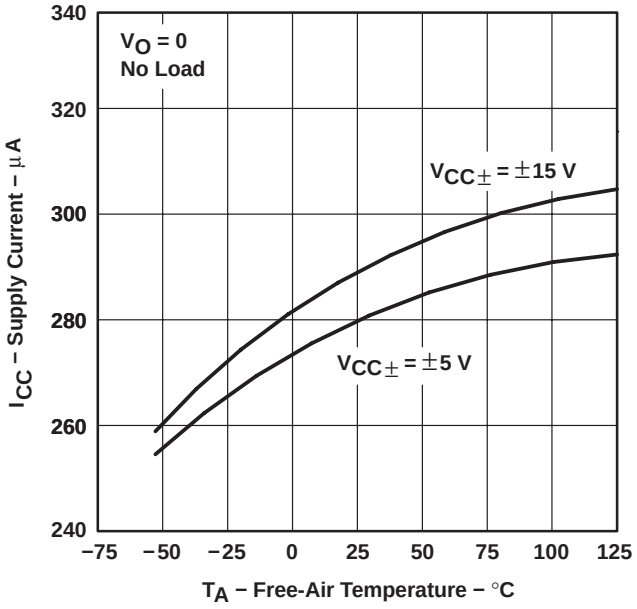


Figure 28

**TLE2062
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

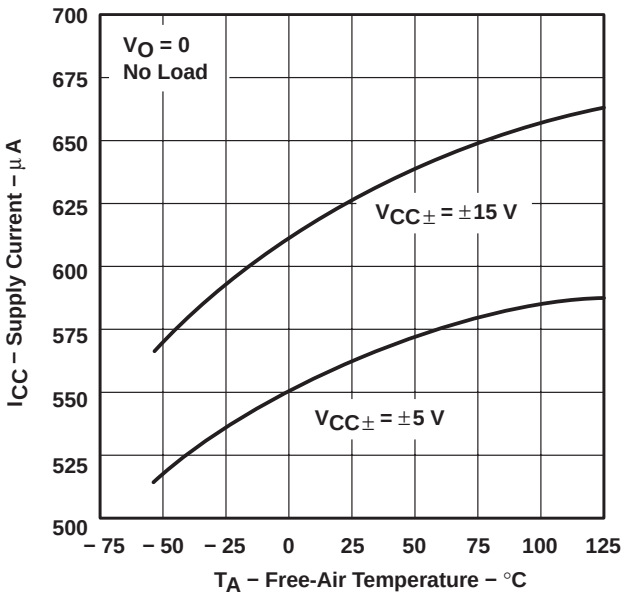


Figure 29

**TLE2064
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

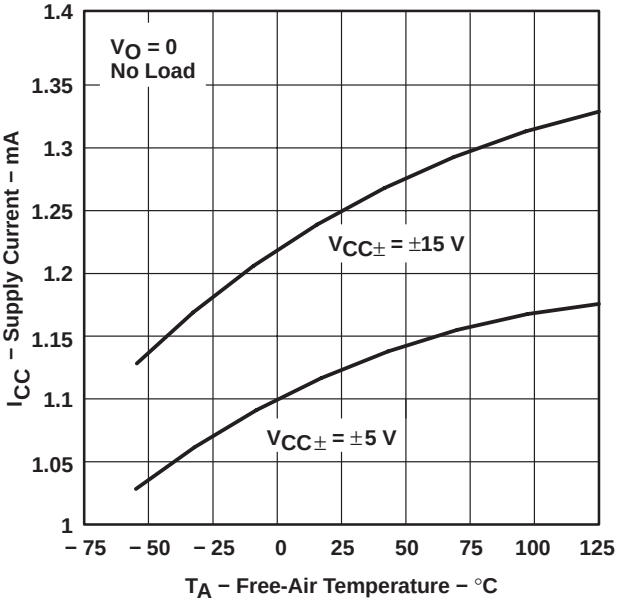


Figure 30

**VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE**

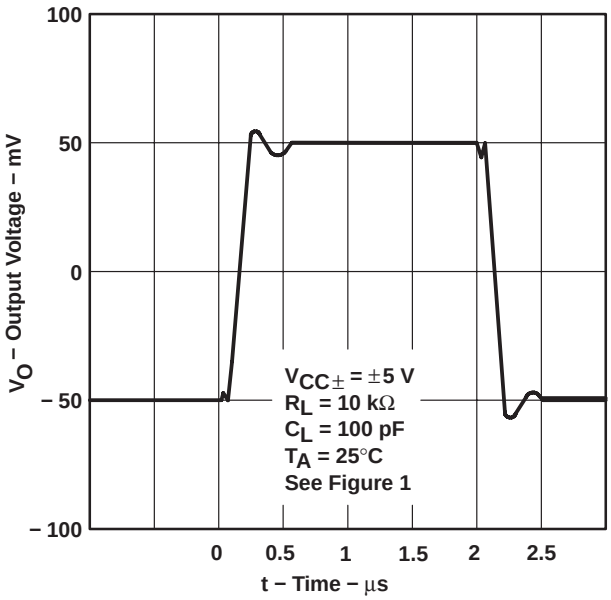


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

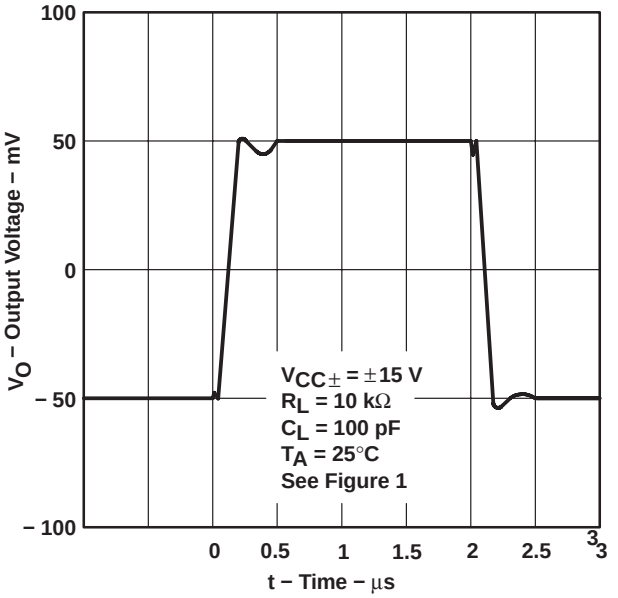


Figure 32

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

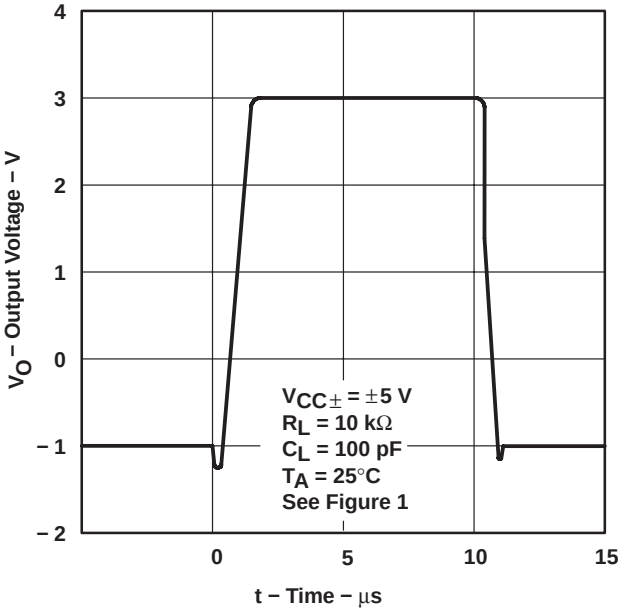


Figure 33

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

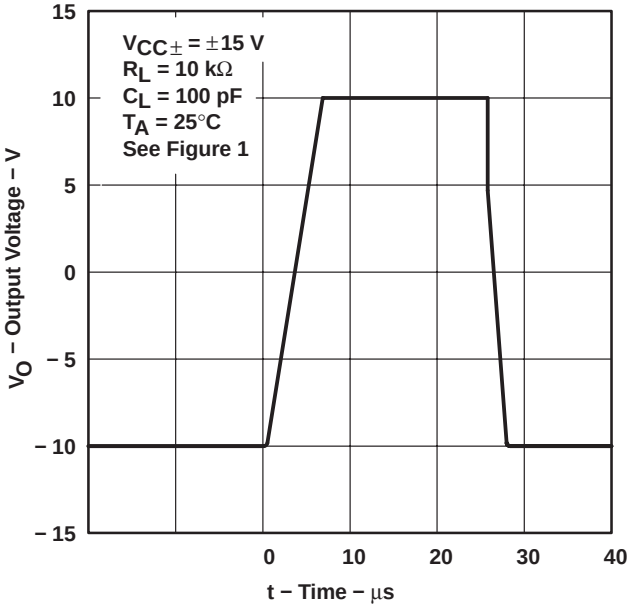


Figure 34

NOISE VOLTAGE
(REFERRED TO INPUT)
0.1 TO 10 Hz

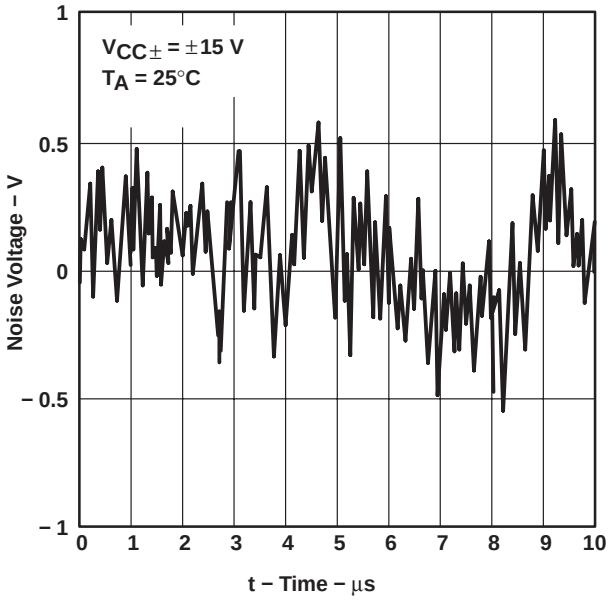


Figure 35

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

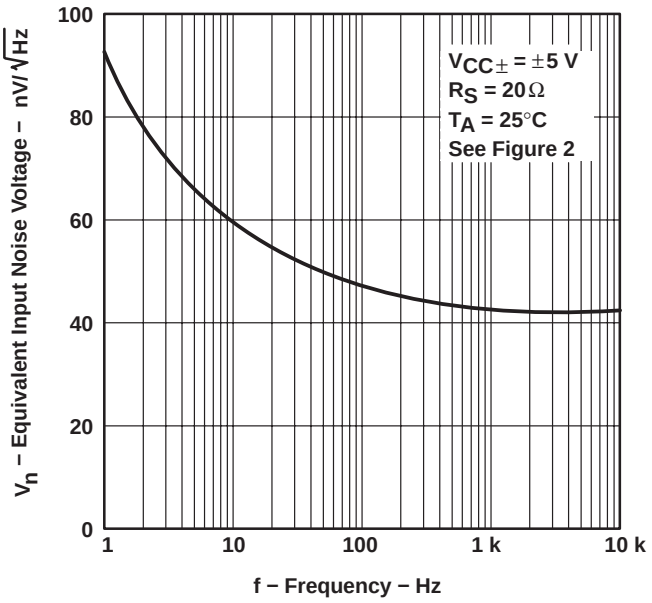


Figure 36

TOTAL HARMONIC DISTORTION vs FREQUENCY

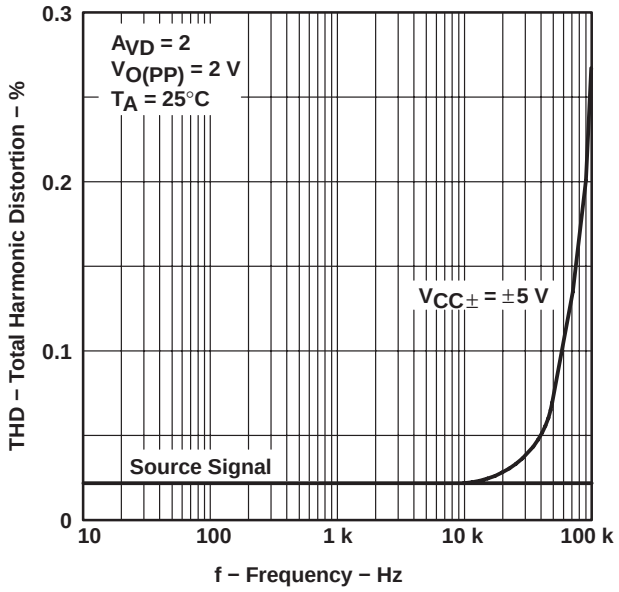


Figure 37

TOTAL HARMONIC DISTORATION vs FREQUENCY

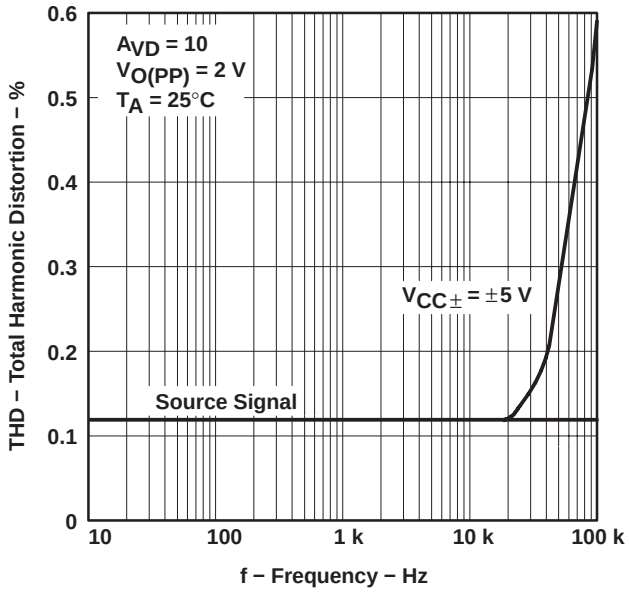


Figure 38

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

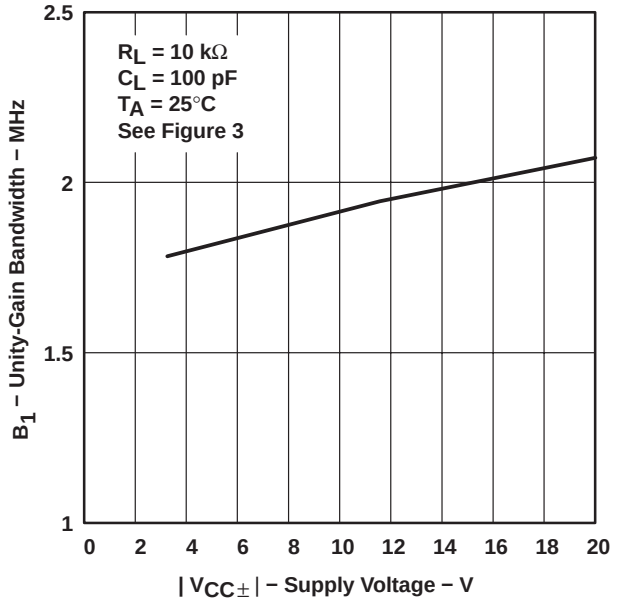


Figure 39

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

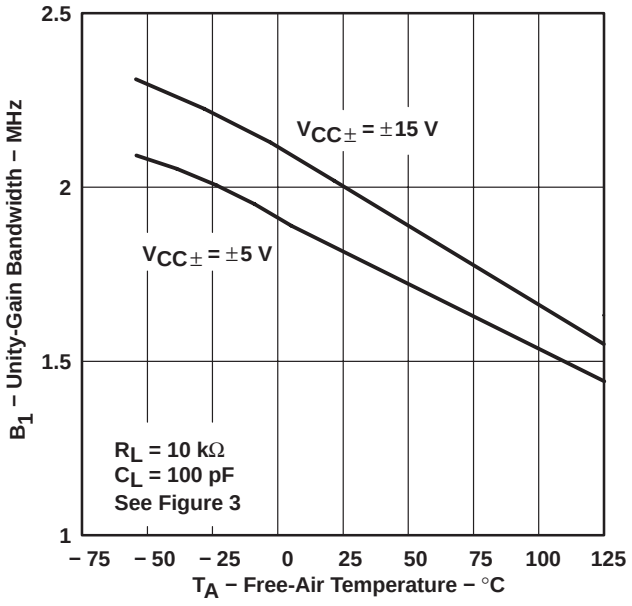


Figure 40

PHASE MARGIN vs SUPPLY VOLTAGE

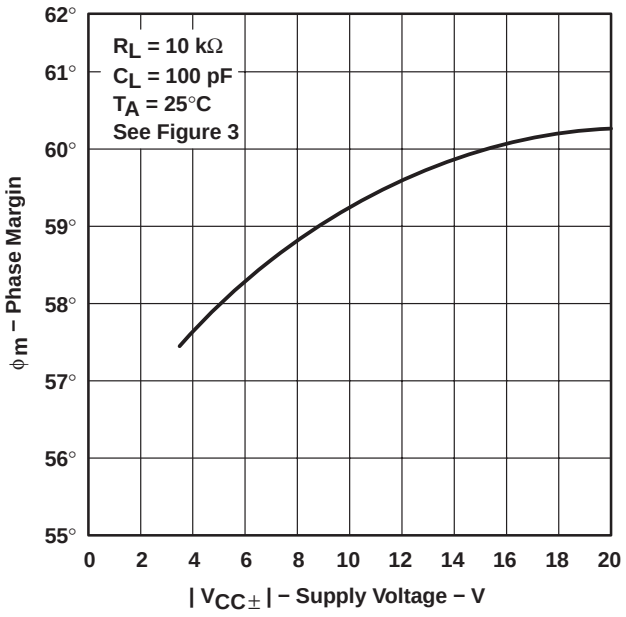


Figure 41

PHASE MARGIN vs LOAD CAPACITANCE

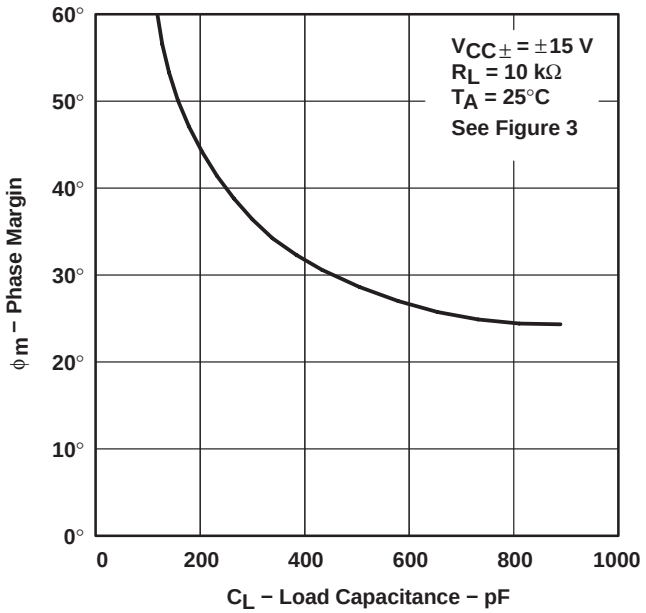


Figure 42

PHASE MARGIN vs FREE-AIR TEMPERATURE

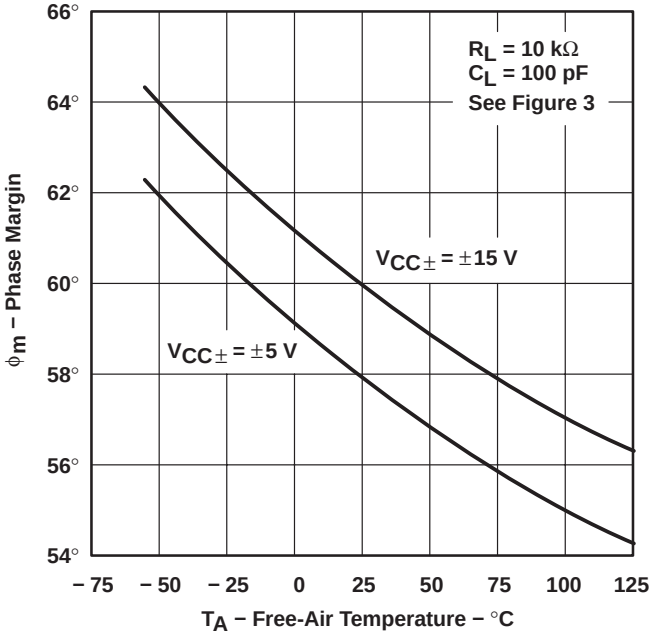


Figure 43

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

input characteristics

The TLE206x, TLE206xA, and TLE206xB are specified with a minimum and a maximum input voltage that if exceeded at either input could cause the device to malfunction. Because of the extremely high input impedance and resulting low bias current requirements, the TLE206x, TLE206xA, and TLE206xB are well suited for low-level signal processing. However, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 44). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

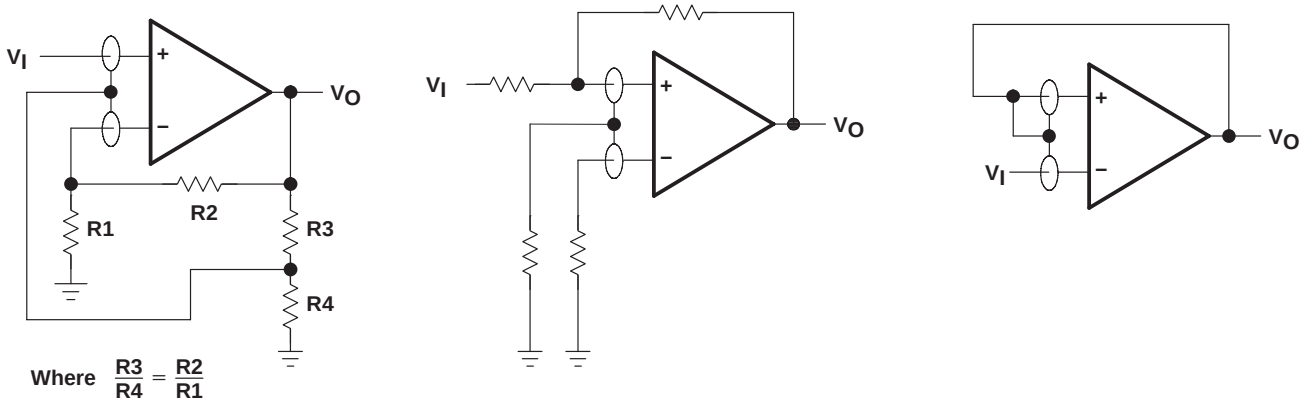


Figure 44. Use of Guard Rings

TLE2061 input offset voltage nulling

The TLE2061 series offers external null pins that can be used to further reduce the input offset voltage. The circuit of Figure 45 can be connected as shown if the feature is desired. When external nulling is not needed, the null pins may be left unconnected.

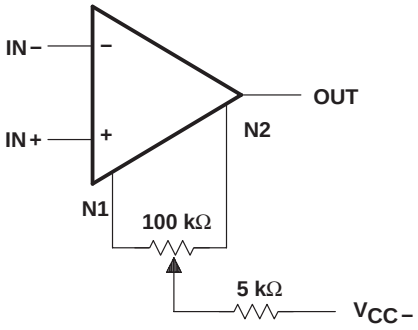


Figure 45. Input Offset Voltage Nulling

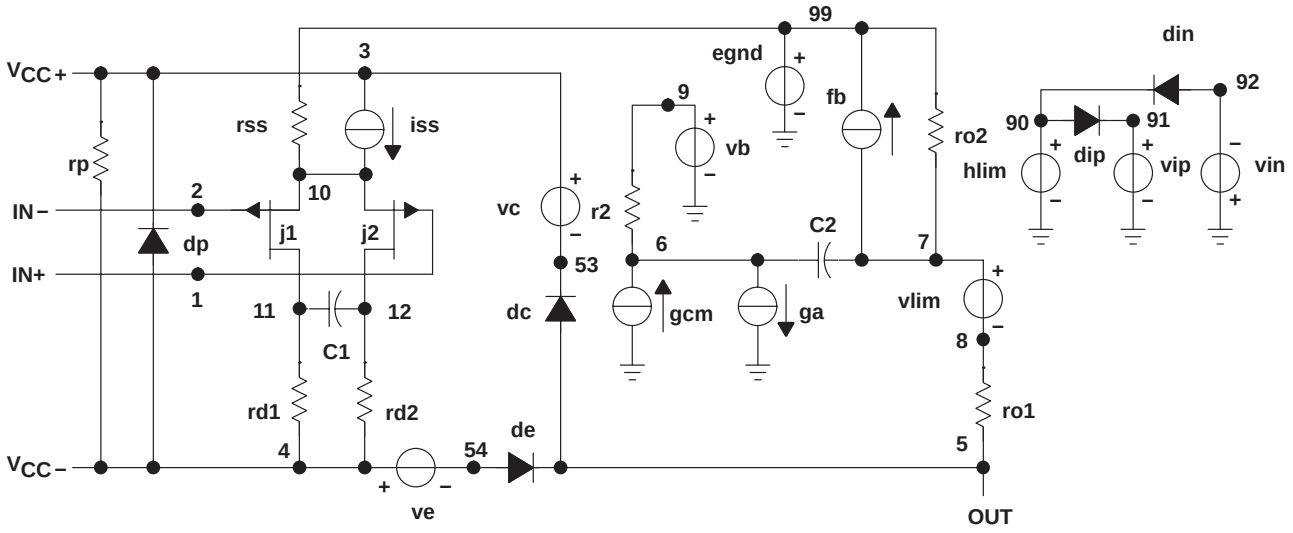
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and the subcircuit in Figure 46 were generated using the TLE206x typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases).

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "*Macromodeling of Integrated Circuit Operational Amplifiers*", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.subckt TLE2062 1 2 3 4 5
  c1   11  12 1.457E-12
  c2    6   7 15.00E-12
  dc    5  53 dx
  de   54   5 dx
  dlp  90  91 dx
  dln  92  90 dx
  dp    4   3 dx
  egnd 99   0 poly (2) (3,0) (4,0) 0 .5 .5
  fb    7  99 poly (5) vb vc ve vlp
+  vln 0 4.357E6 -4E6 4E6 4E6 -4E6
  ga    6   0 11 12 188.5E-6
  gcm   0   6 10 99 3.352E-9
  iss   3  10 dc 51.00E-6
  hlim 90   0 vlim 1k
  j1   11   2 10 jx
  j2   12   1 10 jx
  r2    6   9 100.0E3
  rd1   4  11 5.305E3
  rd2   4  12 5.305E3
  r01   8   5 280
  r02   7  99 280
  rp    3   4 113.2E3
  rss  10  99 3.922E6
  vb    9   0 dc 0
  vc    3  53 dc 2
  ve   54   4 dc 2
  vlim  7   8 dc 0
  vlp  91   0 dc 50
  vln   0  92 dc 50
.model dx  D(Is=800.0E-18)
.model jx  PJF(Is=2.000E-12 Beta = 423E-6
+ Vto = -1)
.ends
```

Figure 46. Boyle Macromodel and Subcircuit

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9080701M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9080701M2A TLE2061MFKB	Samples
5962-9080701MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9080701MPA TLE2061M	Samples
5962-9080702Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9080702Q2A TLE2061 AMFKB	Samples
5962-9080702QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9080702QPA TLE2061AM	Samples
5962-9080703QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9080703QPA TLE2061BM	Samples
5962-9080801MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9080801MPA TLE2062M	Samples
5962-9080803QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9080803QPA TLE2062BM	Samples
5962-9080901M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9080901M2A TLE2064 MFKB	Samples
5962-9080901MCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9080901MCA TLE2064MJB	Samples
5962-9080902M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9080902M2A TLE2064A MFKB	Samples
5962-9080902MDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9080902MDA TLE2064AMWB	Samples
5962-9080903Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9080903Q2A TLE2064 BMFKB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9080903QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9080903QC A TLE2064BMJB	Samples
TLE2061ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2061AC	Samples
TLE2061ACP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2061AC	Samples
TLE2061ACPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2061AC	Samples
TLE2061AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2061AI	Samples
TLE2061AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLE2061AI	Samples
TLE2061AIPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLE2061AI	Samples
TLE2061AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9080702Q2A TLE2061 AMFKB	Samples
TLE2061AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9080702QPA TLE2061AM	Samples
TLE2061BMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9080703QPA TLE2061BM	Samples
TLE2061CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2061C	Samples
TLE2061CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2061C	Samples
TLE2061CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2061C	Samples
TLE2061CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2061CP	Samples
TLE2061ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2061I	Samples
TLE2061IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2061I	Samples
TLE2061IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2061I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2061IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLE2061IP	Samples
TLE2061MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2061M	Samples
TLE2061MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2061M	Samples
TLE2061MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9080701M2A TLE2061MFKB	Samples
TLE2061MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9080701MPA TLE2061M	Samples
TLE2062ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2062AC	Samples
TLE2062ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2062AC	Samples
TLE2062ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2062AC	Samples
TLE2062AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062AI	Samples
TLE2062AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062AI	Samples
TLE2062AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062AI	Samples
TLE2062AMD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2062AM	Samples
TLE2062AMDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2062AM	Samples
TLE2062AMDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2062AM	Samples
TLE2062AMJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLE2062 AMJG	Samples
TLE2062BMJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLE2062 BMJG	Samples
TLE2062BMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9080803QPA TLE2062BM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2062CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2062C	Samples
TLE2062CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2062C	Samples
TLE2062CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2062C	Samples
TLE2062CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2062CP	Samples
TLE2062ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062I	Samples
TLE2062IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062I	Samples
TLE2062IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2062I	Samples
TLE2062IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLE2062IP	Samples
TLE2062IPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLE2062IP	Samples
TLE2062MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2062M	Samples
TLE2062MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2062M	Samples
TLE2062MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLE2062MJG	Samples
TLE2062MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9080801MPA TLE2062M	Samples
TLE2064ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2064AC	Samples
TLE2064ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2064AC	Samples
TLE2064ACN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2064ACN	Samples
TLE2064ACNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2064ACN	Samples
TLE2064AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2064AI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2064AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2064AI	Samples
TLE2064AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2064AI	Samples
TLE2064AMD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2064AM	Samples
TLE2064AMDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2064AM	Samples
TLE2064AMDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2064AM	Samples
TLE2064AMDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2064AM	Samples
TLE2064AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9080902M2A TLE2064A MFKB	Samples
TLE2064AMJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLE2064AMJ	Samples
TLE2064AMWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9080902MDA TLE2064AMWB	Samples
TLE2064BMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9080903Q2A TLE2064 BMFKB	Samples
TLE2064BMJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLE2064BMJ	Samples
TLE2064BMJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9080903QCA TLE2064BMJB	Samples
TLE2064CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLE2064C	Samples
TLE2064CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLE2064C	Samples
TLE2064CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLE2064C	Samples
TLE2064CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLE2064C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2064CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2064CN	Samples
TLE2064CNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2064CN	Samples
TLE2064ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLE2064I	Samples
TLE2064IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLE2064I	Samples
TLE2064IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLE2064I	Samples
TLE2064IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLE2064IN	Samples
TLE2064INE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLE2064IN	Samples
TLE2064MD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2064M	Samples
TLE2064MDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		T2064M	Samples
TLE2064MDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2064M	Samples
TLE2064MDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		T2064M	Samples
TLE2064MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9080901M2A TLE2064 MFKB	Samples
TLE2064MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLE2064MJ	Samples
TLE2064MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9080901MCA TLE2064MJB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLE2061, TLE2061A, TLE2061AM, TLE2061M, TLE2062, TLE2062A, TLE2062AM, TLE2062M, TLE2064, TLE2064A, TLE2064AM, TLE2064M :

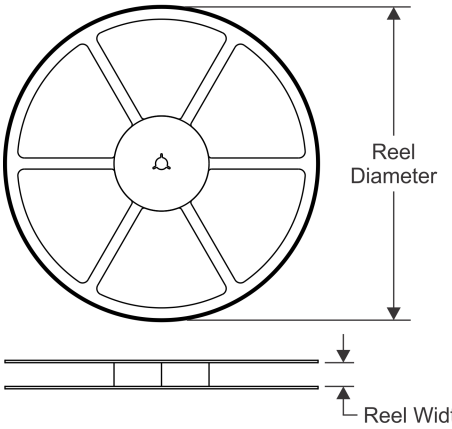
- Catalog: TLE2061A, TLE2061, TLE2062A, TLE2062, TLE2064A, TLE2064
- Military: TLE2061M, TLE2061AM, TLE2062M, TLE2062AM, TLE2064M, TLE2064AM

NOTE: Qualified Version Definitions:

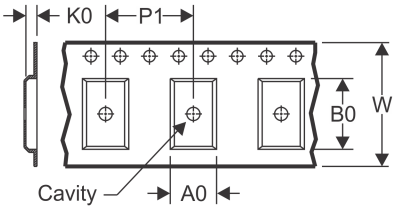
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

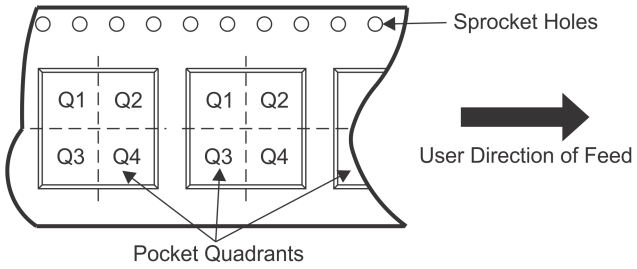


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

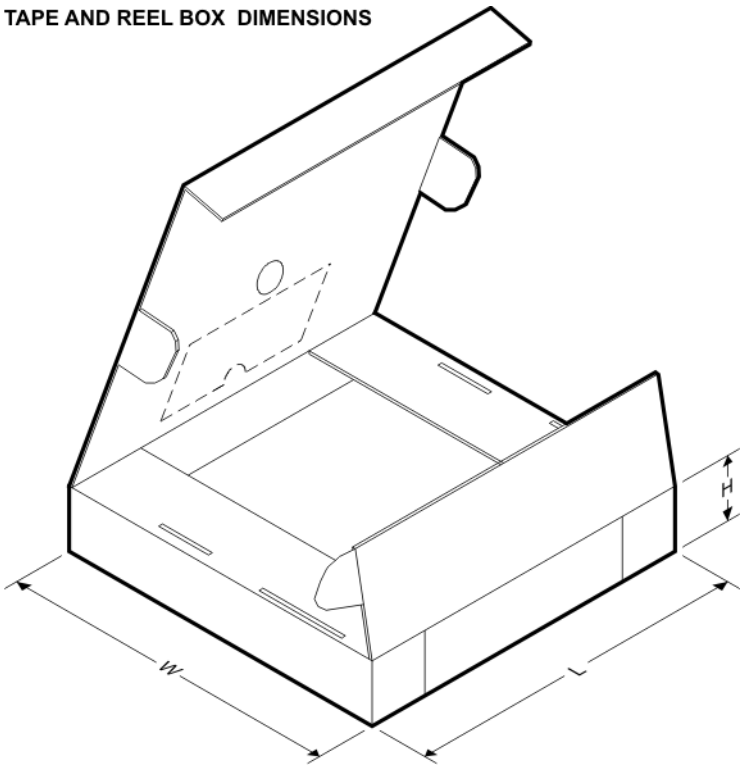
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2061CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2061IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062AMDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2064ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLE2064AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLE2064AMDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLE2064CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLE2064IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLE2064MDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

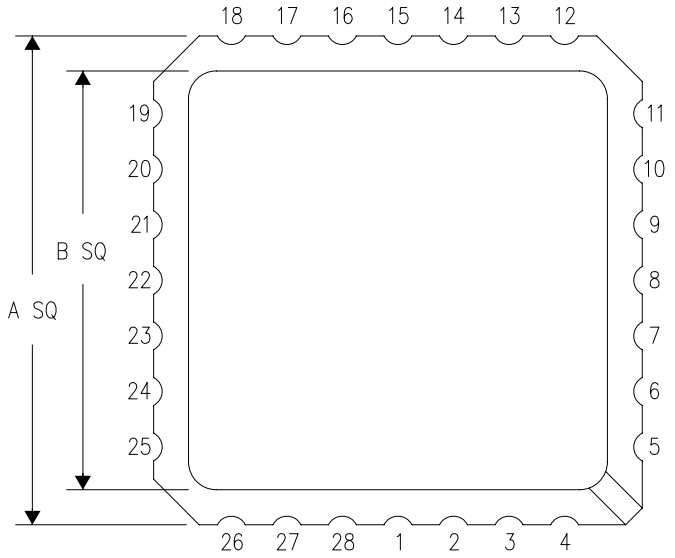


*All dimensions are nominal

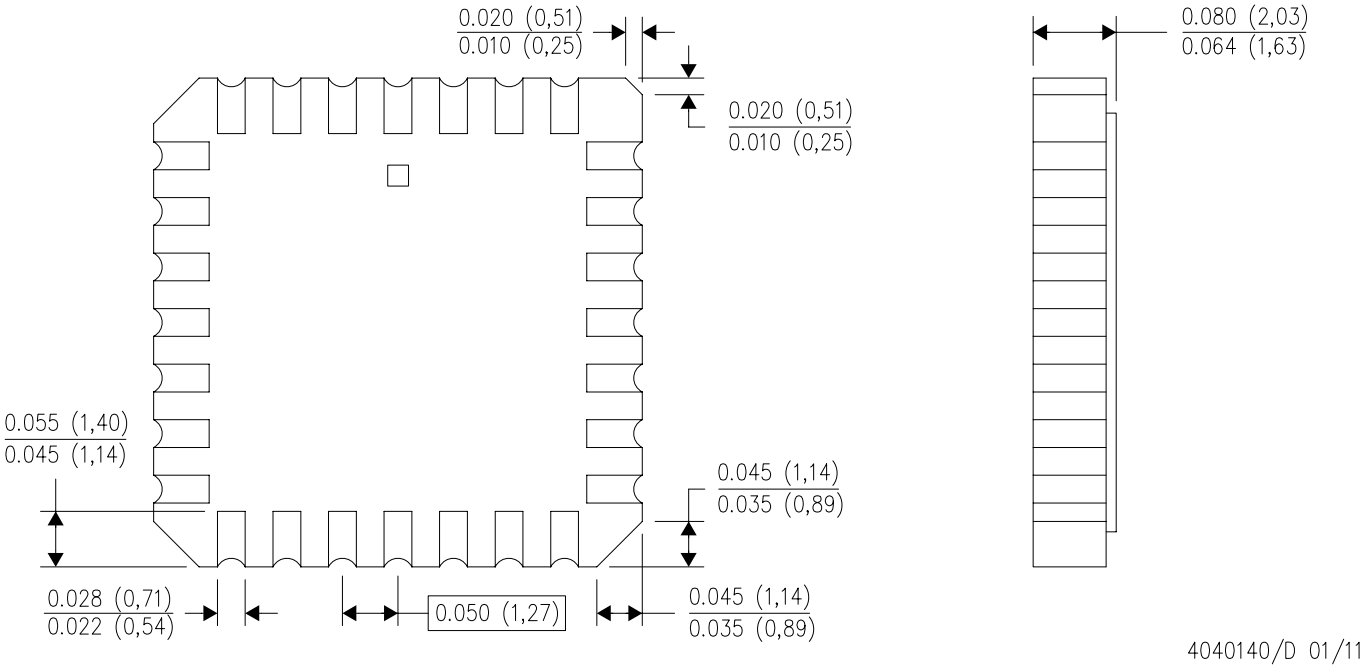
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2061CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2061IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2062ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2062AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2062AMDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2062CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2062IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2064ACDR	SOIC	D	14	2500	350.0	350.0	43.0
TLE2064AIDR	SOIC	D	14	2500	350.0	350.0	43.0
TLE2064AMDR	SOIC	D	14	2500	350.0	350.0	43.0
TLE2064CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLE2064IDR	SOIC	D	14	2500	350.0	350.0	43.0
TLE2064MDR	SOIC	D	14	2500	350.0	350.0	43.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



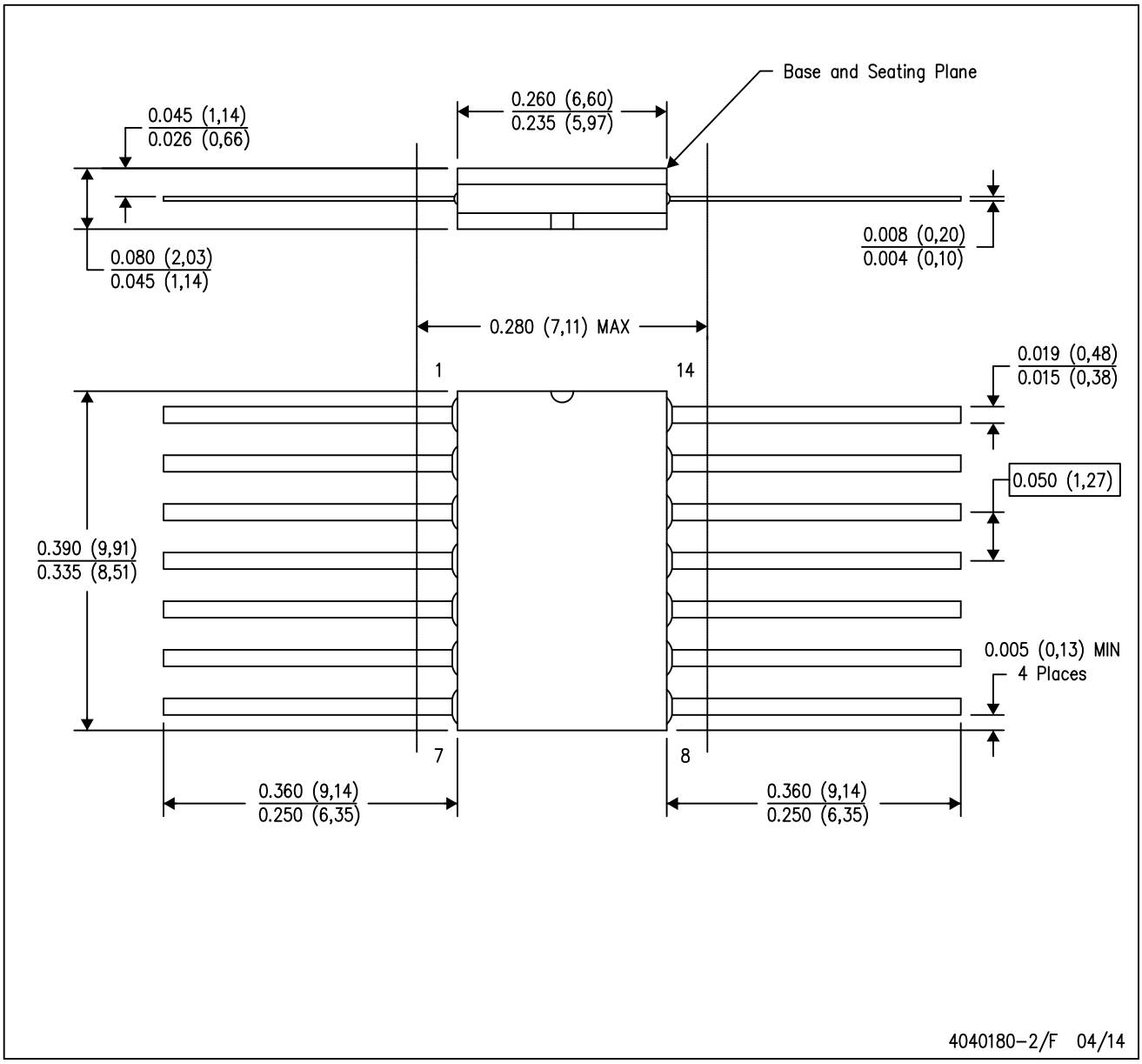
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

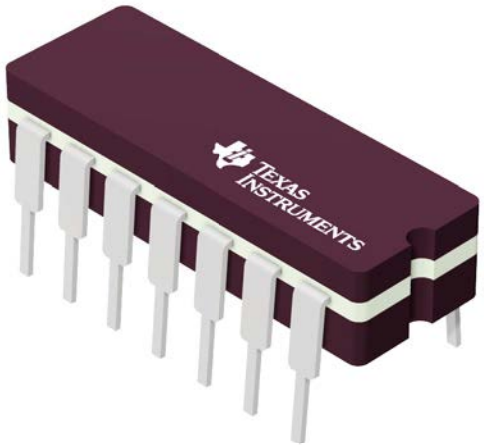


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

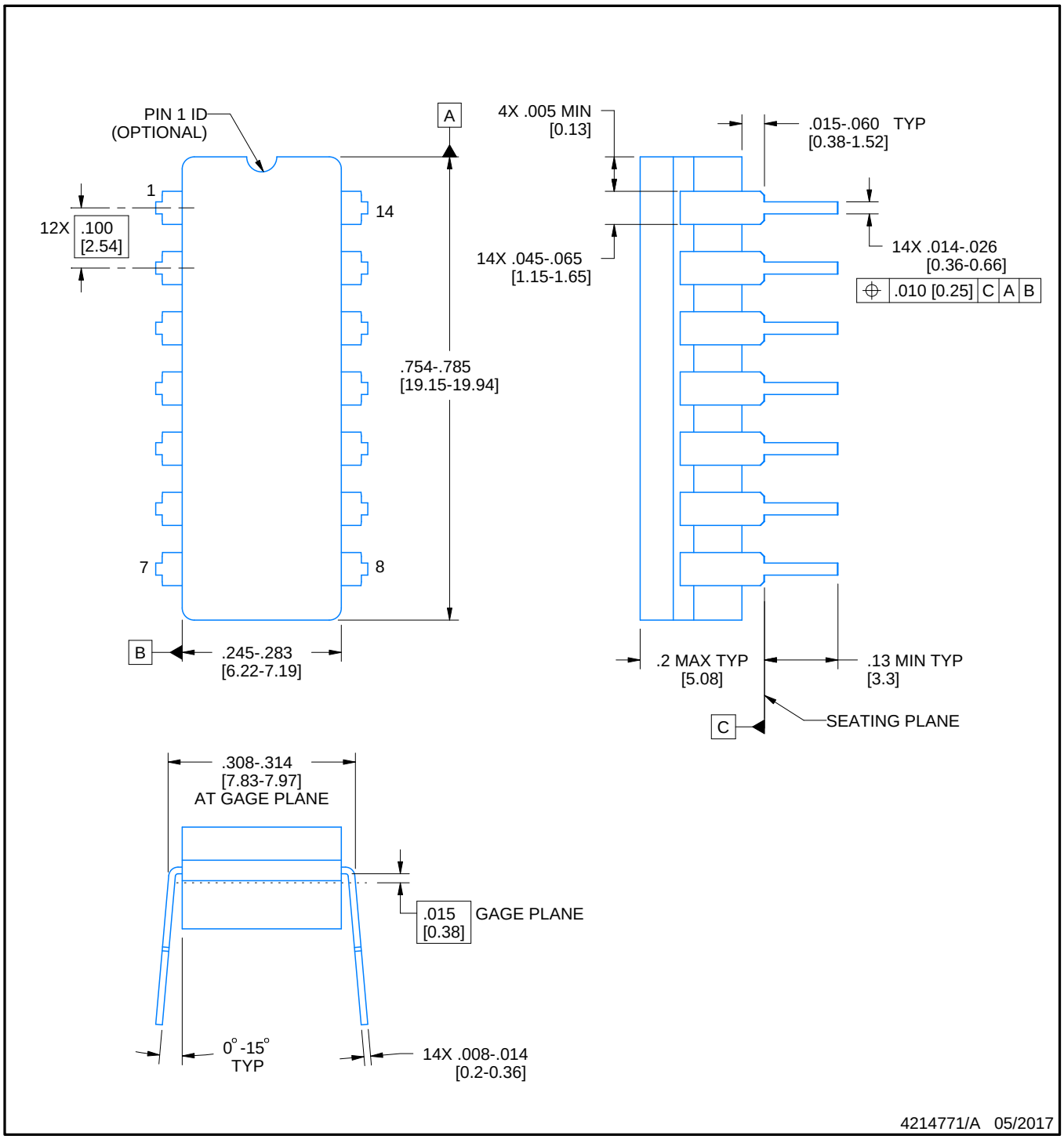
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

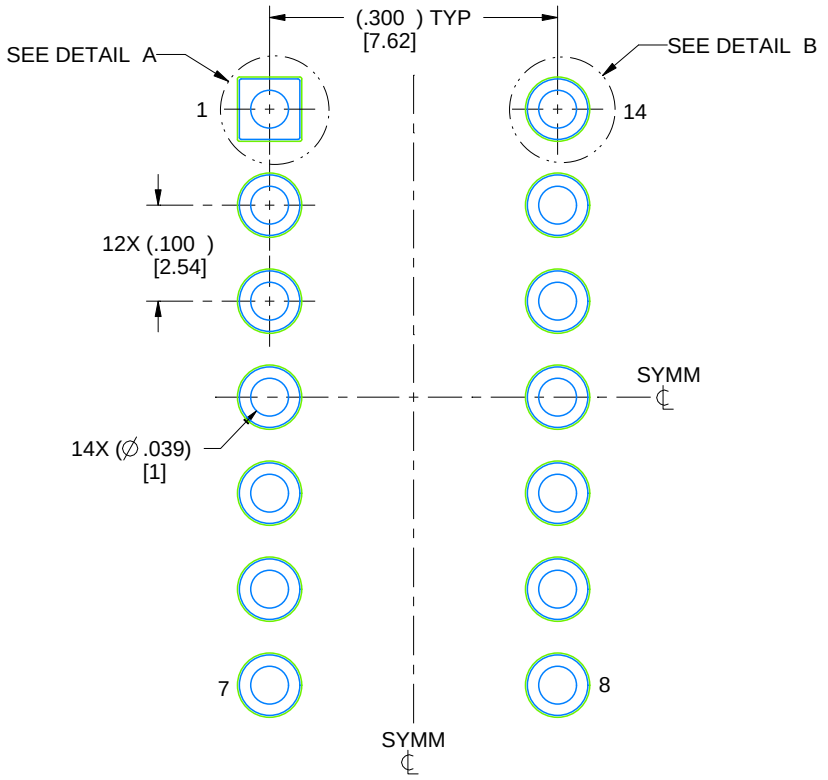
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

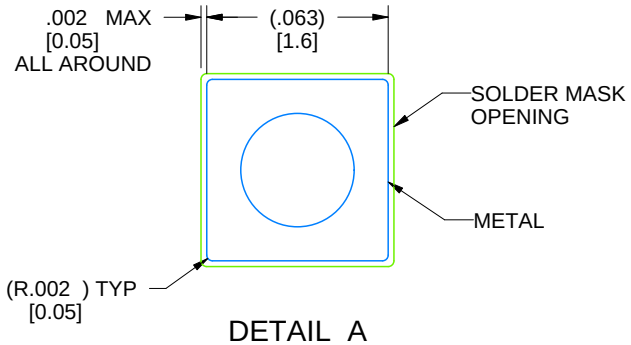
J0014A

CDIP - 5.08 mm max height

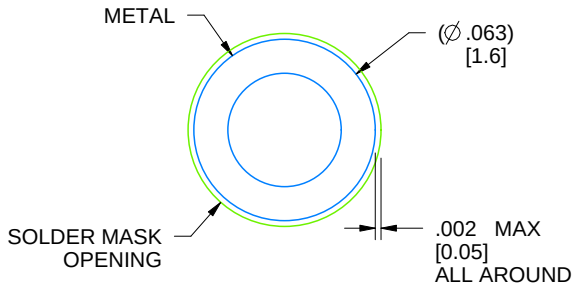
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



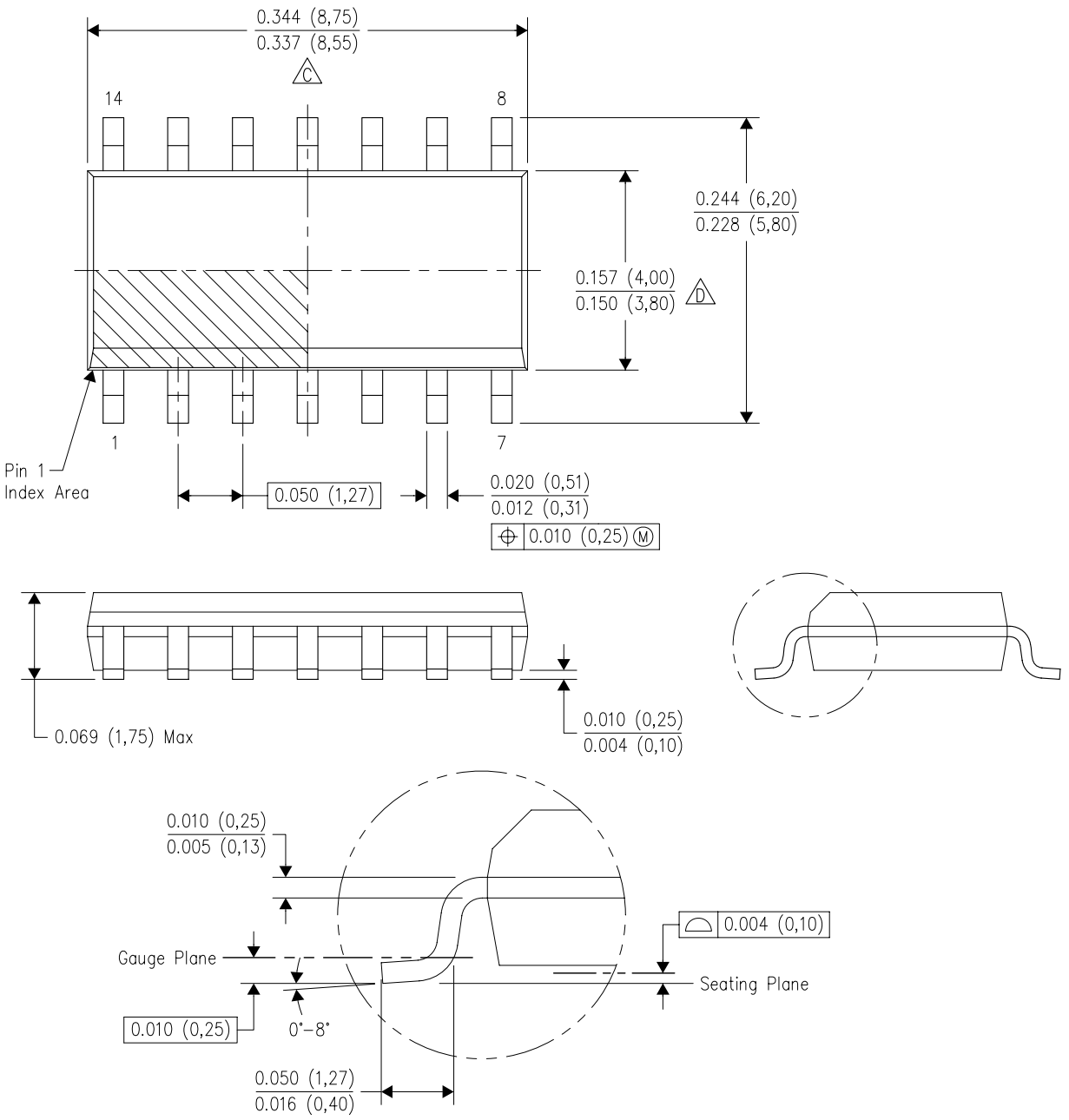
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

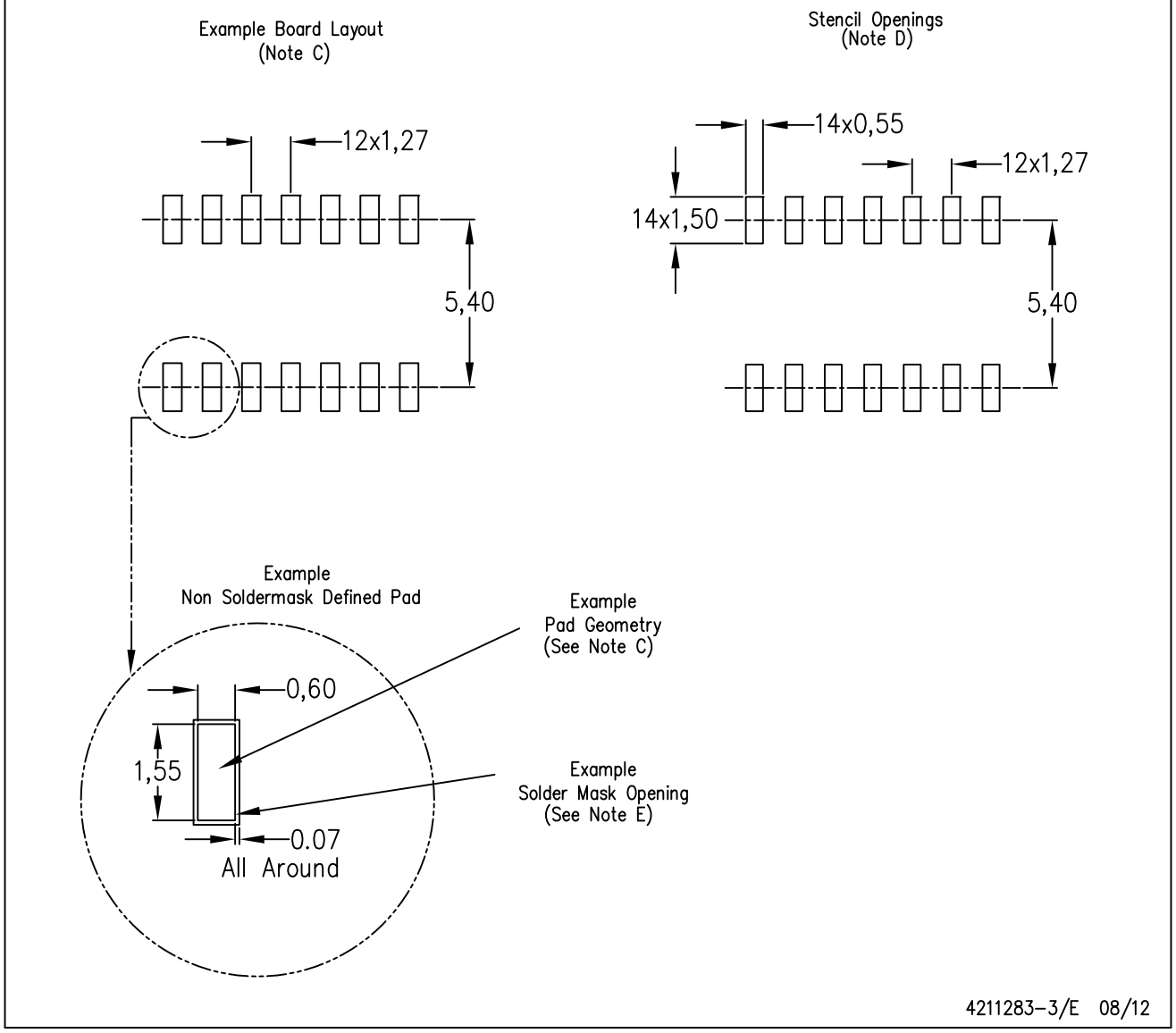
4214771/A 05/2017

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

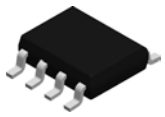


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

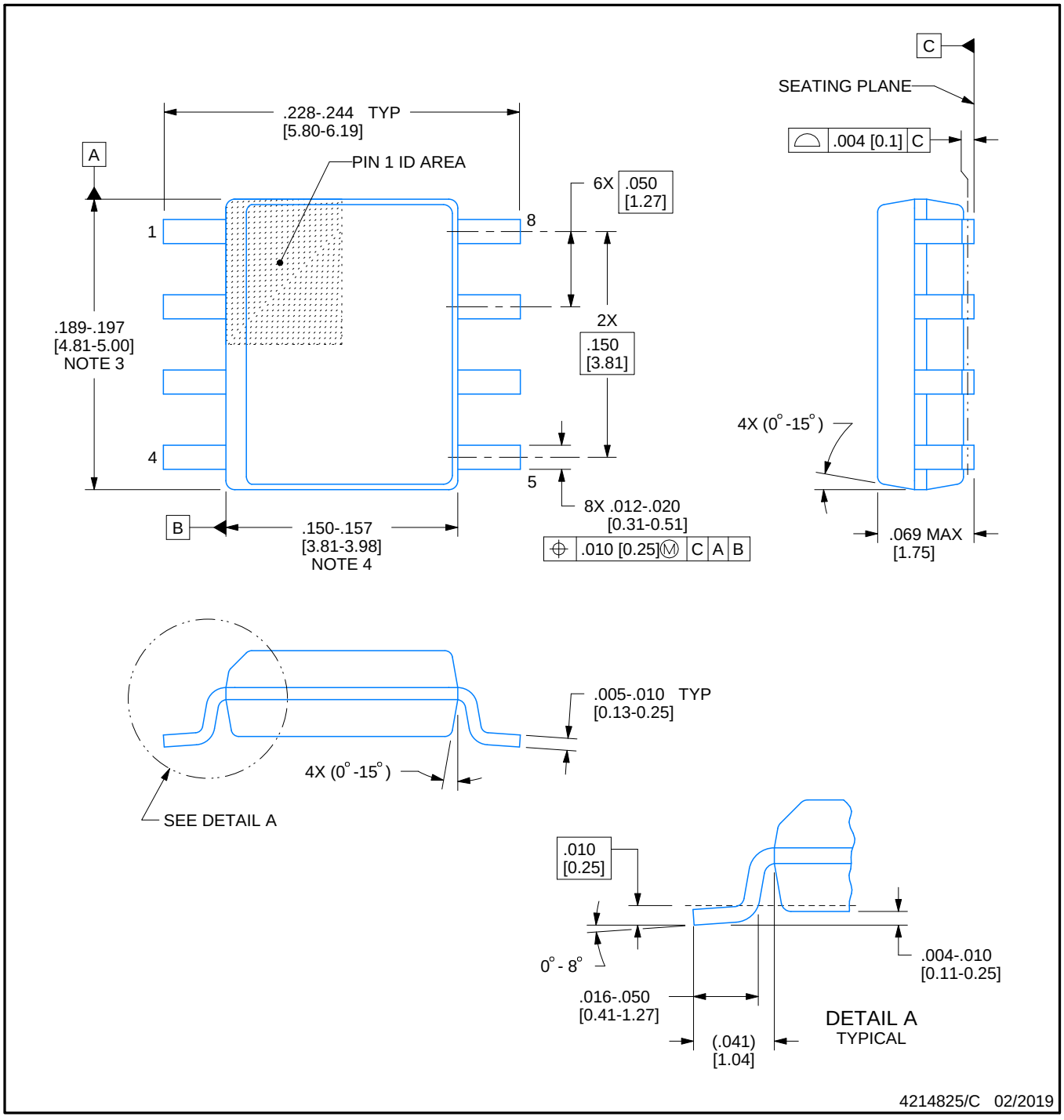


PACKAGE OUTLINE

D0008A

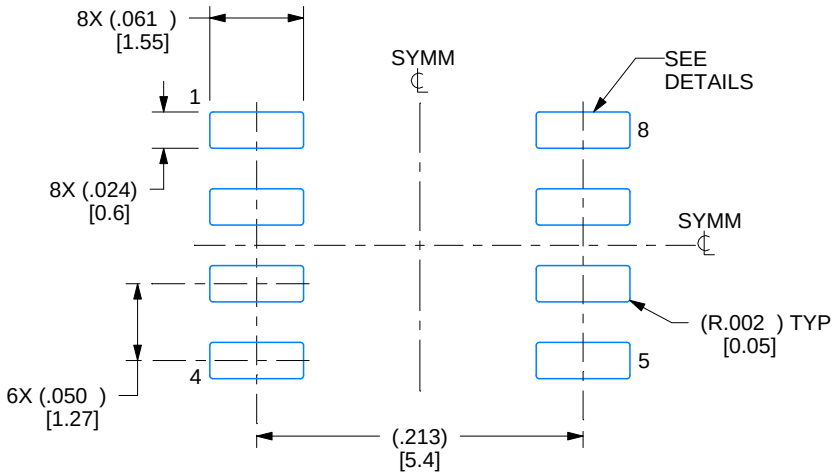
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

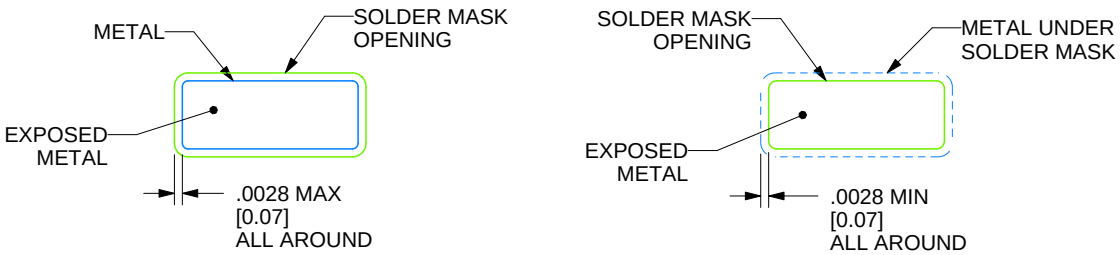


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

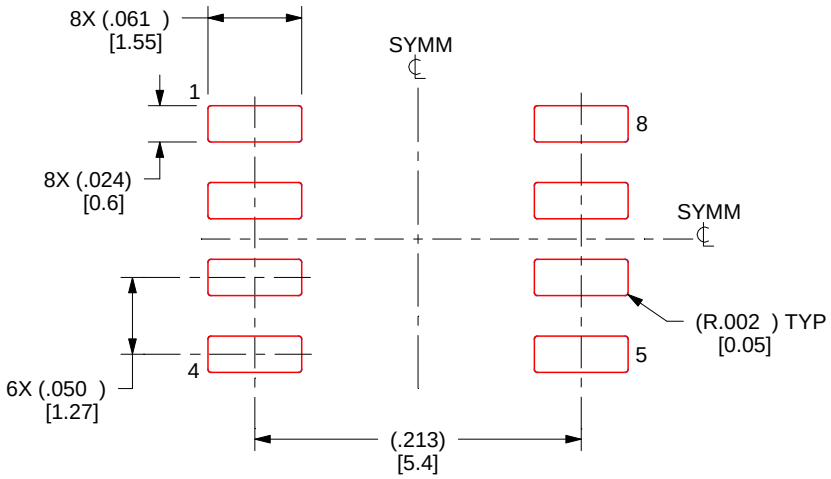
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

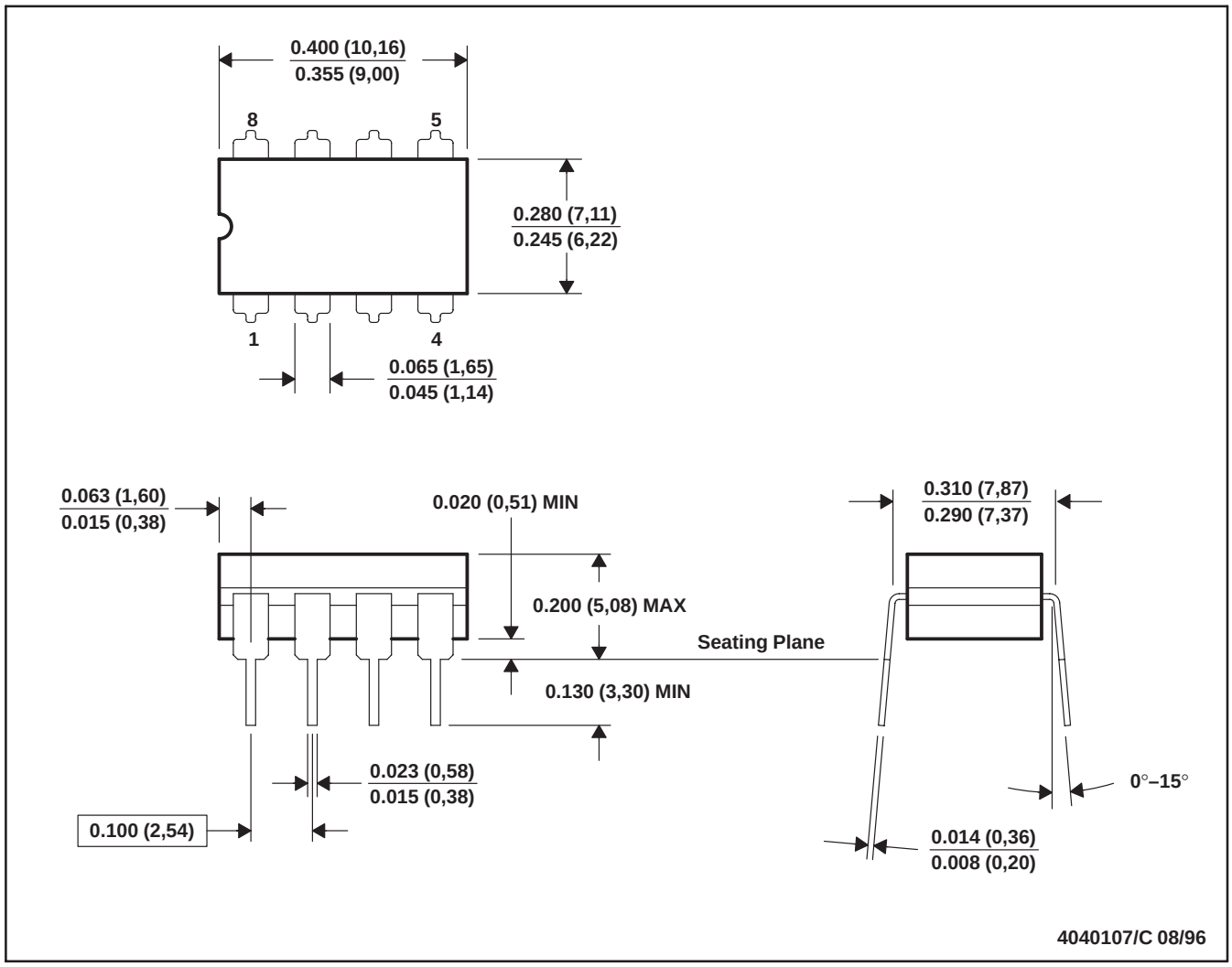
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

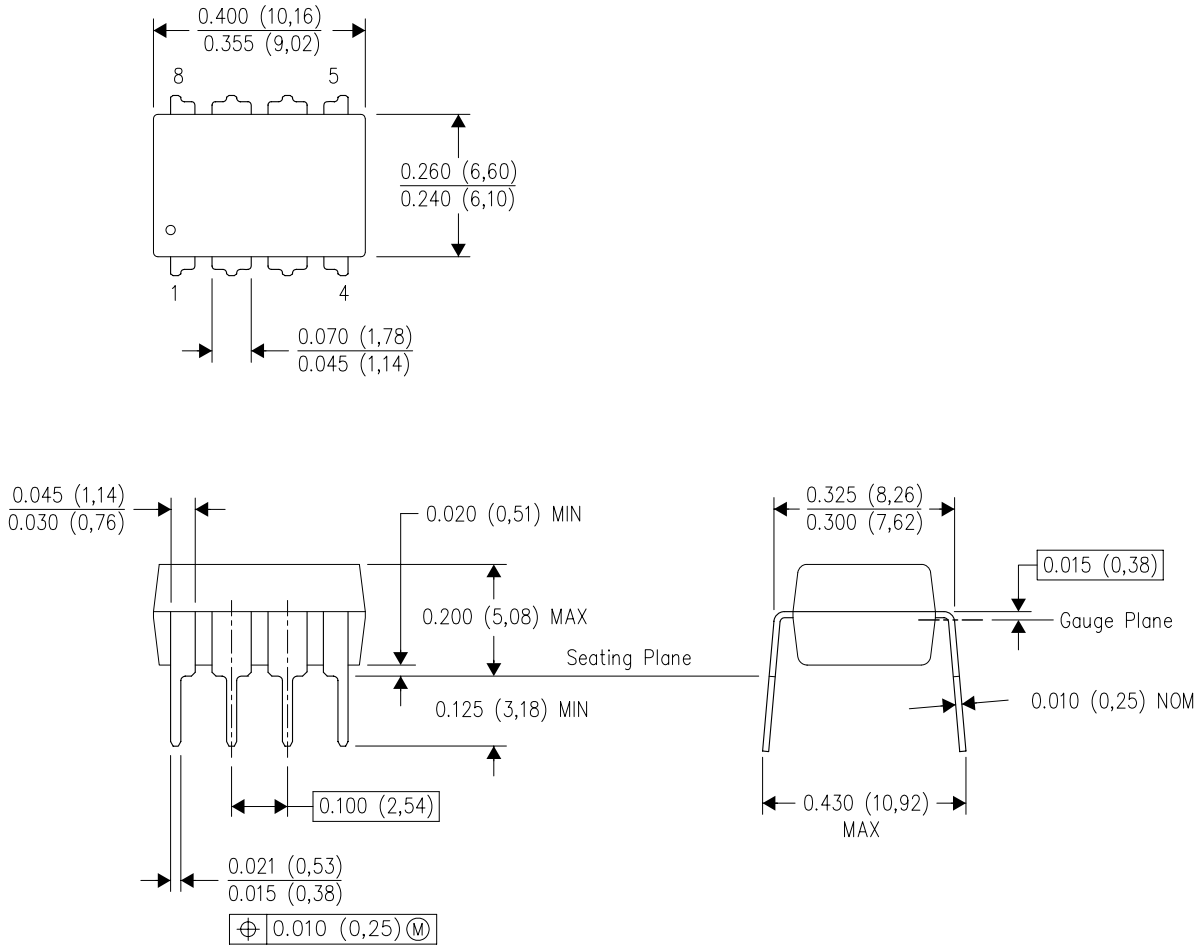
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

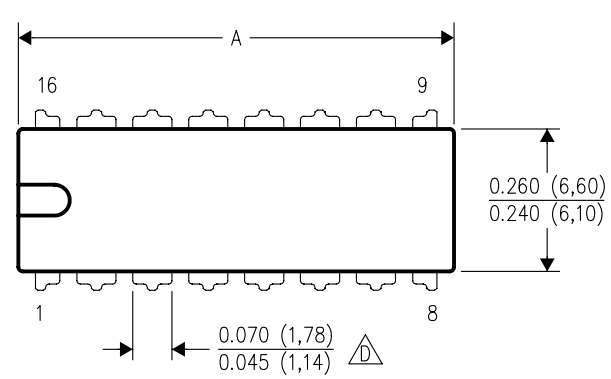


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

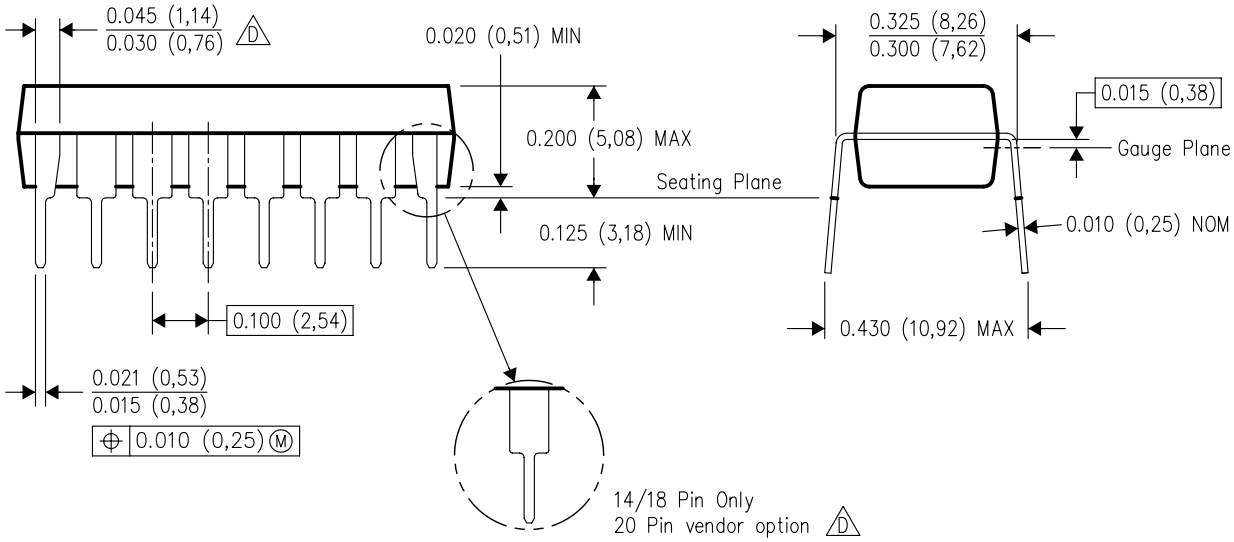
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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