WINSOURCE ELECTRONICS

THE DATASHEET OF

TLE2142MDRG4

- **Low Noise**
  10 Hz . . . 15 nV/√Hz
  1 kHz . . . 10.5 nV/√Hz
- **10000-pF Load Capability**
- **20-mA Min Short-Circuit Output Current**
- **27-V/μs Min Slew Rate**
- **High Gain-Bandwidth Product . . . 5.9 MHz**
- **Low V_{IO} . . . 500 μV Max at 25°C**
- **Single or Split Supply . . . 4 V to 44 V**
- **Fast Settling Time**
  340 ns to 0.1%
  400 ns to 0.01%
- **Saturation Recovery . . . 150 ns**
- **Large Output Swing**
  V_{CC-} +0.1 V to V_{CC+} – 1 V

description

The TLE214x and TLE214xA devices are high-performance, internally compensated operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE214xA is a tighter offset voltage grade of the TLE214x. Both are pin-compatible upgrades to standard industry products.

The design incorporates an input stage that simultaneously achieves low audio-band noise of 10.5 nV/√Hz with a 10-Hz 1/f corner and symmetrical 40-V/μs slew rate typically with loads up to 800 pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.

The devices are stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE214x and TLE214xA are useful for low-droop sample-and-holds and direct buffering of long cables, including 4-mA to 20-mA current loops.

The special design also exhibits an improved insensitivity to inherent integrated circuit component mismatches as is evidenced by a 500-μV maximum offset voltage and 1.7-μV/°C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between V_{CC-} – 0.3 to V_{CC+} – 1.8 V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all-npn output stage provides a nearly rail-to-rail output swing of V_{CC-} – 0.1 to V_{CC+} – 1 V under light current-loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

Both versions can also be used as comparators. Differential inputs of $V_{CC±}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is driven beyond the limits of recommended output swing.

Both the TLE214x and TLE214xA are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The C-suffix devices are characterized for operation from 0°C to 70°C, I-suffix devices from –40°C to 105°C, and M-suffix devices over the full military temperature range of –55°C to 125°C.

TLE2141 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE† (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV	TLE2141ACD	—	TLE2141ACP
	900 μV	TLE2141CD		TLE2141CP
–40°C to 105°C	500 μV	TLE2141AID	—	TLE2141AIP
	900 μV	TLE2141ID		TLE2141IP
–55°C to 125°C	500 μV	—	TLE2141AMJG	—
	900 μV	TLE2141MD	TLE2141MJG	—

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2141ACDR).

TLE2142 AVAILABLE OPTIONS

		PACKAGED DEVICES					
T_A	V_{IO}max AT 25°C	SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP‡ (PW)	CERAMIC FLAT PACK (U)
0°C to 70°C	750 μV	TLE2142ACD	—	—	TLE2142ACP	—	—
	1200 μV	TLE2142CD	—	—	TLE2142CP	TLE2142CPWLE	—
–40°C to 105°C	750 μV	TLE2142AID	—	—	TLC2142AIP	—	—
	1200 μV	TLE2142ID	—	—	TLC2142IP	—	—
–55°C to 125°C	750 μV	TLE2142AMD	TLE2142AMFK	TLE2142AMJG	—	—	TLE2142AMU
	1200 μV	TLE2142MD	TLE2142MFK	TLE2142MJG	—	—	TLE2142MU

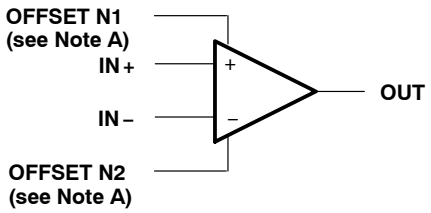
† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2142ACDR).
‡ The PW packages are available left-ended taped and reeled. Add LE the suffix to device type (e.g., TLC2142CPWLE).

TLE2144 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (DW)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	1.5 mV	—	—	—	TLE2144ACN
	2.4 mV	TLE2144CDW	—	—	TLE2144CN
–40°C to 105°C	1.5 mV	—	—	—	TLE2144AIN
	2.4 mV	TLE2144IDW	—	—	TLE2144IN
–55°C to 125°C	1.5 mV	—	TLE2144AMFK	TLE2144AMJ	—
	2.5 mV	TLE2144MDW	TLE2144MFK	TLE2144MJ	—

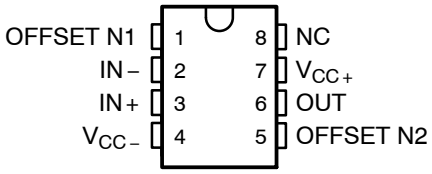
† The DW packages are available taped and reeled. Add R suffix to device type (e.g., TLE2144CDWR).

symbol

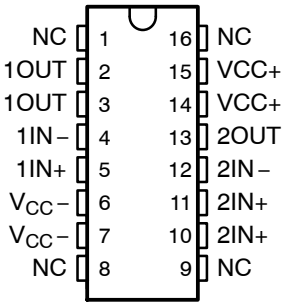


NOTES: A. OFFSET N1 AND OFFSET N2 are only availiable on the TLE2241x devices.

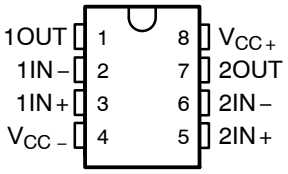
TLE2141
D, JG, OR P PACKAGE
(TOP VIEW)



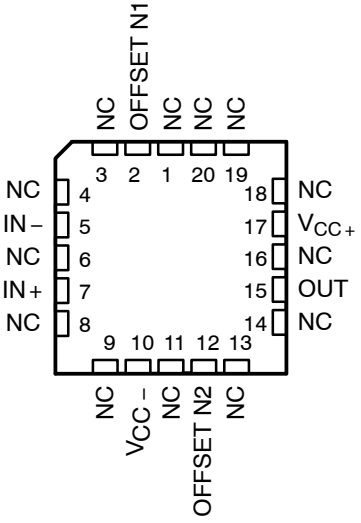
TLE2142
PW PACKAGE
(TOP VIEW)



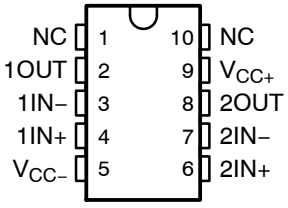
TLE2142
D, JG, OR P PACKAGE
(TOP VIEW)



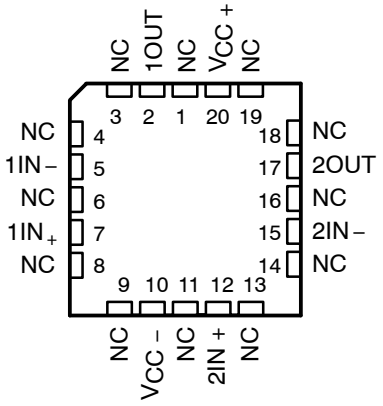
TLE2141
FK PACKAGE
(TOP VIEW)



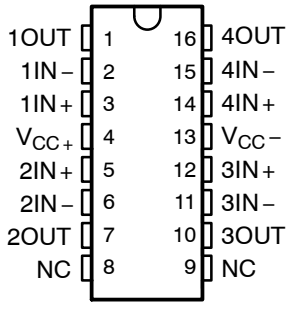
TLE2142
U PACKAGE
(TOP VIEW)



TLE2142
FK PACKAGE
(TOP VIEW)

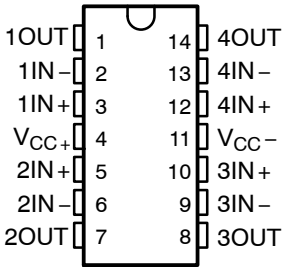


TLE2144
DW PACKAGE
(TOP VIEW)

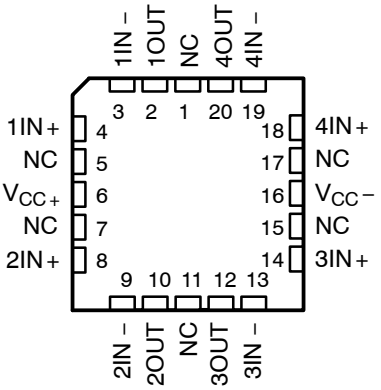


NC – No internal connection

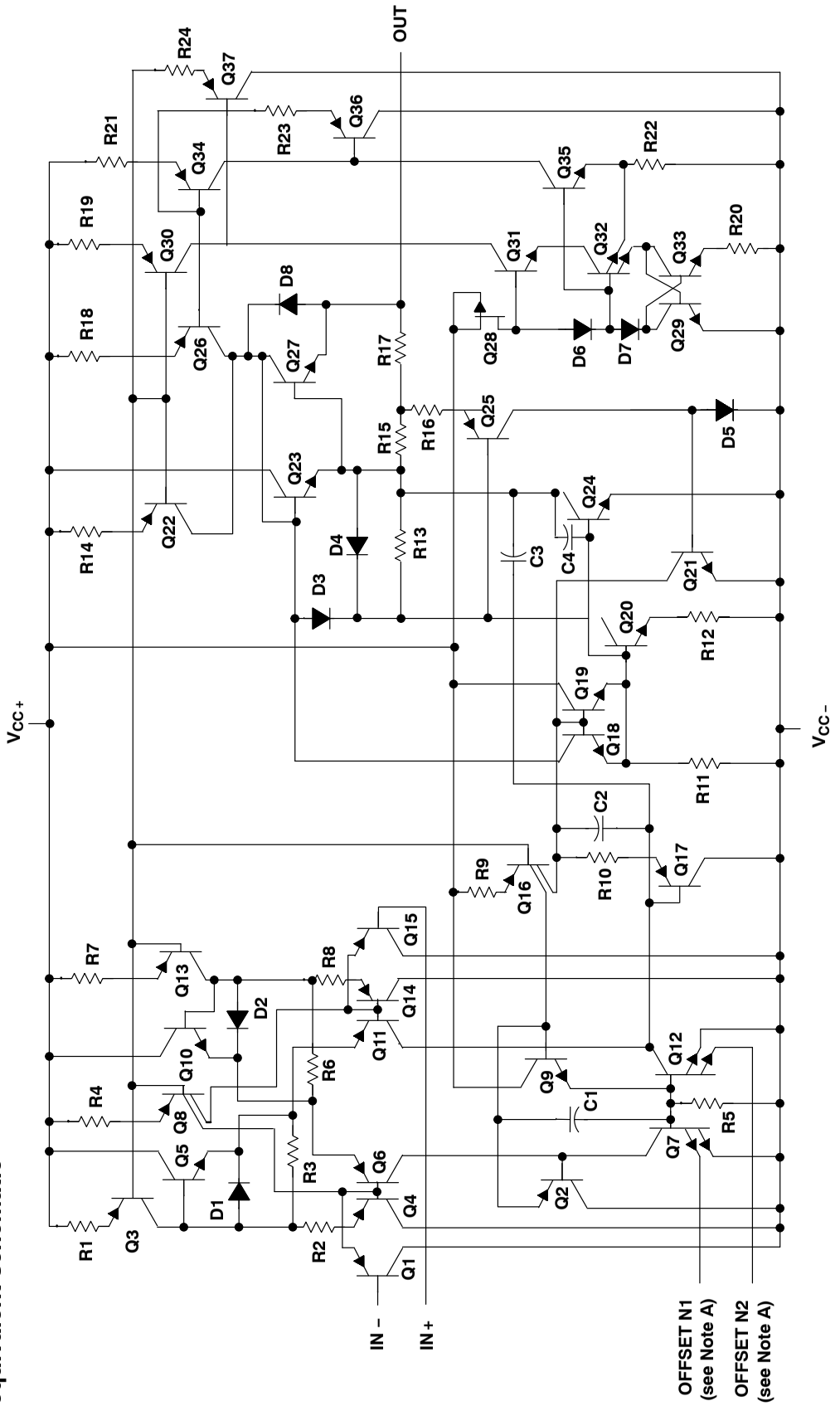
TLE2144
J OR N PACKAGE
(TOP VIEW)



TLE2144
FK PACKAGE
(TOP VIEW)



equivalent schematic



NOTE A: OFFSET N1 AND OFFSET N2 are only availiable on the TLE2141x devices.

ACTUAL DEVICE COMPONENT COUNT			
COMPONENT	TLE2141	TLE2142	TLE2144
Transistors	46	65	130
Resistors	24	43	86
Diodes	8	14	28
Capacitors	4	8	16
Epi-FET	1	1	2

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . . 22 V
Supply voltage, V_{CC-} . . . . . −22 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±44 V
Input voltage range, V_I (any input) . . . . . V_{CC+} to V_{CC-} − 0.3 V
Input current, I_I (each input) . . . . . ±1 mA
Output current, I_O . . . . . ±80 mA
Total current into V_{CC+} . . . . . 80 mA
Total current out of V_{CC-} . . . . . 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package . . . . . 97.1°C/W
DW package . . . . . 57.3°C/W
N package . . . . . 79.7°C/W
P package . . . . . 84.6°C/W
PW package . . . . . 108.4°C/W
Package thermal impedance, θ_{JC} (see Notes 4 and 5): FK package . . . . . 5.6°C/W
J package . . . . . 15.1°C/W
JG package . . . . . 14.5°C/W
U package . . . . . 14.7°C/W
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . −40°C to 105°C
M suffix . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, DW, N, P, or PW package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or JG package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current flows, if input, are brought below V_{CC-} − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7 (plastic) or MIL-STD-883 Method 1012 (ceramic).

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±2	±22	±2	±22	±2	±22	V
Common-mode input voltage, V_{IC}	V_{CC} = 5 V	0	2.9	0	2.7	0	2.7	V
	$V_{CC\pm}$ = ±15 V	−15	12.9	−15	12.7	−15	12.7	
Operating free-air temperature, T_A		0	70	−40	105	−55	125	°C

TLE2141C electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2141C			TLE2141AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, V_{IC} = 2.5 V, R_S = 50 Ω	25°C		225	1400		200	1000	μV
			Full range			1700			1300	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.1			−2.1	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.9			0 to 2.9			
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
			Full range	3.8			3.8			
		I_{OH} = −1.5 mA	25°C	3.8	4		3.8	4		
			Full range	3.7			3.7			
		I_{OH} = −15 mA	25°C	3.2	3.7		3.2	3.7		
			Full range	3.2			3.2			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
			Full range			150			150	
		I_{OL} = 1.5 mA	25°C		150	225		150	225	
			Full range			250			250	
		I_{OL} = 15 mA	25°C		1.2	1.6		1.2	1.6	V
			Full range			1.7			1.7	
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	25			25			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		3.4	4.4		3.4	4.4	mA
			Full range			4.6			4.6	

† Full range is 0°C to 70°C.

TLE2141C operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2141C			TLE2141AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF†,	R_L = 2 kΩ,†		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF†		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF†,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF†		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†,	C_L = 100 pF†		57°			57°		

† R_L and C_L terminated to 2.5 V.

TLE2141C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2141C			TLE2141AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,	25°C		200	900		175	500	μV
				Full range			1300			800	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			150			150	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.6			−1.6	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.9	−15.3 to 13.1		−15 to 12.9	−15.3 to 13.1		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −1.5 mA		25°C	13.7	14		13.7	14		
				Full range	13.6			13.6			
		I_O = −15 mA		25°C	13.1	13.7		13.1	13.7		
				Full range	13			13			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
				Full range	−14.6			−14.6			
		I_O = 1.5 mA		25°C	−14.5	−14.8		−14.5	−14.8		
				Full range	−14.4			−14.4			
		I_O = 15 mA		25°C	−13.4	−13.8		−13.4	−13.8		
				Full range	−13.3			−13.3			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V		25°C	100	450		100	450		V/mV
				Full range	75			75			
r_i	Input resistance	R_L = 2 kΩ		25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0,	No load	25°C		3.5	4.5		3.5	4.5	mA
				Full range			4.7			4.7	

† Full range is 0°C to 70°C.

TLE2141C operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2141C			TLE2141AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR–	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

TLE2142C electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2142C			TLE2142AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		220	1900		200	1500	μV
			Full range			2200			1800	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.1			−2.1	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.9			0 to 2.9			
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
			Full range	3.8			3.8			
		I_{OH} = −1.5 mA	25°C	3.8	4		3.8	4		
			Full range	3.7			3.7			
		I_{OH} = −15 mA	25°C	3.4	3.7		3.4	3.7		
			Full range	3.4			3.4			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
			Full range			150			150	
		I_{OL} = 1.5 mA	25°C		150	225		150	225	
			Full range			250			250	
		I_{OL} = 15 mA	25°C		1.2	1.4		1.2	1.4	V
			Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	25			25			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		6.6	8.8		6.6	8.8	mA
			Full range			9.2			9.2	

† Full range is 0°C to 70°C.

TLE2142C operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142C			TLE2142AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V.

TLE2142C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2142C			TLE2142AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,	25°C		290	1200		275	750	μV
				Full range			1600			1200	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			150			150	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.6			−1.6	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.9	−15.3 to 13.1		−15 to 12.9	−15.3 to 13.1		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −1.5 mA		25°C	13.7	14		13.7	14		
				Full range	13.6			13.6			
		I_O = −15 mA		25°C	13.3	13.7		13.3	13.7		
				Full range	13.2			13.2			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
				Full range	−14.6			−14.6			
		I_O = 1.5 mA		25°C	−14.5	−14.8		−14.5	−14.8		
				Full range	−14.4			−14.4			
		I_O = 15 mA		25°C	−13.4	−13.8		−13.4	−13.8		
				Full range	−13.3			−13.3			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V		25°C	100	450		100	450		V/mV
				Full range	75			75			
r_i	Input resistance	R_L = 2 kΩ		25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω		25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ± 2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0,	No load	25°C		6.9	9		6.9	9	mA
				Full range			9.4			9.4	

† Full range is 0°C to 70°C.

TLE2142C operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142C			TLE2142AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR–	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ,, f =100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

TLE2144C electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2144C			TLE2144AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, V_{IC} = 2.5 V, R_S = 50 Ω	25°C		0.5	3.8		0.5	3	mV
			Full range			4.4			3.6	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			150			150	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.1			−2.1	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.9			0 to 2.9			
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
			Full range	3.8			3.8			
		I_{OH} = −1.5 mA	25°C	3.8	4		3.8	4		
			Full range	3.7			3.7			
		I_{OH} = −15 mA	25°C	3.4	3.7		3.4	3.7		
			Full range	3.4			3.4			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
			Full range			150			150	
		I_{OL} = 1.5 mA	25°C		150	225		150	225	
			Full range			250			250	
		I_{OL} = 15 mA	25°C		1.2	1.6		1.2	1.6	V
			Full range			1.7			1.7	
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ±2.5 V, V_O = 1 V to −1.5 V, R_L = 2 kΩ,	25°C	50	95		50	95		V/mV
			Full range	25			25			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, V_{IC} = 2.5 V, No load,	25°C		13.2	17.6		13.2	17.6	mA
			Full range			18.5			18.5	

† Full range is 0°C to 70°C.

TLE2144C operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144C			TLE2144AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V

TLE2144C electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2144C			TLE2144AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,	25°C		0.6	2.4		0.5	1.5	mV
				Full range			3.2			2.4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			150			150	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	µA
				Full range			−1.6			−1.6	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.9	−15.3 to 13.1		−15 to 12.9	−15 to 13.1		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 µA		25°C	13.8	14.1		13.8	14.1		V
				Full range	13.7			13.7			
		I_O = −1.5 mA		25°C	13.7	14		13.7	14		
				Full range	13.6			13.6			
		I_O = −15 mA		25°C	13.1	13.7		13.1	13.7		
				Full range	13			13			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 µA		25°C	−14.7	−14.9		−14.7	−14.9		V
				Full range	−14.6			−14.6			
		I_O = 1.5 mA		25°C	−14.5	−14.8		−14.5	−14.8		
				Full range	−14.4			−14.4			
		I_O = 15 mA		25°C	−13.4	−13.8		−13.4	−13.8		
				Full range	−13.3			−13.3			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V		25°C	100	170		100	170		V/mV
				Full range	75			75			
r_i	Input resistance	R_L = 2 kΩ		25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0,	No load	25°C		13.8	18		13.8	18	mA
				Full range			18.8			18.8	

† Full range is 0°C to 70°C.

TLE2144C operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144C			TLE2144AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR–	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

TLE2141I electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2141I			TLE2141AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		225	1400		200	1000	μV
			Full range			1900			1500	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.2			−2.2	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.2	3.7		3.2	3.7		
		I_{OH} = −100 μA	Full range	3.8			3.8			
		I_{OH} = −1 mA		3.7			3.7			
		I_{OH} = −10 mA		3.3			3.3			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 μA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.6		1.2	1.6	V
		I_{OL} = 100 μA	Full range			175			175	mV
		I_{OL} = 1 mA				225			225	
		I_{OL} = 10 mA				1.4			1.4	V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	10			10			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		3.4	4.4		3.4	4.4	mA
			Full range			4.6			4.6	

† Full range is −40°C to 105°C.

TLE2141I operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2141I			TLE2141AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF†		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ† f = 100 kHz	C_L = 100 pF†,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF†		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†,	C_L = 100 pF†		57°			57°		

† R_L and C_L terminated to 2.5 V.

TLE2141I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2141I			TLE2141AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,	25°C		200	900		175	500	μV
				Full range			1500			1000	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			200			200	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.7			−1.7	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.1	13.7		13.1	13.7		
		I_O = −100 μA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 μA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	25°C	100	450		100	450		V/mV
				Full range	40			40			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω		25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0,	No load	25°C		3.5	4.5		3.5	4.5	mA
				Full range			4.7			4.7	

† Full range is −40°C to 105°C.

TLE2141I operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2141I			TLE2141AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR–	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

TLE2142I electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2142I			TLE2142AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, V_{IC} = 2.5 V	R_S = 50 Ω,	25°C		220	1900		220	1500	μV
				Full range			2400			2000	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		8	100		8	100	nA
				Full range			200			200	
I_{IB}	Input bias current			25°C		−0.8	−2		−0.8	−2	μA
				Full range			−2.2			−2.2	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
				Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA		25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA			3.8	4		3.8	4		
		I_{OH} = −15 mA			3.4	3.7		3.4	3.7		
		I_{OH} = 100 μA		Full range	3.8			3.8			
		I_{OH} = 1 mA			3.7			3.7			
		I_{OH} = 10 mA			3.5			3.5			
V_{OL}	Low-level output voltage	I_{OI} = 150 μA		25°C		75	125		75	125	mV
		I_{OL} = 1.5 mA				150	225		150	225	
		I_{OL} = 15 mA				1.2	1.4		1.2	1.4	V
		I_{OL} = 100 μA		Full range			175			175	mV
		I_{OL} = 1 mA					225			225	
		I_{OL} = 10 mA					1.2			1.2	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, V_O = 1 V to −1.5 V	R_L = 2 kΩ,	25°C	50	220		50	220		V/mV
				Full range	10			10			
r_i	Input resistance			25°C		70			70		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	118		85	118		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, V_{IC} = 2.5 V	No load,	25°C		6.6	8.8		6.6	8.8	mA
				Full range			9.2			9.2	

† Full range is − 40°C to 105°C.

TLE2142I operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142I			TLE2142AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V.

TLE2142I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2142I			TLE2142I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		290	1200		275	750	μV
				Full range			1800			1400	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			200			200	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.7			−1.7	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.3	13.7		13.3	13.7		
		I_O = −100 μA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.3			13.3			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 μA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		25°C	100	450		100	450		V/mV
				Full range	40			40			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		25°C	85	108		85	108		dB
		R_S = 50 Ω		Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0,	No load	25°C		6.9	9		6.9	9	mA
				Full range			9.4			9.4	

† Full range is −40°C to 105°C.

TLE2142I operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142I			TLE2142AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ,	30	45		30	45		V/μs
SR–	Negative slew rate			30	42		30	42		
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f =100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

TLE2144I electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2144I			TLE2144AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C		0.5	3.8		0.5	3	mV
			Full range			4.8			4	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.2			−2.2	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.4	3.7		3.4	3.7		
		I_{OH} = 100 μA	Full range	3.8			3.8			
		I_{OH} = 1 mA		3.7			3.7			
		I_{OH} = 10 mA		3.5			3.5			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 μA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.6		1.2	1.6	V
		I_{OL} = 100 μA	Full range			175			175	mV
		I_{OL} = 1 mA				225			225	
		I_{OL} = 10 mA				1.4			1.4	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, V_O = 1 V to −1.5 V, R_L = 2 kΩ,	25°C	50	95		50	95		V/mV
			Full range	10			10			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, V_{IC} = 2.5 V, No load,	25°C		13.2	17.6		13.2	17.6	mA
			Full range			18.4			18.4	

† Full range is −40°C to 105°C.

TLE2144I operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144I			TLE2144AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 10 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V

TLE2144I electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2144I			TLE2144AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,	25°C		0.6	2.4		0.5	1.5	mV
				Full range			3.2			2.8	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			200			200	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	µA
				Full range			−1.7			−1.7	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 µA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.1	13.7		13.1	13.7		
		I_O = −100 µA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 µA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 µA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	25°C	100	170		100	170		V/mV
				Full range	40			40			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0,	No load	25°C		13.8	18		13.8	18	mA
				Full range			18.8			18.8	

† Full range is −40°C to 105°C.

TLE2144I operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144I			TLE2144AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR–	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

TLE2141M electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2141M			TLE2141AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		225	1400		200	1000	μV
			Full range			2100			1700	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			250			250	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.3			−2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.2	3.7		3.2	3.7		
		I_{OH} = −100 μA	Full range	3.75			3.75			
		I_{OH} = −1 mA		3.65			3.65			
		I_{OH} = −10 mA		3.25			3.25			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 μA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.4		1.2	1.4	V
		I_{OL} = 100 μA	Full range			200			200	mV
		I_{OL} = 1 mA				250			225	
		I_{OL} = 10 mA				1.25			1.25	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	5			5			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		3.4	4.4		3.4	4.4	mA
			Full range			4.6			4.6	

† Full range is −55°C to 125°C.

TLE2141M operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2141M			TLE2141AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF†		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF†,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1	R_L = 2 kΩ†,		660			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ†,	C_L = 100 pF†		57°			57°		

† R_L and C_L terminated to 2.5 V.

TLE2141M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2141M			TLE2141AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω	25°C		200	900		175	500	μV
				Full range			1700			1200	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			250			250	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.8			−1.8	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.1	13.7		13.1	13.7		
		I_O = −100 μA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 μA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	25°C	100	450		100	450		V/mV
				Full range	20			20			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, V_{IC} = 2.5 V	No load,	25°C		3.5	4.5		3.5	4.5	mA
				Full range			4.7			4.7	

† Full range is −55°C to 125°C.

TLE2141M operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2141M			TLE2141AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 100 pF	R_L = 2 kΩ,	27	45		27	45		V/μs
SR–	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

TLE2142M electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2142M			TLE2142AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		220	1900		200	1500	μV
			Full range			2600			2200	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			200			200	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.3			−2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.4	3.7		3.4	3.7		
		I_{OH} = 100 μA	Full range	3.75			3.75			
		I_{OH} = 1 mA		3.65			3.65			
		I_{OH} = 10 mA		3.45			3.45			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 mA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.4		1.2	1.4	V
		I_{OL} = 100 μA	Full range			200			200	mV
		I_{OL} = 1 mA				250			250	
		I_{OL} = 10 mA				1.25			1.25	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	220		50	220		V/mV
			Full range	5			5			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		6.6	8.8		6.6	8.8	mA
			Full range			9.2			9.2	

† Full range is − 55°C to 125°C.

TLE2142M operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142M			TLE2142AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1,	R_L = 2 kΩ†, C_L = 100 pF		660			660		kHz
ϕ_m	Phase margin	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V.

TLE2142M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2142M			TLE2142AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω	25°C		290	1200		275	750	µV
				Full range			2000			1600	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		µV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			250			250	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	µA
				Full range			−1.8			−1.8	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 µA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.3	13.7		13.3	13.7		
		I_O = −100 µA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.3			13.3			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 µA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 µA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	25°C	100	450		100	450		V/mV
				Full range	20			20			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω		25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, V_{IC} = 2.5 V	No load,	25°C		6.9	9		6.9	9	mA
				Full range			9.4			9.4	

† Full range is −55°C to 125°C.

TLE2142M operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142M			TLE2142AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	R_L = 2 kΩ, C_L = 100 pF	A_{VD} = –1,	27	45		27	45		V/μs
SR–	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		0.4			0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 1 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

TLE2144M electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2144M			TLE2144AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		0.5	3.8		0.5	3	mV
			Full range			5.2			4.4	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current		25°C		8	100		8	100	nA
			Full range			250			250	
I_{IB}	Input bias current		25°C		−0.8	−2		−0.8	−2	μA
			Full range			−2.3			−2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	−0.3 to 3.2		0 to 3	−0.3 to 3.2		V
			Full range	0 to 2.7	−0.3 to 2.9		0 to 2.7	−0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = −150 μA	25°C	3.9	4.1		3.9	4.1		V
		I_{OH} = −1.5 mA		3.8	4		3.8	4		
		I_{OH} = −15 mA		3.4	3.7		3.4	3.7		
		I_{OH} = 100 μA	Full range	3.75			3.75			
		I_{OH} = 1 mA		3.65			3.65			
		I_{OH} = 10 mA		3.45			3.45			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125		75	125	mV
		I_{OL} = 1.5 μA			150	225		150	225	
		I_{OL} = 15 mA			1.2	1.6		1.2	1.6	V
		I_{OL} = 100 μA	Full range			200			200	mV
		I_{OL} = 1 mA				250			250	
		I_{OL} = 10 mA				1.45			1.45	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to −1.5 V	25°C	50	95		50	95		V/mV
			Full range	5			5			
r_i	Input resistance		25°C		70			70		MΩ
c_i	Input capacitance		25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	85	118		85	118		dB
			Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		90	106		dB
			Full range	85			85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		13.2	17.6		13.2	17.6	mA
			Full range			18.4			18.4	

† Full range is −55°C to 125°C.

TLE2144M operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144M			TLE2144AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	A_{VD} = –1, C_L = 500 pF	R_L = 2 kΩ†,		45			45		V/μs
SR–	Negative slew rate				42			42		
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16			0.16		μs
			To 0.01%		0.22			0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92			1.92		pA/√Hz
		f = 1 kHz			0.5			0.5		
THD + N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, A_{VD} = 2,	R_L = 2 kΩ†, f = 10 kHz		0.0052%			0.0052%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ†,	C_L = 100 pF		5.9			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ†, f = 100 kHz	C_L = 100 pF,		5.8			5.8		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_{VD} = 1	R_L = 2 kΩ†,		660			660		kHz
ϕ_m	Phase margin	R_L = 2 kΩ†,	C_L = 100 pF		57°			57°		

† R_L terminates at 2.5 V

TLE2144M electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLE2144M			TLE2144AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0,	R_S = 50 Ω	25°C		0.6	2.4		0.5	1.5	mV
				Full range			4			3.2	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1.7			1.7		μV/°C
I_{IO}	Input offset current			25°C		7	100		7	100	nA
				Full range			250			250	
I_{IB}	Input bias current			25°C		−0.7	−1.5		−0.7	−1.5	μA
				Full range			−1.8			−1.8	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		25°C	−15 to 13	−15.3 to 13.2		−15 to 13	−15.3 to 13.2		V
				Full range	−15 to 12.7	−15.3 to 12.9		−15 to 12.7	−15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		25°C	13.8	14.1		13.8	14.1		V
		I_O = −1.5 mA			13.7	14		13.7	14		
		I_O = −15 mA			13.1	13.7		13.1	13.7		
		I_O = −100 μA		Full range	13.7			13.7			
		I_O = −1 mA			13.6			13.6			
		I_O = −10 mA			13.1			13.1			
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		25°C	−14.7	−14.9		−14.7	−14.9		V
		I_O = 1.5 mA			−14.5	−14.8		−14.5	−14.8		
		I_O = 15 mA			−13.4	−13.8		−13.4	−13.8		
		I_O = 100 μA		Full range	−14.6			−14.6			
		I_O = 1 mA			−14.5			−14.5			
		I_O = 10 mA			−13.4			−13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	25°C	100	170		100	170		V/mV
				Full range	20			20			
r_i	Input resistance			25°C		65			65		MΩ
c_i	Input capacitance			25°C		2.5			2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	25°C	85	108		85	108		dB
				Full range	80			80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		25°C	90	106		90	106		dB
				Full range	85			85			
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	25°C	−25	−50		−25	−50		mA
			V_{ID} = −1 V		20	31		20	31		
I_{CC}	Supply current	V_O = 0, V_{IC} = 2.5 V	No load,	25°C		13.8	18		13.8	18	mA
				Full range			18.8			18.8	

† Full range is −55°C to 125°C

TLE2144M operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2144M			TLE2144AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	R_L = 2 kΩ, C_L = 100 pF	A_{VD} = –1,	27	45		27	45		V/μs
SR–	Negative slew rate			27	42		27	42		
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		0.34			0.34		μs
			To 0.01%		.4			.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω,	f = 10 Hz		15			15		nV/√Hz
		R_S = 20 Ω,	f = 1 kHz		10.5			10.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48			0.48		μV
		f = 0.1 Hz to 10 Hz			0.51			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89			1.89		pA/√Hz
		f = 10 kHz			0.47			0.47		
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, A_{VD} = 10,	R_L = 2 kΩ, f = 10 kHz		0.01%			0.01%		
B_1	Unity-gain bandwidth	R_L = 2 kΩ,	C_L = 100 pF		6			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, f = 100 kHz	C_L = 100 pF,		5.9			5.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1,	R_L = 2 kΩ, C_L = 100 pF		668			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ,	C_L = 100 pF		58°			58°		

TLE2141Y electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2141Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0	R_S = 50 Ω,		200	1000	μV
I_{IO}	Input offset current				7	100	nA
I_{IB}	Input bias current				−0.7	−1.5	μA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		−15 to 13	−15.3 to 13.2		V
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		13.8	14.1		V
		I_O = −1.5 mA		13.7	14		
		I_O = −15 mA		13.3	13.7		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		−14.7	−14.9		V
		I_O = 1.5 mA		−14.5	−14.8		
		I_O = 15 mA		−13.4	−13.8		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	100	450		V/mV
r_i	Input resistance				65		MΩ
c_i	Input capacitance				2.5		pF
z_o	Open-loop output impedance	f = 1 MHz			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	80	108		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		85	106		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	−25	−50		mA
			V_{ID} = −1 V	20	31		
I_{CC}	Supply current	V_O = 0,	No load		3.5	4.5	mA

TLE2142Y electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLE2142Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω,			150	875	μV
I_{IO}	Input offset current				7	100	nA
I_{IB}	Input bias current				−0.7	−1.5	μA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		−15 to 13	−15.3 to 13.2		V
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		13.8	14.1		V
		I_O = −1.5 mA		13.7	14		
		I_O = −15 mA		13.3	13.7		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		−14.7	−14.9		V
		I_O = 1.5 mA		−14.5	−14.8		
		I_O = 15 mA		−13.4	−13.8		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		100	450		V/mV
r_i	Input resistance				65		MΩ
c_i	Input capacitance				2.5		pF
z_o	Open-loop output impedance	f = 1 MHz			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω		80	108		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω		85	106		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	−25	−50		mA
			V_{ID} = −1 V	20	31		
I_{CC}	Supply current	V_O = 0, No load			6.9	9	mA

TLE2144Y electrical characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLE2144Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω			0.3	1.8	mV
I_{IO}	Input offset current				7	100	nA
I_{IB}	Input bias current				−0.7	−1.5	μA
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω		−15 to 13	−15.3 to 13.2		V
V_{OM+}	Maximum positive peak output voltage swing	I_O = −150 μA		13.8	14.1		V
		I_O = −1.5 mA		13.7	14		
		I_O = −15 mA		13.3	13.7		
V_{OM-}	Maximum negative peak output voltage swing	I_O = 150 μA		−14.7	−14.9		V
		I_O = 1.5 mA		−14.5	−14.8		
		I_O = 15 mA		−13.4	−13.8		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ	100	450		V/mV
r_i	Input resistance				65		MΩ
c_i	Input capacitance				2.5		pF
z_o	Open-loop output impedance	f = 1 MHz			30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min,	R_S = 50 Ω	80	108		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V,	R_S = 50 Ω	85	106		dB
I_{OS}	Short-circuit output current	V_O = 0	V_{ID} = 1 V	−25	−50		mA
			V_{ID} = −1 V	20	31		
I_{CC}	Supply current	V_O = 0,	No load		13.8	18	mA

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

TLE2141
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

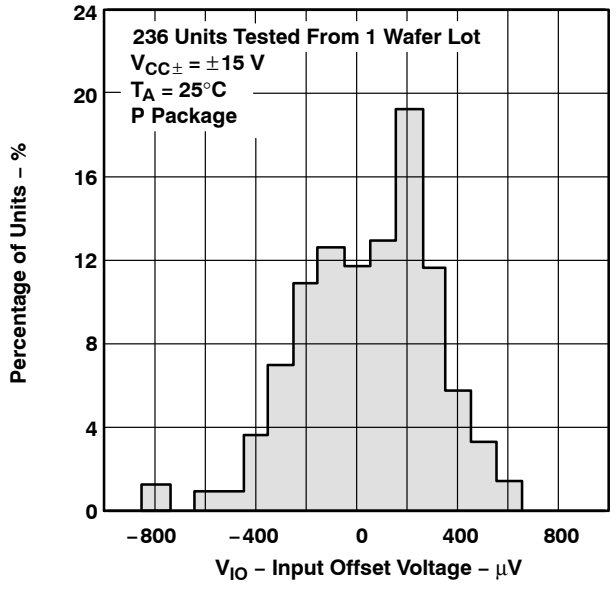


Figure 1

TLE2142
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

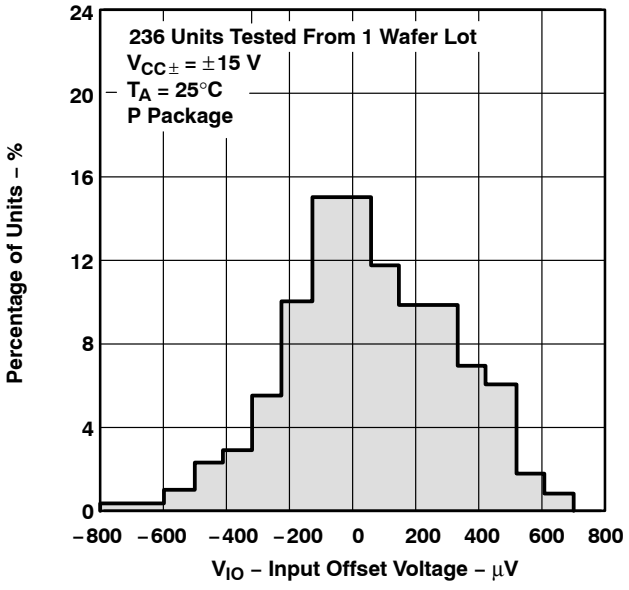


Figure 2

TLE2144
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

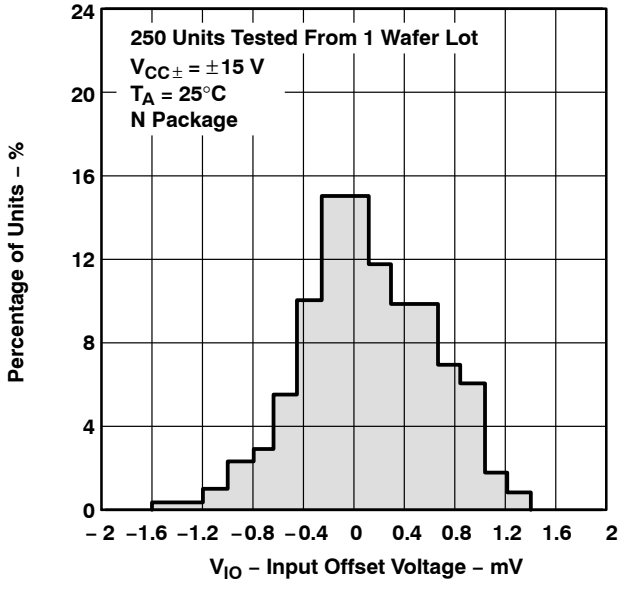


Figure 3

INPUT OFFSET CURRENT†
vs
FREE-AIR TEMPERATURE

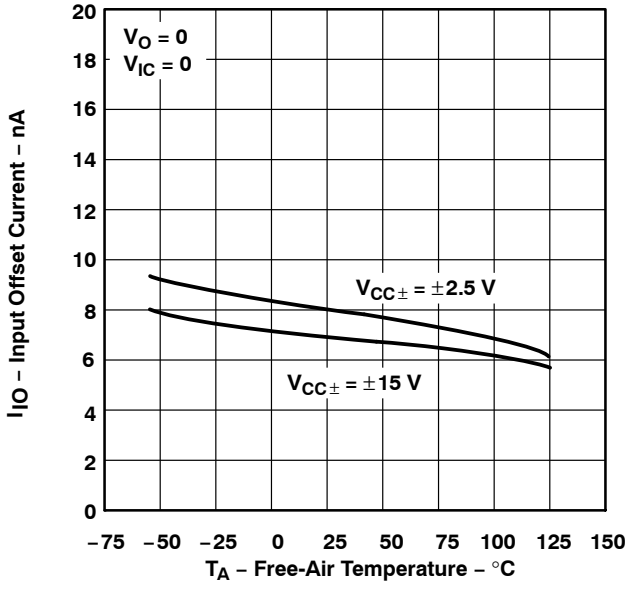


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT† vs COMMON-MODE INPUT VOLTAGE

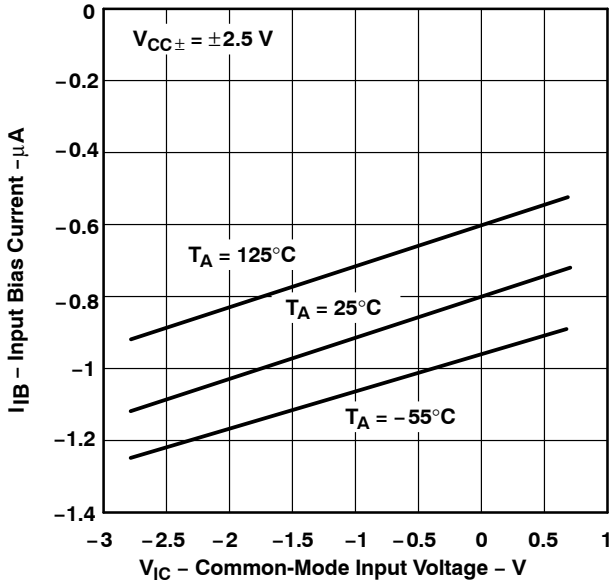


Figure 5

INPUT BIAS CURRENT† vs FREE-AIR TEMPERATURE

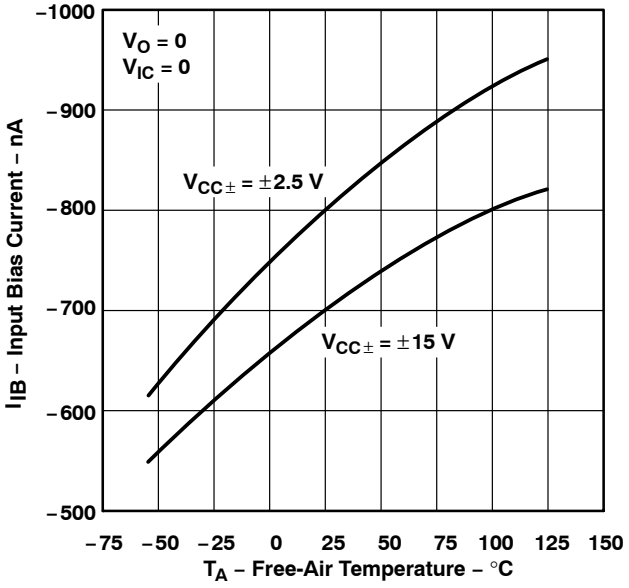


Figure 6

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

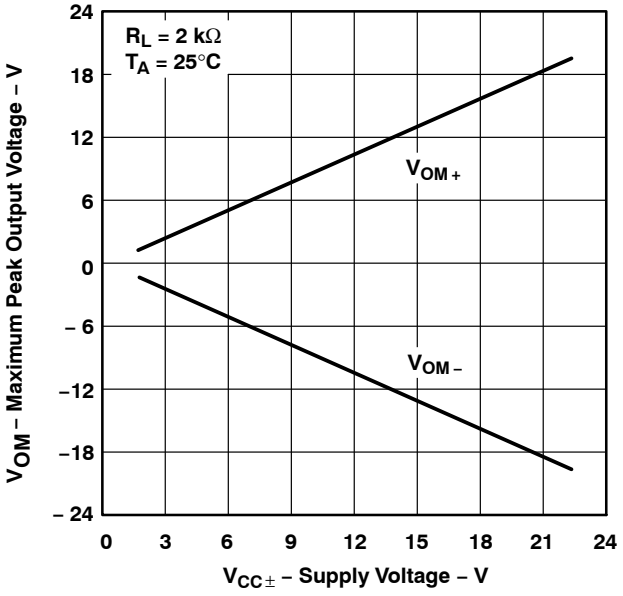


Figure 7

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

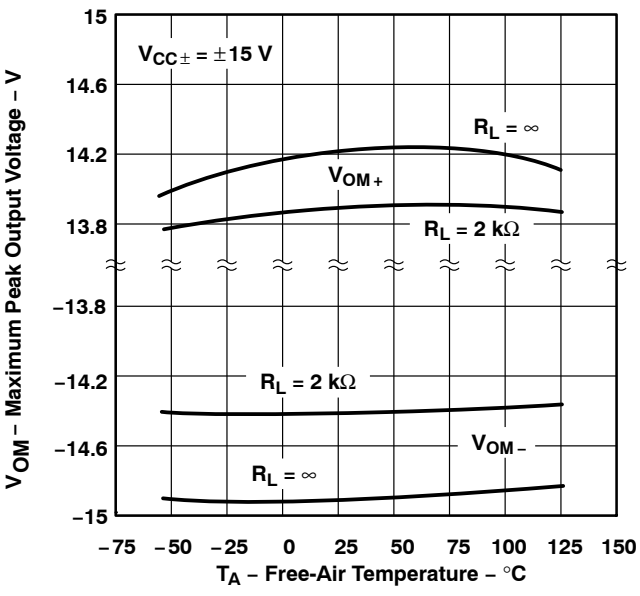


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE† vs OUTPUT CURRENT

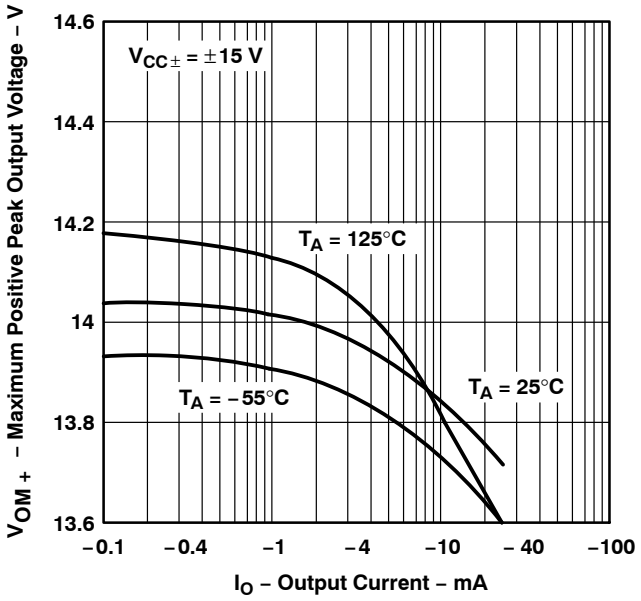


Figure 9

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE† vs OUTPUT CURRENT

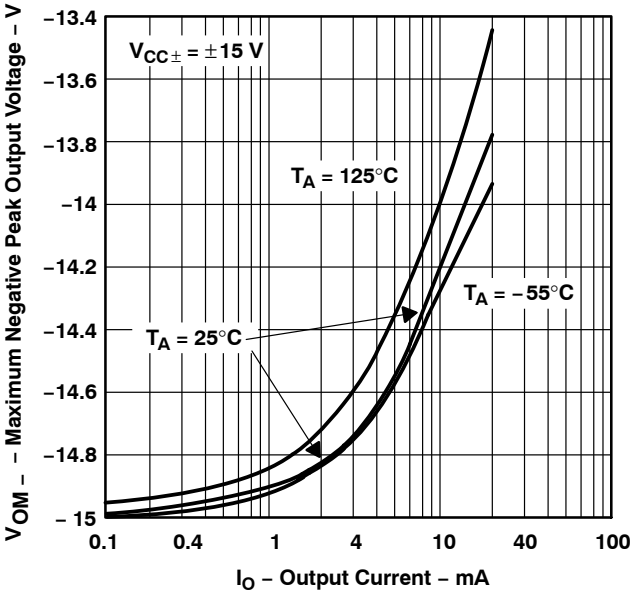


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE vs SETTLING TIME

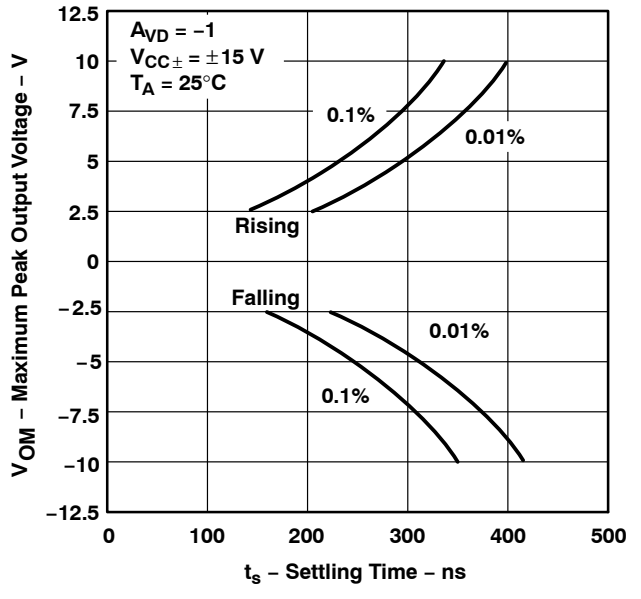


Figure 11

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE† vs FREQUENCY

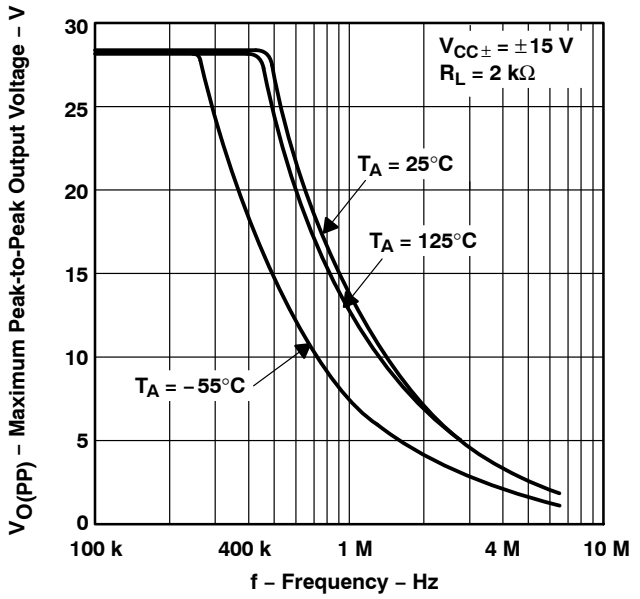


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE† vs OUTPUT CURRENT

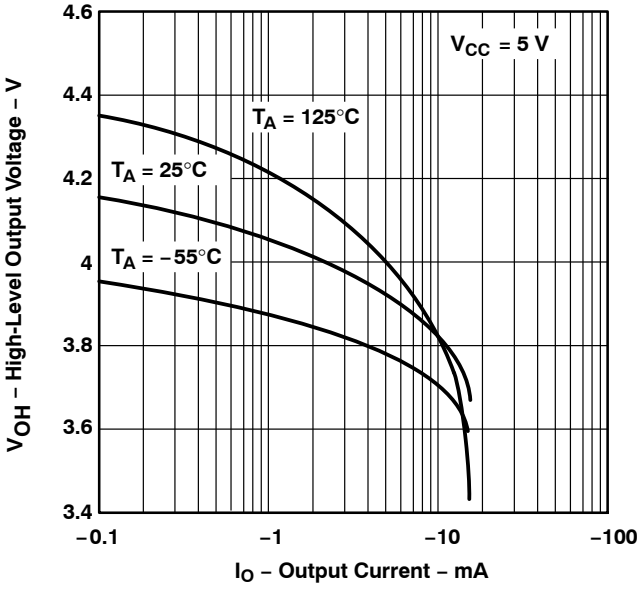


Figure 13

LOW-LEVEL OUTPUT VOLTAGE† vs OUTPUT CURRENT

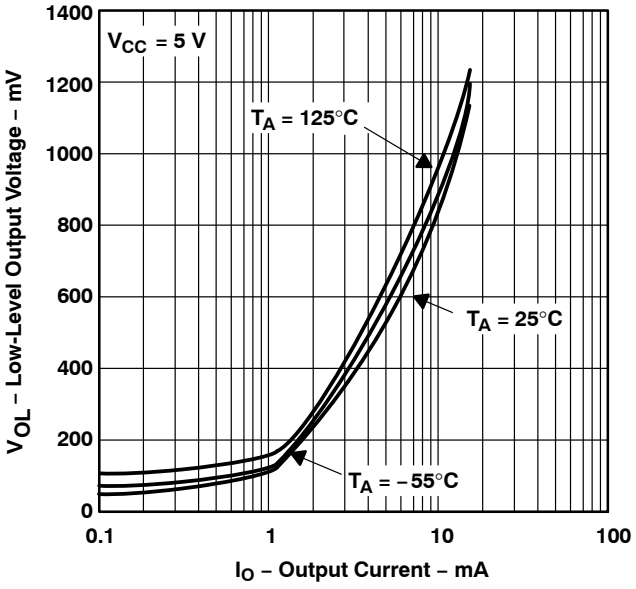


Figure 14

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

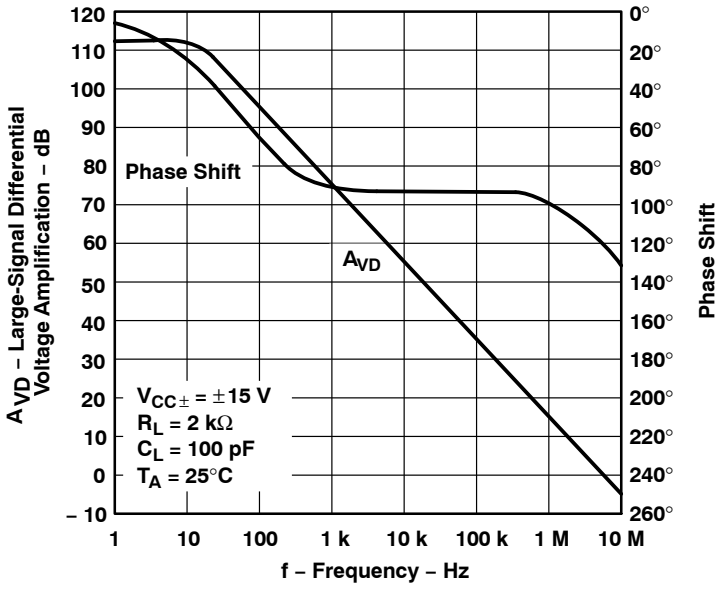


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

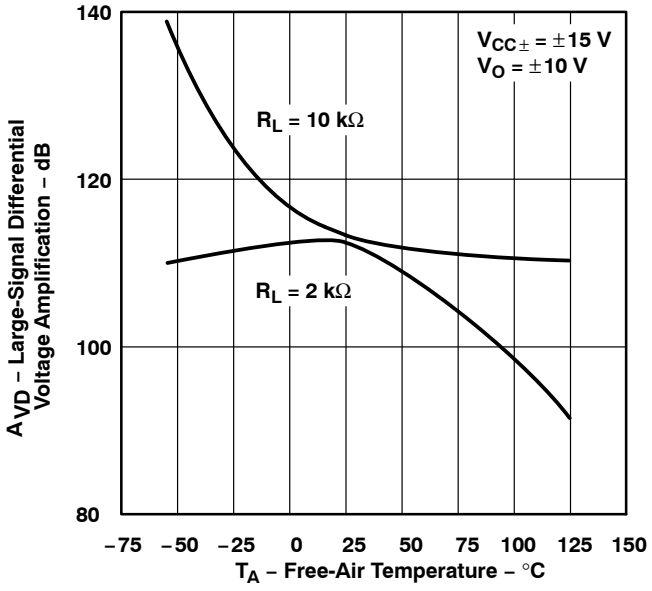


Figure 16

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

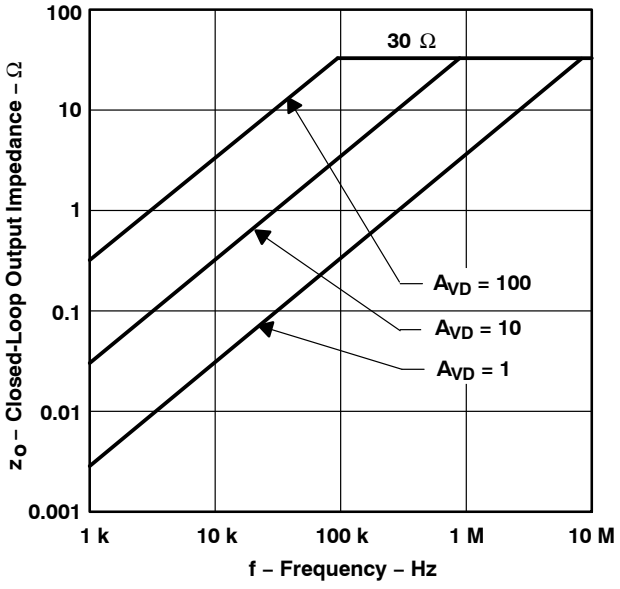


Figure 17

SHORT-CIRCUIT OUTPUT CURRENT† vs FREE-AIR TEMPERATURE

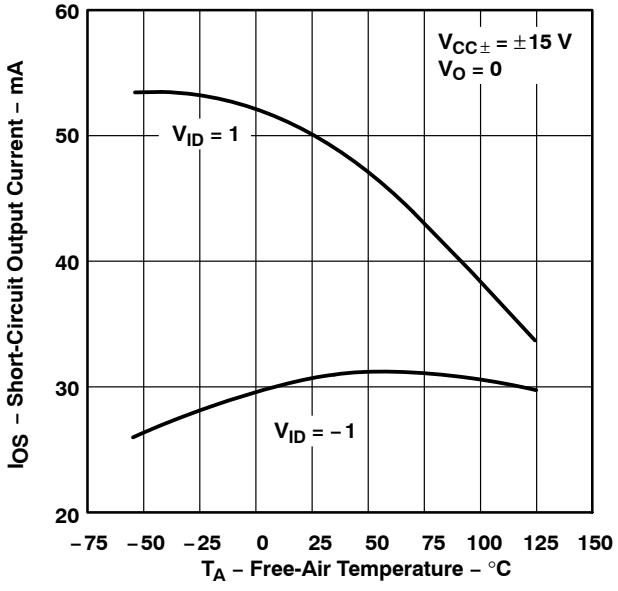


Figure 18

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

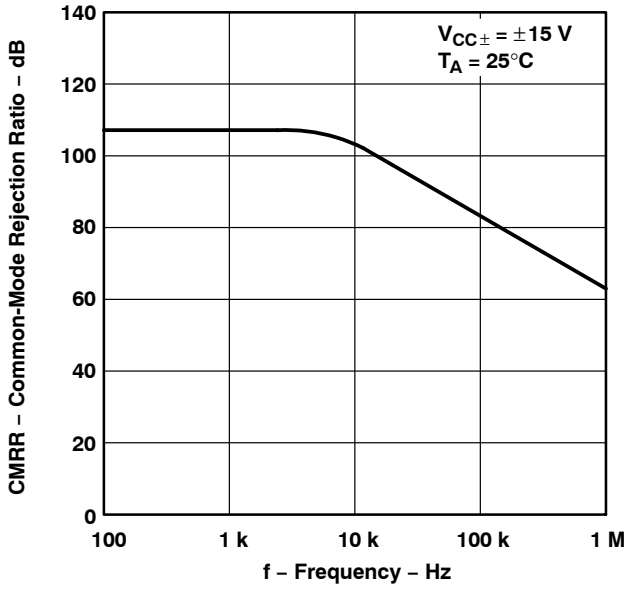


Figure 19

COMMON-MODE REJECTION RATIO† vs FREE-AIR TEMPERATURE

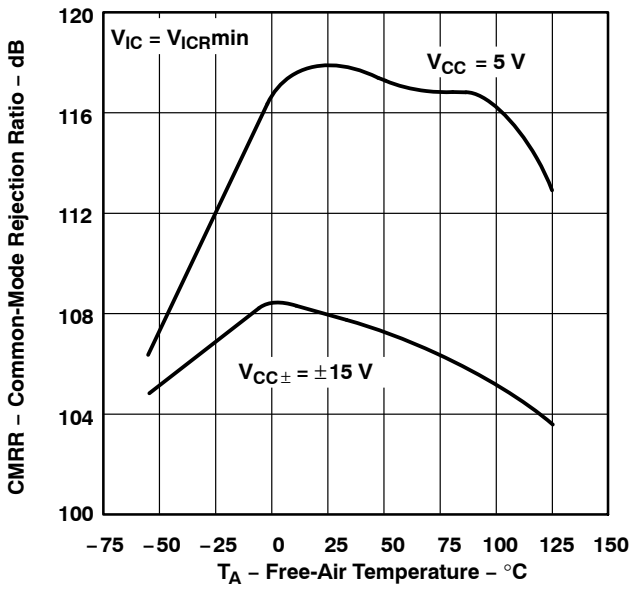


Figure 20

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

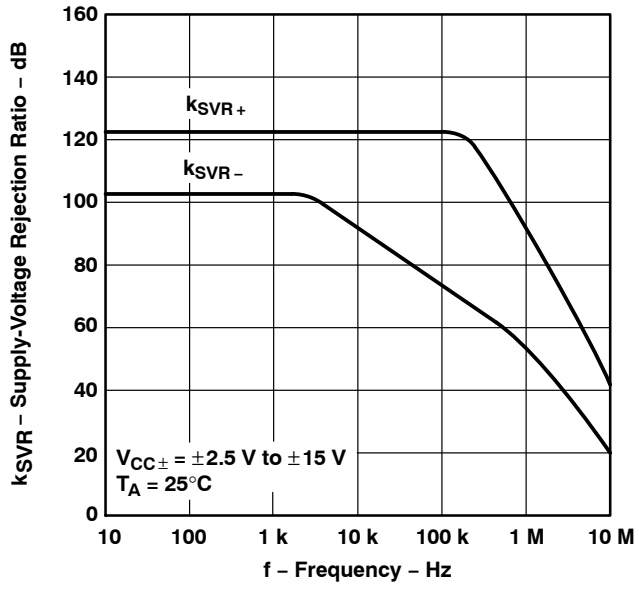


Figure 21

SUPPLY-VOLTAGE REJECTION RATIO† vs FREE-AIR TEMPERATURE

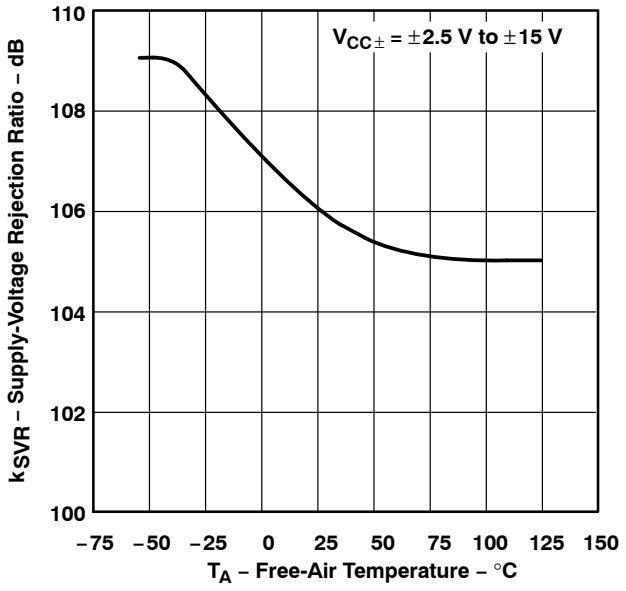


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT† vs SUPPLY VOLTAGE

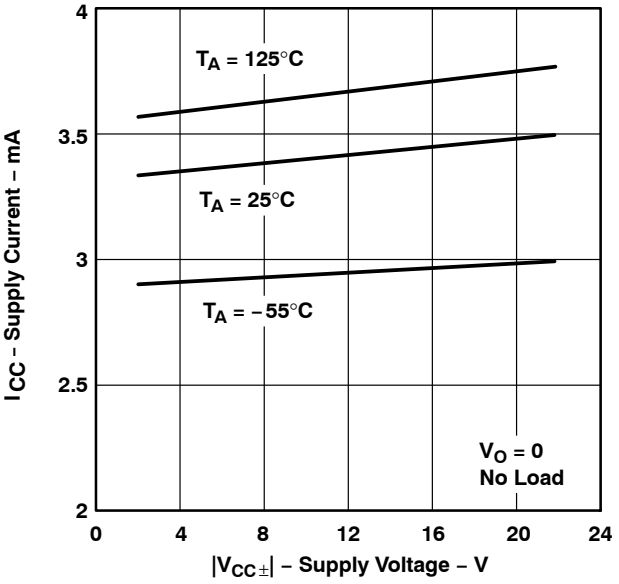


Figure 23

SUPPLY CURRENT† vs FREE-AIR TEMPERATURE

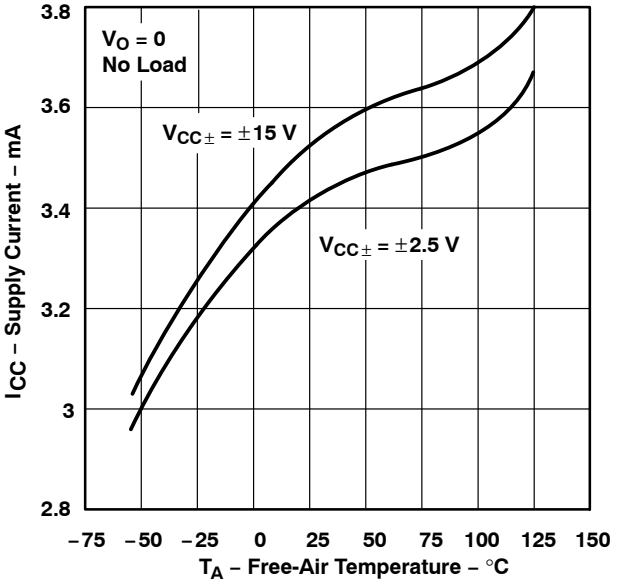


Figure 24

EQUIVALENT INPUT NOISE VOLTAGE† vs FREQUENCY

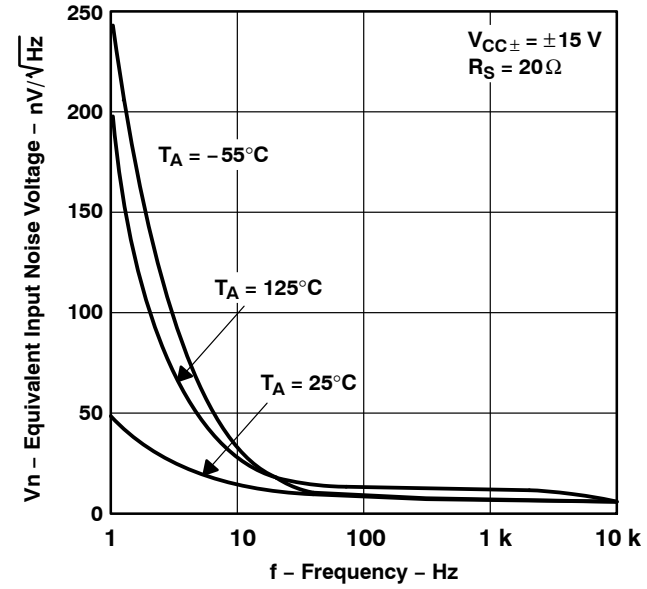


Figure 25

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD

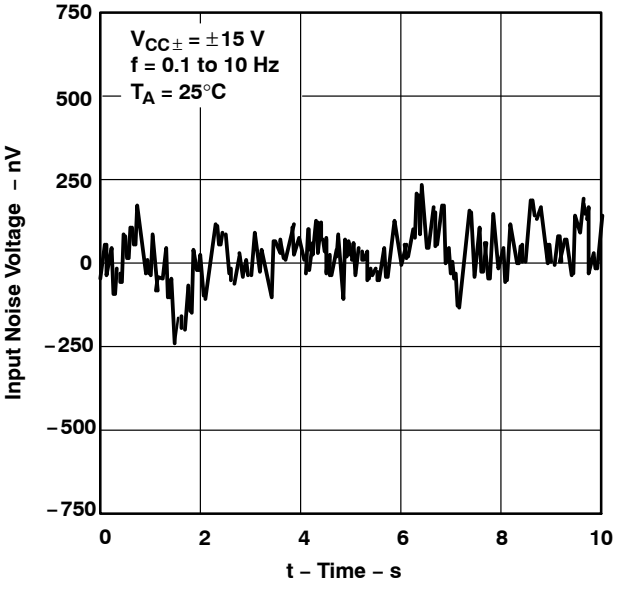


Figure 26

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

NOISE CURRENT† vs FREQUENCY

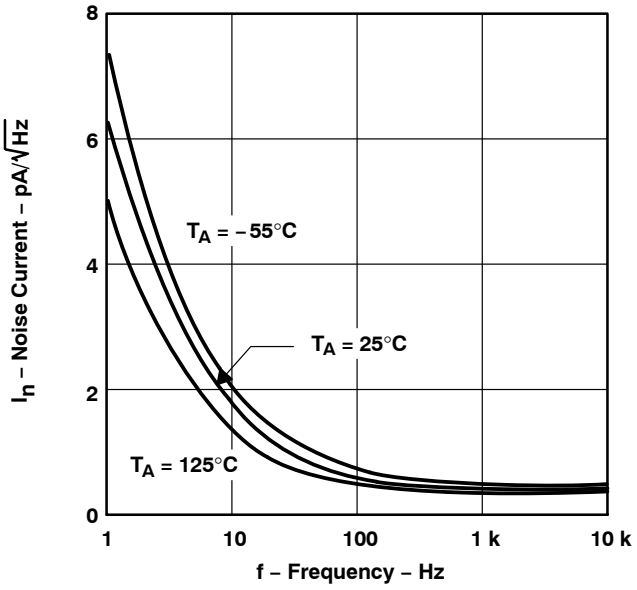


Figure 27

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

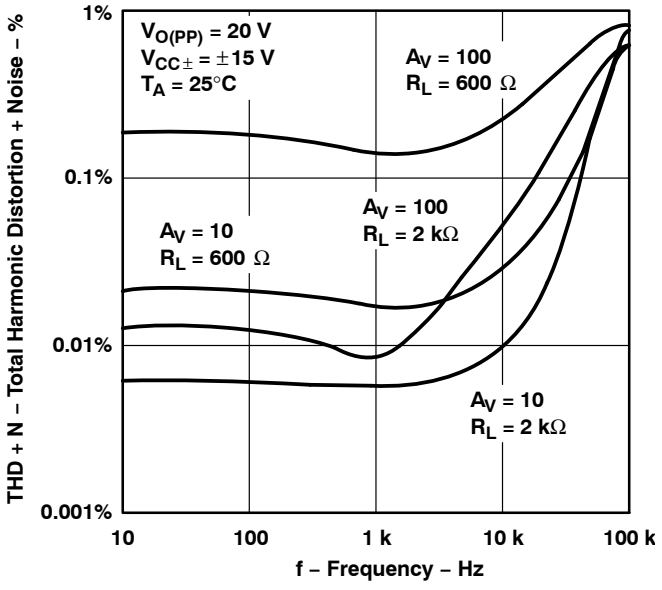


Figure 28

SLEW RATE† vs FREE-AIR TEMPERATURE

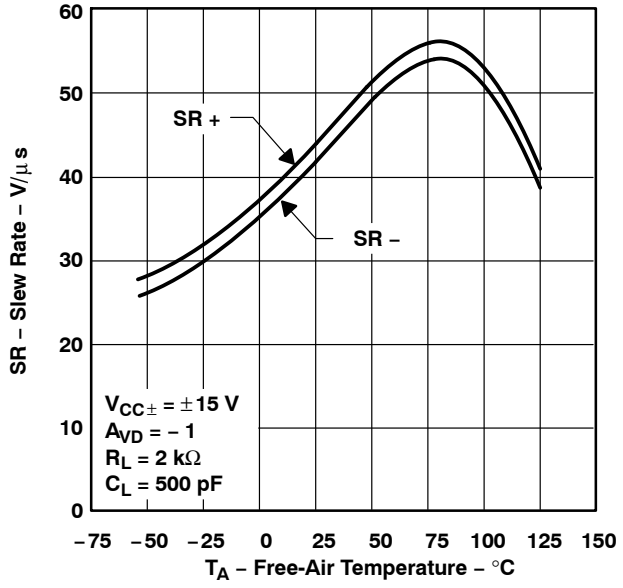


Figure 29

SLEW RATE vs LOAD CAPACITANCE

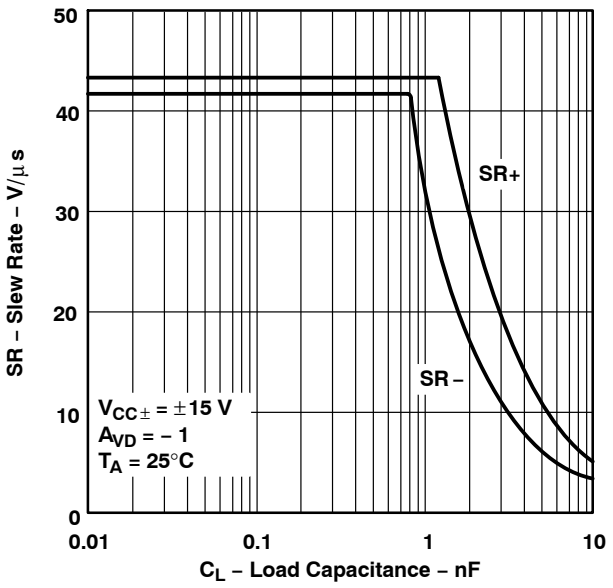


Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

NONINVERTING LARGE-SIGNAL PULSE RESPONSE†

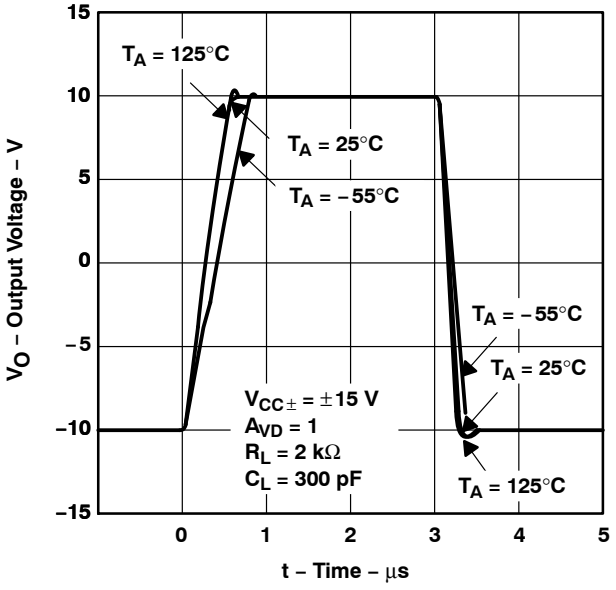


Figure 31

INVERTING LARGE-SIGNAL PULSE RESPONSE†

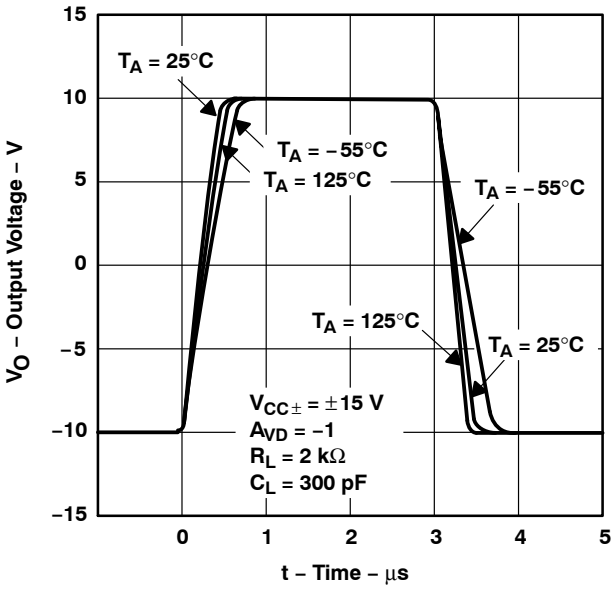


Figure 32

SMALL-SIGNAL PULSE RESPONSE

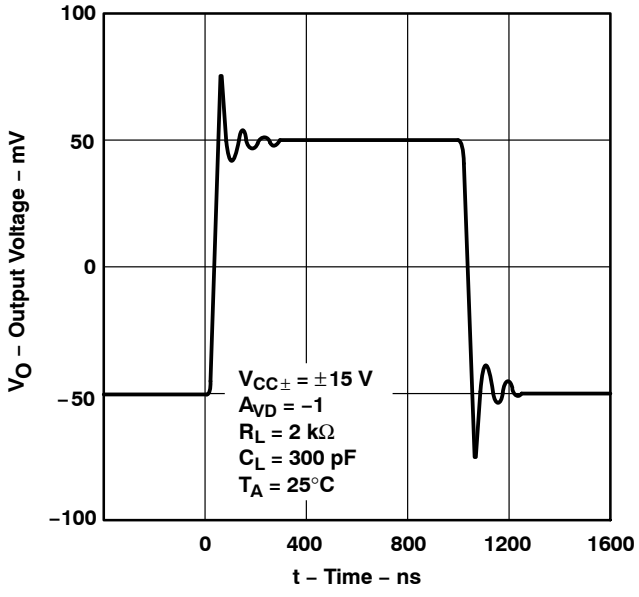


Figure 33

UNITY-GAIN BANDWIDTH† vs LOAD CAPACITANCE

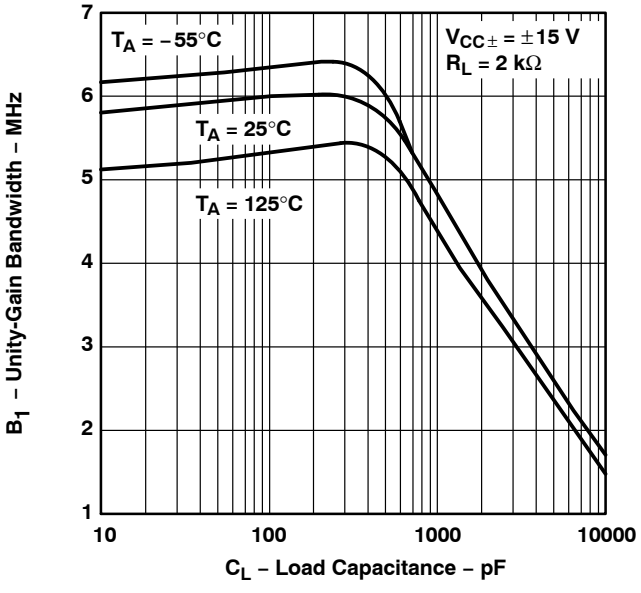


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

GAIN MARGIN† vs LOAD CAPACITANCE

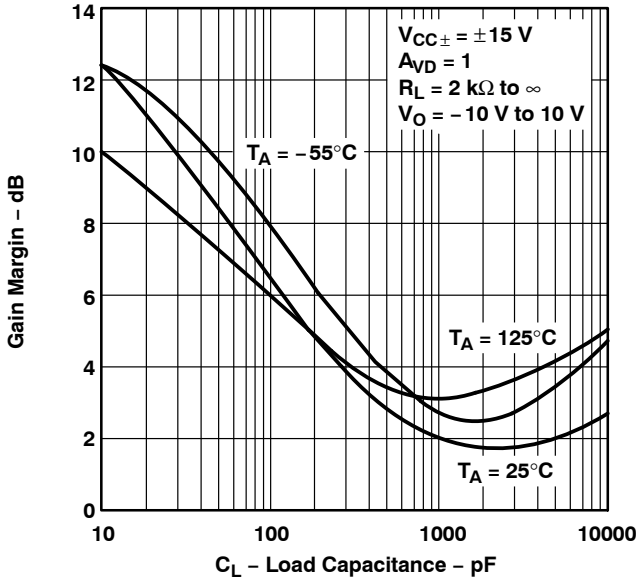


Figure 35

PHASE MARGIN† vs LOAD CAPACITANCE

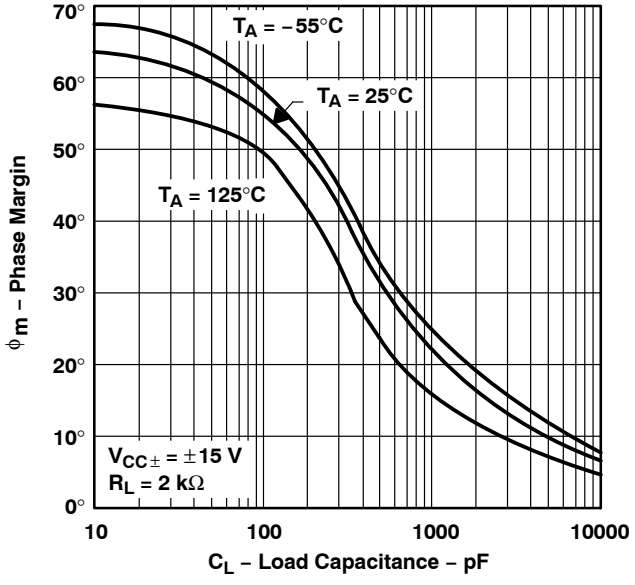


Figure 36

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

input offset voltage nulling

The TLE2141 series offers external null pins that can be used to further reduce the input offset voltage. If this feature is desired, connect the circuit of Figure 37 as shown. If external nulling is not needed, the null pins may be left unconnected.

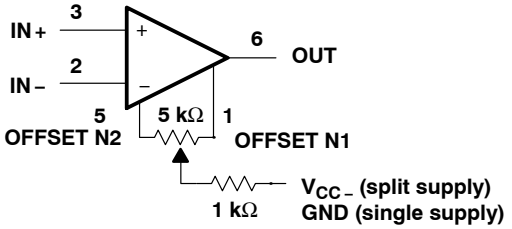


Figure 37. Input Offset Voltage Null Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9321603Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9321603Q2A TLE2142MFKB	Samples
5962-9321603QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9321603QHA TLE2142M	Samples
5962-9321603QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9321603QPA TLE2142M	Samples
5962-9321604Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9321604Q2A TLE2142 AMFKB	Samples
5962-9321604QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9321604QHA TLE2142AM	Samples
5962-9321604QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9321604QPA TLE2142AM	Samples
5962-9321605Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9321605Q2A TLE2144MFKB	Samples
5962-9321605QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9321605QCA TLE2144MJB	Samples
5962-9321606Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9321606Q2A TLE2144 AMFKB	Samples
5962-9321606QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9321606QCA TLE2144AMJB	Samples
TLE2141ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2141AC	Samples
TLE2141ACP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2141AC	Samples
TLE2141AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2141AI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2141AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2141AI	Samples
TLE2141AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2141AI	Samples
TLE2141CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2141C	Samples
TLE2141CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2141C	Samples
TLE2141CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2141C	Samples
TLE2141CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2141CP	Samples
TLE2141CPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2141CP	Samples
TLE2141ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2141I	Samples
TLE2141IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2141I	Samples
TLE2141IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2141IP	Samples
TLE2141IPE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		TLE2141IP	Samples
TLE2141MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2141M	Samples
TLE2141MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2141M	Samples
TLE2142ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2142AC	Samples
TLE2142ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2142AC	Samples
TLE2142ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2142AC	Samples
TLE2142AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2142AI	Samples
TLE2142AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2142AI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2142AMD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	E2142A	Samples
TLE2142AMDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		E2142A	Samples
TLE2142AMDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	E2142A	Samples
TLE2142AMDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		E2142A	Samples
TLE2142AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9321604Q2A TLE2142 AMFKB	Samples
TLE2142AMJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type		TLE2142AMJG	Samples
TLE2142AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9321604QPA TLE2142AM	Samples
TLE2142AMUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9321604QHA TLE2142AM	Samples
TLE2142CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2142C	Samples
TLE2142CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2142C	Samples
TLE2142CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2142C	Samples
TLE2142CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2142C	Samples
TLE2142CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2142CP	Samples
TLE2142CPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	Q2142	Samples
TLE2142ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	2142I	Samples
TLE2142IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	2142I	Samples
TLE2142IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	2142I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2142IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 105	TLE2142IP	Samples
TLE2142MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2142M	Samples
TLE2142MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2142M	Samples
TLE2142MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2142M	Samples
TLE2142MDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2142M	Samples
TLE2142MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9321603Q2A TLE2142MFKB	Samples
TLE2142MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9321603QPA TLE2142M	Samples
TLE2142MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9321603QHA TLE2142M	Samples
TLE2144ACN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2144ACN	Samples
TLE2144AIN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLE2144AIN	Samples
TLE2144AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9321606Q2A TLE2144 AMFKB	Samples
TLE2144AMJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9321606QCA TLE2144AMJB	Samples
TLE2144CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLE2144C	Samples
TLE2144CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLE2144C	Samples
TLE2144CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLE2144C	Samples
TLE2144CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLE2144CN	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2144IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	TLE2144I	Samples
TLE2144IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	TLE2144I	Samples
TLE2144IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 105	TLE2144IN	Samples
TLE2144MDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLE2144M	Samples
TLE2144MDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLE2144M	Samples
TLE2144MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9321605Q2A TLE2144MFKB	Samples
TLE2144MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9321605QCA TLE2144MJB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLE2141, TLE2141A, TLE2142, TLE2142A, TLE2142AM, TLE2142M, TLE2144, TLE2144A, TLE2144AM, TLE2144M :

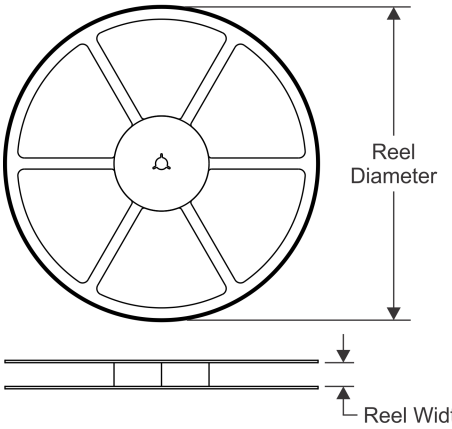
- Catalog: TLE2142A, TLE2142, TLE2144A, TLE2144
- Automotive: TLE2141-Q1, TLE2142-Q1, TLE2142-Q1
- Enhanced Product: TLE2141-EP, TLE2144-EP, TLE2144-EP
- Military: TLE2141M, TLE2141AM, TLE2142M, TLE2142AM, TLE2144M, TLE2144AM

NOTE: Qualified Version Definitions:

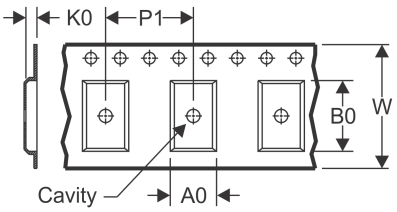
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

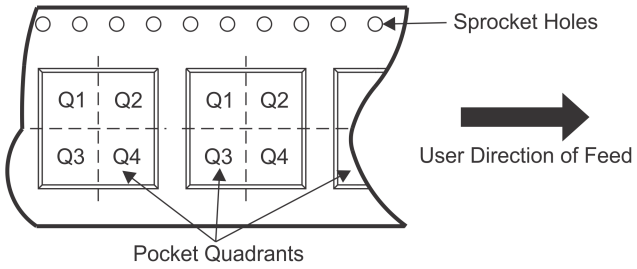


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

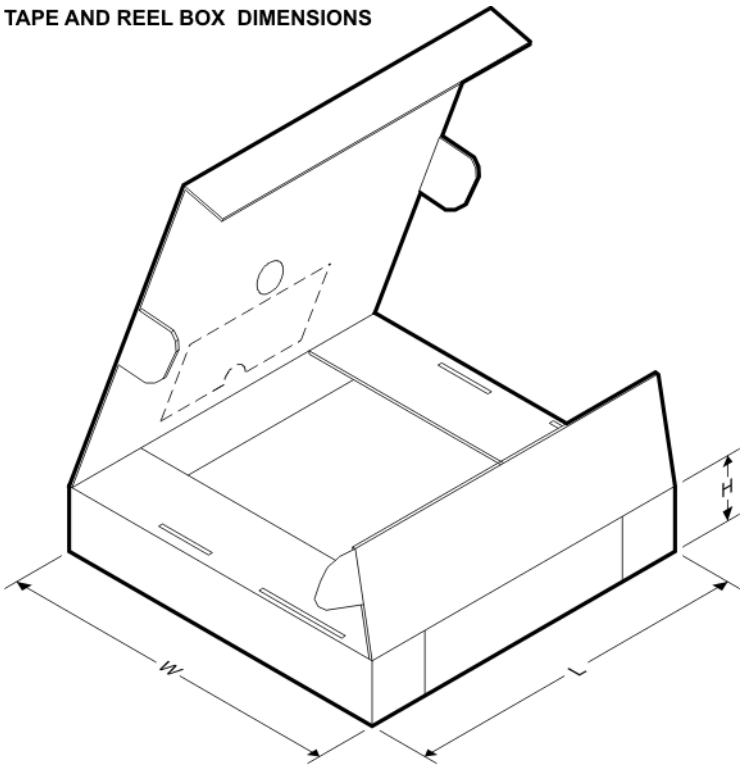
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2141AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2141CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2141IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2141MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2142ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2142AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2142AMDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2142AMDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2142CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2142CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLE2142IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2142MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2142MDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2144CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TLE2144IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

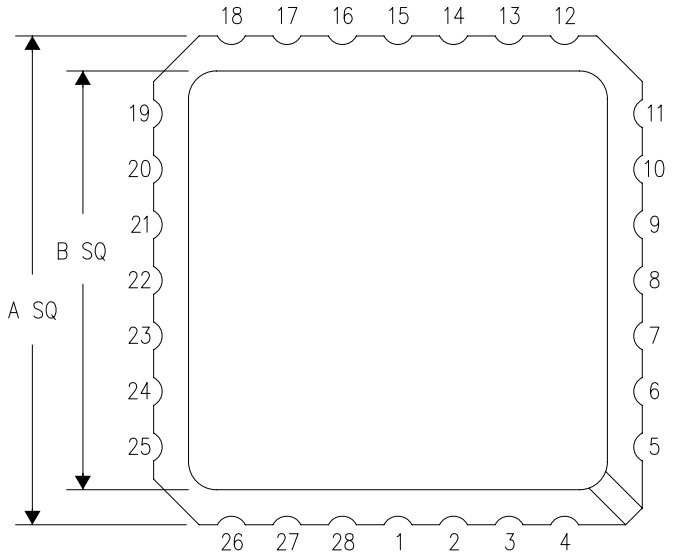


*All dimensions are nominal

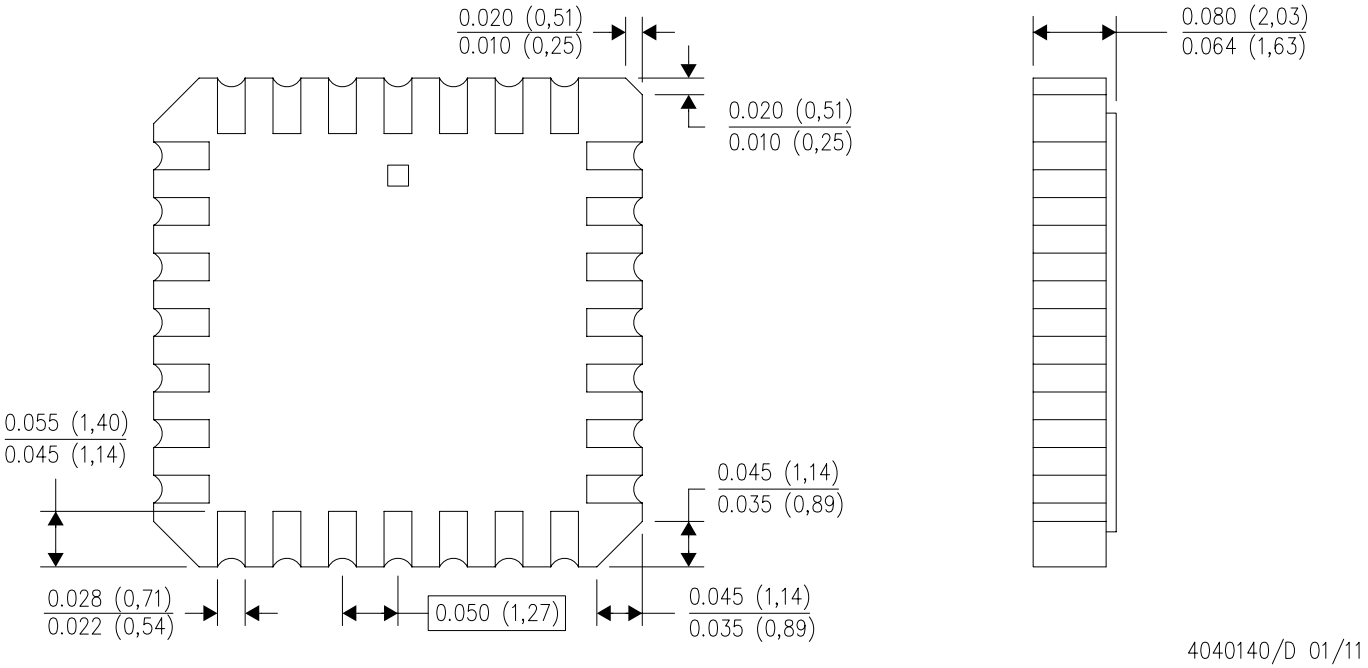
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2141AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2141CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2141IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2141MDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2142ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2142AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2142AMDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2142AMDRG4	SOIC	D	8	2500	350.0	350.0	43.0
TLE2142CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2142CPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TLE2142IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2142MDR	SOIC	D	8	2500	350.0	350.0	43.0
TLE2142MDRG4	SOIC	D	8	2500	350.0	350.0	43.0
TLE2144CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TLE2144IDWR	SOIC	DW	16	2000	350.0	350.0	43.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

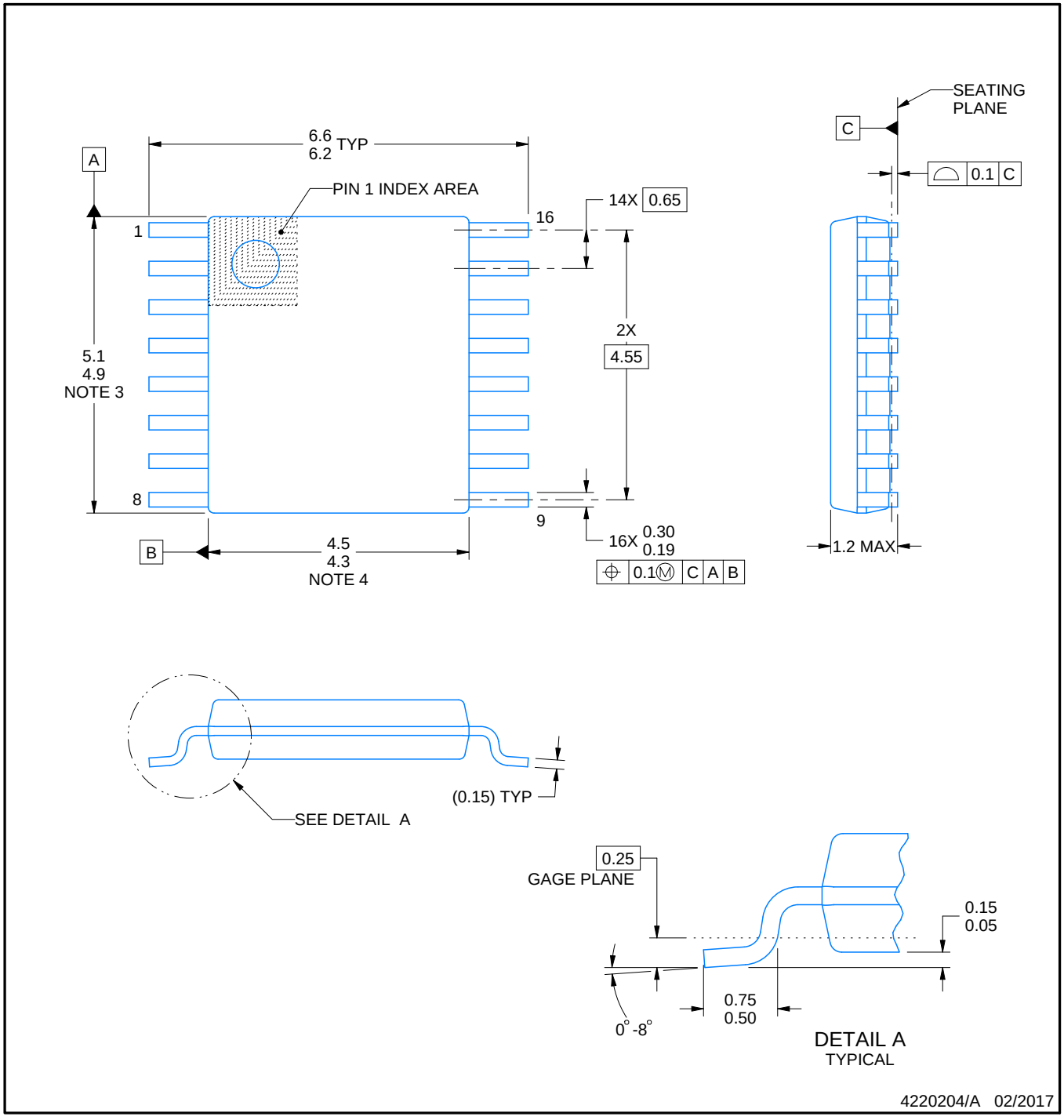
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

PACKAGE OUTLINE

PW0016A

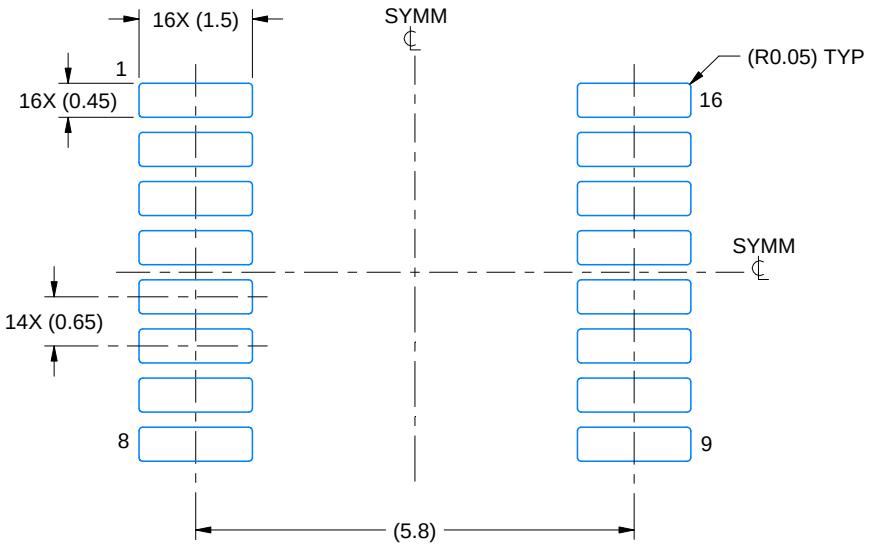
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

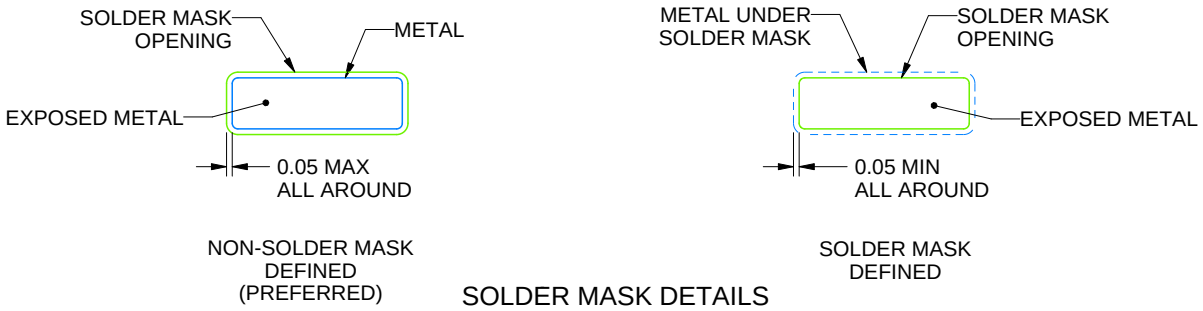


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

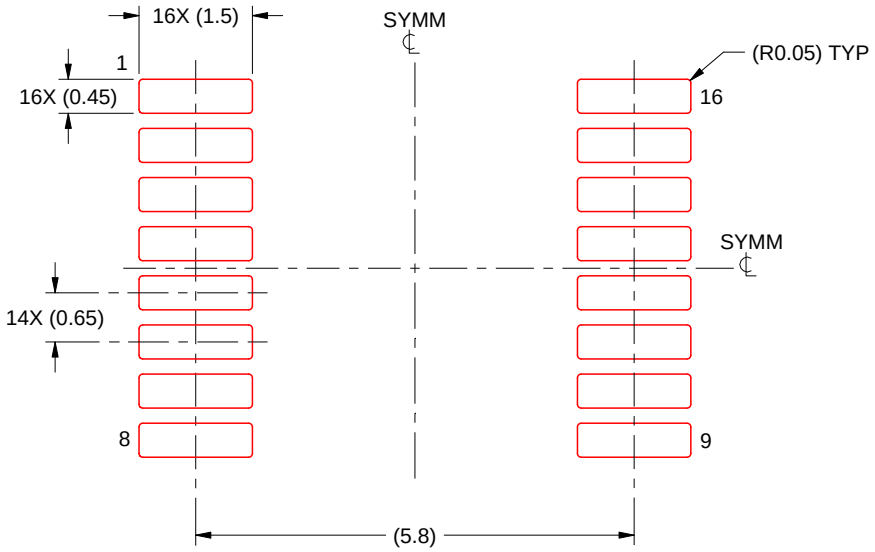


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



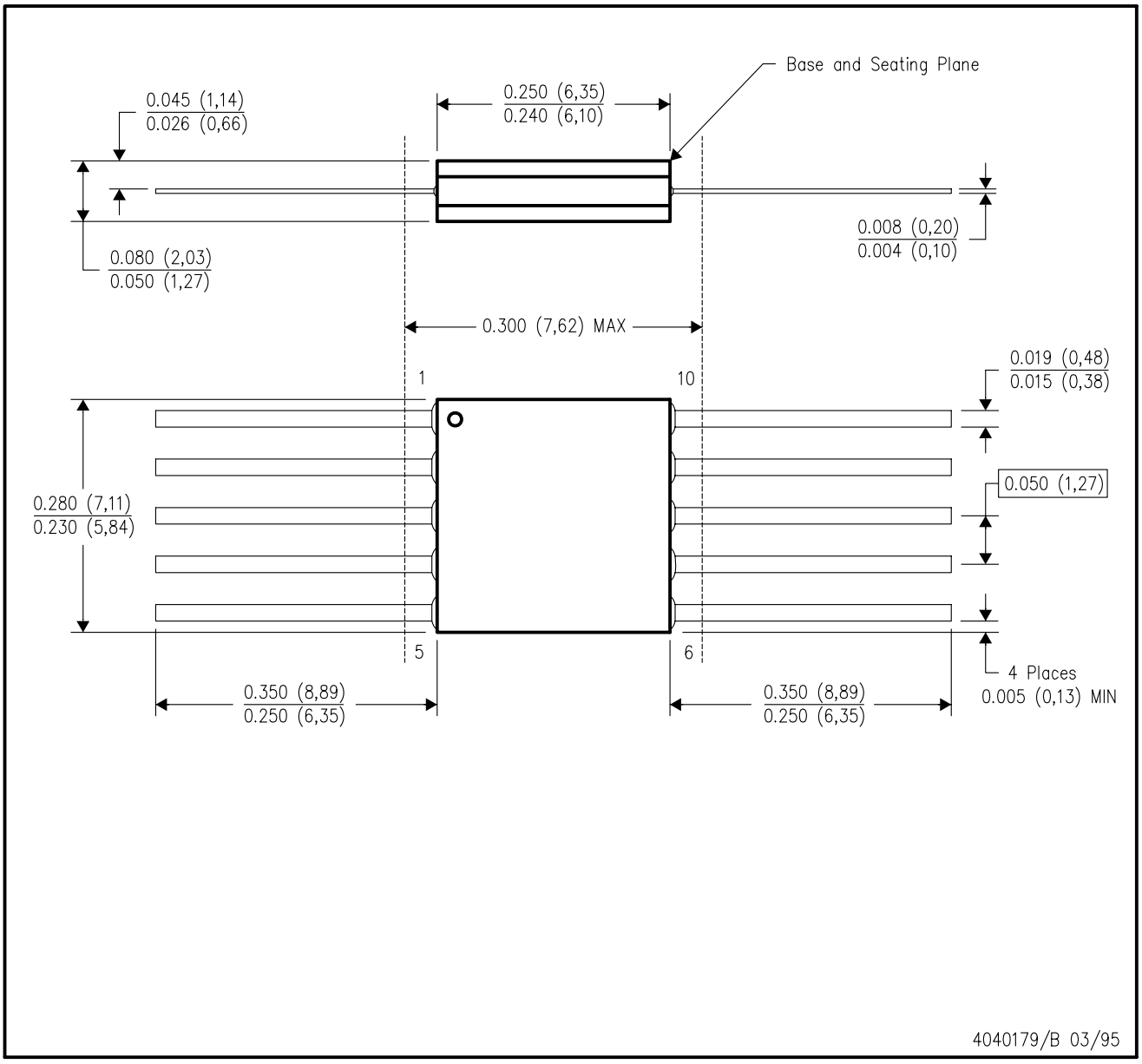
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

U (S–GDFP–F10) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

GENERIC PACKAGE VIEW

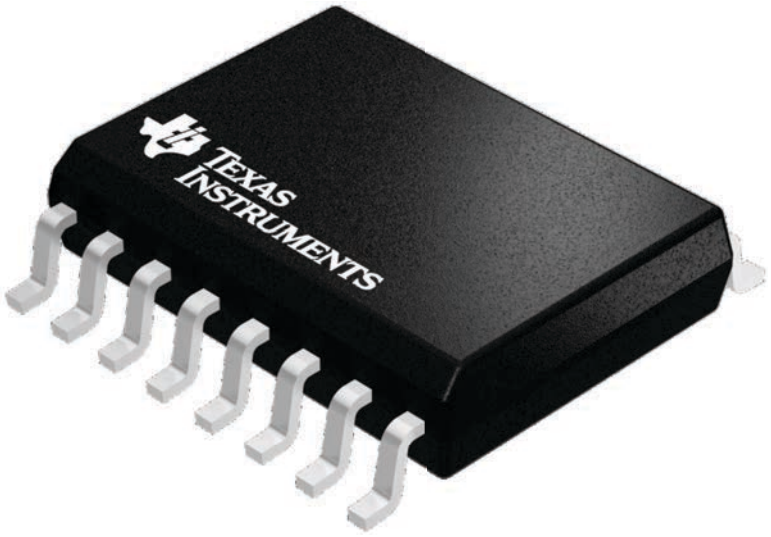
DW 16

SOIC - 2.65 mm max height

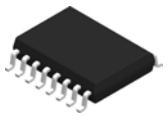
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

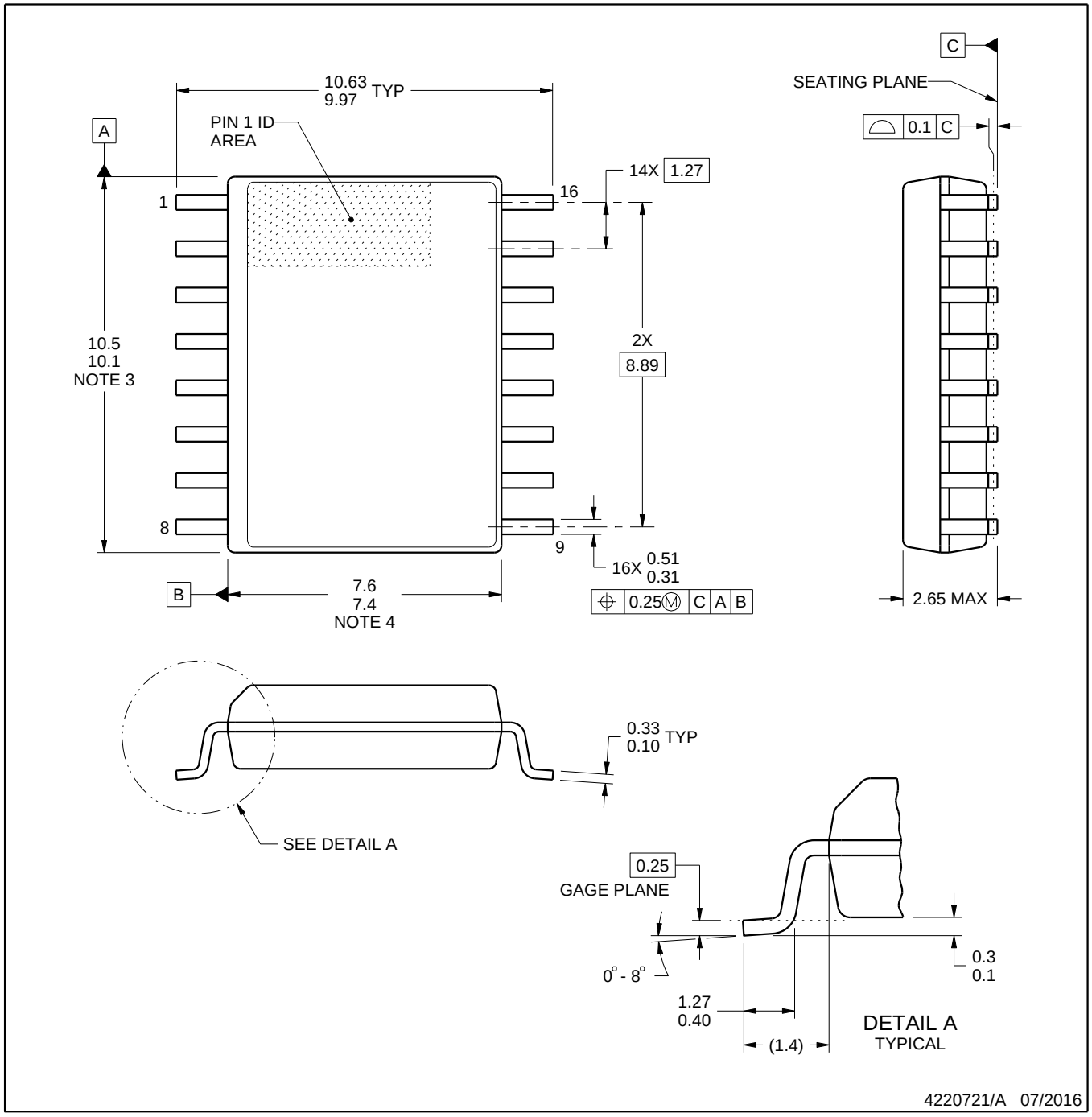


PACKAGE OUTLINE

DW0016A

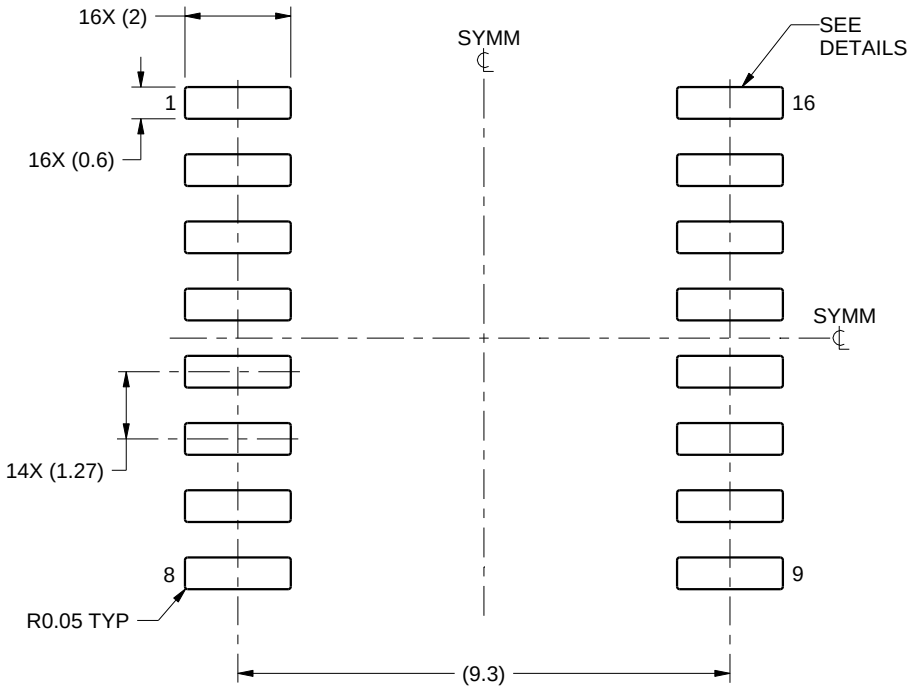
SOIC - 2.65 mm max height

SOIC

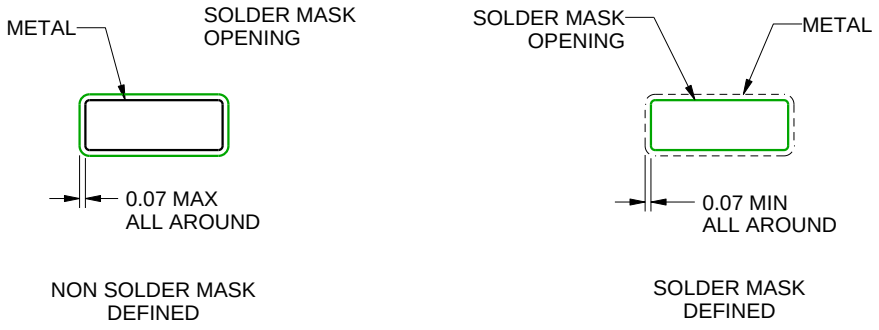


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

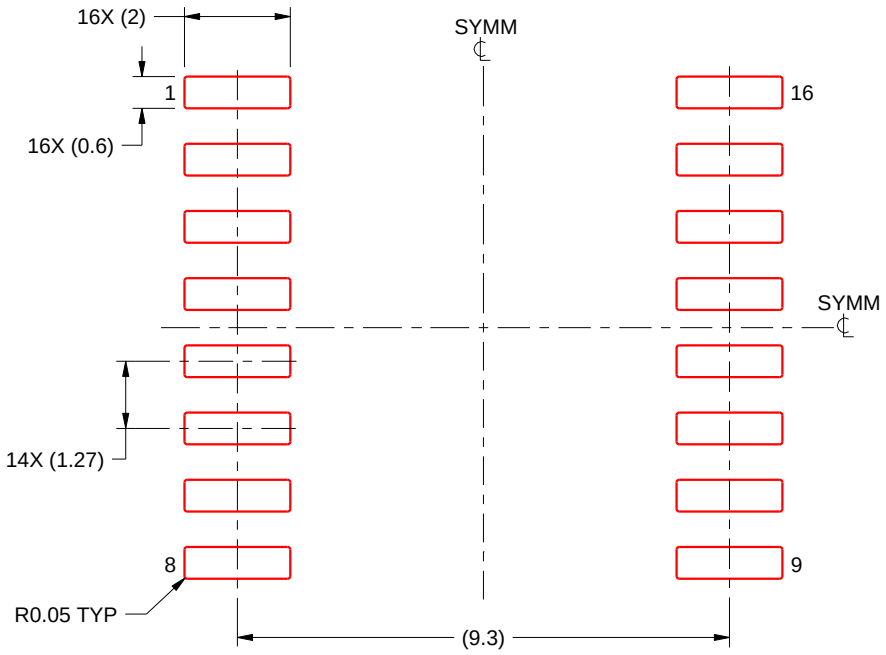


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

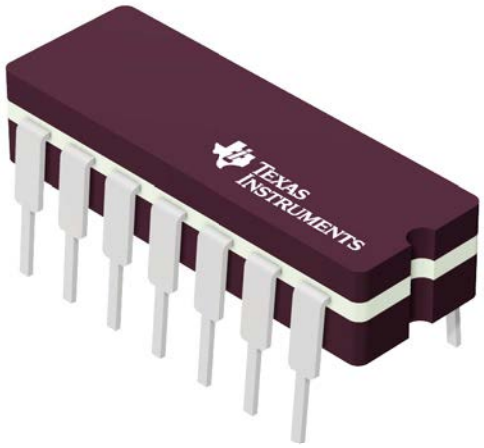
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

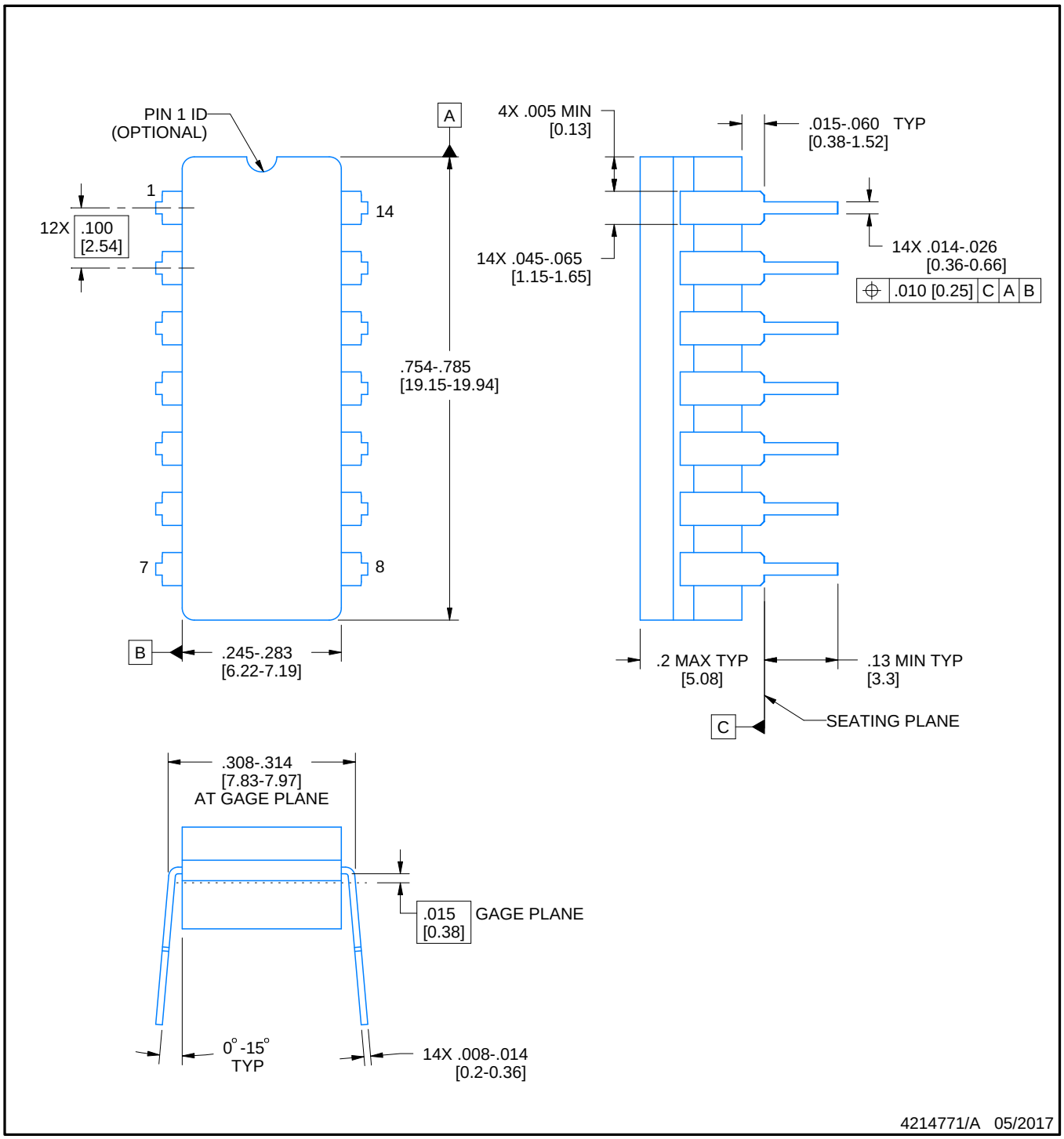
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

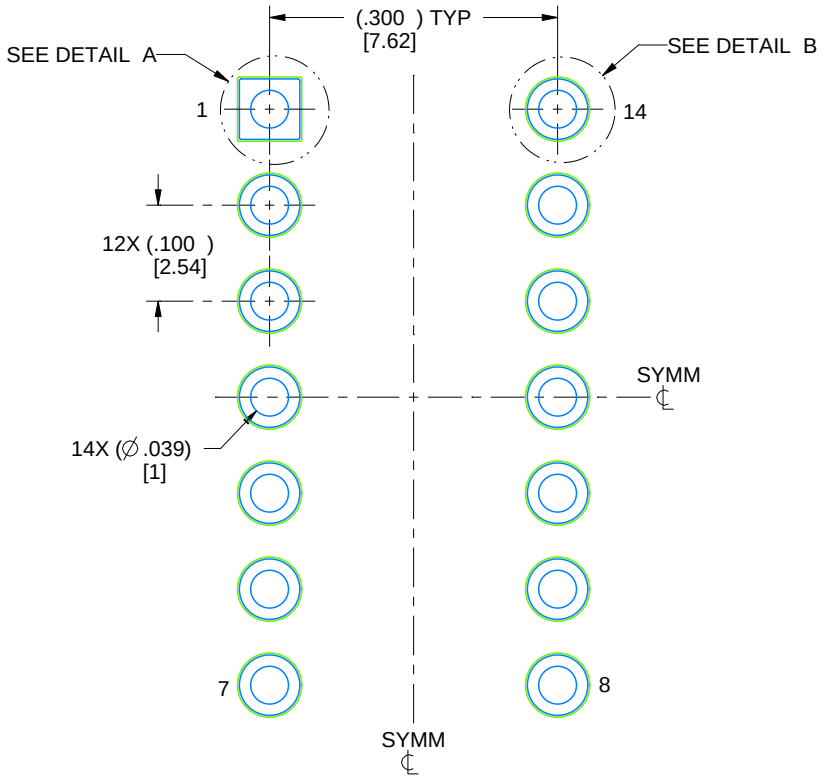
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

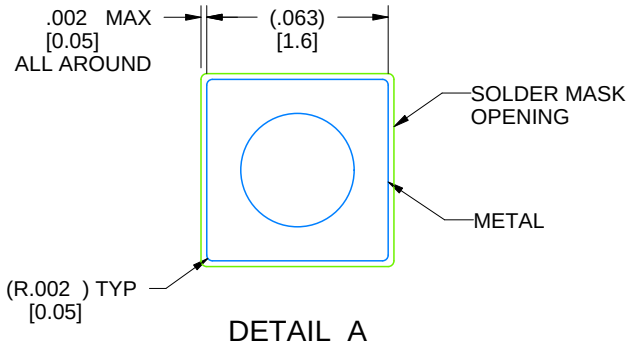
J0014A

CDIP - 5.08 mm max height

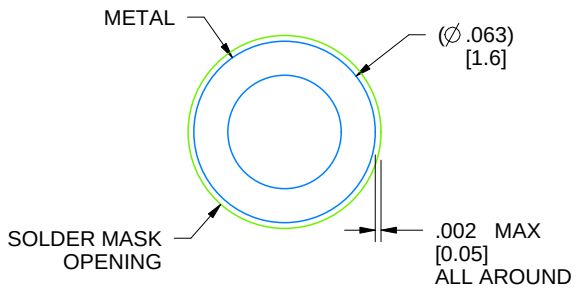
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

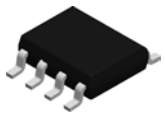


DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

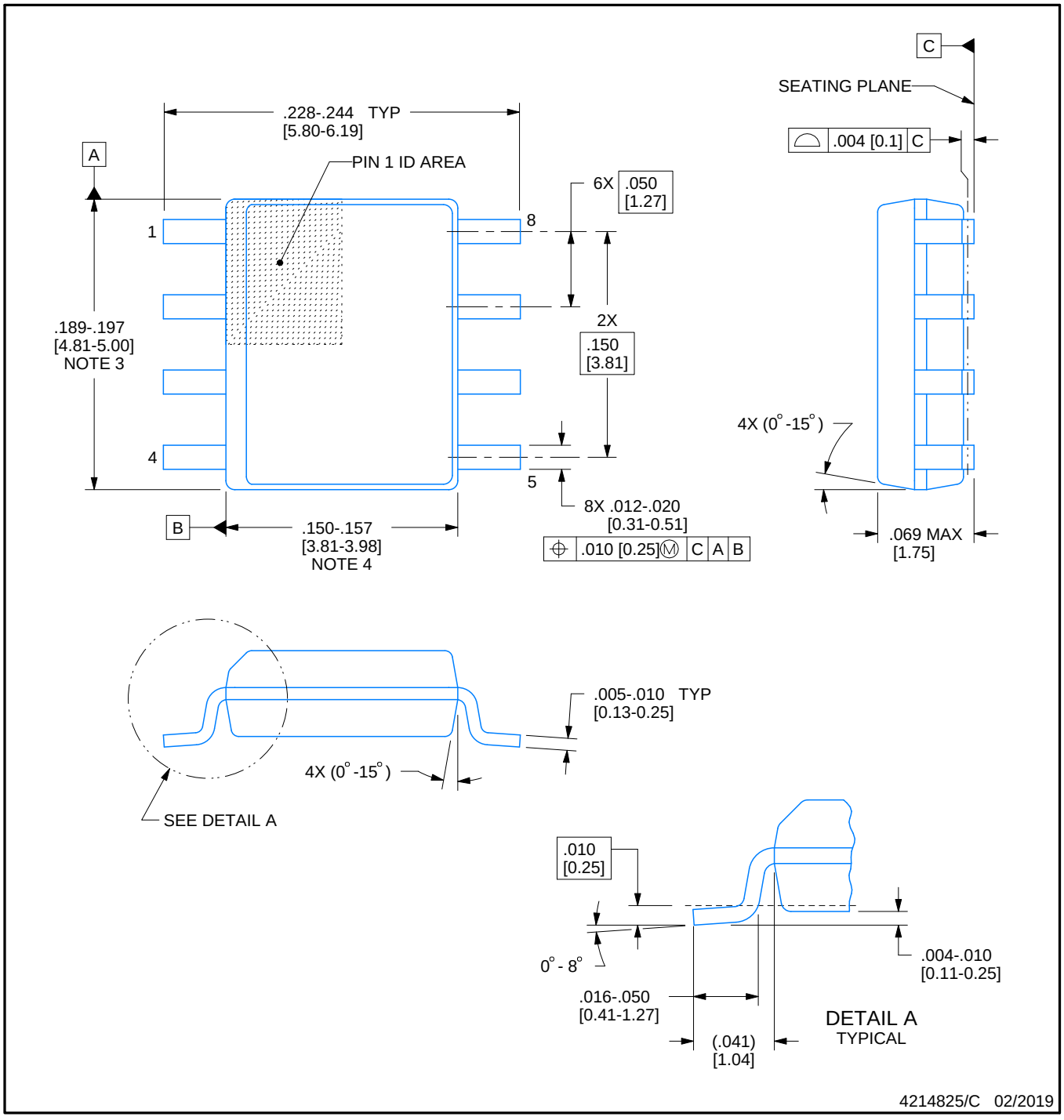


PACKAGE OUTLINE

D0008A

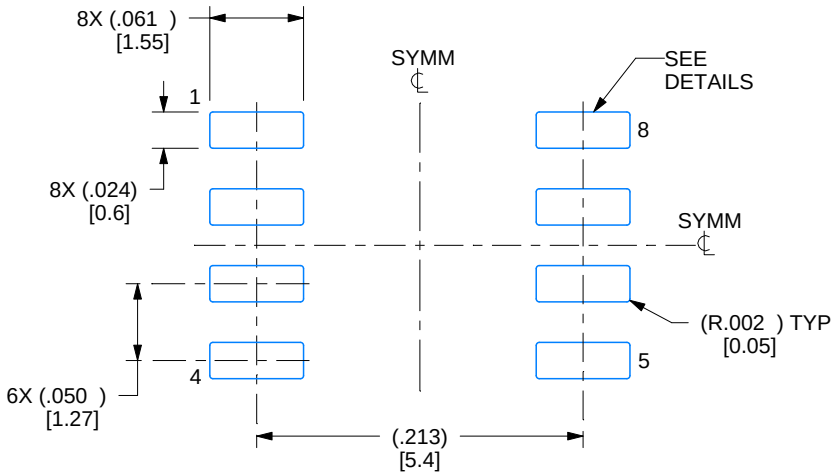
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

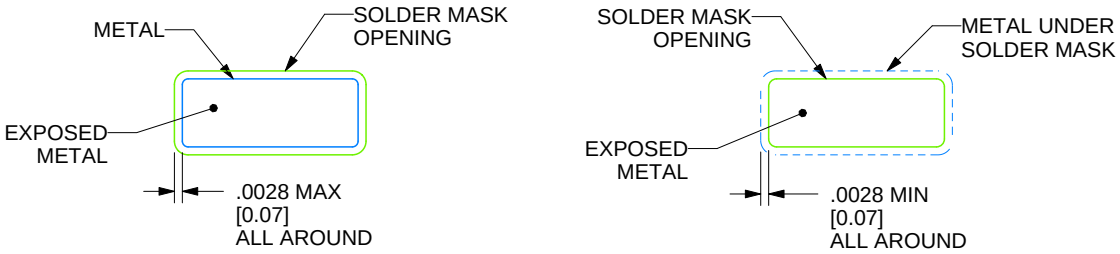


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

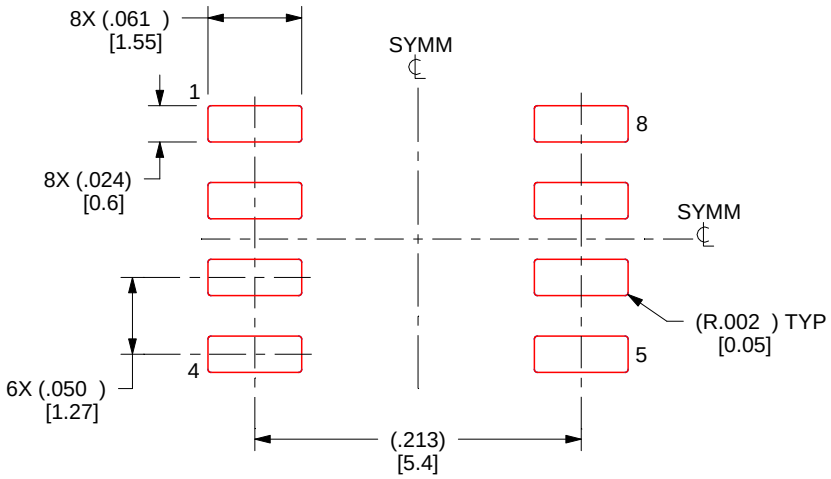
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

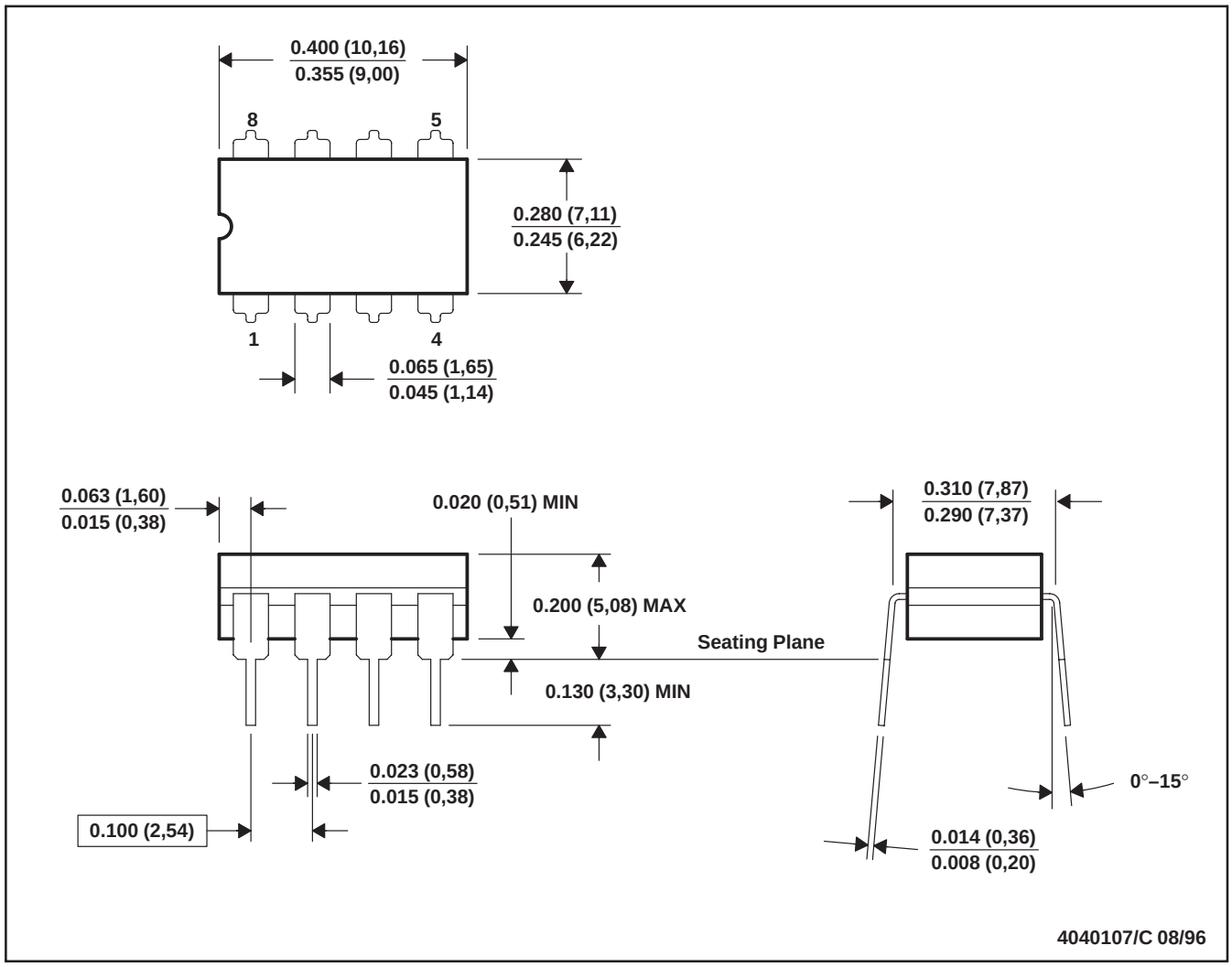
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

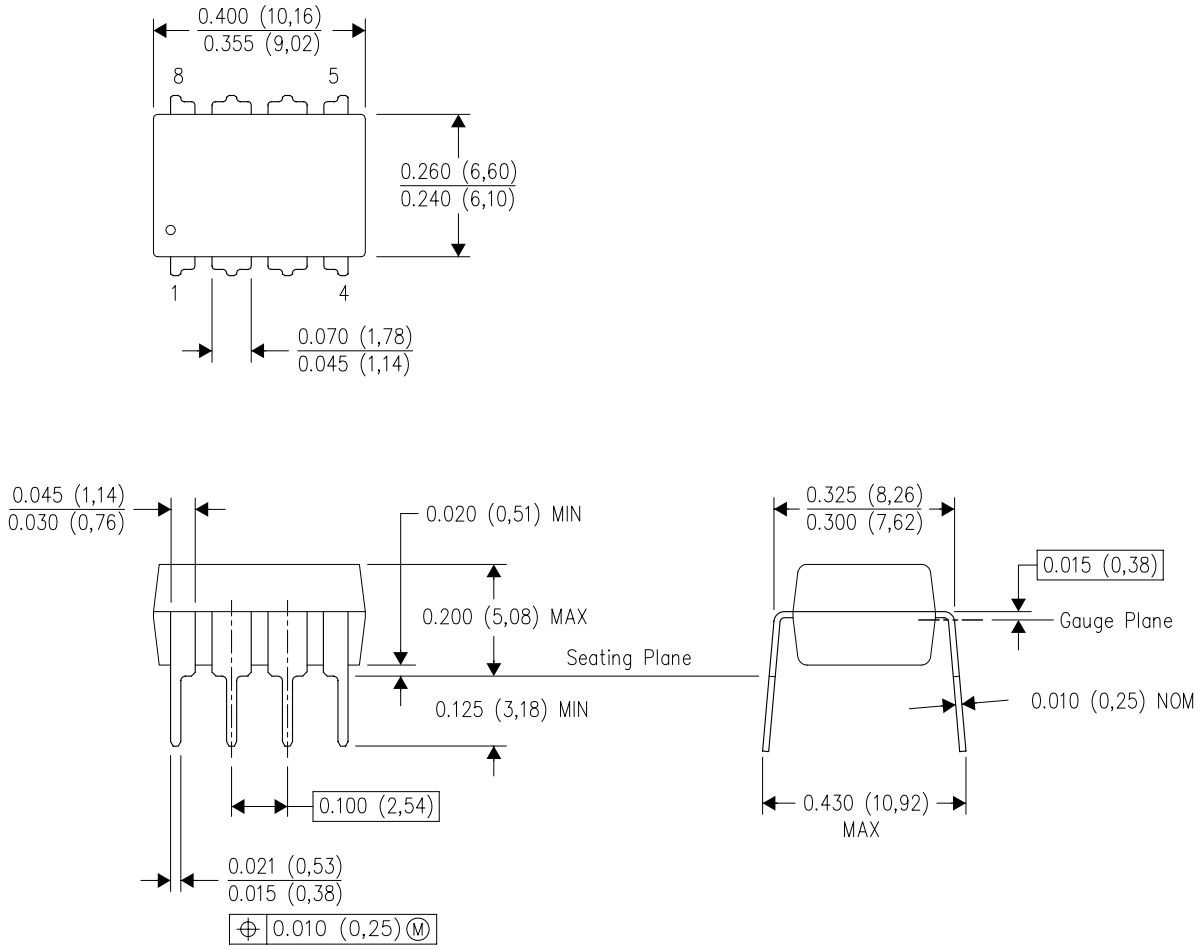
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

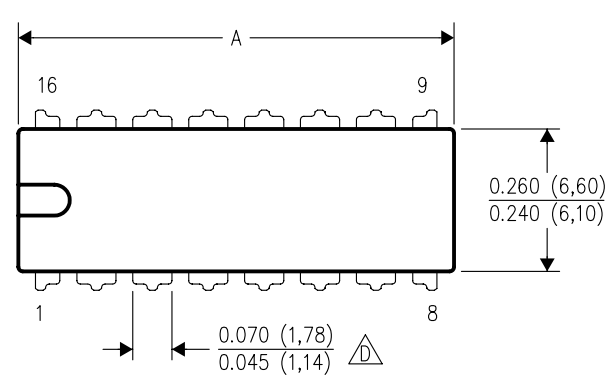


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

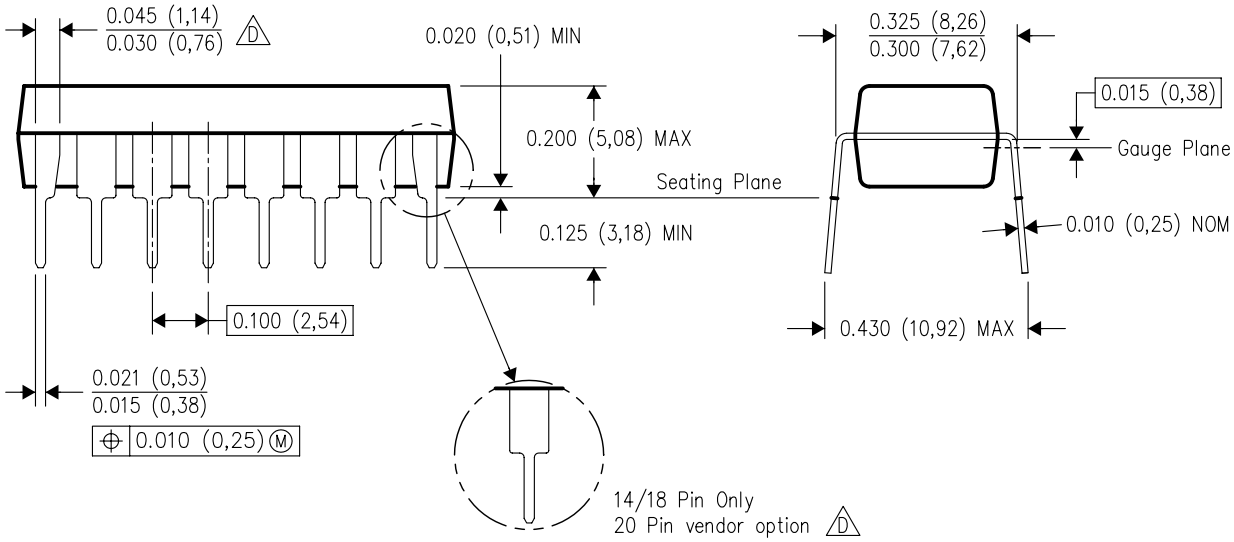
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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