THE DATASHEET OF

TLV2556IPWR

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TLV2556 12-Bit 200-kSPS 11-Channel Low-Power Serial ADC With Internal Reference

1 Features

- 12-Bit Resolution Analog-to-Digital Converter (ADC)
- Up to 200-kSPS (150-kSPS for 3 V) Throughput Over Operating Temperature Range With 12-Bit Output Mode
- 11 Analog Input Channels
- Three Built-In Self-Test Modes
- Inherent Sample and Hold Function
- Programmable Reference Source (2.048 / 4.096 V Internal or External)
- Inherent Sample and Hold Function
- Linearity Error of ±1 LSB (Maximum)
- On-Chip Conversion Clock
- Programmable Conversion Status Output: $\overline{\text{INT}}$ or EOC
- Unipolar or Bipolar Output Operation
- Programmable Most Significant Bit (MSB) or Least Significant Bit (LSB) First
- Programmable Power Down
- Programmable Output Data Length
- SPI-Compatible Serial Interface With I/O Clock Frequencies Up to 15 MHz (CPOL = 0, CPHA = 0)

2 Applications

- Industrial Process Control
- Portable Data Logging
- Battery-Powered Instruments
- Automotive

3 Description

The TLV2556 device is a 12-bit switched-capacitor successive-approximation analog-to-digital converter (ADC). The ADC has three control inputs: chip select ($\overline{\text{CS}}$), the input-output clock, and the address and control input (DATAIN). These inputs communicate with the serial port of a host processor or peripheral through a serial 3-state output.

In addition to the high-speed converter and versatile control capability, the device has an on-chip 14-channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages using configuration register 1. The sample-and-hold function is automatic. At the end of conversion, when programmed as EOC, the pin 19 output goes high to indicate that conversion is complete. If pin 19 is programmed as $\overline{\text{INT}}$, the signal goes low when the conversion is complete. The converter incorporated in the device features differential, high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low error conversion over the full operating temperature range. An internal reference is available and its voltage level is programmable through configuration register 2 (CFGR2).

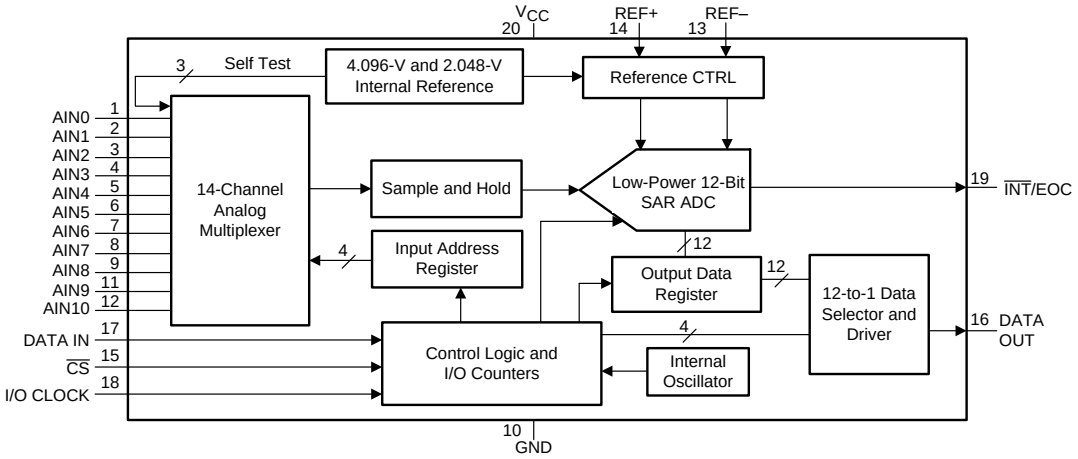
The TLV2556 is characterized for operation from T_A = –40°C to +85°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV2556	SOIC (20)	7.50 mm × 12.80 mm
	TSSOP (20)	4.40 mm × 6.50 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2002) to Revision B	Page
• Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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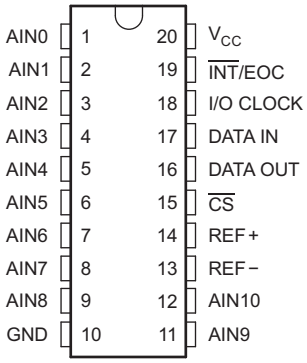
5 Pin Configuration and Functions

DW or PW Package
20-Pin SOIC or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AIN0 to AIN10	1 to 9, 11, 12	I	Analog input. These 11 analog-signal inputs are internally multiplexed.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT, DATA IN, and I/O CLOCK. A low-to-high transition disables DATA IN and I/O CLOCK within a setup time.
DATA IN	17	I	Serial data input. The 4-bit serial data can be used as address selects the desired analog input channel or test voltage to be converted next, or a command to activate other features. The input data is presented with the MSB (D7) first and is shifted in on the first four rising edges of the I/O CLOCK. After the four address/command bits are read into the command register CMR, I/O CLOCK clocks the remaining four bits of configuration in.
DATA OUT	16	O	3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid $\overline{CS}$, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB/LSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB/LSB, and the remaining bits are shifted out in order.
GND	10	—	Ground. GND is the ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
$\overline{INT}$/EOC	19	O	Status output, used to indicate the end of conversion (EOC) or an interrupt ($\overline{INT}$) to host processor. Programmed as $\overline{INT}$ (interrupt): $\overline{INT}$ goes from a high to a low logic level after the conversion is complete and the data is ready for transfer. $\overline{INT}$ is cleared by a rising I/O CLOCK transition. Programmed as EOC: EOC goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and the data is ready for transfer.
I/O CLOCK	18	I	Input /output clock. I/O CLOCK receives the serial input and performs the following four functions: 1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge. 2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of I/O CLOCK. 3. The remaining 11 bits of the previous conversion data are shifted out on DATA OUT. Data changes on the falling edge of I/O CLOCK. 4. Control of the conversion is transferred to the internal state controller on the falling edge of the last I/O CLOCK.
REF+	14	I/O	Positive reference voltage The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum analog input voltage range is determined by the difference between the voltage applied to terminals REF+ and REF–. When the internal reference is used it is capable of driving a 10-kΩ, 10-pF load.
REF–	13	I/O	Negative reference voltage. The lower reference voltage value (nominally ground) is applied to REF–. This pin is connected to analog ground (GND of the ADC) when internal reference is used.
V_{CC}	20	—	Positive supply voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.5	6.5	V
V_I	Input voltage (any input)	–0.3	V_{CC} + 0.3	V
V_O	Output voltage	–0.3	V_{CC} + 0.3	V
V_{ref+}	Positive reference voltage	–0.3	V_{CC} + 0.3	V
$V_{ref–}$	Negative reference voltage	–0.3	V_{CC} + 0.3	V
I_I	Peak input current (any input)	–20	20	mA
	Peak total input current (all inputs)	–30	30	mA
T_J	Operating virtual junction temperature	–40	150	°C
T_A	Operating free-air temperature	–40	85	°C
	Lead temperature 1.6 mm (1/16 inch) from the case for 10 s		260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminal with REF– and GND wired together (unless otherwise noted).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			2.7		5.5	V
	I/O CLOCK frequency	V_{CC} = 4.5 V to 5.5 V	16-bit I/O	0.01		15	MHz
			12-bit I/O	0.01		15	
			8-bit I/O	0.01		15	
		V_{CC} = 2.7 to 3.6 V		0.01		10	
	Tolerable clock jitter, I/O CLOCK	V_{CC} = 4.5 V to 5.5 V				0.38	ns
	Aperature jitter	V_{CC} = 4.5 V to 5.5 V			100		ps
	Analog input voltage(1)	V_{CC} = 4.5 V to 5.5 V		0		REF+ – REF–	V
		V_{CC} = 3 V to 3.6 V		0		REF+ – REF–	
		V_{CC} = 2.7 V to 3 V		0		REF+ – REF–	
V_{IH}	High-level control input voltage	V_{CC} = 4.5 V to 5.5 V		2			V
		V_{CC} = 2.7 V to 3.6 V		2.1			
V_{IL}	Low-level control input voltage	V_{CC} = 4.5 V to 5.5 V				0.8	V
		V_{CC} = 2.7 V to 3.6 V				0.6	
T_A	Operating free-air temperature			–40		85	°C

(1) Analog input voltages greater than the voltage applied to REF+ convert as all ones (111111111111), while input voltages less than the voltage applied to REF– convert as all zeros (000000000000).

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6.4 Thermal Information

THERMAL METRIC[1]		TLV2556 DW (SOIC) 20 PINS	TLV2556 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.0	88.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.4	21.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.7	40.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.3	39.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range, when V_{CC} = 5 V: V_{REF+} = 5 V, I/O CLOCK frequency = 15 MHz, when V_{CC} = 2.7 V: V_{REF+} = 2.5 V, I/O CLOCK frequency = 10 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, I_{OH} = –1.6 mA V_{CC} = 2.7 V, I_{OH} = –0.2 mA	30 pF		2.4			V
		V_{CC} = 4.5 V, I_{OH} = –20 µA V_{CC} = 2.7 V, I_{OH} = –20 µA	30 pF		V_{CC} – 0.1			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 1.6 mA V_{CC} = 2.7 V, I_{OL} = 0.8 mA	30 pF				0.4	V
		V_{CC} = 4.5 V, I_{OL} = 20 µA V_{CC} = 2.7 V, I_{OL} = 20 µA	30 pF				0.1	V
I_{OZ}	High-impedance OFF-state output current	V_O = V_{CC}, $\overline{CS}$ = V_{CC}				1	2.5	µA
		V_O = 0 V, $\overline{CS}$ = V_{CC}				–1	–2.5	µA
I_{CC}	Operating supply current	$\overline{CS}$ = 0 V, External reference	V_{CC} = 5 V				1.2	mA
			V_{CC} = 2.7 V				0.9	mA
		$\overline{CS}$ = 0 V, Internal reference	V_{CC} = 5 V				3	mA
			V_{CC} = 2.7 V				2.4	mA
$I_{CC(PD)}$	Power-down current	For all digital inputs, 0 ≤ V_I ≤ 0.5 V or V_I ≥ V_{CC} – 0.5 V, I/O CLOCK = 0 V	Software power down	Ext. Ref		0.1	1	µA
				Int. Ref		0.1	1	µA
			Auto power down	Ext. Ref		0.1	10	µA
				Int. Ref			1800	µA
I_{IH}	High-level input current	V_I = V_{CC}				0.005	2.5	µA
I_{IL}	Low-level input current	V_I = 0 V				–0.005	–2.5	µA
I_{lkg}	Selected channel leakage current	Selected channel at V_{CC} , Unselected channel at 0 V					1	µA
		Selected channel at 0 V, Unselected channel at V_{CC}					–1	µA
f_{OSC}	Internal oscillator frequency	V_{CC} = 4.5 V to 5.5 V			3.27			MHz
		V_{CC} = 2.7 V to 3.6 V			2.56			MHz
$t_{convert}$	Conversion time (13.5 × (1/f_{OSC}) + 25 ns)	V_{CC} = 4.5 V to 5.5 V					4.15	µs
		V_{CC} = 2.7 V to 3.6 V					5.54	µs
	Internal oscillator frequency switch over voltage				3.6		4.1	V

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

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Electrical Characteristics (continued)

over recommended operating free-air temperature range, when V_{CC} = 5 V: V_{REF+} = 5 V, I/O CLOCK frequency = 15 MHz, when V_{CC} = 2.7 V: V_{REF+} = 2.5 V, I/O CLOCK frequency = 10 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Z_i	Input impedance(2)	Analog inputs	V_{CC} = 4.5 V			600	Ω
			V_{CC} = 2.7 V			500	
C_i	Input capacitance	Analog inputs			45	55	pF
		Control inputs			5	15	

(2) The switch resistance is very nonlinear and varies with input voltage and supply voltage. This is the worst case.

6.6 External Reference Specifications

See (1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{REF-}	Reference input voltage, REF–	V_{CC} = 4.5 V to 5.5 V		–0.1	0	0.1	V
		V_{CC} = 2.7 V to 3.6 V		–0.1	0	0.1	
V_{REF+}	Reference input voltage, REF+	V_{CC} = 4.5 V to 5.5 V		2		V_{CC}	V
		V_{CC} = 2.7 V to 3.6 V		2		V_{CC}	
	External reference input voltage difference (REF+ – REF–)	V_{CC} = 4.5 V to 5.5 V		1.9		V_{CC}	V
		V_{CC} = 2.7 V to 3.6 V		1.9		V_{CC}	
I_{REF}	External reference supply current	$\overline{CS}$ = 0 V	V_{CC} = 4.5 V to 5.5 V			1	mA
			V_{CC} = 2.7 V to 3.6 V			0.7	
Z_{REF}	Reference input impedance	V_{CC} = 5 V	Static	1			MΩ
			During sampling or conversion	6		9	kΩ
		V_{CC} = 2.7 V	Static	1			MΩ
			During sampling or conversion	6		9	kΩ

(1) Add a 0.1-µF capacitor between REF+ and REF– pins when external reference is used.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.

6.7 Internal Reference Specifications

See (1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP(4)	MAX	UNIT
V_{REF-}	Reference input voltage, REF–	V_{CC} = 2.7 V to 5.5 V, REF- = Analog GND			0		V
	Internal reference delta voltage, (REF+ – REF–)	V_{CC} = 5.5 V	Internal 4.096 V selected	3.95	4.065	4.25	V
			Internal 2.048 V selected	1.95	2.019	2.1	
		V_{CC} = 2.7 V	Internal 2.048 V selected	1.95	2.019	2.1	
	Internal reference start-up time	V_{CC} = 5 V	With 10-µF load		20		ms
		V_{CC} = 2.7 V			20		
	Internal reference temperature coefficient	V_{CC} = 2.7 V to 5.5 V			±50		ppm/°C

(1) Add a 0.1-µF capacitor between REF+ and REF– pins when external reference is used.
(2) Add a 0.1-µF capacitor between REF+ and REF– pins.
(3) REF- must be connected to analog GND (the ground of the ADC).
(4) All typical values are at V_{CC} = 5 V, T_A = 25°C.

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6.8 Operating Characteristics

over recommended operating free-air temperature range, when V_{CC} = 5 V: V_{REF+} = 5 V, I/O CLOCK frequency = 15 MHz, when V_{CC} = 2.7 V: V_{REF+} = 2.5 V, I/O CLOCK frequency = 10 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
INL	Integral linearity error(2)		–1		1	LSB
DNL	Differential linearity error		–1		1	LSB
E_O	Offset error(3)	See (4)	–2		2	mV
E_G	Gain error(3)	See (4)	–3		3	mV
E_T	Total unadjusted error(5)			±1.5		LSB
	Self-test output code(6)	Address data input = 1011		2048		
		Address data input = 1100		0		
		Address data input = 1101		4095		

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
(3) Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep value at the offset point.
(4) Analog input voltages greater than the voltage applied to REF+ convert as all ones (111111111111), while input voltages less than the voltage applied to REF– convert as all zeros (000000000000).
(5) Total unadjusted error comprises linearity, zero-scale errors, and full-scale errors.
(6) Both the input address and the output codes are expressed in positive logic.

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6.9 Timing Requirements, V_{REF+} = 5 V

over recommended operating free-air temperature range,
V_{REF+} = 5 V, I/O CLOCK frequency = 15 MHz, V_{CC} = 5 V, Load = 25 pF (unless otherwise noted)

			MIN	MAX	UNIT
t_{w1}	Pulse duration I/O CLOCK high or low		26.7	100000	ns
t_{su1}	Set-up time DATA IN valid before I/O CLOCK rising edge (see Figure 47)		12		ns
t_{h1}	Hold time DATA IN valid after I/O CLOCK rising edge (see Figure 47)		0		ns
t_{su2}	Setup time $\overline{CS}$ low before first rising I/O CLOCK edge(1) (see Figure 48)		25		ns
t_{h2}	Hold time $\overline{CS}$ pulse duration high time (see Figure 48)		100		ns
t_{h3}	Hold time $\overline{CS}$ low after last I/O CLOCK falling edge (see Figure 48)		0		ns
t_{h4}	Hold time DATA OUT valid after I/O CLOCK falling edge (see Figure 49)		2		ns
t_{h5}	Hold time $\overline{CS}$ high after EOC rising edge when $\overline{CS}$ is toggled (see Figure 52)		0		ns
t_{h6}	Hold time $\overline{CS}$ high after $\overline{INT}$ falling edge (seeFigure 52)		0		ns
t_{h7}	Hold time I/O CLOCK low after EOC rising edge or $\overline{INT}$ falling edge when $\overline{CS}$ is held low (seeFigure 53)		10		ns
t_{d1}	Delay time $\overline{CS}$ falling edge to DATA OUT valid (MSB or LSB) (see Figure 46)	Load = 25 pF		28	ns
		Load = 10 pF		20	
t_{d2}	Delay time $\overline{CS}$ rising edge to DATA OUT high impedance (see Figure 46)			10	ns
t_{d3}	Delay time I/O CLOCK falling edge to next DATA OUT bit valid (see Figure 49)		2	20	ns
t_{d4}	Delay time last I/O CLOCK falling edge to EOC falling edge (seeFigure 50)			55	ns
t_{d5}	Delay time last I/O CLOCK falling edge to $\overline{CS}$ falling edge to abort conversion			1.5	µs
t_{d6}	Delay time last I/O CLOCK falling edge to $\overline{INT}$ falling edge (see Figure 50)			$t_{convert}$(max)	ns
t_{d7}	Delay time EOC rising edge or $\overline{INT}$ falling edge to DATA OUT valid: MSB or LSB 1st (see Figure 51)			4	ns
t_{d9}	Delay time I/O CLOCK high to $\overline{INT}$ rising edge when $\overline{CS}$ is held low (see Figure 53)		1	28	ns
t_{t1}	Transition time I/O CLOCK(1) (see Figure 49)			1	µs
t_{t2}	Transition time DATA OUT (see Figure 49)			5	ns
t_{t3}	Transition time $\overline{INT}$/EOC, C_L = 7 pF (see Figure 50 and Figure 51)			2.4	ns
t_{t4}	Transition time DATA IN, $\overline{CS}$			10	µs
t_{cycle}	Total cycle time (sample, conversion and delays)(1)			See (2)	µs
t_{sample}	Channel acquisition time (sample) at 1 kΩ(1) (see Figure 1 through Figure 6)	Source impedance = 25 Ω	600		ns
		Source impedance = 100 Ω	650		
		Source impedance = 500 Ω	700		
		Source impedance = 1 kΩ	1000		

(1) I/O CLOCK period = 8 × [1/(I/O CLOCK frequency)] or 12 × [1/(I/O CLOCK frequency)] or 16 × [1/(I/O CLOCK frequency)], depending on I/O format selected
(2) $t_{convert}$(max) + I/O CLOCK period (8/12/16 CLKs)(1)

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6.10 Timing Requirements, V_{REF+} = 2.5 V

over recommended operating free-air temperature range,
V_{REF+} = 2.5 V, I/O CLOCK frequency = 10 MHz, V_{CC} = 2.7 V, Load = 25 pF (unless otherwise noted)

			MIN	MAX	UNIT
t_{w1}	Pulse duration I/O CLOCK high or low		40	100000	ns
t_{su1}	Set-up time DATA IN valid before I/O CLOCK rising edge (see Figure 47)		22		ns
t_{h1}	Hold time DATA IN valid after I/O CLOCK rising edge (see Figure 47)		0		ns
t_{su2}	Setup time $\overline{CS}$ low before first rising I/O CLOCK edge(1) (see Figure 48)		33		ns
t_{h2}	Hold time $\overline{CS}$ pulse duration high time (see Figure 48)		100		ns
t_{h3}	Hold time $\overline{CS}$ low after last I/O CLOCK falling edge (see Figure 48)		0		ns
t_{h4}	Hold time DATA OUT valid after I/O CLOCK falling edge (see Figure 49)		2		ns
t_{h5}	Hold time $\overline{CS}$ high after EOC rising edge when $\overline{CS}$ is toggled (see Figure 52)		0		ns
t_{h6}	Hold time $\overline{CS}$ high after $\overline{INT}$ falling edge (see Figure 52)		0		ns
t_{h7}	Hold time I/O CLOCK low after EOC rising edge or $\overline{INT}$ falling edge when $\overline{CS}$ is held low (see Figure 53)		10		ns
t_{d1}	Delay time $\overline{CS}$ falling edge to DATA OUT valid (MSB or LSB) (see Figure 46)	Load = 25 pF		30	ns
		Load = 10 pF		22	
t_{d2}	Delay time $\overline{CS}$ rising edge to DATA OUT high impedance (see Figure 46)			10	ns
t_{d3}	Delay time I/O CLOCK falling edge to next DATA OUT bit valid (see Figure 49)		2	33	ns
t_{d4}	Delay time last I/O CLOCK falling edge to EOC falling edge (see Figure 50)			75	ns
t_{d5}	Delay time last I/O CLOCK falling edge to $\overline{CS}$ falling edge to abort conversion			1.5	µs
t_{d6}	Delay time last I/O CLOCK falling edge to $\overline{INT}$ falling edge (see Figure 50)			$t_{convert}$(max)	ns
t_{d7}	Delay time EOC rising edge or $\overline{INT}$ falling edge to DATA OUT valid: MSB or LSB 1st (see Figure 51)			20	ns
t_{d9}	Delay time I/O CLOCK high to $\overline{INT}$ rising edge when $\overline{CS}$ is held low (see Figure 53)			55	ns
t_{t1}	Transition time I/O CLOCK(1) (see Figure 49)			1	µs
t_{t2}	Transition time DATA OUT (see Figure 49)			5	ns
t_{t3}	Transition time $\overline{INT}$/EOC, C_L = 7 pF (see Figure 50 and Figure 51)			4	ns
t_{t4}	Transition time DATA IN, $\overline{CS}$			10	µs
t_{cycle}	Total cycle time (sample, conversion and delays)(1)			See (2)	µs
t_{sample}	Channel acquisition time (sample), at 1 kΩ(1) (see Figure 1 through Figure 6)	Source impedance = 25 Ω	800		ns
		Source impedance = 100 Ω	850		
		Source impedance = 500 Ω	1000		
		Source impedance = 1 kΩ	1600		

(1) I/O CLOCK period = 8 × [1/(I/O CLOCK frequency)] or 12 × [1/(I/O CLOCK frequency)] or 16 × [1/(I/O CLOCK frequency)], depending on I/O format selected
(2) $t_{convert}$(max) + I/O CLOCK period (8/12/16 CLKs)()

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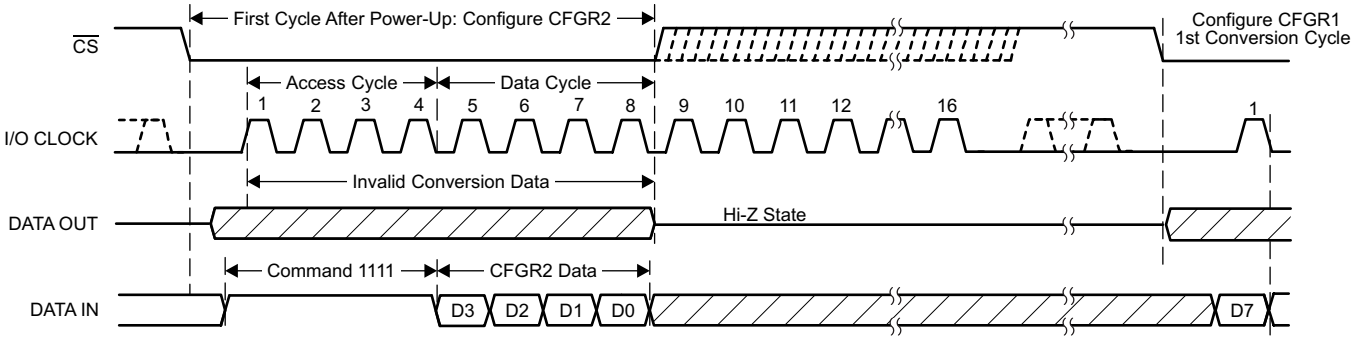
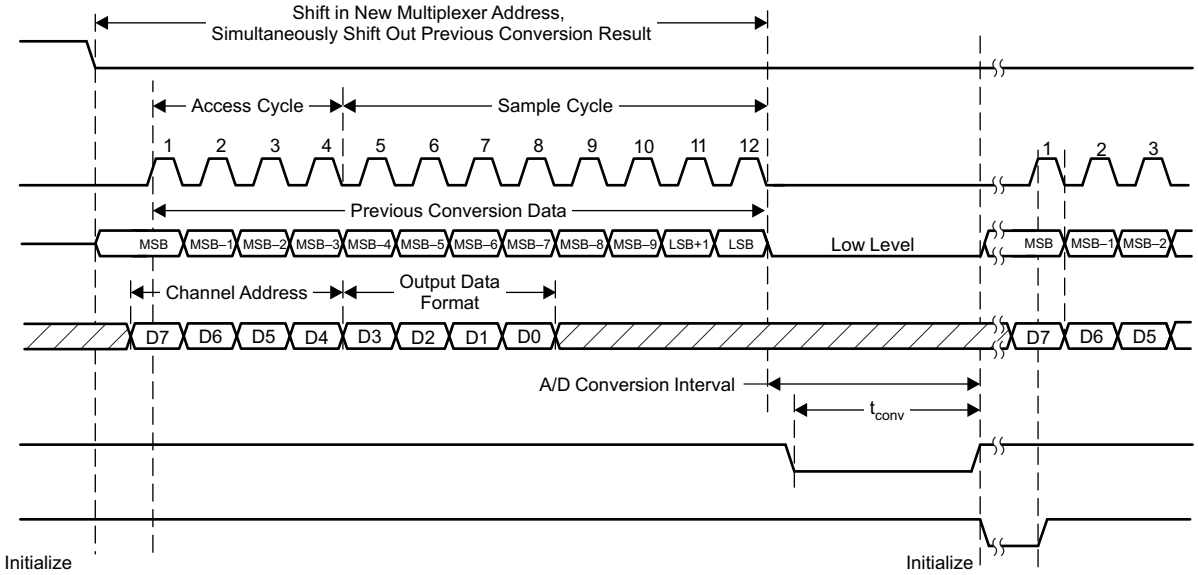


NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set-up time after the $\overline{CS}$ falling edge before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 1. Timing for CFGR2 Configuration

The host must configure CFGR2 before valid device conversions can begin. This can be accessed through command 1111. This can be done using eight, twelve, or sixteen I/O CLOCK clocks. (A minimum of eight is required to fully program CFGR2.)

After CFGR2 is configured, the following cycle configures CFGR1 and a valid sample or conversion is performed. $\overline{CS}$ can be held low for each remaining cycle. First valid conversion output data is available on the third cycle after power up.



NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set-up time after the $\overline{CS}$ falling edge before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 2. Timing for 12-Clock Transfer Not Using $\overline{CS}$ With DATA OUT Set for MSB First

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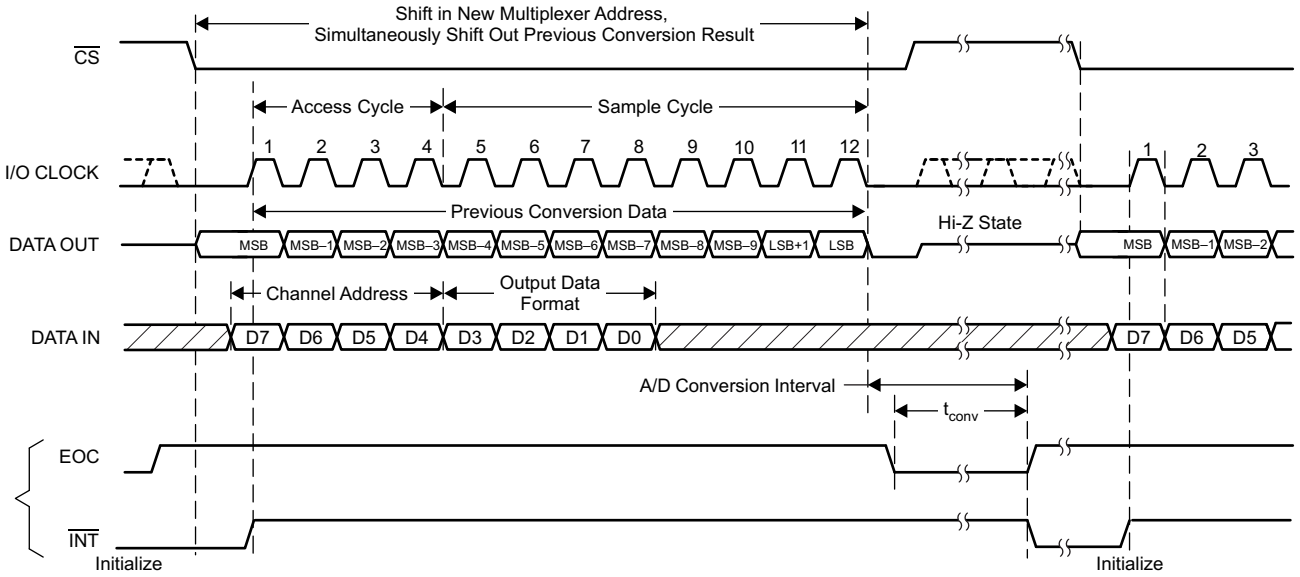
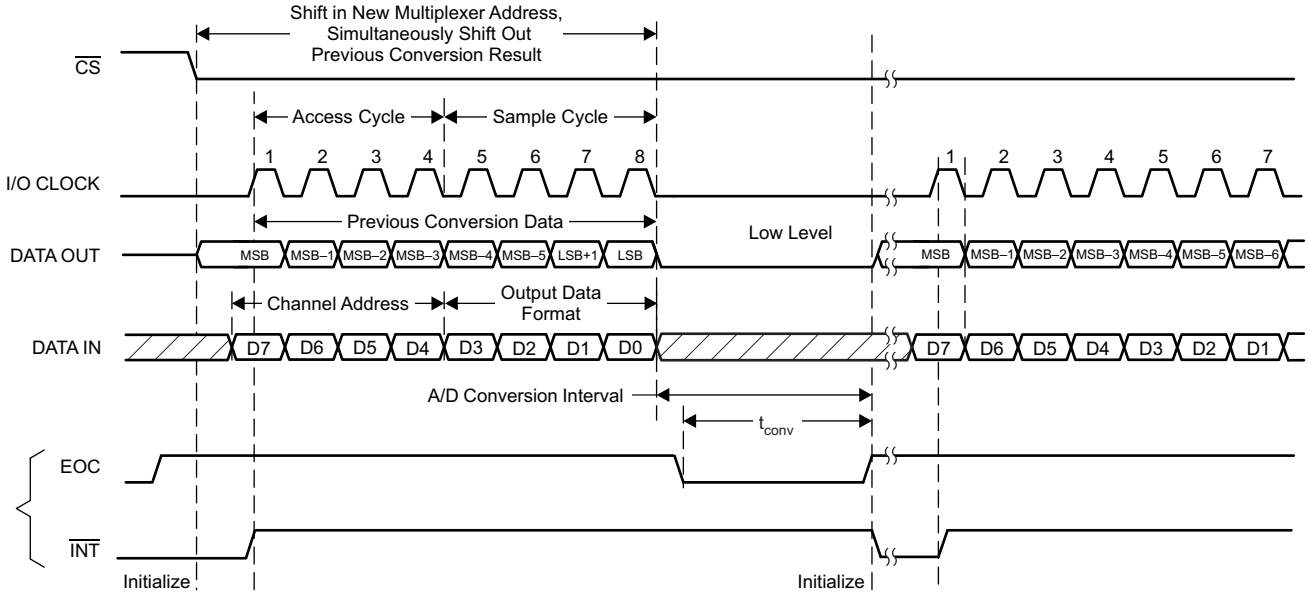


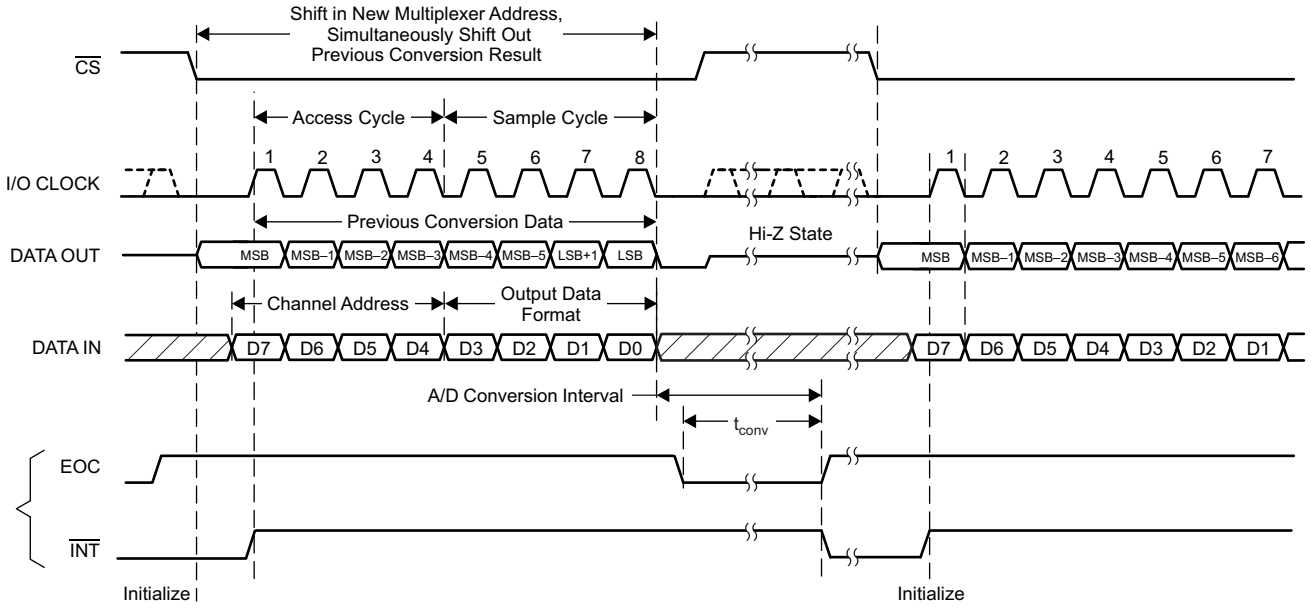
NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set-up time after the $\overline{CS}$ falling edge before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 3. Timing for 12-Clock Transfer Using $\overline{CS}$ With DATA OUT Set for MSB First



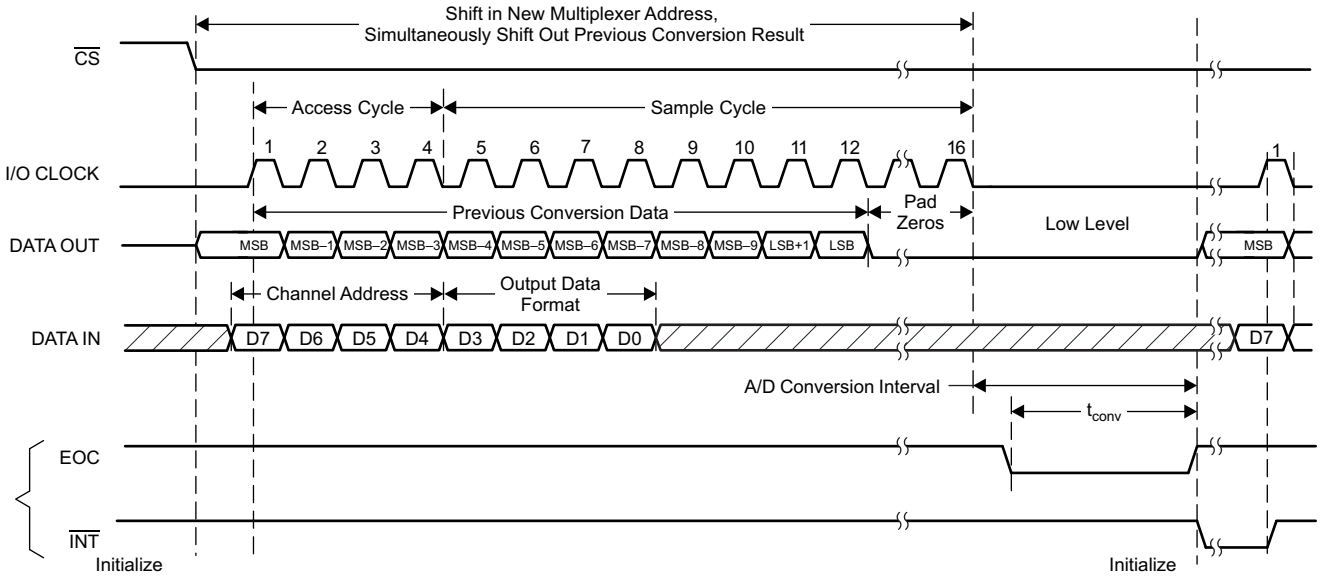
NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set-up time after the $\overline{CS}$ falling edge before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 4. Timing for 8-Clock Transfer Not Using $\overline{CS}$ With DATA OUT Set for MSB First



NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set-up time after the $\overline{CS}$ falling edge before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 5. Timing for 8-Clock Transfer Using $\overline{CS}$ With DATA OUT Set for MSB First



NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set-up time after the $\overline{CS}$ falling edge before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 6. Timing for 16-Clock Transfer Not Using $\overline{CS}$ With DATA OUT Set for MSB First

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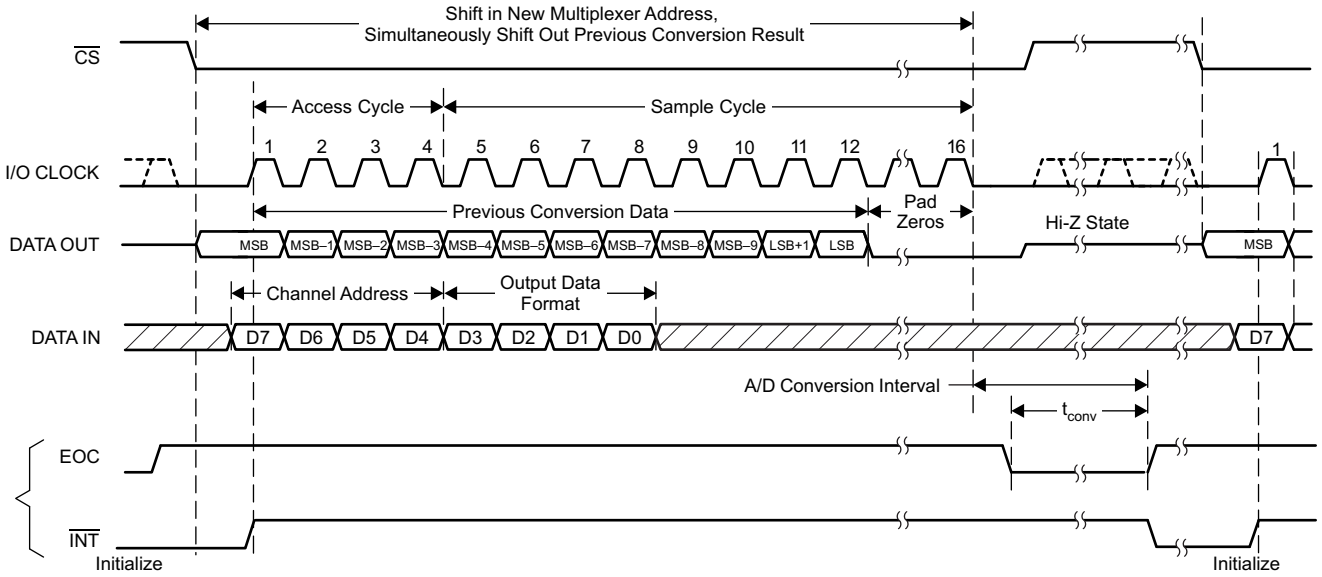
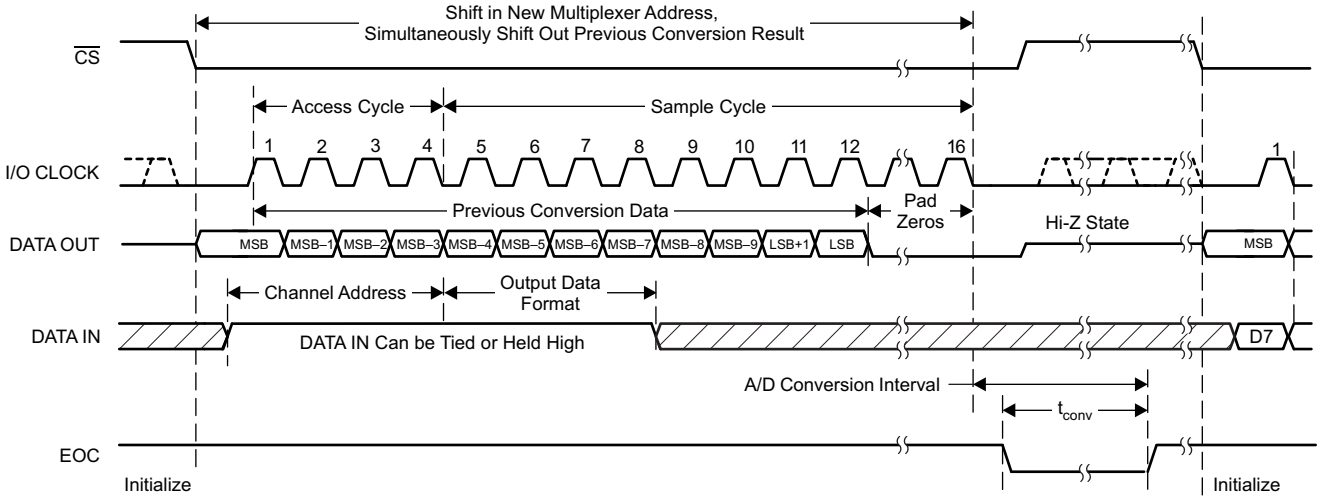


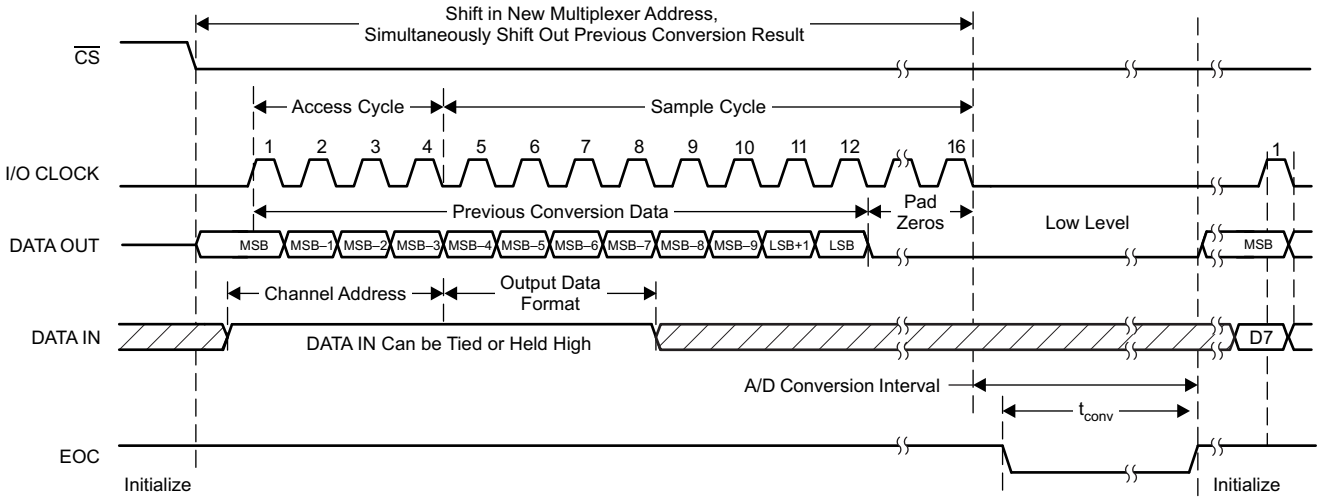
NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set-up time after the $\overline{CS}$ falling edge before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 7. Timing for 16-Clock Transfer Using $\overline{CS}$ With DATA OUT Set for MSB First



NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set-up time after the $\overline{CS}$ falling edge before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 8. Timing for Default Mode Using $\overline{CS}$: (16-Clock Transfer, MSB First, Ext. Ref, Pin 19 = EOC, Input = AIN0)



NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a set-up time after the $\overline{CS}$ falling edge before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

Figure 9. Timing for Default Mode Not Using $\overline{CS}$:(16-Clock Transfer, MSB First Ext. Ref, Pin 19 = EOC, Input = AIN0)

To remove the device from default mode, CFGR2 – D0 must be reset to 0. Valid sample or convert cycles can resume on the cycle following the CFGR2 configuration.

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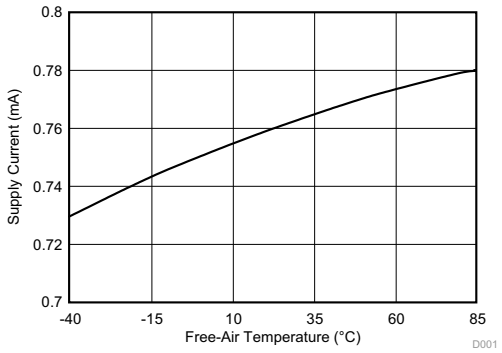
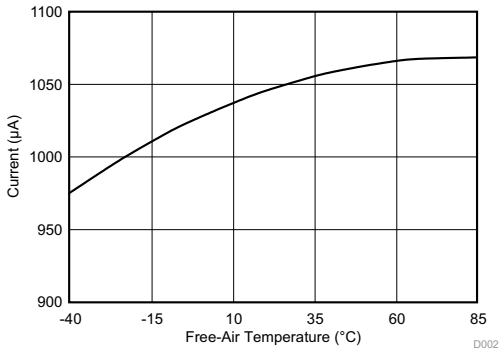
6.11 Typical Characteristics

V_{REF-} = 0 V



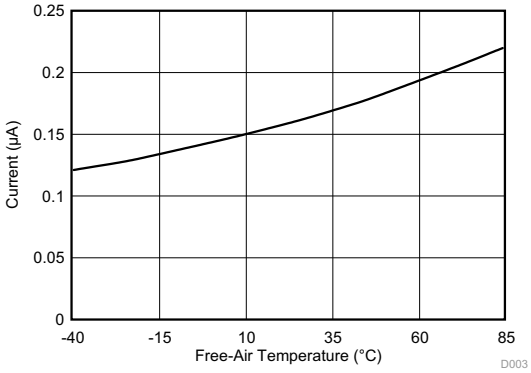
V_{CC} = 3.3 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS

Figure 10. Supply Current vs Free-Air Temperature



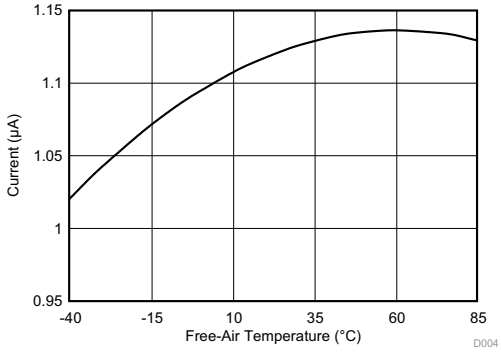
V_{CC} = 3.3 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS

Figure 11. Auto Power Down vs Free-Air Temperature



V_{CC} = 3.3 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS

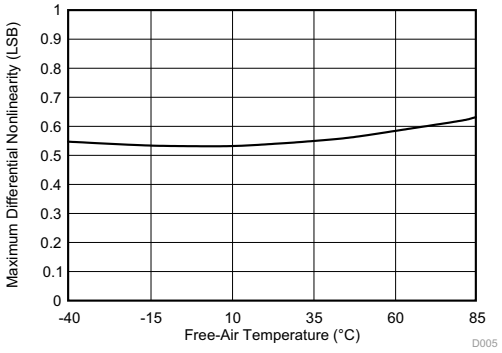
Figure 12. Software Power Down vs Free-Air Temperature



\

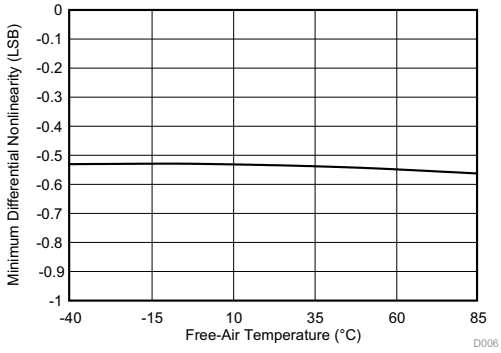
V_{CC} = 3.3 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS

Figure 13. 2.048-V Internal Reference Current vs Free-Air Temperature



V_{CC} = 2.7 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS

Figure 14. Maximum Differential Nonlinearity vs Free-Air Temperature



V_{CC} = 2.7 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS

Figure 15. Minimum Differential Nonlinearity vs Free-Air Temperature

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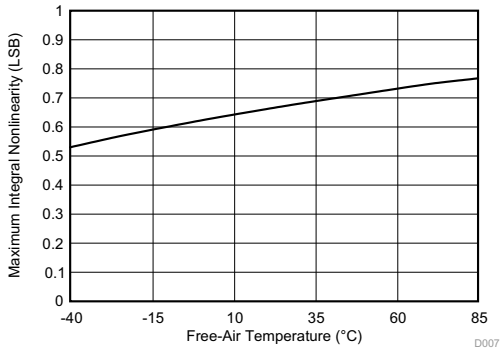
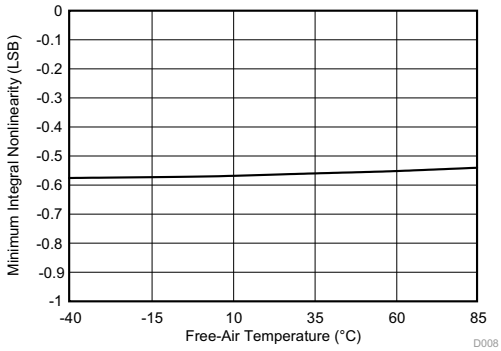
Typical Characteristics (continued)

V_{REF-} = 0 V



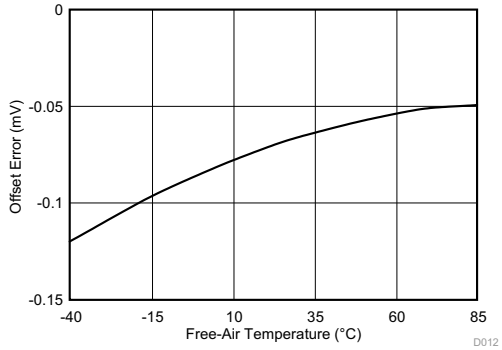
V_{CC} = 2.7 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS

Figure 16. Maximum Integral Nonlinearity vs Free-Air Temperature



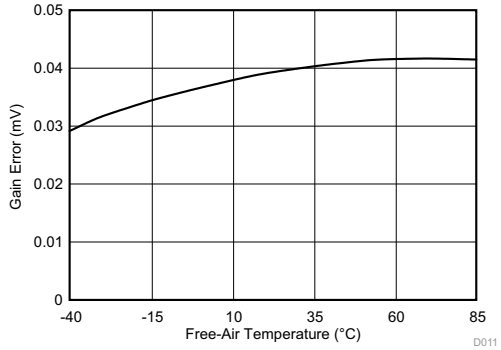
V_{CC} = 2.7 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS

Figure 17. Minimum Integral Nonlinearity vs Free-Air Temperature



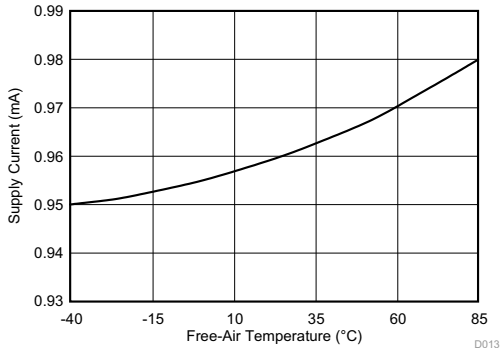
V_{CC} = 3.3 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS

Figure 18. Offset Error vs Free-Air Temperature



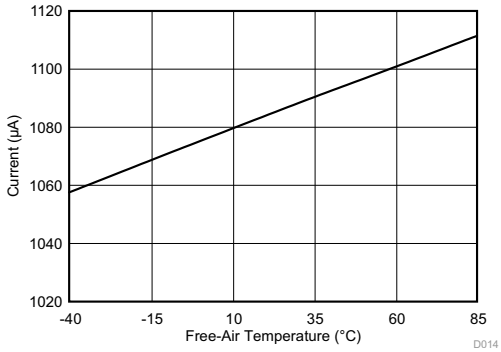
V_{CC} = 3.3 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS

Figure 19. Gain Error vs Free-Air Temperature



V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 20. Supply Current vs Free-Air Temperature



V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 21. Auto Power Down vs Free-Air Temperature

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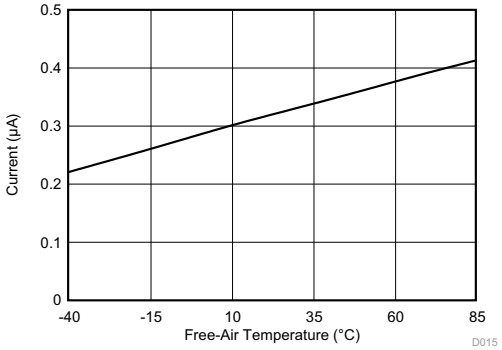
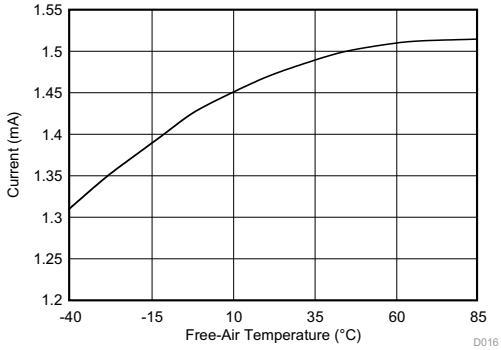
Typical Characteristics (continued)

$V_{REF–}$ = 0 V



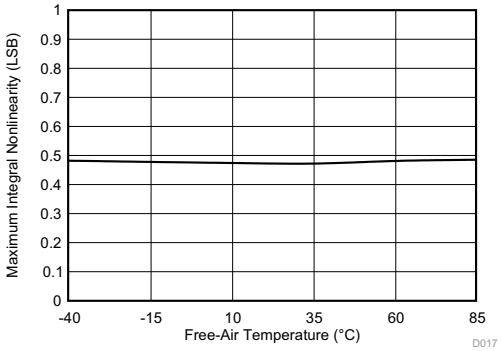
V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 22. Software Power Down vs Free-Air Temperature



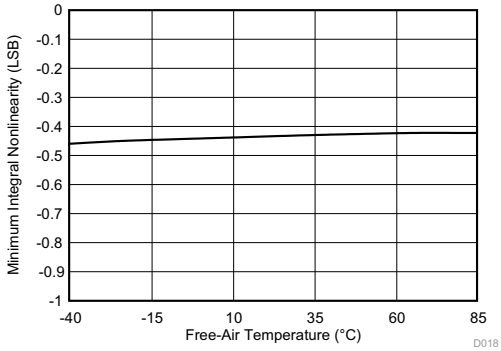
V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 23. 4.096 V Internal Reference Current vs Free-Air Temperature



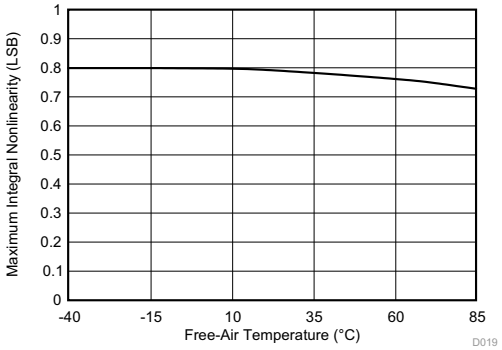
V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 24. Maximum Differential Nonlinearity vs Free-Air Temperature



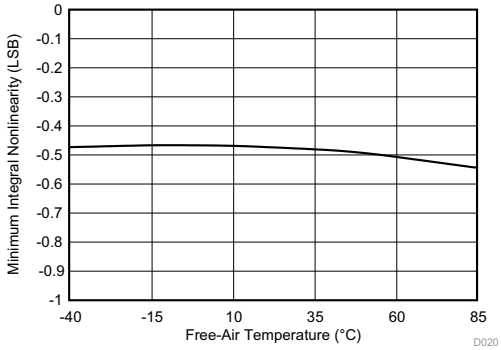
V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 25. Minimum Differential Nonlinearity vs Free-Air Temperature



V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 26. Maximum Integral Nonlinearity vs Free-Air Temperature

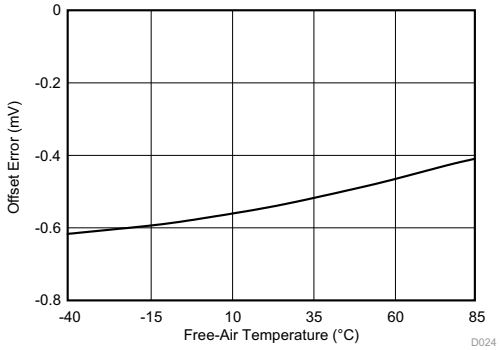


V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 27. Minimum Integral Nonlinearity vs Free-Air Temperature

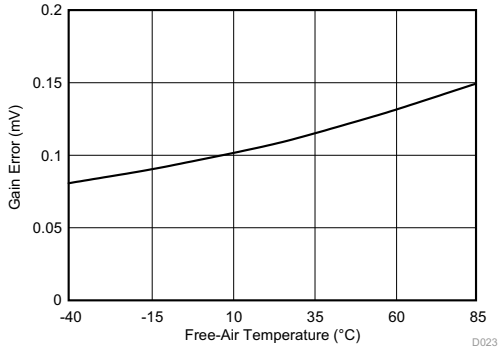
Typical Characteristics (continued)

V_{REF-} = 0 V



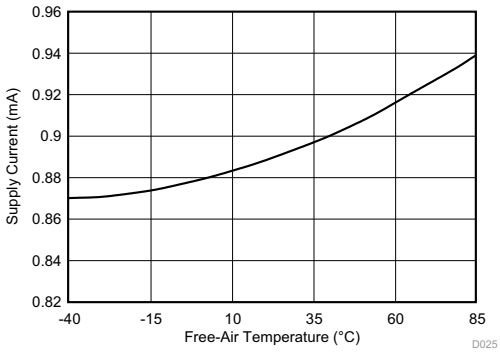
V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 28. Offset Error vs Free-Air Temperature



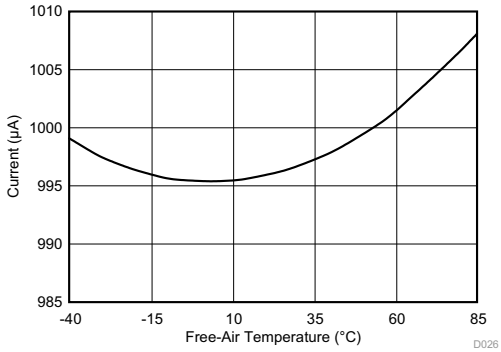
V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 29. Gain Error vs Free-Air Temperature



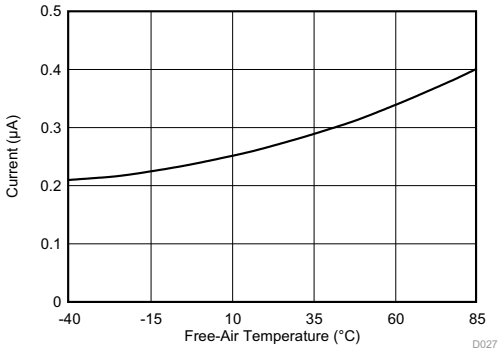
V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 30. Supply Current vs Free-Air Temperature



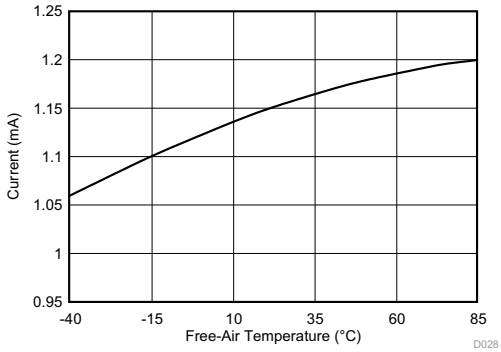
V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 31. Auto Power Down vs Free-Air Temperature



V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 32. Software Power Down vs Free-Air Temperature



V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 33. Internal Reference Current vs Free-Air Temperature

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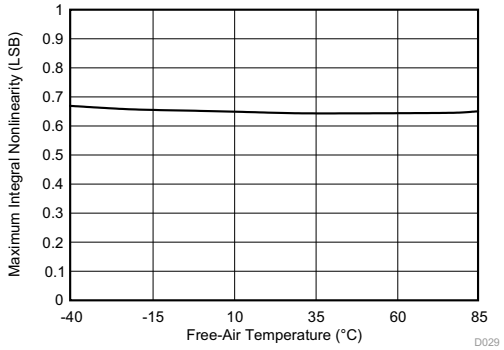
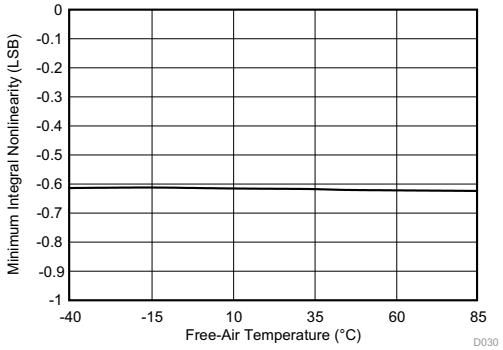
Typical Characteristics (continued)

V_{REF-} = 0 V



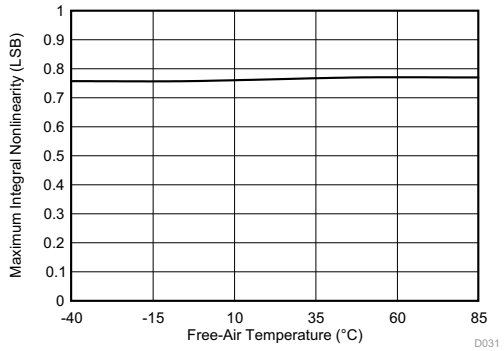
V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 34. Maximum Differential Nonlinearity vs Free-Air Temperature



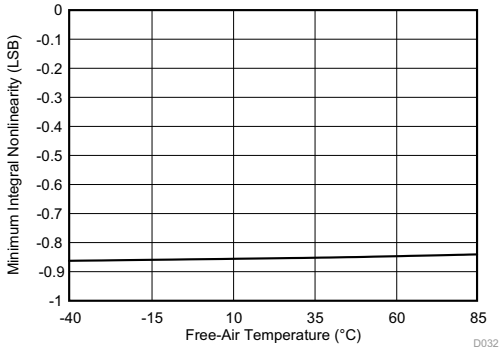
V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 35. Minimum Differential Nonlinearity vs Free-Air Temperature



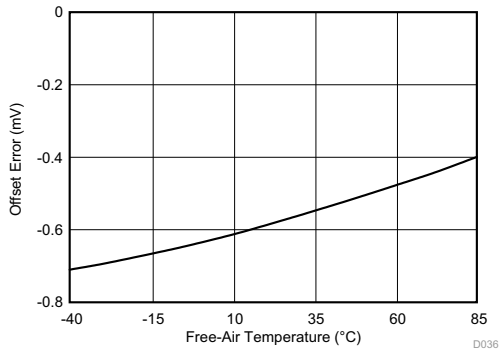
V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 36. Maximum Integral Nonlinearity vs Free-Air Temperature



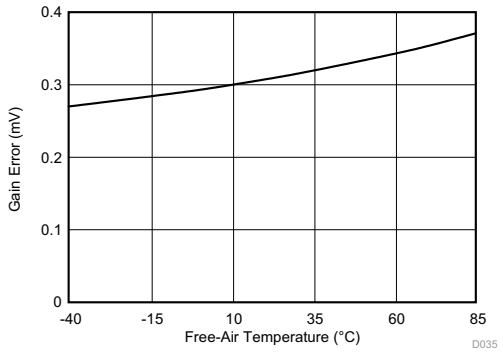
V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 37. Minimum Integral Nonlinearity vs Free-Air Temperature



V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 38. Offset Error vs Free-Air Temperature



V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS

Figure 39. Gain Error vs Free-Air Temperature

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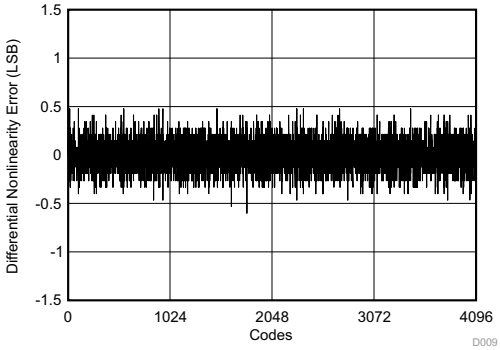
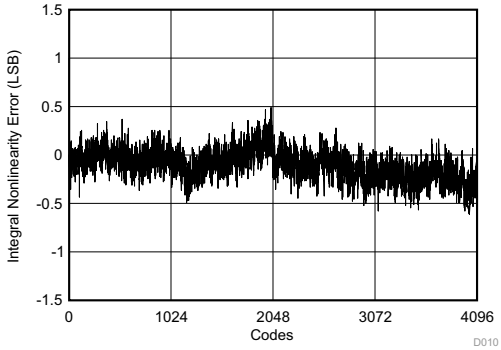
Typical Characteristics (continued)

V_{REF-} = 0 V



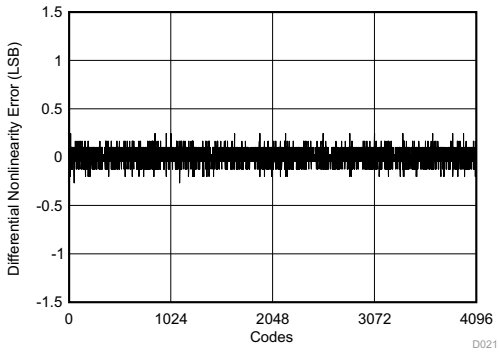
V_{CC} = 2.7 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS T_A = 25°C

Figure 40. Differential Nonlinearity vs Digital Output Code



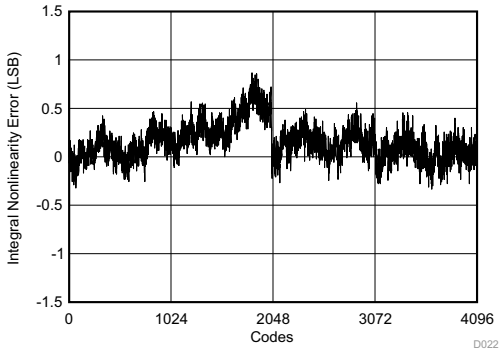
V_{CC} = 2.7 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 150 kSPS T_A = 25°C

Figure 41. Integral Nonlinearity vs Digital Output Code



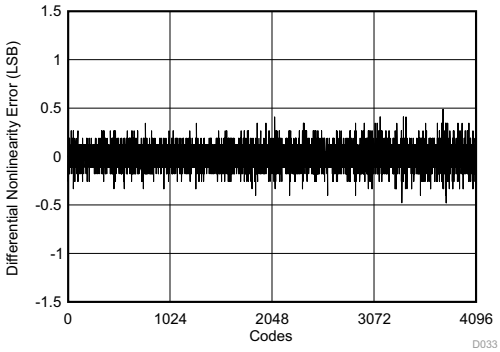
V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS T_A = 25°C

Figure 42. Differential Nonlinearity vs Digital Output Code



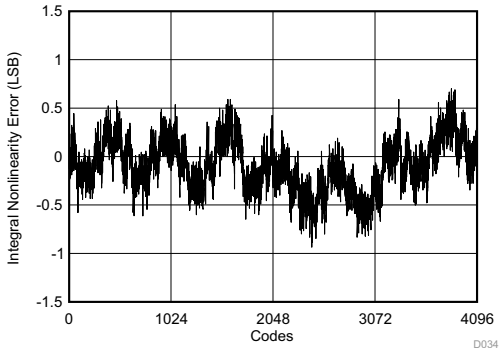
V_{CC} = 5.5 V V_{REF+} = 4.096 V V_{REF-} = 0 V
I/O clock = 15 MHz f_{SAMP} = 200 kSPS T_A = 25°C

Figure 43. Integral Nonlinearity vs Digital Output Code



V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 200 kSPS T_A = 25°C

Figure 44. Differential Nonlinearity vs Digital Output Code



V_{CC} = 5.5 V V_{REF+} = 2.048 V V_{REF-} = 0 V
I/O clock = 10 MHz f_{SAMP} = 200 kSPS T_A = 25°C

Figure 45. Integral Nonlinearity vs Digital Output Code

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7 Parameter Measurement Information

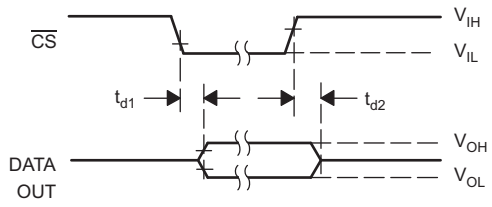

Figure 46. DATA OUT to Hi-Z Voltage Waveforms

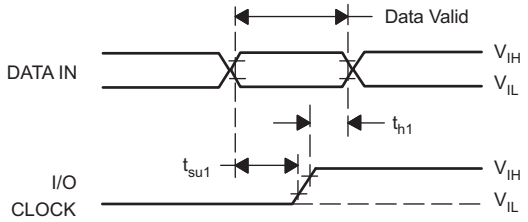

Figure 47. DATA IN and I/O CLOCK Voltage

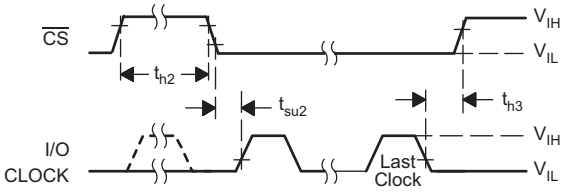

Figure 48. $\overline{CS}$ and I/O CLOCK Voltage Waveforms

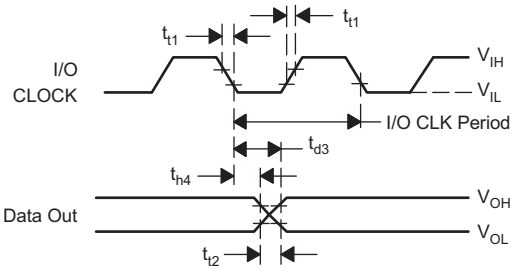

Figure 49. I/O CLOCK and DATA OUT Voltage Waveforms

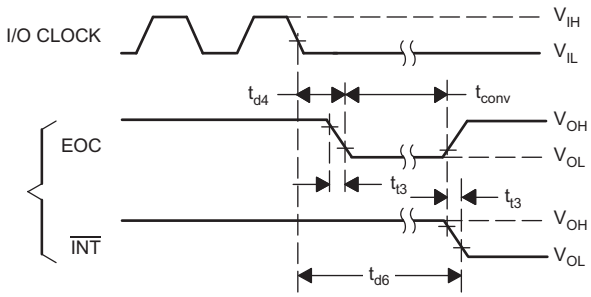

Figure 50. I/O CLOCK and EOC Voltage Waveforms

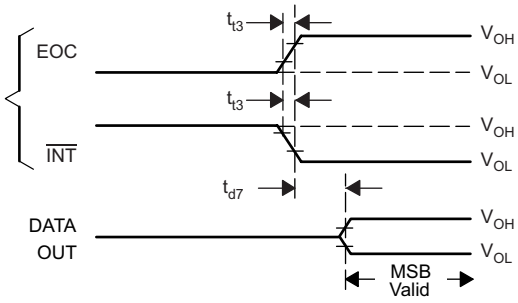

Figure 51. EOC and DATA OUT Voltage Waveforms

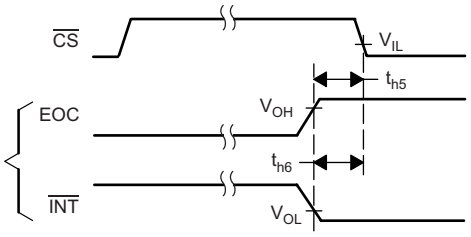

Figure 52. $\overline{CS}$ and EOC Waveforms

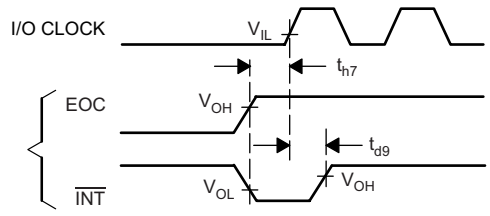

Figure 53. I/O CLOCK and EOC Voltage Waveforms

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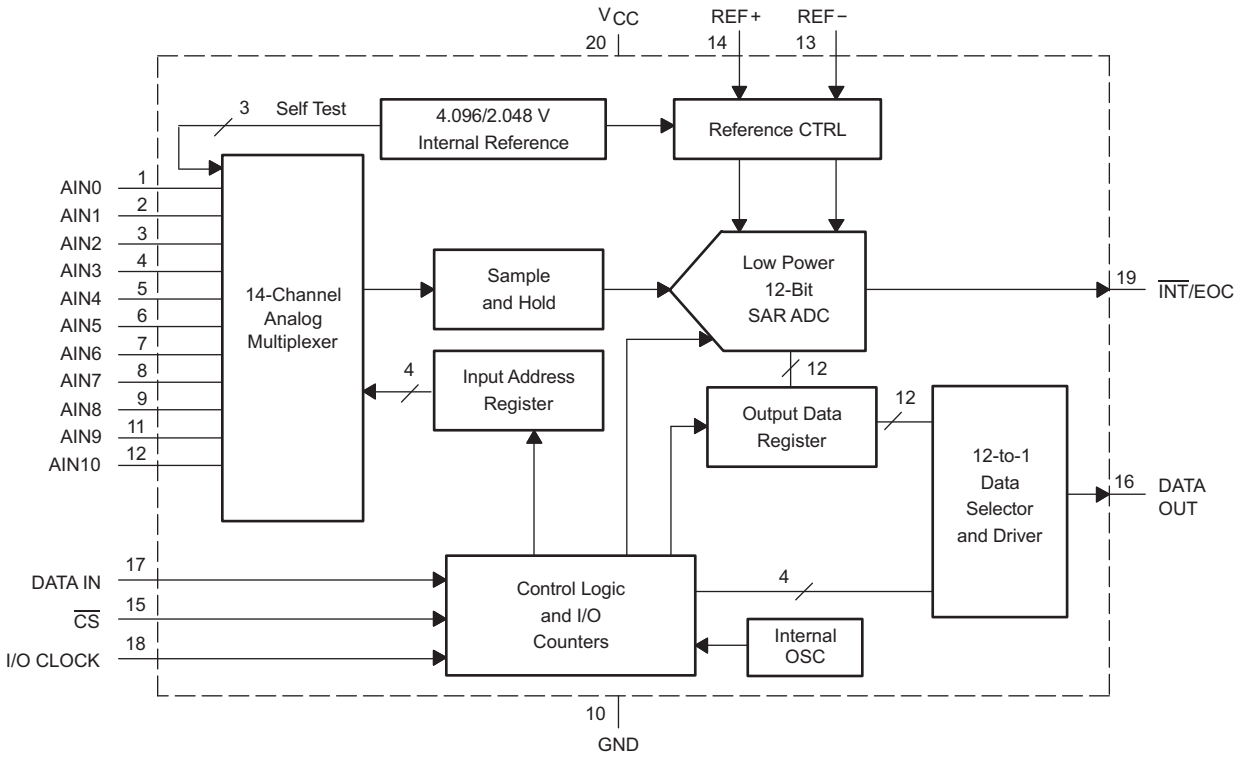
8 Detailed Description

8.1 Overview

Initially, with chip select ($\overline{CS}$) high, I/O CLOCK and DATA IN are disabled and DATA OUT is in the high-impedance state. $\overline{CS}$ going low begins the conversion sequence by enabling I/O CLOCK and DATA IN and removes DATA OUT from the high-impedance state. The input data is an 8-bit data stream consisting of a 4-bit address or command (D7–D4) and a 4-bit configuration data (D3–D0). There are two sets of configuration registers, configuration register 1 – CFGR1 and configuration register 2 – CFGR2. CFGR1, which controls output data format configuration, consists of a 2-bit data length select (D3–D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0) that are applied to any command (from DATA IN) except for command 1111b. CFGR2, which provides configuration information other than data format, consists of a 2-bit reference select (D3–D2), an EOC/$\overline{INT}$ program bit (D1), and a default mode select bit (D0) that are applied to command 1111b. The I/O CLOCK sequence applied to the I/O CLOCK terminal transfers this data to the input data register. During this transfer, the I/O CLOCK sequence also shifts the previous conversion result from the output data register to DATA OUT. I/O CLOCK receives the input sequence of 8, 12, or 16 clock cycles long depending on the data-length selection in the input data register. Sampling of the analog input begins on the fourth falling edge of the input I/O CLOCK sequence and is held after the last falling edge of the I/O CLOCK sequence. The last falling edge of the I/O CLOCK sequence also takes EOC low (if pin 19 = EOC) and begins the conversion.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Converter Operation

The operation of the converter is organized as a succession of three distinct cycles: 1) the data I/O cycle, 2) the sampling cycle, and 3) the conversion cycle. The first two are partially overlapped.

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Feature Description (continued)

8.3.1.1 Data I/O Cycle

The data I/O cycle is defined by the externally provided I/O CLOCK and lasts 8, 12, or 16 clock periods, depending on the selected output data length. During the I/O cycle, the following two operations take place simultaneously. An 8-bit data stream consisting of address/command and configuration information is provided to DATA IN. This data is shifted into the device on the rising edge of the first eight I/O CLOCK clocks. Data input is ignored after the first eight clocks during 12- or 16-clock I/O transfers. The data output, with a length of 8, 12, or 16 bits, is provided serially on DATA OUT. When $\overline{CS}$ is held low, the first output data bit occurs on the rising edge of EOC. When $\overline{CS}$ is toggled between conversions, the first output data bit occurs on the falling edge of CS. This data is the result of the previous conversion period, and after the first output data bit, each succeeding bit is clocked out on the falling edge of each succeeding I/O CLOCK.

8.3.1.2 Sampling Period

During the sampling period, one of the analog inputs is internally connected to the capacitor array of the converter to store the analog input signal. The converter starts sampling the selected input immediately after the four address/command bits have been clocked into the input data register. Sampling starts on the fourth falling edge of I/O CLOCK. The converter remains in the sampling mode until the eighth, twelfth, or sixteenth falling edge of I/O CLOCK depending on the data-length selection.

After the 8-bit data stream has been clocked in, DATA IN must be held at a fixed digital level until EOC goes high or $\overline{INT}$ goes low (indicating that the conversion is complete) to maximize the sampling accuracy and minimize the influence of external digital noise.

8.3.1.3 Conversion Cycle

A conversion cycle is started only after the I/O cycle is completed, which minimizes the influence of external digital noise on the accuracy of the conversion. This cycle is transparent to the user because it is controlled by an internal clock (oscillator). The total conversion time is equal to 13.5 OSC clocks plus a small delay (~25 ns) to start the OSC. During the conversion period, the device performs a successive-approximation conversion on the analog input voltage.

When programmed as EOC, pin 19 goes low at the start of the conversion cycle and goes high when the conversion is complete and the output data register is latched. After EOC goes low, the analog input can be changed without affecting the conversion result. Because the delay from the falling edge of the last I/O CLOCK to the falling edge of EOC is fixed, any time-varying analog input signals can be digitized at a fixed rate without introducing systematic harmonic distortion or noise due to timing uncertainty.

When programmed as $\overline{INT}$, pin 19 goes low when the conversion is complete and the output data register is latched. The next I/O CLOCK rising edge clears the $\overline{INT}$ output. The time from the last I/O CLOCK falling edge to the falling $\overline{INT}$ edge is equivalent to the EOC delay mentioned above plus the maximum conversion time. $\overline{INT}$ is cancelled by (or brought to high) by either the next $\overline{CS}$ falling edge or the next SCLK rising edge (when $\overline{CS}$ is held low all of the time for multiple cycles). When $\overline{CS}$ is held low continuously (for multiple cycles) MSB output occurs after the first rising edge of I/O CLOCK after EOC is inactive or the falling edge of $\overline{INT}$.

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Feature Description (continued)

8.3.2 Power Up and Initialization

After power up, $\overline{CS}$ must be taken from high to low to begin an I/O cycle. The $\overline{INT}$/EOC pin is initially high, and both configuration registers are set to all zeroes. The contents of the output data register are random, and the first conversion result should be ignored. To initialize during operation, $\overline{CS}$ is taken high and is then returned low to begin the next I/O cycle, as shown in Table 1. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

Table 1. Operational Terminology

CYCLE	DESCRIPTION
Current (N) I/O cycle	The entire I/O CLOCK sequence that transfers address and control data into the data register and clocks the digital result from the previous conversion from DATA OUT.
Current (N) conversion cycle	The conversion cycle starts immediately after the current I/O cycle. The end of the current I/O cycle is the last clock falling edge in the I/O CLOCK sequence. The current conversion result is loaded into the output register when conversion is complete.
Current (N) conversion result	The current conversion result is serially shifted out on the next I/O cycle.
Previous (N – 1) conversion cycle	The conversion cycle just prior to the current I/O cycle
Next (N + 1) I/O cycle	The I/O period that follows the current conversion cycle

Example: In 12-bit mode, the result of the current conversion cycle is a 12-bit serial-data stream clocked out during the next I/O cycle. The current I/O cycle must be exactly 12 bits long to maintain synchronization, even when this corrupts the output data from the previous conversion. The current conversion is begun immediately after the twelfth falling edge of the current I/O cycle.

8.3.3 Default Mode

When the DATA IN pin is held high, the ADC goes into hardware default mode because the CFGR2 bits are all programmed to the default values after 8 I/O CLOCKs. This means the ADC is programmed for an external reference and pin 19 as EOC. In addition, channel AIN0 is selected. The first conversion is invalid therefore the conversion result should be ignored. On the next cycle, AIN0 is sampled and converted. This mode of operation is valid when $\overline{CS}$ is toggled or held low after the first cycle.

To remove the device from hardware default mode, CFGR2 bit D0 must be reset to 0. When this is done, the host must program CFGR1 on the next cycle and disregard the result from the conversion of the current cycle.

8.3.4 Data Input

The data input is internally connected to an 8-bit serial-input address and control register. The register defines the operation of the converter and the output data length. The host provides the input data byte with the MSB first. Each data bit is clocked in on the rising edge of the I/O CLOCK sequence (see Table 2 for the data input-register format).

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Table 2. Command Set (CMR) and Configuration

SDI D[7:4]		COMMAND
BINARY	HEX	
0000b	0h	SELECT analog input channel 0
0001b	1h	SELECT analog input channel 1
0010b	2h	SELECT analog input channel 2
0011b	3h	SELECT analog input channel 3
0100b	4h	SELECT analog input channel 4
0101b	5h	SELECT analog input channel 5
0110b	6h	SELECT analog input channel 6
0111b	7h	SELECT analog input channel 7
1000b	8h	SELECT analog input channel 8
1001b	9h	SELECT analog input channel 9
1010b	Ah	SELECT analog input channel 10
1011b	Bh	SELECT TEST, Voltage = (V_{REF+} + $V_{REF–}$)/2
1100b	Ch	SELECT TEST, Voltage = REFM
1101b	Dh	SELECT TEST, Voltage = REFP
1110b	Eh	SW POWERDOWN (analog + reference)
1111b	Fh	ACCESS CFGR2

CFGR1 SDI D[3:0]	CONFIGURATION
D[3:2]	01: 8-bit output length X0: 12-bit output length(1) 11: 16-bit output length
D1	0: MSB out first 1: LSB out first
D0	0: Unipolar binary 1: Bipolar 2s complement

CFGR2 SDI D[3:0]	CONFIGURATION
D[3:2]	00: Internal 4.096 reference 01: Internal 2.048 reference 11: External reference (default)
D1	0: Pin 19 output EOC (default) 1: Pin 19 output $\overline{INT}$
D0	0: Normal mode (CFGR1 needs to be programmed) 1: Default mode enabled (D[3:0] of CFGR1 and D[3:1] of CFGR2 set to default)

(1) Select 12-bit output mode to achieve 200-kSPS sampling rate.

8.3.5 Data Input – Address/Command Bits

The four MSBs (D7–D4) of the input data register are the address or command. These bits can be used to address one of the 11 input channels, select one of three reference-test voltages, activate the software power-down mode, or access the second configuration register, CFGR2. All address/command bits affect the current conversion, which is the conversion that immediately follows the current I/O cycle. They also allow access to CFGR1 except for command 1111b, which allows access to CFGR2.

8.3.6 Data Output Length

CFGR1 bits (D3 and D2) of the data register select the output data length. The data-length selection is valid for the current I/O cycle (the cycle in which the data is read). The data-length selection, being valid for the current I/O cycle, allows device start-up without losing I/O synchronization. A data length of 8, 12, or 16 bits can be selected. Because the converter has 12-bit resolution, a data length of 12 bits is suggested.

With D3 and D2 set to 00 or 10, the device is in the 12-bit data-length mode and the result of the current conversion is output as a 12-bit serial data stream during the next I/O cycle. The current I/O cycle must be exactly 12 bits long for proper synchronization, even when this means corrupting the output data from a previous conversion. The current conversion is started immediately after the twelfth falling edge of the current I/O cycle.

With bits D3 and D2 set to 11, the 16-bit data-length mode is selected, which allows convenient communication with 16-bit serial interfaces. In the 16-bit mode, the result of the current conversion is output as a 16-bit serial data stream during the next I/O cycle with the four LSBs always reset to 0 (pad bits). The current I/O cycle must be exactly 16 bits long to maintain synchronization even when this means corrupting the output data from the previous conversion. The current conversion is started immediately after the sixteenth falling edge of the current I/O cycle.

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With bits D3 and D2 set to 01, the 8-bit data-length mode is selected, which allows fast communication with 8-bit serial interfaces. In the 8-bit mode, the result of the current conversion is output as an 8-bit serial data stream during the next I/O cycle. The current I/O cycle must be exactly eight bits long to maintain synchronization, even when this means corrupting the output data from the previous conversion. The four LSBs of the conversion result are truncated and discarded. The current conversion is started immediately after the eighth falling edge of the current I/O cycle.

Because the D3 and D2 register settings take effect on the I/O cycle when the data length is programmed, there can be a conflict with the previous cycle if the data-word length was changed. This may occur when the data format is selected to be least significant bit first, because at the time the data length change becomes effective (six rising edges of I/O CLOCK), the previous conversion result has already started shifting out. In actual operation, when different data lengths are required within an application and the data length is changed between two conversions, no more than one conversion result can be corrupted and only when it is shifted out in LSB-first format.

8.3.7 LSB Out First

D1 in the CFGR1 controls the direction of the output (binary) data transfer. When D1 is reset to 0, the conversion result is shifted out MSB first. When set to 1, the data is shifted out LSB first. Selection of MSB first or LSB first always affects the next I/O cycle and not the current I/O cycle. When changing from one data direction to another, the current I/O cycle is never disrupted.

8.3.8 Bipolar Output Format

D0 in the CFGR1 controls the binary data format used to represent the conversion result. When D0 is cleared to 0, the conversion result is represented as unipolar (unsigned binary) data. Nominally, the conversion result of an input voltage equal to or less than V_{REF-} is a code with all zeros (000...0) and the conversion result of an input voltage equal to or greater than V_{REF+} is a code of all ones (111...1). The conversion result of (V_{REF+} + V_{REF-})/2 is a code of a one followed by zeros (100...0).

When D0 is set to 1, the conversion result is represented as bipolar (signed binary) data. Nominally, conversion of an input voltage equal to or less than V_{REF-} is a code of a one followed by zeros (100...0), and the conversion of an input voltage equal to or greater than V_{REF+} is a code of a zero followed by all ones (011...1). The conversion result of (V_{REF+} + V_{REF-})/2 is a code of all zeros (000...0). The MSB is interpreted as the sign bit. The bipolar data format is related to the unipolar format in that the MSBs are always each other's complement.

Selection of the unipolar or bipolar format always affects the current conversion cycle, and the result is output during the next I/O cycle. When changing between unipolar and bipolar formats, the data output during the current I/O cycle is not affected.

8.3.9 Reference

The device has a built-in reference with a programmable level of 2.048 V or 4.096 V. If the internal reference is used, REF+ is set to 2.048 V or 4.096 V and REF– is set to analog GND. An external reference can also be used through two reference input pins, REF+ and REF–, if the reference source is programmed as external, as shown in Figure 54. The voltage levels applied to these pins establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively. The values of REF+, REF–, and the analog input must not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF–.

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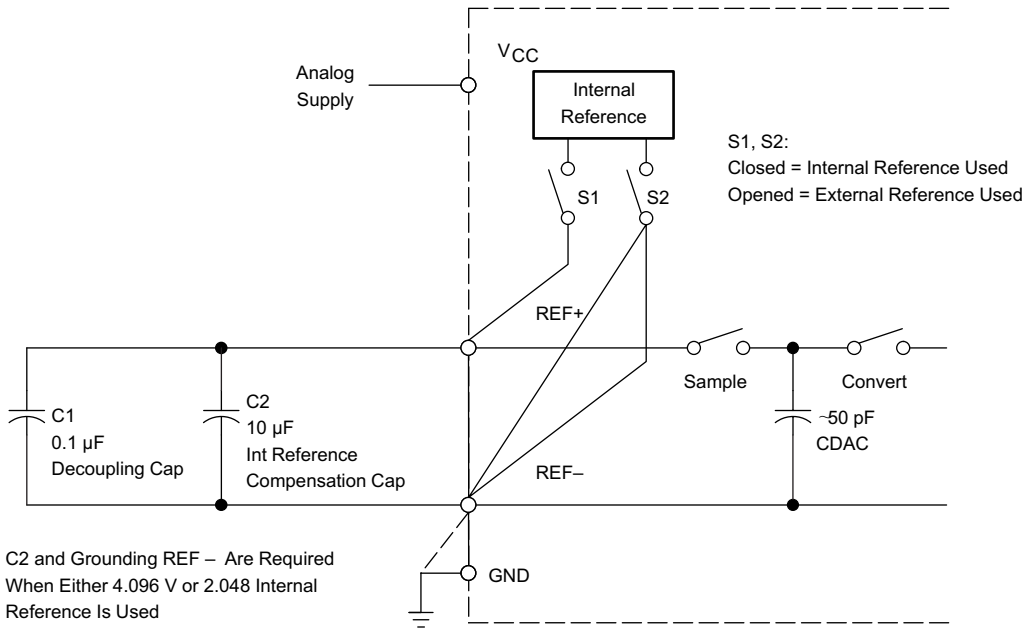

Figure 54. Reference Block

8.3.10 $\overline{\text{INT}}$/EOC Output

Pin 19 outputs the status of the ADC conversion. When programmed as EOC, the output indicates the beginning and the end of conversion. In the reset state, EOC is always high. During the sampling period (beginning after the fourth falling edge of the I/O CLOCK sequence), EOC remains high until the internal sampling switch of the converter is safely opened. The opening of the sampling switch occurs after the eighth, twelfth, or sixteenth I/O CLOCK falling edge, depending on the data-length selection in the input data register. After the EOC signal goes low, the analog input signal can be changed without affecting the conversion result.

The EOC signal goes high again after the conversion is completed and the conversion result is latched into the output data register. The rising edge of EOC returns the converter to a reset state and a new I/O cycle begins. On the rising edge of EOC, the first bit of the current conversion result is on DATA OUT when $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is toggled between conversions, the first bit of the current conversion result occurs on DATA OUT at the falling edge of $\overline{\text{CS}}$.

When programmed as $\overline{\text{INT}}$, the output indicates that the conversion is completed and the output data is ready to be read. In the reset state, $\overline{\text{INT}}$ is always high. $\overline{\text{INT}}$ is high during the sampling period and until the conversion is complete. After the conversion is finished and the output data is latched, $\overline{\text{INT}}$ goes low and remains low until it is cleared by the host. When $\overline{\text{CS}}$ is held low, the MSB (or LSB) of the conversion result is presented on DATA OUT on the falling edge of $\overline{\text{INT}}$. A rising I/O CLOCK edge clears the interrupt.

8.3.11 Chip-Select Input ($\overline{\text{CS}}$)

$\overline{\text{CS}}$ enables and disables the device. During normal operation, $\overline{\text{CS}}$ should be low. Although the use of $\overline{\text{CS}}$ is not necessary to synchronize a data transfer, it can be brought high between conversions to coordinate the data transfer of several devices sharing the same bus.

When $\overline{\text{CS}}$ is brought high, the serial-data output is immediately brought to the high-impedance state, releasing its output data line to other devices that may share it. After an internally generated debounce time, I/O CLOCK is inhibited, thus preventing any further change in the internal state.

When $\overline{\text{CS}}$ is subsequently brought low again, the device is reset. $\overline{\text{CS}}$ must be held low for an internal debounce time before the reset operation takes effect. After $\overline{\text{CS}}$ is debounced low, I/O CLOCK must remain inactive (low) for a minimum time before a new I/O cycle can start.

$\overline{\text{CS}}$ can interrupt any ongoing data transfer or any ongoing conversion. When $\overline{\text{CS}}$ is debounced low long enough before the end of the current conversion cycle, the previous conversion result is saved in the internal output buffer and shifted out during the next I/O cycle.

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When $\overline{CS}$ is held low continuously for multiple cycles, the first data bit of the newly completed conversion occurs on DATA OUT on the rising edge of EOC or falling edge of $\overline{INT}$. Note that the first cycle in the series still requires a transition $\overline{CS}$ from high to low. When a new conversion is started after the last falling edge of I/O CLOCK, EOC goes low and the serial output is forced low until EOC goes high again.

When $\overline{CS}$ is toggled between conversions, the first data bit occurs on DATA OUT on the falling edge of $\overline{CS}$. On each subsequent falling edge of I/O CLOCK after the first data bit appears, the data is changed to the next bit in the serial conversion result until the required number of bits has been output.

8.3.12 Power-Down Features

When command (D7–D4) 1110b is clocked into the input data register during the first four I/O CLOCK cycles, the software power-down mode is selected. Software power down is activated on the falling edge of the fourth I/O CLOCK pulse.

During software power down, all internal circuitry is put in a low-current standby mode. The internal reference (if being used) is powered down. No conversion is performed. The internal output buffer keeps the previous conversion cycle data results provided that all digital inputs are held above V_{CC} – 0.5 V or below 0.5 V. The I/O logic remains active so the current I/O cycle must be completed even when the power-down mode is selected. Upon power-on reset and before the first I/O cycle, the converter normally begins in the power-down mode. The device remains in the software power-down mode until a valid input address (other than command 1110b) is clocked in. Upon completion of that I/O cycle, a normal conversion is performed with the results being shifted out during the next I/O cycle. If using the internal reference, care must be taken to allow the reference to power on completely before a valid conversion can be performed. It requires 1 ms to resume from a software power down.

The ADC also has an auto power-down mode. This is transparent to users. The ADC goes into auto power down within 1 I/O CLOCK cycle after the conversion is complete and resumes, with a small delay after an active $\overline{CS}$ is sent to the ADC. This mode keeps built-in reference so resumption is fast enough to be used between cycles.

8.3.13 Analog MUX

The 11 analog inputs, 3 internal voltages, and power-down mode are selected by the input multiplexer according to the input addresses shown in Table 2 . The input multiplexer is a break-before-make type to reduce input-to-input noise rejection resulting from channel switching. Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK and continues for the remaining I/O CLOCK pulses. The sample is held on the falling edge of the last I/O CLOCK pulse. The three internal test inputs are applied to the multiplexer, then sampled and converted in the same manner as the external analog inputs. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

8.4 Device Functional Modes

The ADC has an auto power-down mode. This is transparent to users. The ADC gets into auto power-down within one I/O CLOCK cycle after the conversion is complete and resumes, with a small delay, after an active $\overline{CS}$ is sent to the ADC. The resumption is fast enough to be used between cycles.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

As with most SAR ADCs, the inputs of the TLV2556 are not high-impedance ports. At the start of the sampling phase, the selected input channel experiences a load current, as the internal analog switches close and the sampling capacitor starts to charge (or discharge). This load current decays over time and varies in a non-linear fashion with respect to input voltage.

The load current is supplied by the input signal source which has non-zero output impedance. As a result, the load current drops non-zero voltage across the output impedance of the signal source creating a time-decaying, non-linear error between the signal source output and the ADC input. This is called sampling error, and if the sampling error does not decay to less than 1 LSB before the end of the sampling window when the sampling switch opens and conversion begins, the ADC output is inaccurate.

The rate of decay of the sampling error and its non-linearity over input voltage are highly sensitive to source impedance. In other words, for larger values of source impedance, the sampling error decays more slowly over time, resulting in greater residual error at the end of the sampling window that is also more non-linear over the ADC input voltage range. Non-linearity in the ADC input translates to non-linearity or harmonic distortion in the ADC output. Harmonic distortion degrades ADC resolution and translates to a decrease in the ADC's effective number of bits (ENOB). Therefore, driving the ADC input with a low-impedance source is critical for conversion accuracy.

In addition to keeping source impedance as low as possible, TI recommends the following measures for minimizing input sampling error and harmonic distortion associated with the TLV2556 while operating the device at maximum 200-kSPS throughput:

1. For AC inputs, the maximum input signal frequency on all channels must be limited to well below the maximum Nyquist rate of 100 kHz. Figure 55 shows how ENOB degrades as input frequency increases.
2. For DC inputs, ensure that there are no large step-function changes (greater than VREF / 4) between successive input channels in the scanning order at the highest throughput. If possible, it is advisable to scan the input channels so that the difference in the DC voltage levels between any two successive channels is minimized to ensure 12-bit sampling accuracy. For larger voltage changes between channels, higher accuracy can be achieved by reducing the throughput.
3. The stability of the ADC reference input voltage, which is a DC signal, is critical for ADC accuracy. The reference source experiences large instantaneous changes in load current during the ADC conversion phase, and therefore, low source impedance is required for excellent load regulation and stability.

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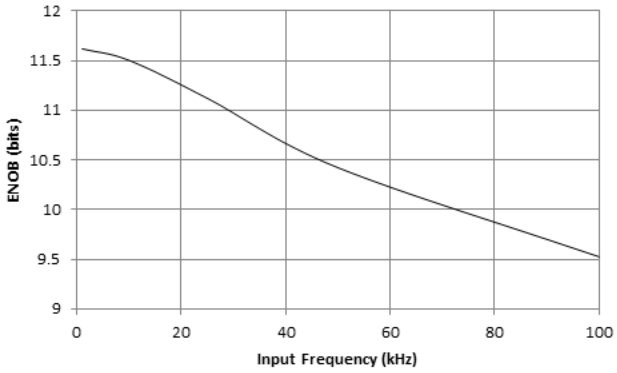
Application Information (continued)



R_{source} = 50 Ω f_s = 200KSPS Ext. 4.096 V Ref.

Figure 55. ENOB as a Function of Input Signal Frequency

9.2 Typical Application

Figure 56 shows a typical application where the TLV2556 is used to acquire multiple AC signals while operating at its maximum sampling rate of 200 kSPS.

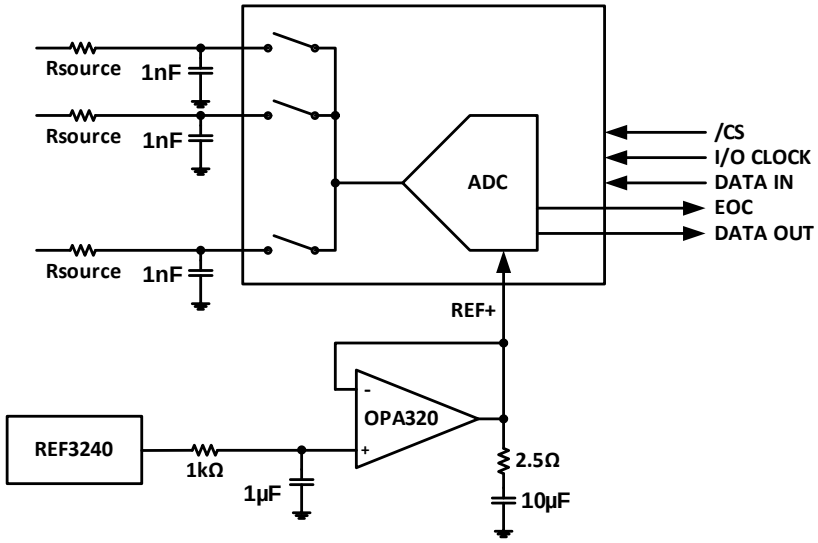


Figure 56. Typical Application Block Diagram

9.2.1 Design Requirements

The design is optimized for superior dynamic performance (low harmonic distortion, high ENOB) while the ADC is multiplexing input channels at maximum sampling rate. Of course, the underlying assumption, based on *Application Information*, is that the bandwidths of the input signals are much less than 100 kHz. For example, according to Figure 55, the TLV2556 provides better than 11.5 ENOB for AC inputs below 10 kHz.

9.2.2 Detailed Design Procedure

Good dynamic performance while the ADC is multiplexing inputs at maximum sampling rate requires low source impedance on the input channels being addressed. To make the input source impedance less sensitive to line inductance, especially in cases where the signal sources may be located far away from the ADC, it may be necessary to use operational amplifier buffers located close to the ADC input pins.

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Typical Application (continued)

The procedure for estimating the maximum tolerable value of input source impedance on a given channel for achieving the desired ENOB (for example ENOB > 11.5) in a multiplexed application is as follows:

1. Using a low impedance signal source, apply a full-scale sinusoidal signal of suitably low frequency to the ADC input channel of interest, CHx.
2. Using a second low impedance source, apply a full-scale sinusoid that has the same frequency as the signal on CHx but is 180° out-of-phase, to a second ADC input channel, CHy, that serves as the control element in the experiment.
3. Initiate conversions with the ADC continuously multiplexing between CHx and CHy in each conversion cycle.
4. Re-arrange the output data by channel, and for each of the two channels, compute SINAD from its FFT and estimate ENOB for that channel as ENOB = (SINAD[dB] – 1.76) / 6.02.
5. Increase the series resistance on CHx by a discrete amount and repeat steps 1 through 5 until the ENOB of CHx has degraded sufficiently relative to CHy (which should remain unchanged).

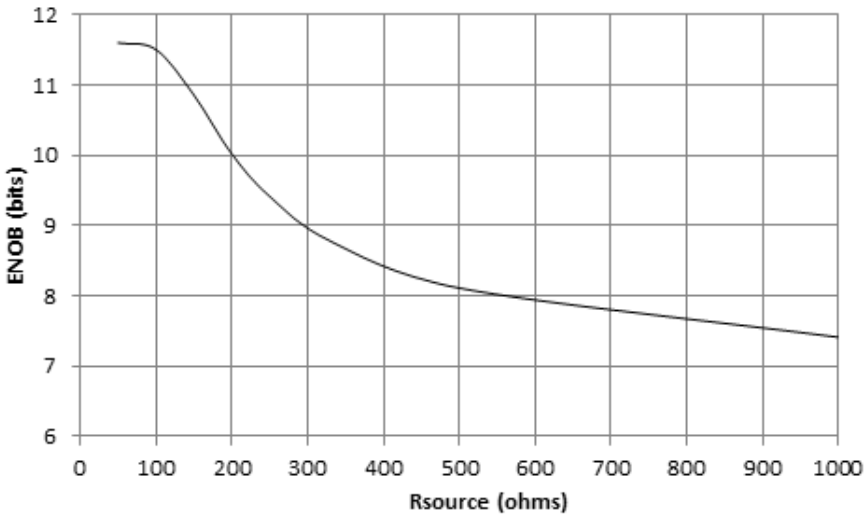
The external 1-nF decoupling capacitors (recommend C0G/NP0 type for constant capacitance versus voltage) on the input channels are required for supplying the instantaneous change in the load current demand of the ADC during the sampling phase after an input channel is selected. In other words, the decoupling capacitor effectively reduces the output impedance of the source at high frequencies.

Similarly, the reference pin also requires decoupling for low output impedance at high frequency. However, the larger magnitude of reference pin load currents during the ADC conversion phase necessitates a decoupling capacitor of a much higher value. The extra ESR (2.5 Ω) is required for stabilizing the OPA320 output as it drives the 10-µF load.

The OPA320 is a wide-band, low-noise, low-power operational amplifier that is unity gain stable and can operate on a single +5-V system supply while supporting rail-to-rail signal swing at its input and output. These properties make it an ideal choice for being used as a high-precision (stable, low-noise) reference buffer that has enough loop gain over frequency to support low output impedance over a wide bandwidth.

9.2.3 Application Curve

Figure 57 was generated by sweeping R_{source} between 50 Ω and 1 kΩ following the procedure detailed in *Detailed Design Procedure*.



f_{IN} = 1 kHz f_s = 200 kSPS Ext. 4.096 V Ref.

Figure 57. ENOB as a Function of Input Source Impedance

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10 Power Supply Recommendations

The TLV2556 is designed to operate from a single power supply voltage between 2.7 and 5.5 V. The ADC supply voltage must be well regulated. A 1-µF ceramic decoupling capacitor is required and must be placed as close as possible to the device to minimize inductance along the load current path.

Many modern microcontrollers have interfaces that support only up to 3.3-V logic levels, which is incompatible with the TLV2556 when the device is operated on a 5-V power supply. In such cases, 5-V to 3.3-V digital level translators may be used to facilitate communication between the TLV2556 and the microcontroller host.

11 Layout

11.1 Layout Guidelines

- All decoupling capacitors must be located as close as possible to the loads they are supplying.
- Large copper fill areas or thick traces are recommended wherever possible to provide low-inductance current paths between decoupling capacitors and their loads
- Ensure that there are no vias or discontinuities in the forward or return current paths that can cause the current-loop area and therefore the loop inductance to increase.
- For high-frequency current paths routed across PCB layers, multiple vias can be placed close together (but not obstructing the current path) to lower inductance.

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11.2 Layout Example

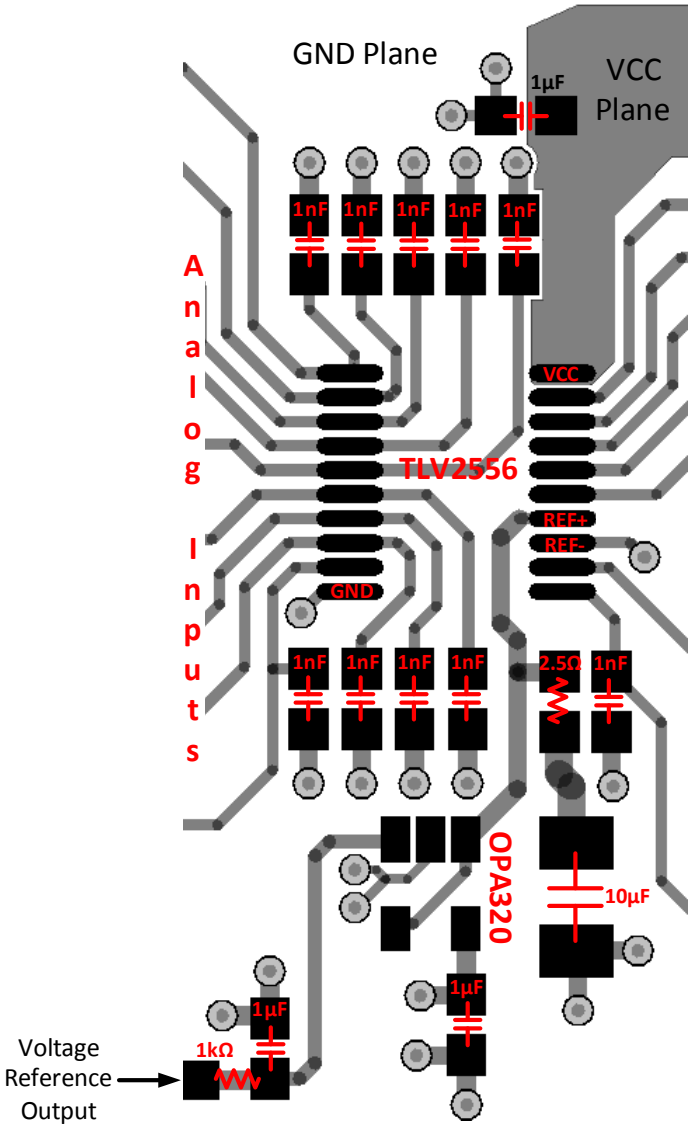

Figure 58. Layout Example Schematic

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2556IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV2556I	Samples
TLV2556IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV2556I	Samples
TLV2556IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2556	Samples
TLV2556IPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2556	Samples
TLV2556IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2556	Samples
TLV2556IPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2556	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV2556 :

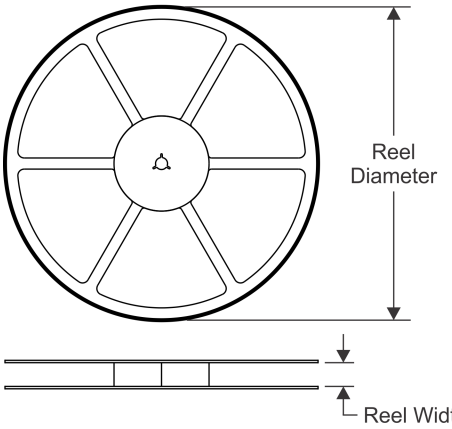
- Enhanced Product: TLV2556-EP

NOTE: Qualified Version Definitions:

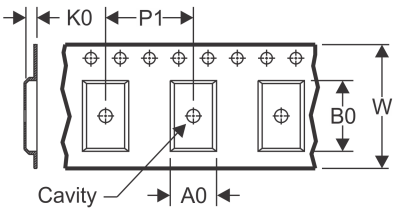
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

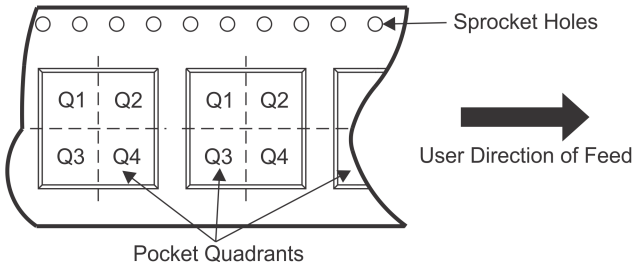


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

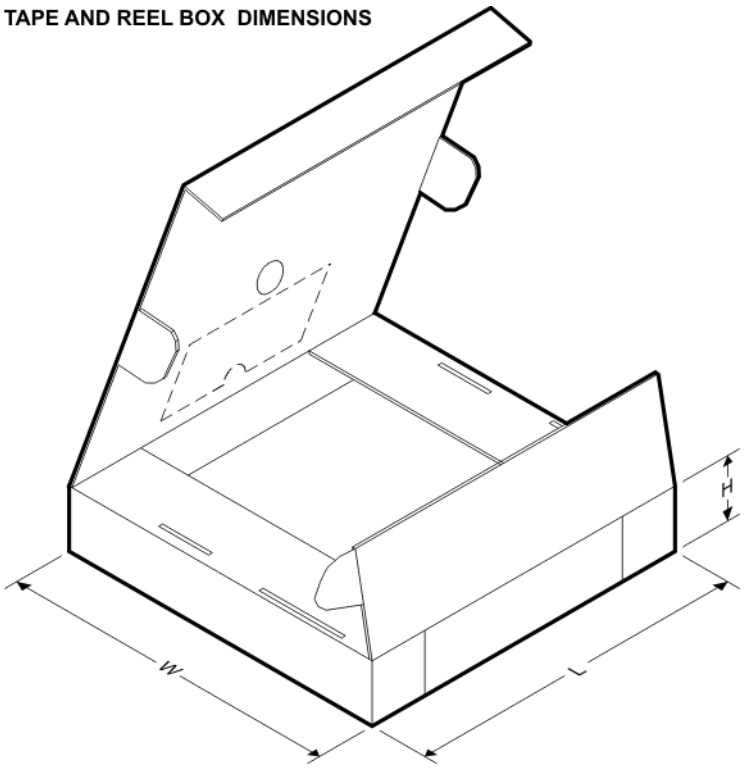
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2556IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV2556IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2556IDWR	SOIC	DW	20	2000	350.0	350.0	43.0
TLV2556IPWR	TSSOP	PW	20	2000	350.0	350.0	43.0

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