THE DATASHEET OF

TMP105YZCR

Digital Temperature Sensor with Two-Wire Interface

Check for Samples: TMP105

FEATURES

- **SUPPORTS 1.8V I²C™ BUS**
- **TWO ADDRESSES**
- **DIGITAL OUTPUT: Two-Wire Serial Interface**
- **RESOLUTION: 9- to 12-Bits, User-Selectable**
- **ACCURACY:**
  - **±2.0°C (max) from –25°C to +85°C**
  - **±3.0°C (max) from –40°C to +125°C**
- **LOW QUIESCENT CURRENT: 50µA, 1.5µA Standby**
- **NO POWER-UP SEQUENCE REQUIRED, I²C PULLUPS CAN BE ENABLED PRIOR TO V+**

APPLICATIONS

- **CELL PHONES**
- **COMPUTER PERIPHERAL THERMAL PROTECTION**
- **NOTEBOOK COMPUTERS**
- **BATTERY MANAGEMENT**
- **THERMOSTAT CONTROLS**
- **ENVIRONMENTAL MONITORING AND HVAC**

DESCRIPTION

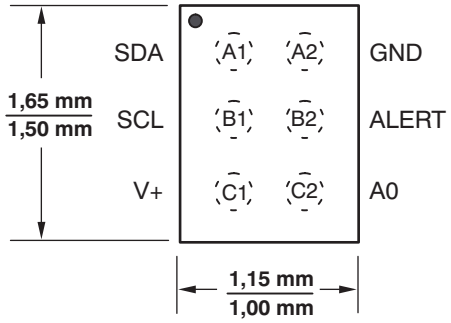
The TMP105 is a two-wire, serial output temperature sensor available in a WCSP package. Requiring no external components, the TMP105 is capable of reading temperatures with a resolution of 0.0625°C.

The TMP105 features a Two-Wire interface that is SMBus-compatible, with the TMP105 allowing up to two devices on one bus. The TMP105 features an SMBus Alert function.

The TMP105 is ideal for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.

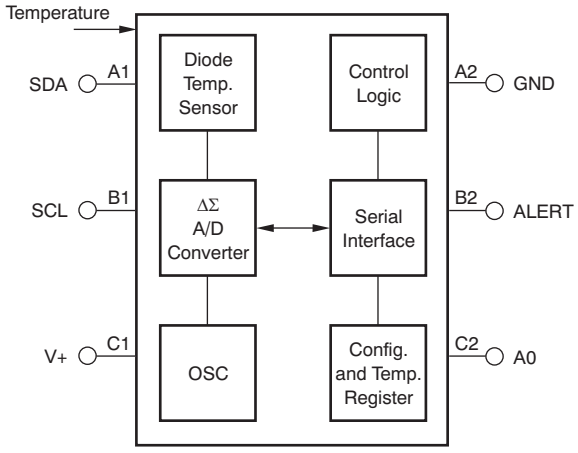
The TMP105 is specified for operation over a temperature range of –40°C to +125°C.

YZC LEAD- FREE
2 X 3 ARRAY
(TOP VIEW)



(Bump Side Down)

Note: Pin A1 is marked with a *0* for Pb-free (YZC)



TMP105

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PACKAGE	PART NUMBER	SYMBOL
Wafer chip-scale package (YZC)	TMP105YZC	EY

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the product folder at www.ti.com.

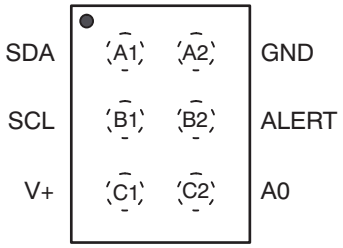
ABSOLUTE MAXIMUM RATINGS(1)

Power Supply, V+		7.0V
Input Voltage(2)		–0.5V to 7.0V
Input Current		10mA
Operating Temperature Range		–55°C to +127°C
Storage Temperature Range		–60°C to +130°C
Junction Temperature (T_J max)		+150°C
ESD Rating:	Human Body Model (HBM)(3)	2000V
	Charged-Device Model (CDM)(4)	500V
	Machine Model (MM)(5)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input voltage rating applies to all TMP105 input voltages.
(3) HBM testing has been tested to TI specifications JEDEC JESD22-A114C.01.
(4) CDM testing has been tested to TI specifications JEDEC EIA/JESD22-A115A.
(5) MM testing has been tested to TI specifications JEDEC JESD22-C101C.

PIN ASSIGNMENTS

WCSP-6 PACKAGE
(TOP VIEW)



(Bump Side Down)

Note: Pin 1 is determined by orienting the package marking as indicated in the diagram.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +125°C, and V+ = 2.6V to 3.3V, unless otherwise noted.

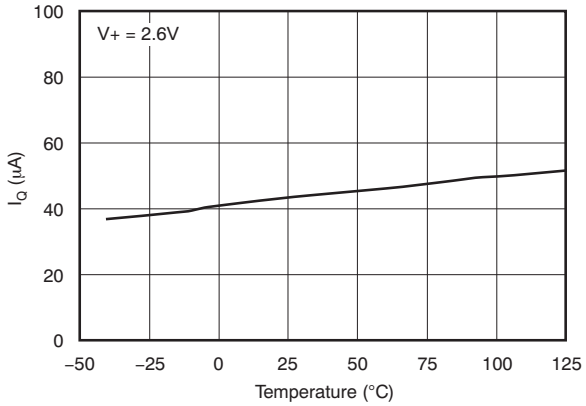
PARAMETER	CONDITION	TMP105			UNIT
		MIN	TYP	MAX	
TEMPERATURE INPUT					
Range		–40		+125	°C
Accuracy (Temperature Error)	–25°C to +85°C		±0.5	±2.0	°C
	–40°C to +125°C		±1.0	±3.0	°C
vs Supply			0.2	±0.5	°C/V
Resolution(1)	Selectable		0.0625		°C
DIGITAL INPUT/OUTPUT (SCL, SDA, ALERT)					
Input Capacitance			3		pF
Input Logic Levels:					
V_{IH}		1.2		6.0	V
V_{IL}		–0.5		0.6	V
Leakage Input Current, I_{IN}	0V ≤ V_{IN} ≤ 6V			1	µA
Input Voltage Hysteresis	SCL and SDA Pins		100		mV
Output Logic Levels:					
V_{OL} SDA	I_{OL} = 3mA	0	0.15	0.4	V
V_{OL} ALERT	I_{OL} = 4mA	0	0.15	0.4	V
Resolution	Selectable		9 to 12		Bits
Conversion Time	9-Bit		27.5	37.5	ms
	10-Bit		55	75	ms
	11-Bit		110	150	ms
	12-Bit		220	300	ms
Timeout Time		25	54	74	ms
DIGITAL INPUT (A0)					
Input Capacitance			3		pF
Input Logic Levels:					
V_{IH}		0.7 x (V+)		(V+) + 0.5	V
V_{IL}		–0.5		0.3 x (V+)	V
Leakage Input Current, I_{IN}	0V ≤ V_{IN} ≤ V+			1	µA
POWER SUPPLY					
Operating Range		2.6		3.3	V
Quiescent Current I_Q	Serial Bus Inactive		50	85	µA
	Serial Bus Active, SCL Freq = 400kHz		100		µA
Shutdown Current I_{SD}	Serial Bus Inactive		1.5	3	µA
	Serial Bus Active, SCL Freq = 400kHz		60		µA
TEMPERATURE RANGE					
Specified Range		–40		+125	°C
Operating Range		–55		+127	°C
Thermal Resistance θ_{JA}			240		°C/W

(1) Specified for 12-bit resolution.

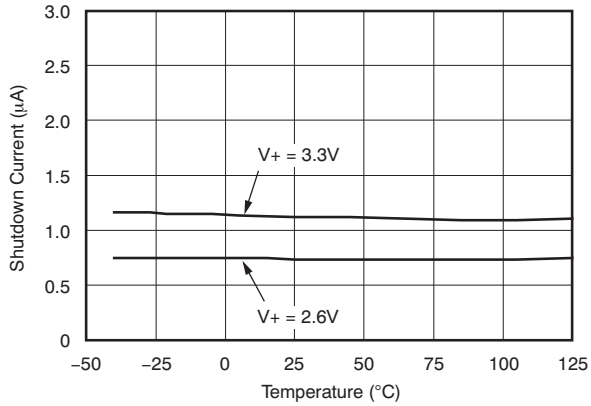
TYPICAL CHARACTERISTICS

At T_A = +25°C and V+ = 2.8V, unless otherwise noted.

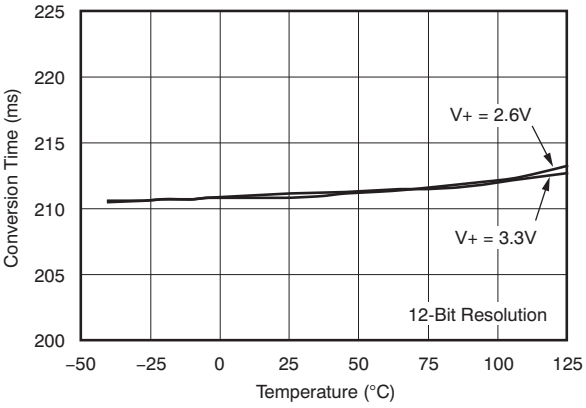
QUIESCENT CURRENT vs TEMPERATURE



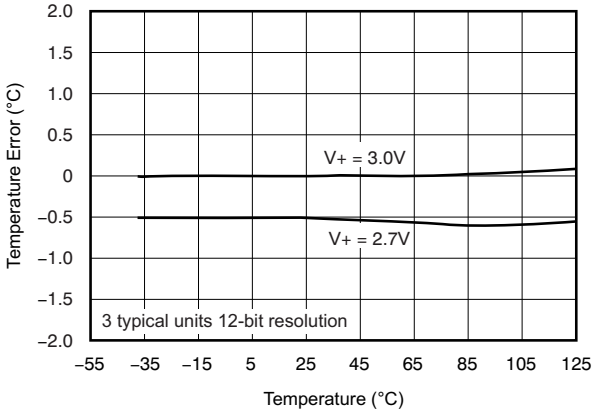
SHUTDOWN CURRENT vs TEMPERATURE



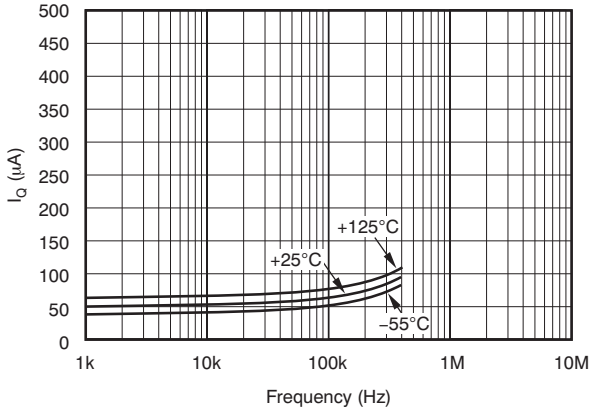
CONVERSION TIME vs TEMPERATURE



TEMPERATURE ACCURACY vs TEMPERATURE



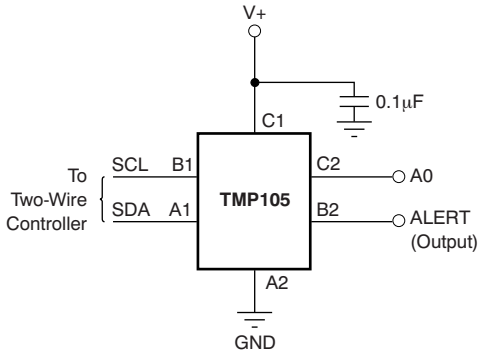
QUIESCENT CURRENT WITH BUS ACTIVITY vs TEMPERATURE



APPLICATIONS INFORMATION

The TMP105 is a digital temperature sensor that is optimal for thermal management and thermal protection applications. The TMP105 is Two-Wire and SMBus interface-compatible, and is specified over a temperature range of –40°C to +125°C.

The TMP105 requires no external components for operation except for pull-up resistors on SCL, SDA, and ALERT, although a 0.1µF bypass capacitor is recommended, as shown in Figure 1. SCL, SDA and ALERT can be tied to a 1.8V supply or V+ through pull-up resistors. A0 should be tied to V+ or GND.



Note: SCL, SDA, and ALERT pins require pull-up resistors.

Figure 1. Typical Connections of the TMP105

The sensing device of the TMP105 is the chip itself. Thermal paths run through the package leads. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

To maintain accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature.

POINTER REGISTER

Figure 2 shows the internal register structure of the TMP105. The 8-bit Pointer Register of the devices is used to address a given data register. The Pointer Register uses the two LSBs to identify which of the data registers should respond to a read or write command. Table 1 identifies the bits of the Pointer Register byte. Table 2 describes the pointer address of the registers available in the TMP105. Power-up reset value of P1/P0 is 00.

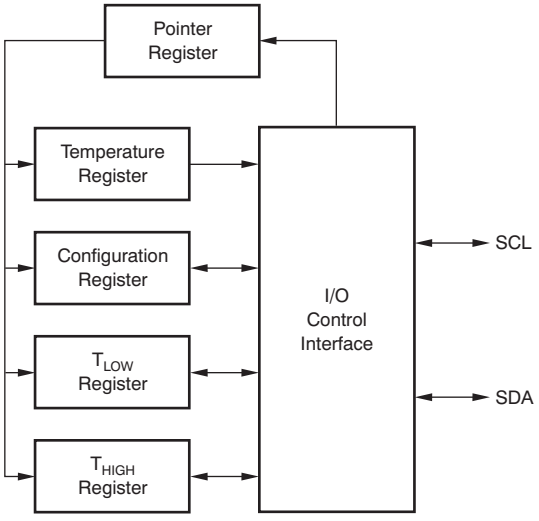


Figure 2. Internal Register Structure of the TMP105

Table 1. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

Table 2. Pointer Addresses of the TMP105

P1	P0	REGISTER
0	0	Temperature Register (Read Only)
0	1	Configuration Register (Read/Write)
1	0	T_{LOW} Register (Read/Write)
1	1	T_{HIGH} Register (Read/Write)

TEMPERATURE REGISTER

The Temperature Register of the TMP105 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 3 and Table 4. Note that byte 1 is the most significant byte; byte 2 is the least significant byte (sent in this order). The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Data format for temperature is summarized in Table 5. Following power-up or reset, the Temperature Register will read 0°C until the first conversion is complete.

Table 3. Byte 1 of Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Table 4. Byte 2 of Temperature Register

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

Table 5. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration Register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits in the Temperature Register are used with the unused LSBs set to zero.

CONFIGURATION REGISTER

The Configuration Register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format of the Configuration register for the TMP105 is shown in Table 6, followed by a breakdown of the register bits. The power-up/reset value of the Configuration Register is all bits equal to 0.

Table 6. Configuration Register Format

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD

SHUTDOWN MODE (SD)

The Shutdown Mode of the TMP105 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically 1.5μA. Shutdown Mode is enabled when the SD bit is 1; the device will shut down once the current conversion is completed. When SD is equal to 0, the device will maintain a continuous conversion state.

THERMOSTAT MODE (TM)

The Thermostat Mode bit of the TMP105 indicates to the device whether to operate in Comparator Mode (TM = 0) or Interrupt Mode (TM = 1). For more information on comparator and interrupt modes, see the *High and Low Limit Registers* section.

POLARITY (POL)

The Polarity Bit of the TMP105 allows the user to adjust the polarity of the ALERT pin output. If POL = 0, the ALERT pin will be active LOW, as shown in Figure 3. For POL = 1, the ALERT pin will be active HIGH, and the state of the ALERT pin is inverted.

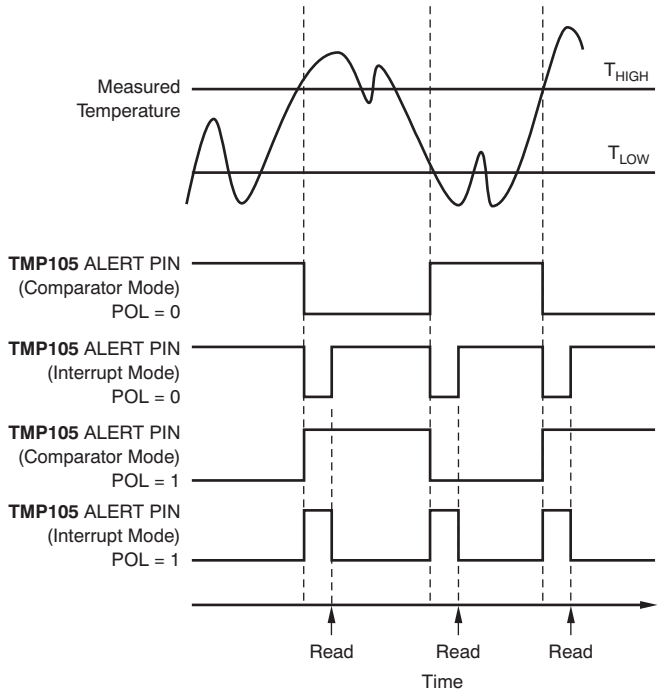


Figure 3. Output Transfer Function Diagrams

FAULT QUEUE (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} Registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 7 defines the number of measured faults that may be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see the *High and Low Limit Registers* section.

Table 7. Fault Settings of the TMP105

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

CONVERTER RESOLUTION (R1/R0)

The Converter Resolution bits control the resolution of the internal analog-to-digital (A/D) converter. This control allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table 8 identifies the resolution bits and the relationship between resolution and conversion time.

Table 8. Resolution of the TMP105

R1	R0	RESOLUTION	CONVERSION TIME (typical)
0	0	9 Bits (0.5°C)	27.5ms
0	1	10 Bits (0.25°C)	55ms
1	0	11 Bits (0.125°C)	110ms
1	1	12 Bits (0.0625°C)	220ms

ONE-SHOT (OS)

The TMP105 features a One-Shot Temperature Measurement Mode. When the device is in Shutdown Mode, writing a '1' to the OS bit starts a single temperature conversion. The device will return to the shutdown state at the completion of the single conversion. This option is useful to reduce power consumption in the TMP105 when continuous temperature monitoring is not required. When the Configuration Register is read, the OS always reads zero.

HIGH AND LOW LIMIT REGISTERS

In Comparator Mode (TM = 0), the ALERT pin of the TMP105 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt Mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or until the device successfully responds to the SMBus Alert Response address. The ALERT pin clears if the device is placed in Shutdown Mode. Once the ALERT pin is cleared, it will only become active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin becomes active and remains active until cleared by a read operation of any register or a successful response to the SMBus Alert Response address. When the ALERT pin clears, the above cycle will repeat, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This reset also clears the state of the internal registers in the device returning the device to Comparator Mode (TM = 0).

Both operational modes are represented in Figure 3. Table 9 and Table 10 describe the format for the T_{HIGH} and T_{LOW} Registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and T_{LOW} are:

T_{HIGH} = 80°C and T_{LOW} = 75°C

The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

Table 9. Bytes 1 and 2 of T_{HIGH} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	H3	H2	H1	H0	0	0	0	0

Table 10. Bytes 1 and 2 of T_{LOW} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
2	L3	L2	L1	L0	0	0	0	0

All 12 bits for the Temperature, T_{HIGH}, and T_{LOW} Registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

SERIAL INTERFACE

The TMP105 operates only as a slave device on the Two-Wire bus and SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP105 supports the transmission protocol for fast (1kHz to 400kHz) mode. All data bytes are transmitted MSB first.

SERIAL BUS ADDRESS

To communicate with the TMP105, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The TMP105 features one address pin allowing up to two devices to be connected per bus. Pin logic levels are described in Table 11. The address pin of the TMP105 is read after reset, at start of communication, or in response to a Two-Wire address acquire request. Following reading of the state of the pin, the address is latched to minimize power dissipation associated with detection.

Table 11. Address Pin and Slave Addresses for the TMP105

A0	SLAVE ADDRESS
0	1001000
1	1001001

BUS OVERVIEW

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge Bit. During data transfer SDA must remain stable while SCL is HIGH, as any change in SDA while SCL is HIGH will be interpreted as a control signal.

Once all data has been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH.

WRITING/READING TO THE TMP105

Accessing a particular register on the TMP105 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit LOW. Every write operation to the TMP105 requires a value for the Pointer Register. (Refer to Figure 5.)

When reading from the TMP105, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit LOW, followed by the Pointer Register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit HIGH to initiate the read command. See Figure 6 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register byte, as the TMP105 remembers the Pointer Register value until it is changed by the next write operation.

Note that register bytes are sent most significant byte first, followed by the least significant byte.

SLAVE MODE OPERATIONS

The TMP105 can operate as a slave receiver or slave transmitter.

Slave Receiver Mode:

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit LOW. The TMP105 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer Register. The TMP105 then acknowledges reception of the Pointer Register byte. The next byte or bytes are written to the register addressed by the Pointer Register. The TMP105 acknowledges reception of each data byte. The master may terminate data transfer by generating a START or STOP condition.

Slave Transmitter Mode:

The first byte is transmitted by the master and is the slave address, with the R/$\overline{W}$ bit HIGH. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer Register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master may terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

SMBus ALERT FUNCTION

The TMP105 supports the SMBus Alert function. When the TMP105 is operating in Interrupt Mode (TM = 1), the ALERT pin of the TMP105 may be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP105 is active, the devices will acknowledge the SMBus Alert command and respond by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte will indicate if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the ALERT condition. This bit will be HIGH if the temperature is greater than or equal to T_{HIGH}. This bit will be LOW if the temperature is less than T_{LOW}. Refer to Figure 7 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command will determine which device will clear its ALERT status. If the TMP105 wins the arbitration, its ALERT pin will become inactive at the completion of the SMBus Alert command. If the TMP105 loses the arbitration, its ALERT pin will remain active.

GENERAL CALL

The TMP105 responds to a Two-Wire General Call address (0000000) if the eighth bit is 0. The device will acknowledge the General Call address and respond to commands in the second byte. If the second byte is 00000100, the TMP105 will latch the status of the address pin, but will not reset. If the second byte is 00000110, the TMP105 will latch the status of the address pin and reset the internal registers to their power-up values.

TIMEOUT FUNCTION

The TMP105 will reset the serial interface if either SCL or SDA are held LOW for 54ms (typ) between a START and STOP condition. The TMP105 will release the bus if it is pulled LOW and will wait for a START condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1kHz for SCL operating frequency.

TIMING DIAGRAMS

The TMP105 is Two-Wire and SMBus-compatible. Figure 4 to Figure 7 describe the various operations on the TMP105. Bus definitions are given below. Parameters for Figure 4 are defined in Table 12.

Bus Idle:

Both SDA and SCL lines remain HIGH.

Start Data Transfer:

A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer:

A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer:

The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge:

Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge on the last byte that has been transmitted by the slave.

Table 12. Timing Diagram Definitions for the TMP105

PARAMETER		FAST MODE		UNITS
		MIN	MAX	
SCL Operating Frequency	$f_{(SCL)}$	1	400	kHz
Bus Free Time Between STOP and START Condition	$t_{(BUF)}$	600		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	100		ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$	100		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	100		ns
Data Hold Time	$t_{(HDDAT)}$	0		ns
Data Setup Time	$t_{(SUDAT)}$	100		ns
SCL Clock LOW Period	$t_{(LOW)}$	1300		ns
SCL Clock HIGH Period	$t_{(HIGH)}$	600		ns
Clock/Data Fall Time	t_F		300	ns
Clock/Data Rise Time for SCLK ≤ 100kHz	t_R		300 1000	ns ns

TWO-WIRE TIMING DIAGRAMS

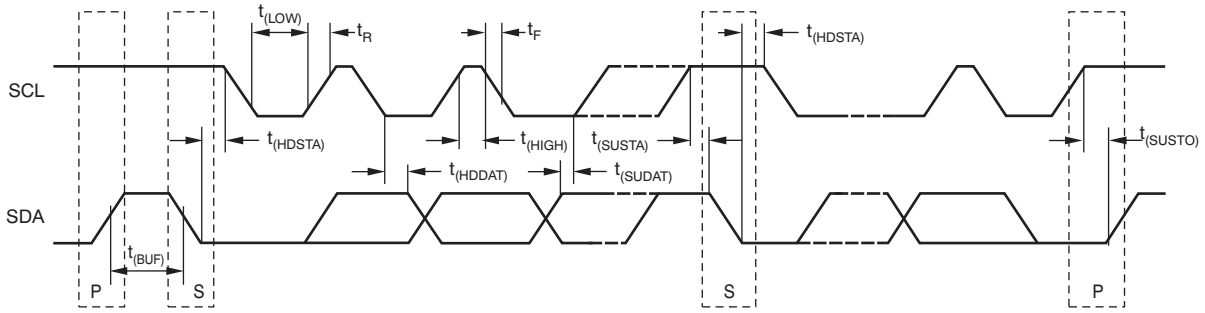


Figure 4. Two-Wire Timing Diagram

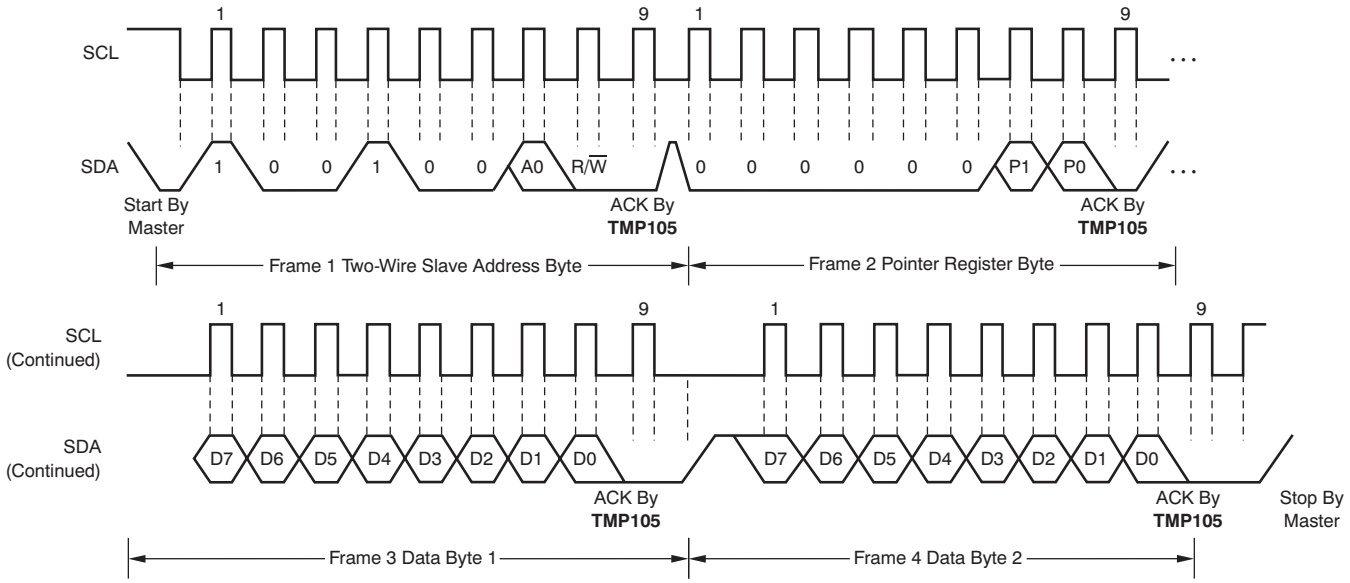


Figure 5. Two-Wire Timing Diagram for TMP105 Write Word Format

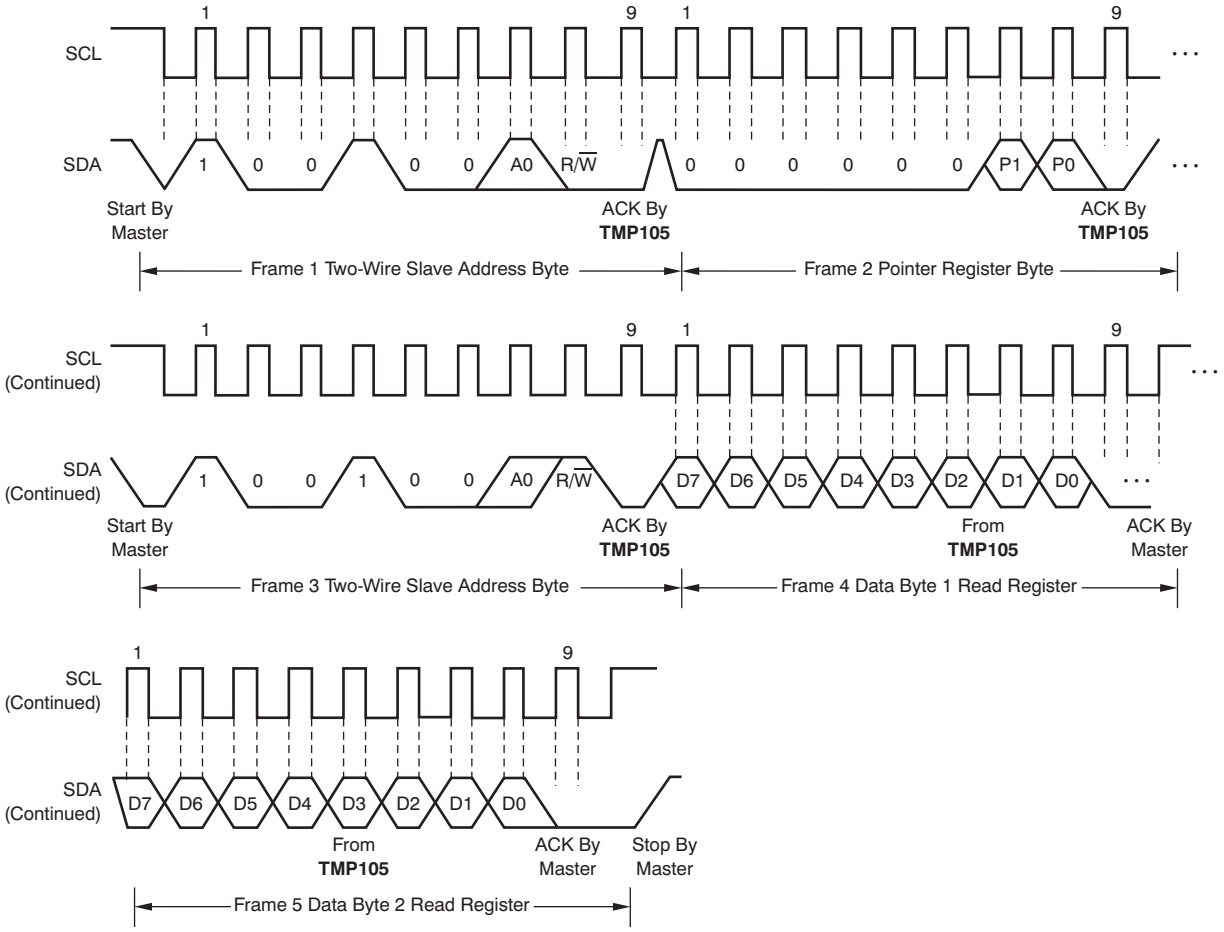


Figure 6. Two-Wire Timing Diagram for Read Word Format

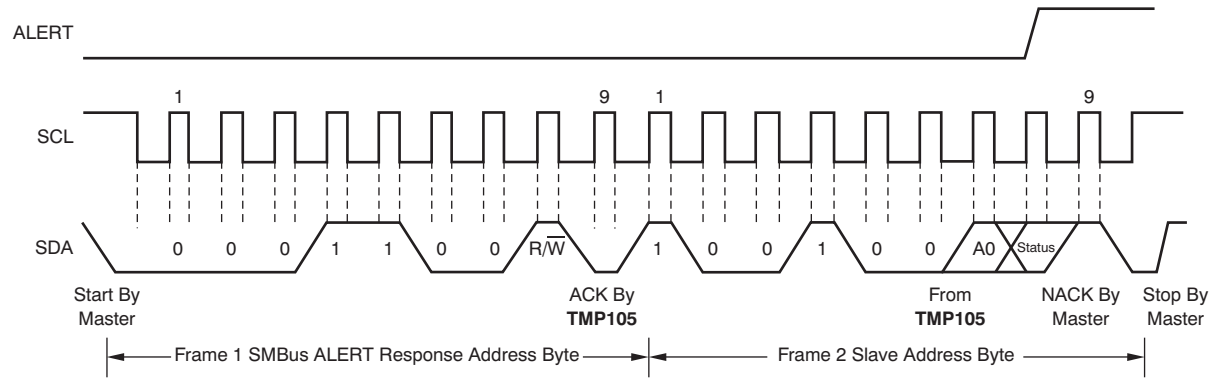


Figure 7. Timing Diagram for SMBus ALERT

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April, 2008) to Revision D **Page**

- Updated document format to current standards 1
- Added *Absolute Maximum Ratings* table 2
- In the Electrical Specifications table, changed from: *DIGITAL INPUT/OUTPUT* to: *DIGITAL INPUT/OUTPUT (SCL, SDA, ALERT)* 3
- In the Electrical Specifications table, added the *DIGITAL INPUT (A0)* section 3
- Changed max spec for V_{IH} logic level 3
- Changed test conditions for leakage input current 3
- Updated *Temperature Accuracy vs Temperature* typical characteristic graph 4
- Added text to the *Application Information* section, first paragraph 5
- Corrected typos in Figure 1 5

Changes from Revision B (January, 2006) to Revision C **Page**

- Added labels to *Temperature Accuracy vs Temperature* typical characteristic graph 4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP105YZCR	ACTIVE	DSBGA	YZC	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EY	Samples
TMP105YZCT	ACTIVE	DSBGA	YZC	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

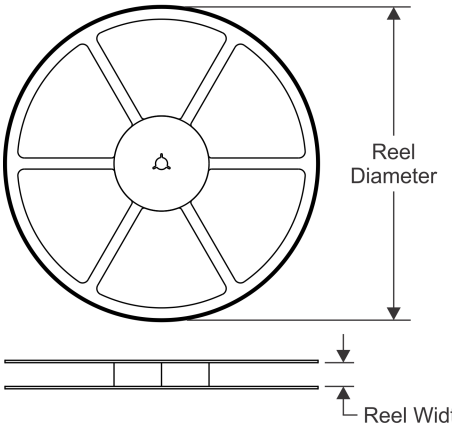
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

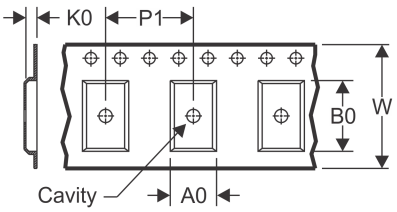
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

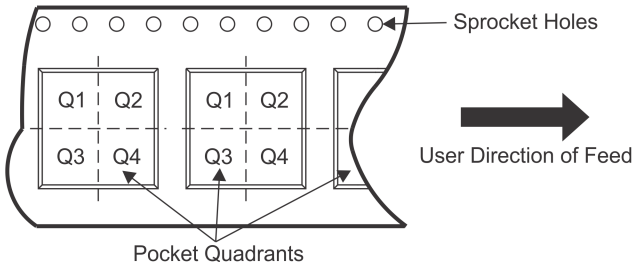


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

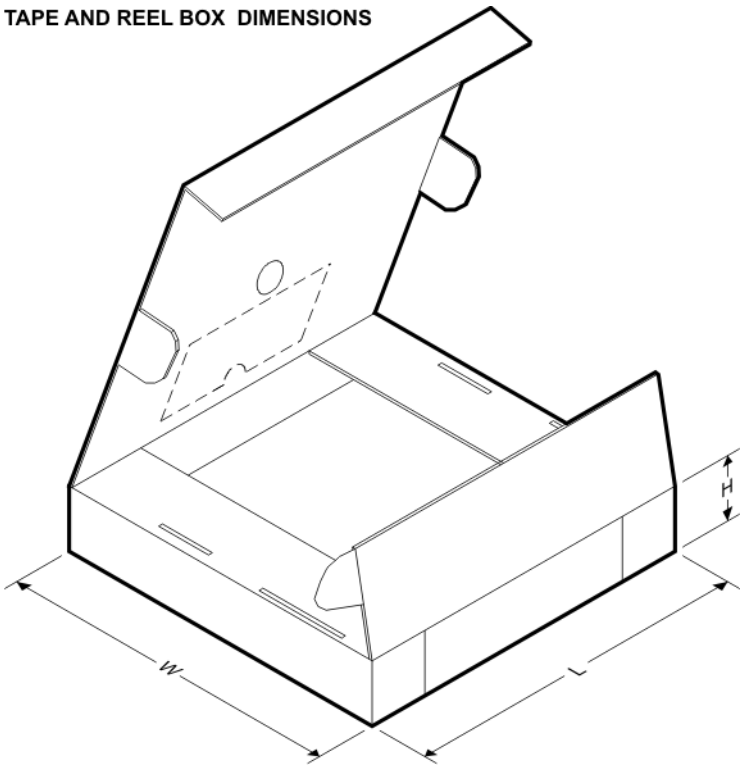
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP105YZCR	DSBGA	YZC	6	3000	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1
TMP105YZCT	DSBGA	YZC	6	250	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

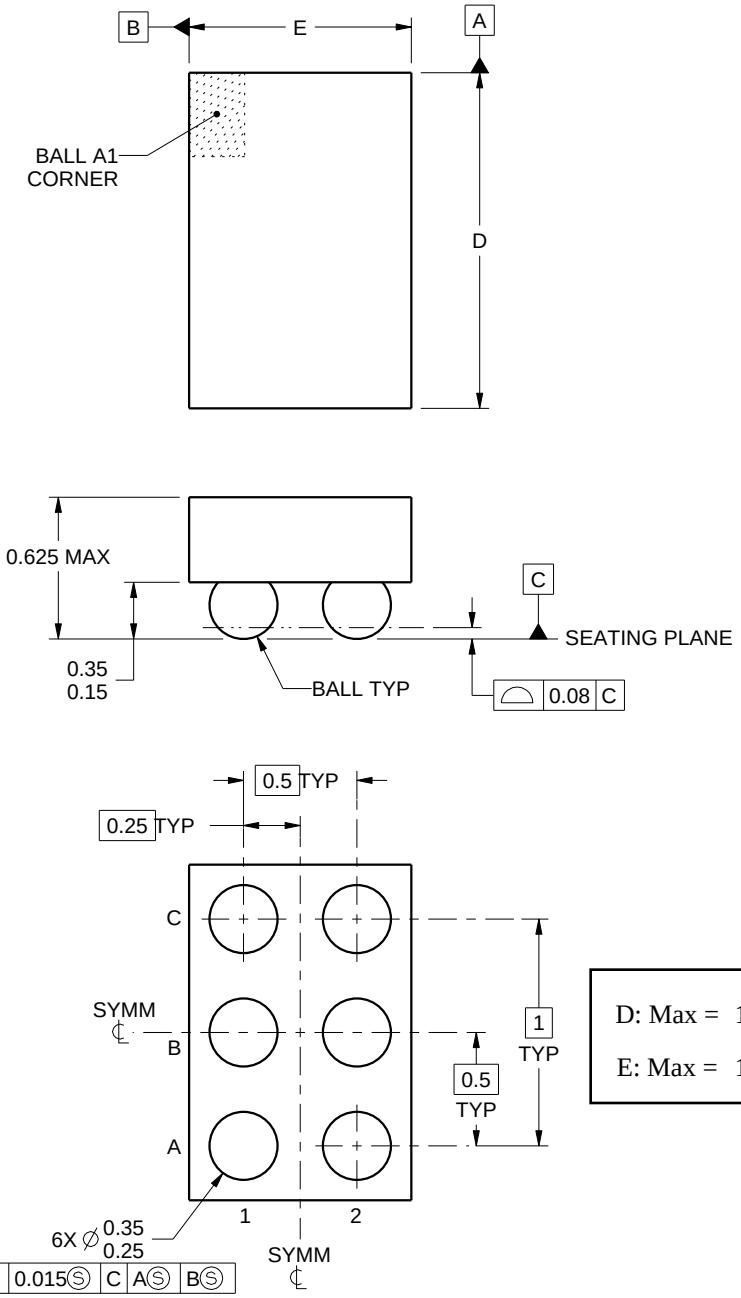
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP105YZCR	DSBGA	YZC	6	3000	220.0	220.0	35.0
TMP105YZCT	DSBGA	YZC	6	250	220.0	220.0	35.0

PACKAGE OUTLINE

YZC0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



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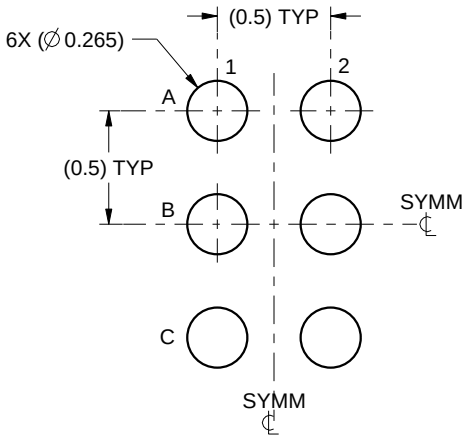
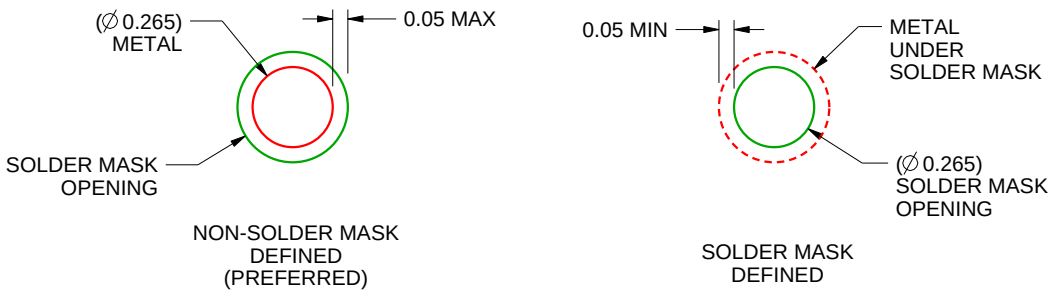
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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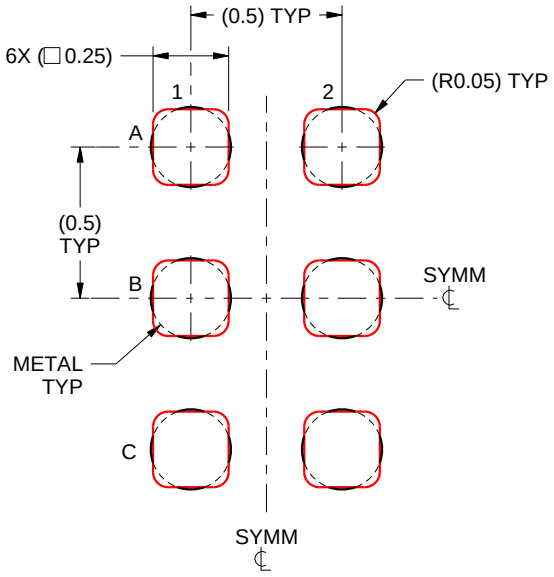
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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