



# THE DATASHEET OF TPIC1021DR



## TPIC1021 LIN Physical Interface

### 1 Features

- LIN Physical Layer Specification Revision 2.0 compliant. Conforms to SAEJ2602 Recommended Practice for LIN
- LIN Bus Speed up to 20 kbps
- ESD Protection to 12 kV (Human Body Model) on LIN Pin
- LIN Pin Handles Voltage from –40 V to 40 V
- Survives Transient Damage in Automotive Environment (ISO 7637)
- Operation with Supply from 7-V to 27-V DC
- Two Operation Modes: Normal and Low-Power (Sleep) Mode
- Low Current Consumption in Low Power Mode
- Wake-Up Available from LIN Bus, Wake-Up Input (External Switch) or Host MCU
- Interfaces to MCU with 5-V or 3.3-V I/O Pins
- Dominant State Timeout Protection on TXD Pin
- Wake-Up Request on RXD Pin
- Control of External Voltage Regulator (INH Pin)
- Integrated Pull-Up Resistor and Series Diode for LIN Slave Applications
- Low EME (Electromagnetic Emissions), High EMI (Electromagnetic Immunity)
- Bus Terminal Short-Circuit Protected for Short to Battery or Short to Ground
- Thermally Protected
- Ground Disconnection Fail-Safe at System Level
- Ground Shift Operation at System Level
- Unpowered Node Does Not Disturb the Network

### 2 Applications

- Industrial Sensing
- White Goods Distributed Control

### 3 Description

The TPIC1021 is the LIN (Local Interconnect Network) physical interface, which integrates the serial transceiver with wake up and protection features. The LIN bus is a single wire, bi-directional bus typically used for low-speed in-vehicle networks using baud rates between 2.4 kbps and 20 kbps.

The LIN bus has two logical values: the dominant state (voltage near ground) represents a logic 0 and the recessive state (voltage near battery) and represents logic 1.

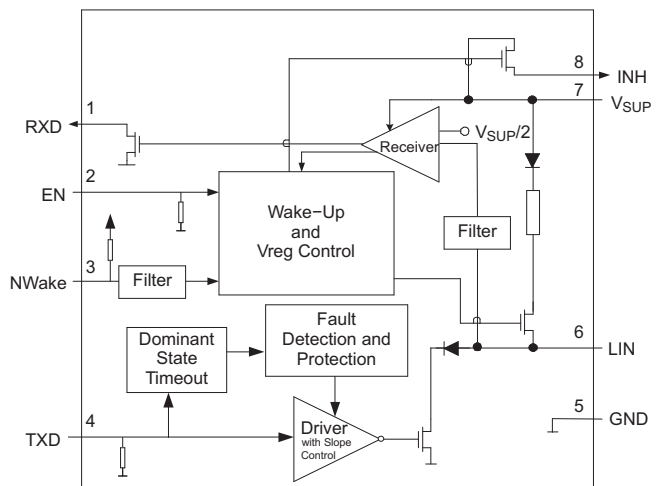
In the recessive state the LIN bus is pulled high by the TPIC1021's internal pull-up resistor (30 k $\Omega$ ) and series diode, so no external pullup components are required for slave applications. Master applications require an external pullup resistor (1 k $\Omega$ ) plus a series diode.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE  | BODY SIZE (NOM)   |
|-------------|----------|-------------------|
| TPIC1021    | SOIC (8) | 4.90 mm x 3.91 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Functional Block Diagram



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## 4 Revision History

### Changes from Revision C (July 2005) to Revision D

**Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... **1**

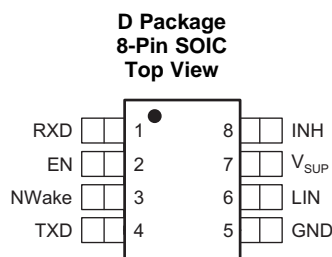
## 5 Description (continued)

The LIN Protocol output data stream on the TXD pin is converted by the TPIC1021 into the LIN bus signal through a current limited, wave-shaping low-side driver with control as outlined by the LIN Physical Layer Specification Revision 2.0. The receiver converts the data stream from the LIN bus and outputs the data stream via the RXD pin.

In Low Power mode, the TPIC1021 requires very low quiescent current even though the wake-up circuits remain active allowing for remote wake up via the LIN bus or local wake ups via NWake or EN pins.

The TPIC1021 has been designed for operation in the harsh automotive environment. The device can handle LIN bus voltage swing from 40 V down to ground and survive  $-40$  V. The device also prevents back feed current through the LIN pin to the supply input in case of a ground shift or supply voltage disconnection. It also features under-voltage, over temperature, and loss of ground protection. In the event of a fault condition the output is immediately switched off and remains off until the fault condition is removed.

## 6 Pin Configuration and Functions



### Pin Functions

| PIN |                  | TYPE   | DESCRIPTION   |
|-----|------------------|--------|---|
| NO. | NAME             |        |   |
| 1   | RXD              | O      | RXD output (open drain) pin interface reporting state of LIN bus voltage                |
| 2   | ED               | I      | Enable input pin  |
| 3   | NWake            | I      | High voltage input pin for device wake up   |
| 4   | TXD              | I      | TXD input pin interface to control state of LIN output                                  |
| 5   | GND              | I      | Ground connection   |
| 6   | LIN              | I/O    | LIN bus pin single wire transmitter and receiver  |
| 7   | V <sub>SUP</sub> | Supply | Device supply pin (connected to battery in series with external reverse blocking diode) |
| 8   | INH              | O      | Inhibit pin controls external voltage regulator with inhibit input                      |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                 |  | MIN  | MAX | UNIT |
|---------------------------------|--|------|-----|------|
| V <sub>SUP</sub> <sup>(2)</sup> | Supply line supply voltage   | 0    | 27  | V    |
|                                 |  | 0    | 40  | V    |
|                                 | NWake DC and transient input voltage (through 33-kΩ serial resistor) | −1   | 40  | V    |
|                                 | Logic pin input voltage (RXD, TXD, EN)                               | −0.3 | 5.5 | V    |
|                                 | LIN DC input voltage   | −40  | 40  | V    |
| T <sub>A</sub>                  | Operational free-air temperature                                     | −40  | 125 | °C   |
| T <sub>J</sub>                  | Junction temperature   | −40  | 150 | °C   |
|                                 | Thermal shutdown   |      | 200 | °C   |
|                                 | Thermal shutdown hysteresis  |      | 25  | °C   |
| T <sub>stg</sub>                | Storage temperature range  | −40  | 165 | °C   |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

### 7.2 ESD Ratings

|                    |                         |  | VALUE              | UNIT   |   |
|--------------------|-------------------------|--|--------------------|--------|---|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)(2)</sup> | LIN pin            | ±12000 | V |
|                    |                         |  | NWake pin          | ±9000  |   |
|                    |                         |  | All other pins     | ±3000  |   |
|                    |                         | Machine model <sup>(3)</sup>   | LIN and NWake pins | ±400   |   |
|                    |                         |  | All other pins     | ±200   |   |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
- (3) The machine model is a 200-pF capacitor through a 10-Ω resistor and a 0.75-μH coil.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                  |                     | MIN | NOM | MAX | UNIT |
|------------------|---------------------|-----|-----|-----|------|
| T <sub>SUP</sub> | Supply voltage      | 7   |     | 27  | V    |
| T <sub>AMB</sub> | Ambient temperature | −40 |     | 125 | °C   |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | TPIC1021 | UNIT |
|-------------------------------|--|----------|------|
|                               |  | D (SOIC) |      |
|                               |  | 8 PINS   |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 145      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 61.9     | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 55.5     | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 14.3     | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 55       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

 $V_{SUP} = 7\text{ V to }27\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

| PARAMETER   |  | TEST CONDITIONS   | MIN                   | TYP <sup>(1)</sup>   | MAX                    | UNIT          |
|---|--|---|-----------------------|----------------------|------------------------|---------------|
| <b>SUPPLY</b>                                       |  |   |                       |                      |                        |               |
|   | Operational supply voltage <sup>(2)</sup>          |   | 7                     | 14                   | 27                     | V             |
|   | Nominal supply line voltage <sup>(2)</sup>         |   | 7                     | 14                   | 18                     | V             |
|   | $V_{SUP}$ undervoltage threshold <sup>(2)</sup>    |   |                       | 4.5                  |                        | V             |
| $I_{CC}$  | Supply Current                                     | Normal Mode, EN = 1, Bus dominant (total bus load > 500 $\Omega$ ) <sup>(3)</sup>                       |                       | 1.2                  | 2.5                    | mA            |
|   |  | Standby Mode, EN = 0, Bus dominant (total bus load > 500 $\Omega$ ) <sup>(3)</sup>                      |                       | 1                    | 2.1                    | mA            |
|   |  | Normal Mode, EN = 1, Bus recessive  |                       | 300                  | 500                    | $\mu\text{A}$ |
|   |  | Standby Mode, EN = 0, Bus recessive   |                       | 300                  | 500                    | $\mu\text{A}$ |
|   |  | Low Power Mode, EN = 0, $V_{SUP} < 14\text{ V}$ , $NW_{Wake} = V_{SUP}$ , $LIN = V_{SUP}$               |                       | 20                   | 50                     | $\mu\text{A}$ |
|   |  | Low Power Mode, EN = 0, $14\text{ V} < V_{SUP} < 27\text{ V}$ , $NW_{Wake} = V_{SUP}$ , $LIN = V_{SUP}$ |                       | 50                   | 100                    | $\mu\text{A}$ |
| <b>RXD OUTPUT PIN</b>                               |  |   |                       |                      |                        |               |
| $V_O$   | Output voltage                                     |   | -0.3                  |                      | 5.5                    | V             |
| $I_{OL}$  | Low-level output current, open drain               | LIN = 0 V, RXD = 0.4 V  | 3.5                   |                      |                        | mA            |
| $I_{IKG}$   | Leakage current, high-level                        | LIN = $V_{SUP}$ , RXD = 5 V   | -5                    | 0                    | 5                      | $\mu\text{A}$ |
| <b>TXD INPUT PIN</b>                                |  |   |                       |                      |                        |               |
| $V_{IL}$  | Low-level input voltage <sup>(2)</sup>             |   | -0.3                  |                      | 0.8                    | V             |
| $V_{IH}$  | High-level input voltage <sup>(2)</sup>            |   | 2                     |                      | 5.5                    | V             |
| $V_{IT}$  | Input threshold hysteresis voltage <sup>(2)</sup>  |   | 30                    |                      | 500                    | mV            |
|   | Pull-down resistor                                 |   | 125                   | 350                  | 800                    | k $\Omega$    |
| $I_{IL}$  | Low-level input current                            | TXD = 0   | -5                    | 0                    | 5                      | $\mu\text{A}$ |
| <b>LIN PIN (Referenced to <math>V_{SUP}</math>)</b> |  |   |                       |                      |                        |               |
| $V_{OH}$  | High-level output voltage <sup>(2)</sup>           | LIN recessive, TXD = High, $I_O = 0\text{ mA}$  | $V_{SUP}-1\text{V}$   |                      |                        | V             |
| $V_{OL}$  | Low-level output voltage <sup>(2)</sup>            | LIN dominant, TXD = Low, $I_O = 40\text{ mA}$   | 0                     |                      | $0.2 \times V_{SUP}$   | V             |
|   | Pull-up resistor to $V_{SUP}$                      |   | 20                    | 30                   | 60                     | k $\Omega$    |
| $I_L$   | Limiting current                                   | TXD = Low   | 50                    | 150                  | 250                    | mA            |
| $I_{IKG}$   | Leakage current                                    | LIN = $V_{SUP}$   | -5                    | 0                    | 5                      | $\mu\text{A}$ |
| $V_{IL}$  | Low-level input voltage <sup>(2)</sup>             | LIN dominant  | $0 \times V_{SUP}$    |                      | $0.4 \times V_{SUP}$   | V             |
| $V_{IH}$  | High-level input voltage <sup>(2)</sup>            | LIN recessive   | $0.6 \times V_{SUP}$  |                      | $V_{SUP}$              | V             |
| $V_{IT}$  | Input threshold voltage <sup>(2)</sup>             |   | $0.4 \times V_{SUP}$  | $0.5 \times V_{SUP}$ | $0.6 \times V_{SUP}$   | V             |
| $V_{hys}$   | Hysteresis voltage <sup>(2)</sup>                  |   | $0.05 \times V_{SUP}$ |                      | $0.175 \times V_{SUP}$ | V             |
| $V_{IL}$  | Low-level input voltage for wake-up <sup>(2)</sup> |   | 0                     |                      | $0.4 \times V_{SUP}$   | V             |
| <b>EN PIN</b>                                       |  |   |                       |                      |                        |               |
| $V_{IL}$  | Low-level input voltage <sup>(2)</sup>             |   | -0.3                  |                      | 0.8                    | V             |
| $V_{IH}$  | High-level input voltage <sup>(2)</sup>            |   | 2                     |                      | 5.5                    | V             |
| $V_{hys}$   | Hysteresis voltage <sup>(2)</sup>                  |   | 30                    |                      | 500                    | mV            |
|   | Pull-down resistor                                 |   | 125                   | 350                  | 800                    | k $\Omega$    |
| $I_{IL}$  | Low-level input current                            | EN = 0 V  | -5                    | 0                    | 5                      | $\mu\text{A}$ |
| <b>INH PIN</b>                                      |  |   |                       |                      |                        |               |

(1) Typical values are give for  $V_{SUP} = 14\text{ V}$  at  $25^\circ\text{C}$ .

(2) All voltages are defined with respect to ground; positive currents flow into the TPIC1021 device.

(3) In the dominant state the supply current increases as the supply voltage increases due to the integrated LIN slave termination resistance. At higher voltages the majority of supply current is through the termination resistance. The minimum resistance of the LIN slave termination is 20 k $\Omega$  so the maximum supply current attributed to the termination is:  $I_{SUP}(\text{dom}) \text{ max termination} \approx (V_{SUP} - (V_{LIN\_Dominant} + 0.7\text{ V}) / 20\text{ k}\Omega$ .

## Electrical Characteristics (continued)

 $V_{SUP} = 7\text{ V to }27\text{ V}$ ,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$  (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS   | MIN         | TYP <sup>(1)</sup> | MAX           | UNIT             |
|--|---|-------------|--------------------|---------------|------------------|
| $V_O$ DC output voltage                          | Transient voltage   | -0.3        |                    | $V_{SUP}+0.3$ | V                |
| $I_O$ Output current                             |   | -50         |                    | 2             | mA               |
| $R_{on}$ On state resistance                     | Between $V_{SUP}$ and INH, INH = 2 mA drive, Normal or Standby Mode | 25          | 40                 | 100           | $\Omega$         |
| $I_{IKG}$ Leakage current                        | Low Power mode, $0 < INH < V_{SUP}$                                 | -5          | 0                  | 5             | $\mu\text{A}$    |
| <b>NWake PIN</b>                                 |   |             |                    |               |                  |
| $V_{IL}$ Low-level input voltage <sup>(2)</sup>  |   | -0.3        |                    | $V_{SUP}-3.3$ | V                |
| $V_{IH}$ High-level input voltage <sup>(2)</sup> |   | $V_{SUP}-1$ |                    | $V_{SUP}+0.3$ | V                |
| Pull-up current                                  | NWake = 0 V   | -40         | -10                | -4            | $\mu\text{A}$    |
| $I_{IKG}$ Leakage current                        | $V_{SUP} = \text{NWake}$  | -5          | 0                  | 5             | $\mu\text{A}$    |
| <b>THERMAL SHUTDOWN</b>                          |   |             |                    |               |                  |
| Shutdown junction thermal temperature            |   |             | 185                |               | $^\circ\text{C}$ |

## 7.6 Timing Requirements

|               |   | MIN   | NOM | MAX   | UNIT                 |
|---------------|---|---|-----|-------|----------------------|
| D1            | Duty cycle 1 <sup>(1)</sup> (2)                                 | $T_{HREC(max)} = 0.744 \times V_{SUP}$ , $T_{HDOM(max)} = 0.581 \times V_{SUP}$ , $V_{SUP} = 7.0\text{ V to }18\text{ V}$ , $t_{BIT} = 50\ \mu\text{s}$ (20 kbps), See <a href="#">Figure 1</a>   |     | 0.396 |                      |
| D2            | Duty cycle 2 <sup>(1)</sup> (2)                                 | $T_{HREC(max)} = 0.284 \times V_{SUP}$ , $T_{HDOM(max)} = 0.422 \times V_{SUP}$ , $V_{SUP} = 7.6\text{ V to }18\text{ V}$ , $t_{BIT} = 50\ \mu\text{s}$ (20 kbps), See <a href="#">Figure 1</a>   |     | 0.581 |                      |
| D3            | Duty cycle 3 <sup>(1)</sup> (2)                                 | $T_{HREC(max)} = 0.778 \times V_{SUP}$ , $T_{HDOM(max)} = 0.616 \times V_{SUP}$ , $V_{SUP} = 7.0\text{ V to }18\text{ V}$ , $t_{BIT} = 96\ \mu\text{s}$ (10.4 kbps), See <a href="#">Figure 1</a> |     | 0.417 |                      |
| D4            | Duty cycle 4 <sup>(1)</sup> (2)                                 | $T_{HREC(max)} = 0.251 \times V_{SUP}$ , $T_{HDOM(max)} = 0.389 \times V_{SUP}$ , $V_{SUP} = 7.6\text{ V to }18\text{ V}$ , $t_{BIT} = 96\ \mu\text{s}$ (10.4 kbps), See <a href="#">Figure 1</a> |     | 0.590 |                      |
| $t_{rx\_pdr}$ | Receiver rising propagation delay time                          | $R_L = 2.4\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See <a href="#">Figure 1</a>  |     | 6     | $\mu\text{s}$        |
| $t_{rx\_pdf}$ | Receiver rising propagation delay time                          | $R_L = 2.4\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , See <a href="#">Figure 1</a>  |     | 6     | $\mu\text{s}$        |
| $t_{rx\_sym}$ | Symmetry of receiver propagation delay time (rising edge)       | with respect to falling edge, See <a href="#">Figure 1</a>  |     | -2    | 2 $\mu\text{s}$      |
| $t_{NWake}$   | NWake filter time for local wake-up                             | See <a href="#">Figure 1</a>  |     | 25    | 50 100 $\mu\text{s}$ |
| $t_{LINBUS}$  | LIN wake-up filter time (dominant time for wake-up via LIN bus) | See <a href="#">Figure 1</a>  |     | 25    | 50 100 $\mu\text{s}$ |
| $t_{DST}$     | Dominant state timeout <sup>(3)</sup>                           | See <a href="#">Figure 1</a>  |     | 6     | 9 14 ms              |

(1) Duty cycle =  $t_{BUS\_rec(min)} / (2 \times t_{BIT})$

(2) Duty Cycles: LIN Driver bus load conditions (CLINBUS, RLINBUS): Load1 = 1 nF, 1 k $\Omega$ ; Load2 = 6.8 nF, 660  $\Omega$ ; Load3 = 10 nF, 500  $\Omega$ . Duty Cycles 3 and 4 are defined for 10.4 kbps operation. The TPIC1021 also meets these lower speed requirements, while it is capable of the higher speed 20.0 kbps operation as specified by Duty Cycles 1 and 2. SAEJ2602 derives propagation delay equations from the LIN 2.0 duty cycle definitions, for details please refer to the SAEJ2602 specification.

(3) Dominant state timeout will limit the minimum data rate to 2.4 kbps.

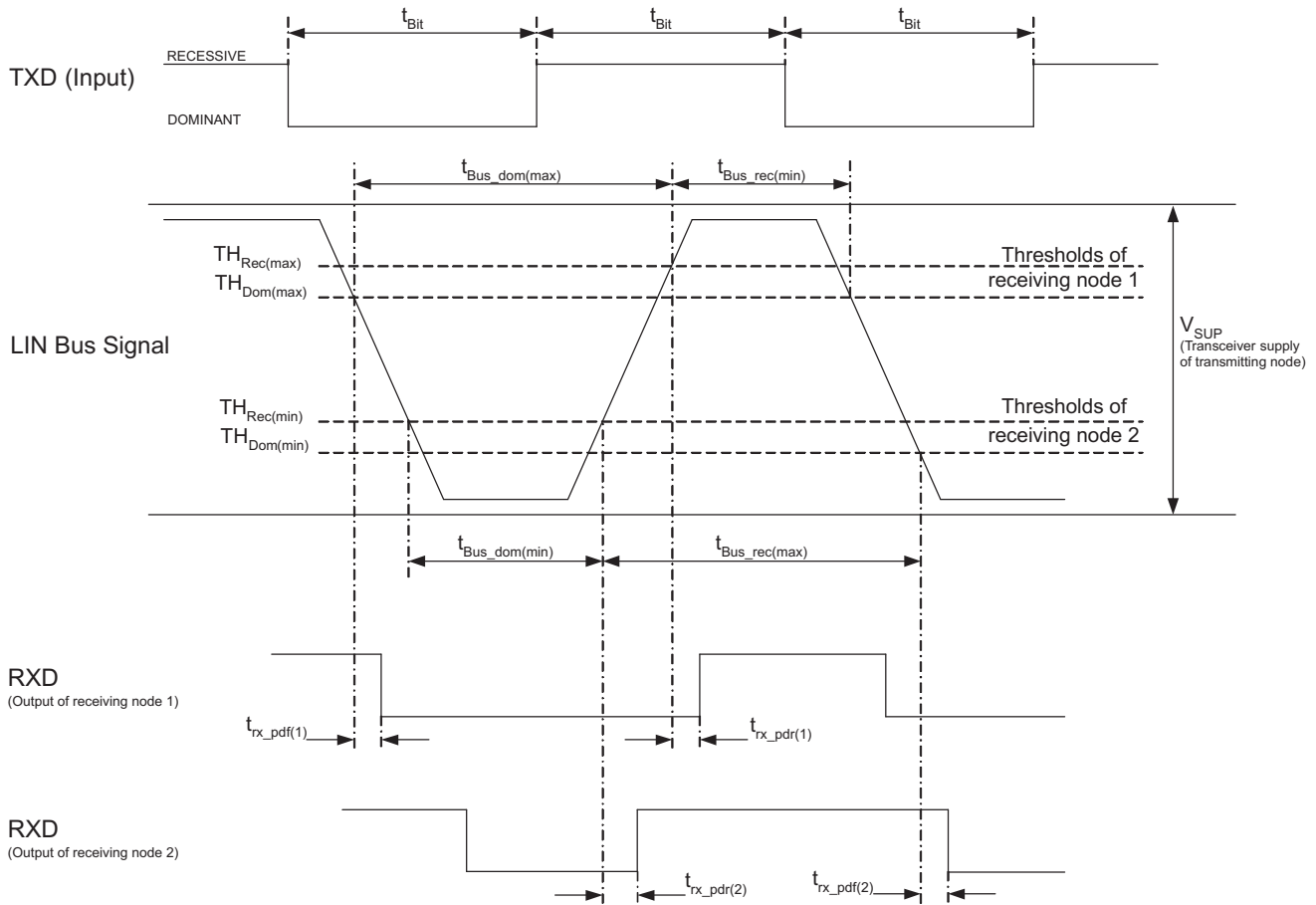


Figure 1. Definition of Bus Timing Parameters

## 7.7 Typical Characteristics

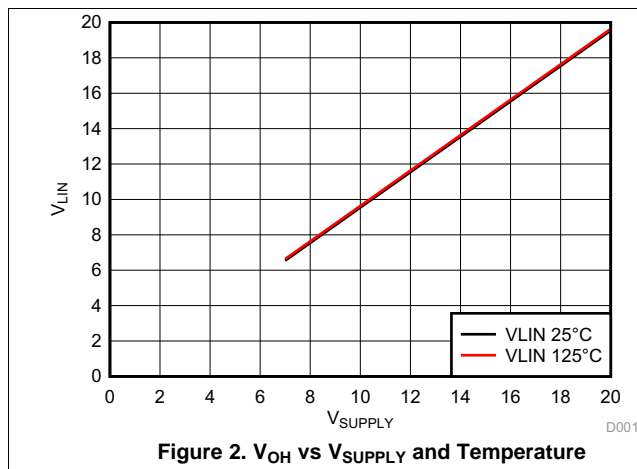


Figure 2.  $V_{OH}$  vs  $V_{SUPPLY}$  and Temperature

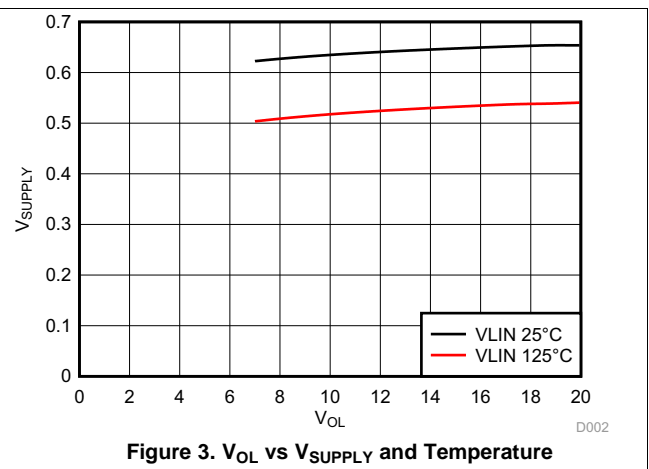


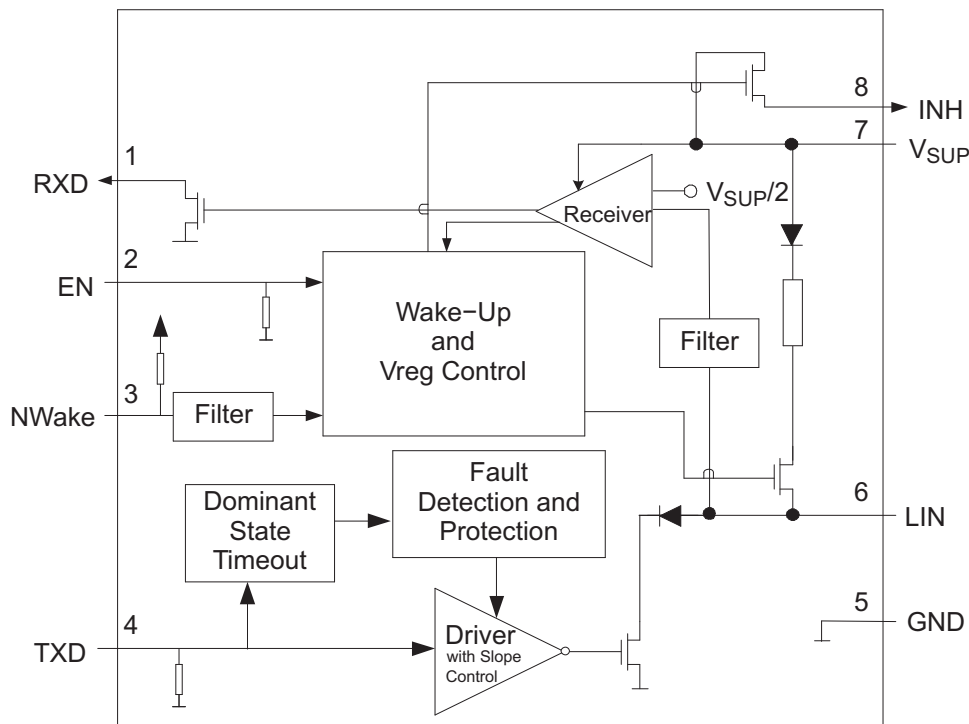
Figure 3.  $V_{OL}$  vs  $V_{SUPPLY}$  and Temperature

## 8 Detailed Description

### 8.1 Overview

The TPIC1021 is a LIN (Local Interconnect Network) physical layer transceiver which integrates a serial transceiver with wake up and protection features. The LIN bus is a single wire, bi-directional bus that typically is used in low speed in vehicle networks with data rates that range from 2.4 kbps to 20 kbps.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 LIN Bus Pin

This I/O pin is the single-wire LIN bus transmitter and receiver.

##### 8.3.1.1 Transmitter Characteristics

The driver is a low side transistor with internal current limitation and thermal shutdown. There is an internal 30-k $\Omega$  pull-up resistor with a serial diode structure to  $V_{sup}$  so no external pull-up components are required for LIN slave mode applications. An external pull-up resistor of 1 k $\Omega$  plus a series diode to  $V_{sup}$  must be added when the device is used for master node applications.

Voltage on the LIN pin can go from -40 V to +40 V DC without any currents other than through the pull-up resistance. There are no reverse currents from the LIN bus to supply ( $V_{sup}$ ), even in the event of a ground shift or loss of supply ( $V_{sup}$ ).

The LIN thresholds and AC parameters are compatible LIN Protocol Specification Revision 2.0.

During a thermal shut down condition the driver is disabled.

##### 8.3.1.2 Receiver Characteristics

The characteristic thresholds of the receiver are ratio-metric with the device supply pin. Typical thresholds are 50%, with a hysteresis between 5% and 17.5% of supply.

## Feature Description (continued)

### 8.3.2 Transmit Input Pin (TXD)

This pin is the interface to the MCU's LIN Protocol Controller or SCI/UART used to control the state of the LIN output. When TXD is low, LIN output is dominant (near ground). When TXD is high, LIN output is recessive (near battery). TXD input structure is compatible with microcontrollers with 3.3 V and 5.0 V I/O. This pin has an internal pull-down resistor.

#### 8.3.2.1 TXD Dominant State Timeout

If the TXD pin is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by TPIC1021's Dominant State Timeout Timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on the TXD pin for longer than  $t_{DST}$ , the transmitter is disabled thus allowing the LIN bus to return to the recessive state and communication to resume on the bus. The timer is reset by a rising edge on TXD pin.

### 8.3.3 Receive Output Pin (RXD)

This pin is the interface to the LIN protocol controller or SCI/UART of the MCU, which reports the state of the LIN bus voltage. LIN recessive (near battery) is represented by a high level on RXD and LIN dominant (near ground) is represented by a low level on RXD. The RXD output structure is an open-drain output stage. This allows the TPIC1021 to be used with 3.3 V and 5 V I/O microcontrollers. If the microcontroller's RXD pin does not have an integrated pull-up, an external pull-up resistor to the microcontroller I/O supply voltage is required.

#### 8.3.3.1 RXD Wake-up Request

When the TPIC1021 has been in low power mode and encounters a wake-up event from the LIN bus or NWake pin the RXD pin will go LOW while the device enters and remains in Standby Mode (until EN is re-asserted high and the device enters Normal Mode).

### 8.3.4 Ground (GND)

This is the TPIC1021 device ground connection. The TPIC1021 can operate with a ground shift as long as the ground shift does not reduce  $V_{SUP}$  below the minimum operating voltage. If there is a loss of ground at the ECU level, the TPIC1021 will not have a significant current consumption on the LIN pin while in the recessive state (<100  $\mu$ A sourced via the LIN pin) and for the dominant state the pull-up resistor should be active.

### 8.3.5 Enable Input Pin (EN)

The enable input pin controls the operation mode of the TPIC1021 (Normal or Low Power Mode). When enable is high, the TPIC1021 is in normal mode allowing a transmission path from TXD to LIN and from LIN to RXD. When the enable input is low, the device is put into low power (sleep) mode and there are no transmission paths. The device can enter normal operating mode only after being woken up. The enable pin has an internal pull-down resistor to ensure the device remains in low power mode even if the enable pin floats.

### 8.3.6 NWake Input Pin (NWake)

The NWake input pin is a high-voltage input used to wake up the TPIC1021 from low power mode. NWake is usually connected to an external switch in the application. A falling edge on NWake with a low that is asserted longer than the filter time ( $t_{NWAKE}$ ) results in a local wake-up. The NWake pin provides an internal pull-up current source to  $V_{SUP}$ .

### 8.3.7 Inhibit Output Pin (INH)

The inhibit output pin is used to control an external voltage regulator that has an inhibit input. When the TPIC1021 is in normal operating mode, the inhibit high-side switch is enabled and the external voltage regulator is activated. When TPIC1021 is in low power mode, the inhibit switch is turned off, which disables the voltage regulator. A wake-up event on for the TPIC1021 will return the INH pin to  $V_{SUP}$  level. The INH pin output current is limited to 2 mA. The INH pin can also drive an external transistor connected to an MCU interrupt input.

## 8.4 Device Functional Modes

### 8.4.1 Operating States

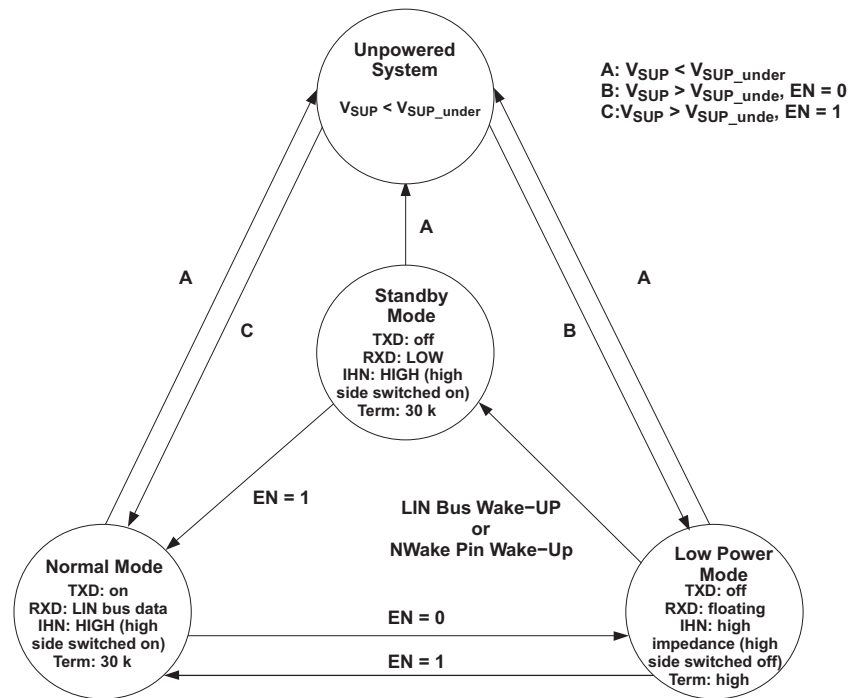


Figure 4. Operating States Diagram

Table 1. Operating Modes

| MODE      | EN | RXD          | LIN BUS TERMINATION | INH            | TRANSMITTER | COMMENTS   |
|-----------|----|--------------|---------------------|----------------|-------------|--|
| Low Power | 0  | Floating     | High impedance      | High impedance | Off         |  |
| Standby   | 0  | Low          | 30 kΩ (typical)     | High           | Off         | Wake-up event detected, waiting on MCU to set EN |
| Normal    | 1  | LIN bus data | 30 kΩ (typical)     | High           | On          |  |

#### 8.4.1.1 Normal Mode

This is the normal operational mode where the receiver and driver are active. The receiver detects the data stream on the LIN bus and outputs it on the RXD pin for the LIN controller where recessive on the LIN bus is a digital high and dominate on the LIN bus is digital low. The driver will transmit input data on the TXD pin to the LIN bus.

### 8.4.1.2 Low Power Mode

The power saving mode for the TPIC1021 and the default state after power-up (assuming EN=0). Even with the extremely low current consumption in this mode, the TPIC1021 can still wake-up from LIN bus activity, a falling edge on the NWake pin or if EN is set high. The LIN bus and NWake pins are filtered to prevent false wake-up events. The wake-up events must be active for their respective time periods:  $t_{LINBUS}$ ,  $t_{NWake}$ .

The low power mode is entered by setting the EN pin low.

While the device is in low power mode the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short-circuited to ground).
- The normal receiver is disabled.
- The INH pin is high impedance.
- EN input, NWake input and the LIN wake-up receiver are active.

### 8.4.1.3 Wake-Up Events

There are three ways to wake-up the TPIC1021 from Low Power Mode.

- Remote wake-up via recessive (high) to dominant (low) state transition on LIN Bus where dominant bus state of 50% threshold is detected. The dominant state must be held for  $t_{LINBUS}$  filter time (to eliminate false wake ups from disturbances on the LIN Bus).
- Local wake-up via falling edge on NWake pin which is held low for filter time  $t_{NWake}$  (to eliminate false wake ups from disturbances on NWake).
- Local wake-up via EN being set high

### 8.4.1.4 Standby Mode

This mode is entered whenever a wake-up event occurs via the LIN bus or NWake pin while the TPIC1021 is in low power mode. The LIN bus slave termination circuit and the INH pin are turned on when standby mode is entered. The application system will power up once the INH pin is driven high assuming it is using a voltage regulator connected via INH pin. Standby Mode is signaled via a low level on RXD pin.

When EN pin is set high while the TPIC1021 is in Standby Mode the device returns to Normal Mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are turned on.

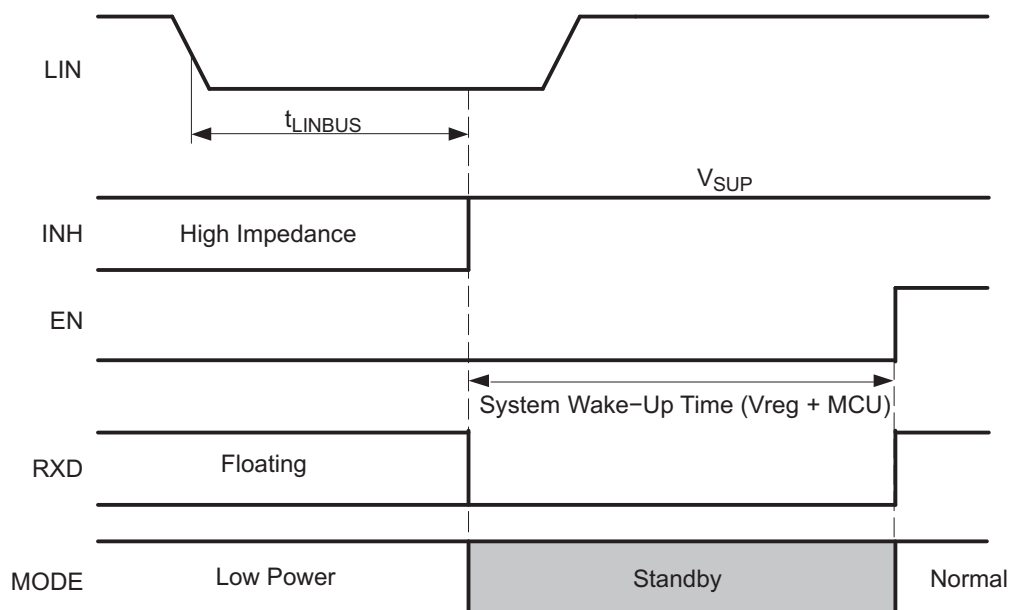
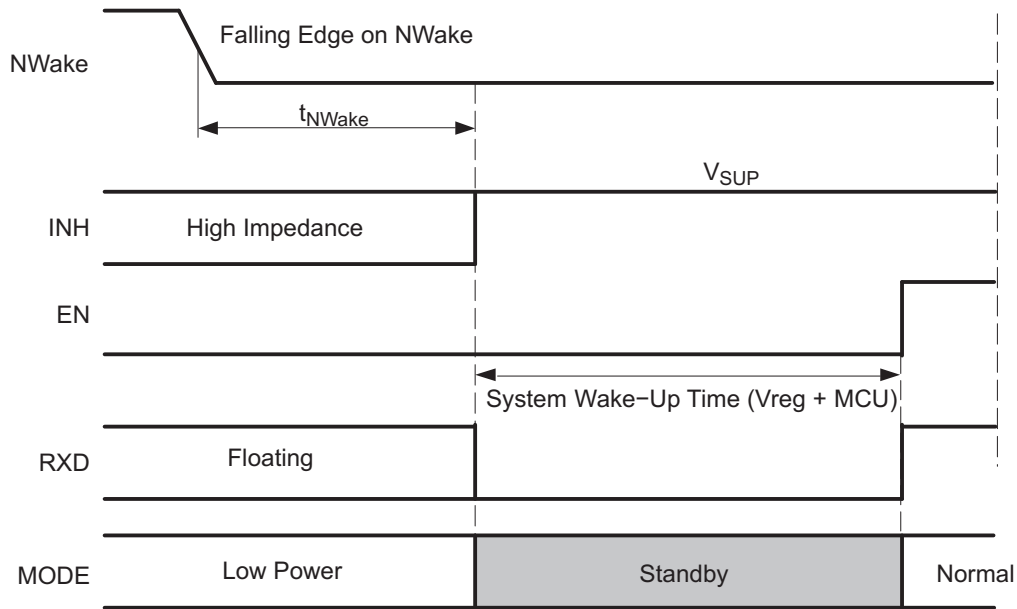


Figure 5. Wake-Up Via LIN Bus Timing Diagram



**Figure 6. Wake-Up Via NWake Timing Diagram**

#### 8.4.2 Supply Voltage ( $V_{SUP}$ )

This is the TPIC1021 device power supply pin. This pin is connected to the battery through an external reverse battery blocking diode. The continuous DC operating voltage range for the TPIC1021 is from 7 V to +27 V. The  $V_{SUP}$  is protected for harsh automotive conditions of up to +40 V.

The device contains a reset circuit to avoid false bus messages during undervoltage conditions when  $V_{SUP}$  is less than  $V_{SUP\_UNDER}$ .

## 9 Application and Implementation

### NOTE

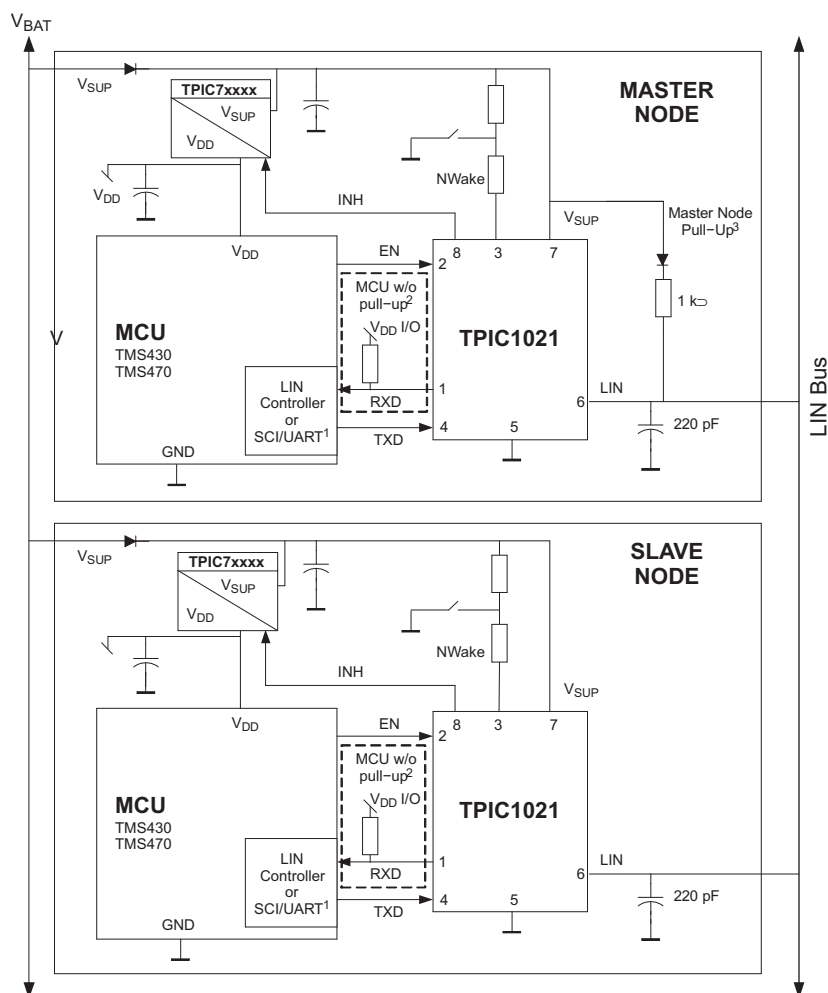
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPIC1021 can be used as both a slave device and a master device in a LIN network. It comes with the ability to support both remote wake-up requests and local wake-up requests.

### 9.2 Typical Application

The device comes with an integrated 30-k $\Omega$  pullup resistor and series diode for slave applications, and for master applications an external 1-k $\Omega$  pullup with series blocking diode can be used. Figure 7 shows the device being used in both types of applications.



- (1) See 1 in the [Design Requirements](#) section
- (2) See 2 in the [Design Requirements](#) section
- (3) See 3 in the [Design Requirements](#) section

Figure 7. Typical Application Schematic

## Typical Application (continued)

### 9.2.1 Design Requirements

For this design, use these requirements:

1. RXD on MCU or LIN Slave has internal pullup, no external pullup resistor is needed.
2. RXD on MCU or LIN Slave without internal pull-up, requires external pullup resistor.
3. Master Node applications require an external 1-k $\Omega$  pullup resistor and serial diode.

### 9.2.2 Detailed Design Procedure

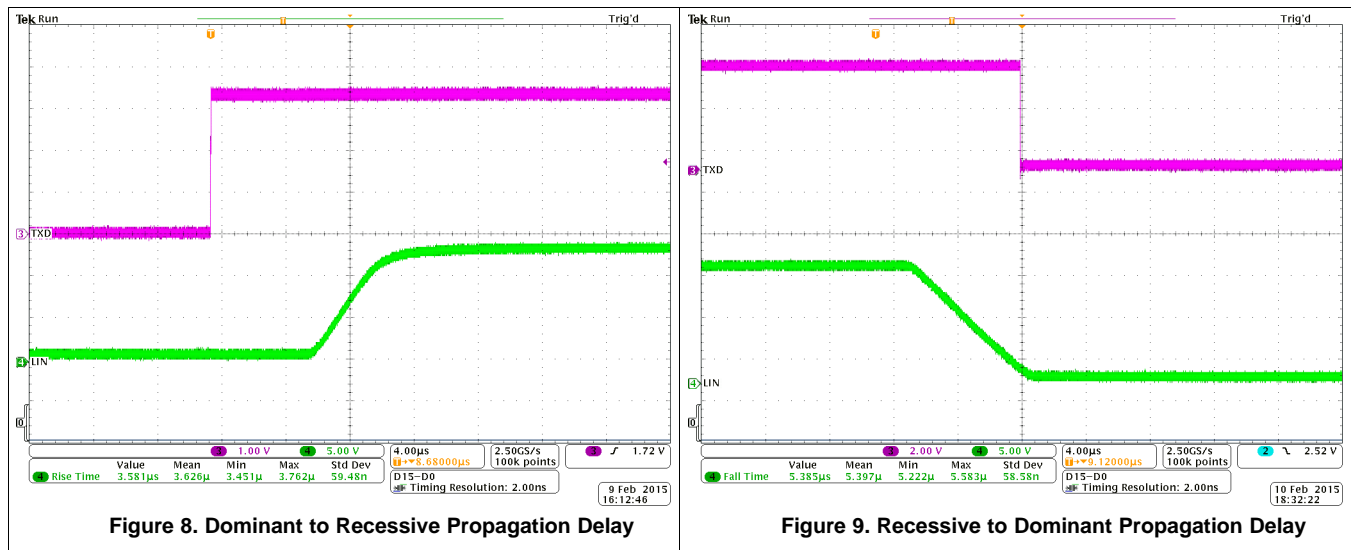
The RXD output structure is an open-drain output stage. This allows the TPIC1021 to be used with 3.3-V and 5-V I/O microcontrollers. If the RXD pin of the microcontroller does not have an integrated pull-up, an external pullup resistor to the microcontroller I/O supply voltage is required.

The  $V_{SUP}$  pin of the device should be decoupled with a 100-nF capacitor as close to the supply pin of the device as possible.

The NWAKE pin is a high voltage wake-up input to the device. If this pin is not being used it should be tied to  $V_{SUP}$ .

### 9.2.3 Application Curves

Figure 8 and Figure 9 show the propagation delay from the TXD pin to the LIN pin for both the recessive to dominant and dominant to recessive states under lightly loaded conditions.



## 10 Power Supply Recommendations

The TPIC1021 was designed to operate directly off car battery, or any other DC supply ranging from 7 V to 27 V. A 100-nF decoupling capacitor should be placed as close to the  $V_{SUP}$  pin of the device as possible.



## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| TPIC1021D        | NRND          | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | T1021                   |         |
| TPIC1021DG4      | NRND          | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | T1021                   |         |
| TPIC1021DR       | NRND          | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | T1021                   |         |
| TPIC1021DRG4     | NRND          | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   |              | T1021                   |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPIC1021DR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TPIC1021DRG4 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPIC1021DR   | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| TPIC1021DRG4 | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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