



**THE DATASHEET OF  
TPIC6A596DWG4**



# TPIC6A596 POWER LOGIC 8-BIT SHIFT REGISTER

SLIS094A – MARCH 2000 – REVISED MAY 2005

- Low  $r_{DS(on)}$  . . . 1  $\Omega$  Typ
- Output Short-Circuit Protection
- Avalanche Energy . . . 75 mJ
- Eight 350-mA DMOS Outputs
- 50-V Switching Capability
- Enhanced Cascading for Multiple Stages
- All Registers Cleared With Single Input
- Low Power Consumption

## description

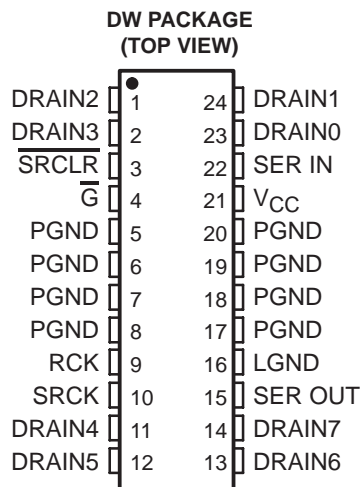
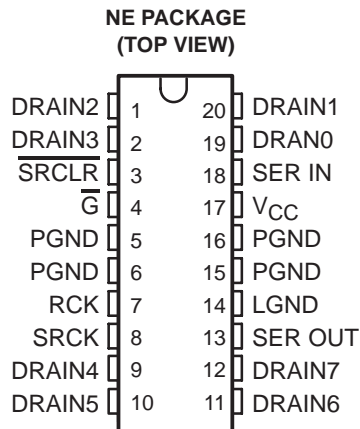
The TPIC6A596 is a monolithic, high-voltage, high-current power logic 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit, D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ( $\overline{SRCLR}$ ) is high. When  $\overline{SRCLR}$  is low, all registers in the device are cleared. When output enable  $\overline{G}$  is held high, all data in the output buffers is held low and all drain outputs are off. When  $\overline{G}$  is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and a 350-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6A596 is offered in a thermally-enhanced dual-in-line (NE) package and a wide-body surface-mount (DW) package. The TPIC6A596 is characterized for operation over the operating case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

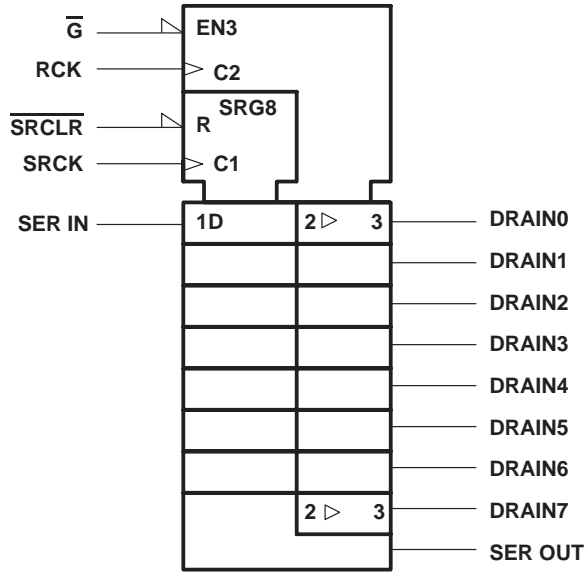
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# TPIC6A596 POWER LOGIC 8-BIT SHIFT REGISTER

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## logic symbol†

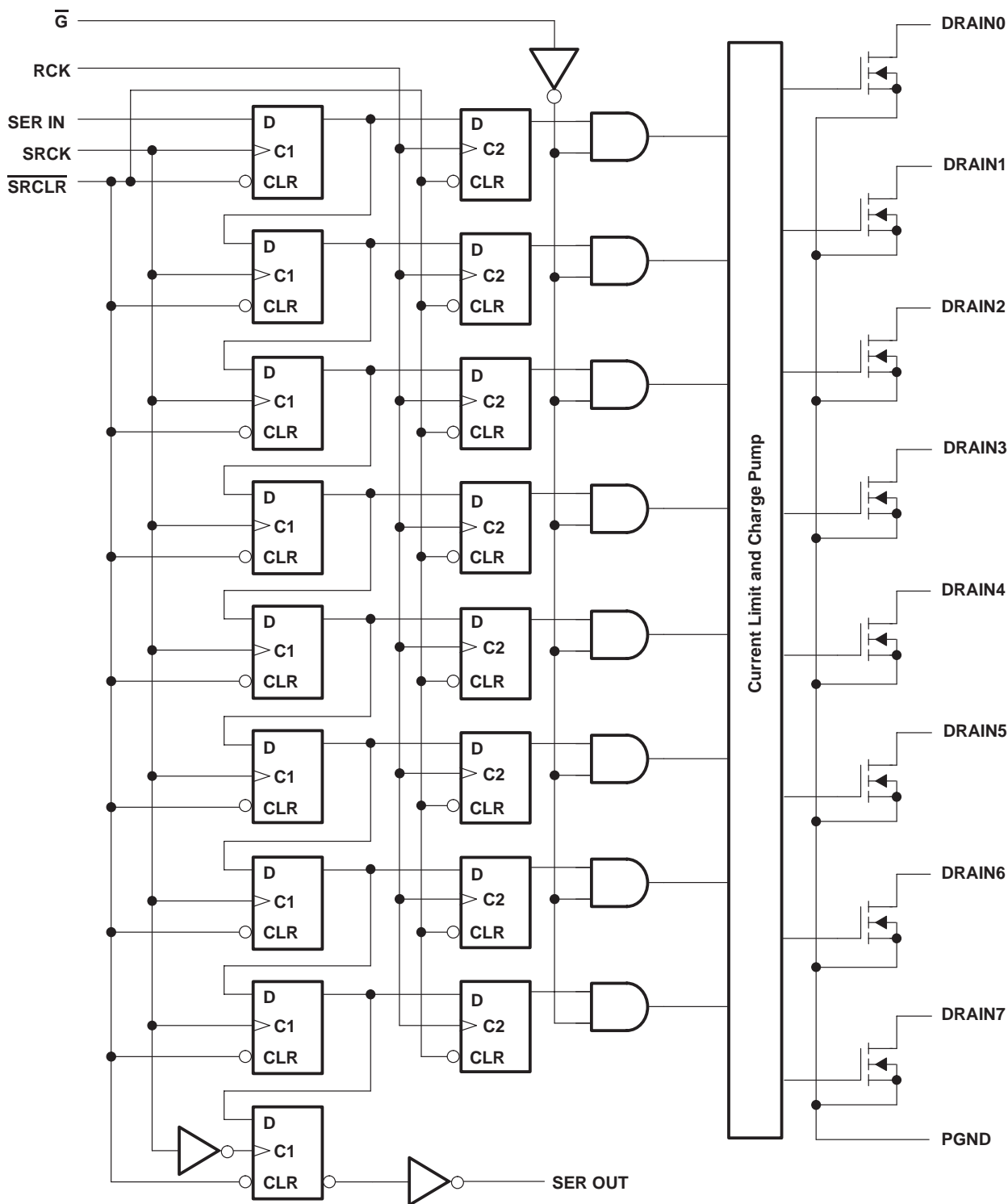


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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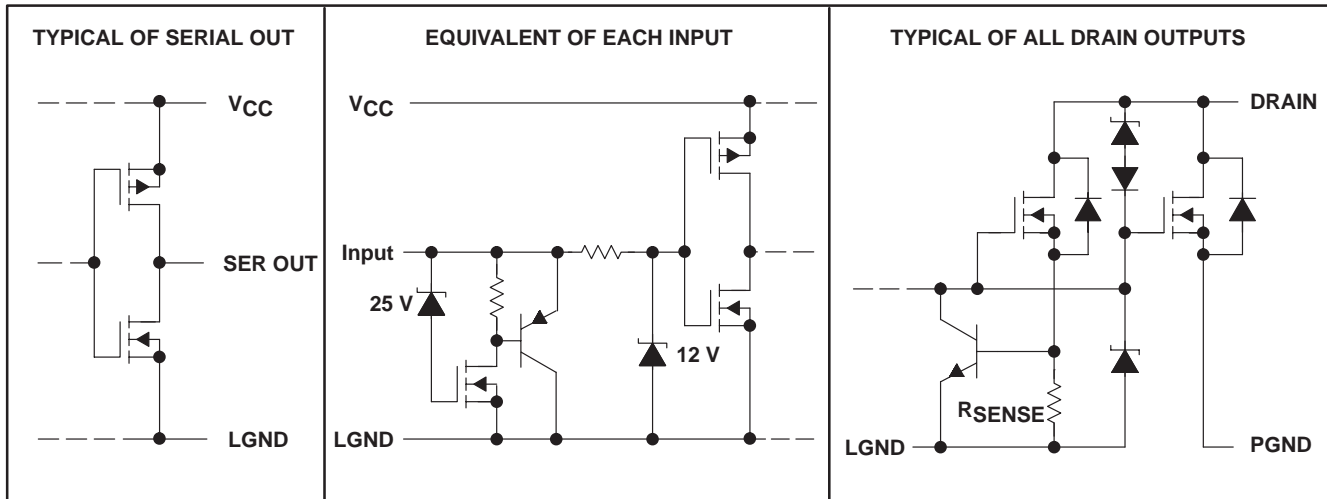
logic diagram (positive logic)



# TPIC6A596 POWER LOGIC 8-BIT SHIFT REGISTER

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## schematic of inputs and outputs



## absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, $V_{CC}$ (see Note 1)	7 V
Logic input voltage range, $V_I$	-0.3 V to 7 V
Power DMOS drain-to-source voltage, $V_{DS}$ (see Note 2)	50 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current (see Note 3)	2 A
Pulsed drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25^\circ\text{C}$ (see Note 3)	1.1 A
Continuous drain current, each output, all outputs on, $I_{Dn}$ , $T_A = 25^\circ\text{C}$	350 mA
Peak drain current, single output, $T_A = 25^\circ\text{C}$ (see Note 3)	1.1 A
Single-pulse avalanche energy, $E_{AS}$ (see Figure 6)	75 mJ
Avalanche current, $I_{AS}$ (see Note 4)	600 mA
Continuous total dissipation	See Dissipation Rating Table
Operating case temperature range, $T_C$	-40°C to 125°C
Operating virtual junction temperature range, $T_J$	-40°C to 150°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to LGND and PGND.  
 2. Each power DMOS source is internally connected to PGND.  
 3. Pulse duration  $\leq 100 \mu\text{s}$  and duty cycle  $\leq 2\%$ .  
 4. DRAIN supply voltage = 15 V, starting junction temperature ( $T_{JS}$ ) = 25°C,  $L = 210 \text{ mH}$ ,  $I_{AS} = 600 \text{ mA}$  (see Figure 6).

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$ POWER RATING
DW	1750 mW	14 mW/°C	350 mW
NE	2500 mW	20 mW/°C	500 mW

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## recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, $V_{CC}$	4.5	5.5	V
High-level input voltage, $V_{IH}$	$0.85 V_{CC}$	$V_{CC}$	V
Low-level input voltage, $V_{IL}$	0	$0.15 V_{CC}$	V
Pulsed drain output current, $T_C = 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ (see Notes 3 and 5)	-1.8	0.6	A
Setup time, SER IN high before SRCK $\uparrow$ , $t_{su}$ (see Figure 2)	10		ns
Hold time, SER IN high after SRCK $\uparrow$ , $t_h$ (see Figure 2)	10		ns
Pulse duration, $t_w$ (see Figure 2)	20		ns
Operating case temperature, $T_C$	-40	125	$^\circ\text{C}$

NOTES: 3. Pulse duration  $\leq 100\ \mu\text{s}$  and duty cycle  $\leq 2\%$ .  
5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

## electrical characteristics, $V_{CC} = 5\text{ V}$ , $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$ Drain-to-source breakdown voltage	$I_D = 1\text{ mA}$	50			V
$V_{SD}$ Source-to-drain diode forward voltage	$I_F = 350\text{ mA}$ , See Note 3		0.8	1.1	V
$V_{OH}$ High-level output voltage, SER OUT	$I_{OH} = -20\ \mu\text{A}$	$V_{CC} - 0.1$	$V_{CC}$		V
	$I_{OH} = -4\text{ mA}$	$V_{CC} - 0.5$	$V_{CC} - 0.2$		
$V_{OL}$ Low-level output voltage, SER OUT	$I_{OL} = 20\ \mu\text{A}$		0	0.1	V
	$I_{OL} = 4\text{ mA}$		0.2	0.5	
$I_{IH}$ High-level input current	$V_I = V_{CC}$			1	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_I = 0$			-1	$\mu\text{A}$
$I_{O(chop)}$ Output current at which chopping starts	$T_C = 25^\circ\text{C}$ , See Note 5 and Figures 3 and 4	0.6	0.8	1.1	A
$I_{CC}$ Logic supply current	$I_O = 0$ , $V_I = V_{CC}$ or 0		0.5	5	mA
$I_{CC(FRQ)}$ Logic supply current at frequency	$f_{SRCK} = 5\text{ MHz}$ , $I_O = 0$ , $C_L = 30\text{ pF}$ , $V_I = V_{CC}$ or 0, $V_{CC} = 5\text{ V}$ , See Figure 7		1.3		mA
$I_{(nom)}$ Nominal current	$V_{DS(on)} = 0.5\text{ V}$ , $V_{CC} = 5\text{ V}$ , $I_{(nom)} = I_D$ , $T_C = 85^\circ\text{C}$ , See Notes 5, 6, and 7		350		mA
$I_D$ Drain current, off-state	$V_{DS} = 40\text{ V}$ , $T_C = 25^\circ\text{C}$		0.1	1	$\mu\text{A}$
	$V_{DS} = 40\text{ V}$ , $T_C = 125^\circ\text{C}$		0.2	5	
$r_{DS(on)}$ Static drain-source on-state resistance	$I_D = 350\text{ mA}$ , $T_C = 25^\circ\text{C}$	See Notes 5 and 6 and Figures 10 and 11	1	1.5	$\Omega$
	$I_D = 350\text{ mA}$ , $T_C = 125^\circ\text{C}$		1.7	2.5	

NOTES: 5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at  $T_C = 85^\circ\text{C}$ .

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## switching characteristics, $V_{CC} = 5\text{ V}$ , $T_C = 25^\circ\text{C}$

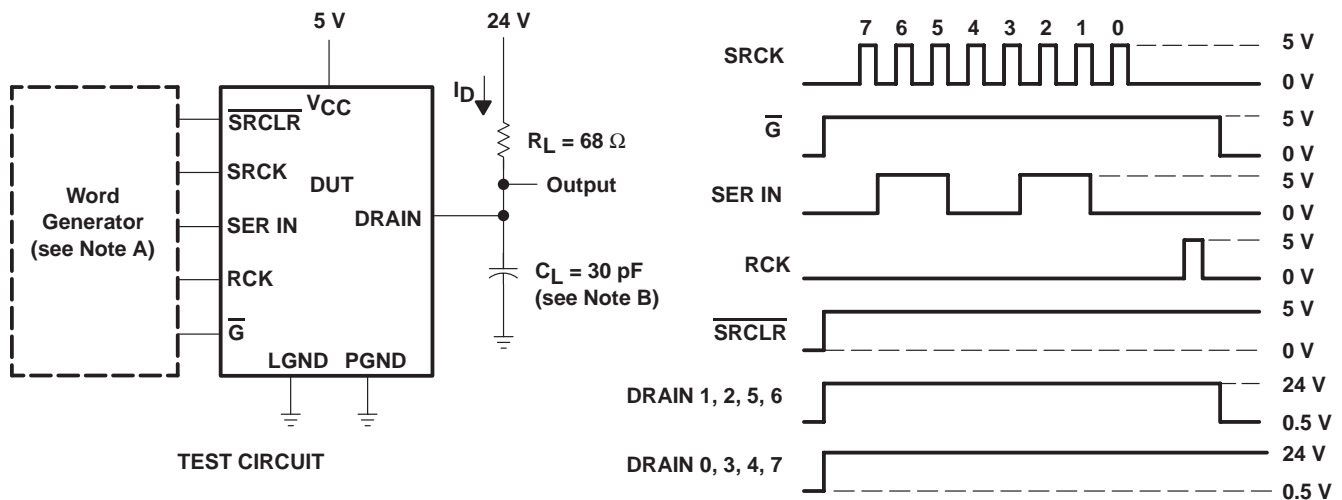
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PHL}$	Propagation delay time, high-to-low-level output from $\overline{G}$	$C_L = 30\text{ pF}$ , $I_D = 350\text{ mA}$ , See Figures 1, 2, and 12		30		ns
$t_{PLH}$	Propagation delay time, low-to-high-level output from $\overline{G}$			125		ns
$t_r$	Rise time, drain output			60		ns
$t_f$	Fall time, drain output			30		ns
$t_{pd}$	Propagation delay time, SRCK $\downarrow$ to SEROUT	$C_L = 30\text{ pF}$ , $I_D = 350\text{ mA}$ , See Figure 2		20		ns
$f(\text{SRCK})$	Serial clock frequency	$C_L = 30\text{ pF}$ , $I_D = 350\text{ mA}$ , See Note 8			10	MHz
$t_a$	Reverse-recovery-current rise time	$I_F = 350\text{ mA}$ , $di/dt = 20\text{ A}/\mu\text{s}$ , See Notes 5 and 6 and Figure 5		100		ns
$t_{rr}$	Reverse-recovery time			300		ns

- NOTES: 5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
 8. This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SRCK  $\rightarrow$  SEROUT propagation delay and setup time plus some timing margin.

## thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	DW		10	$^\circ\text{C}/\text{W}$
		NE	All eight outputs with equal power	10	
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW		50	$^\circ\text{C}/\text{W}$
		NE	All eight outputs with equal power	50	

## PARAMETER MEASUREMENT INFORMATION

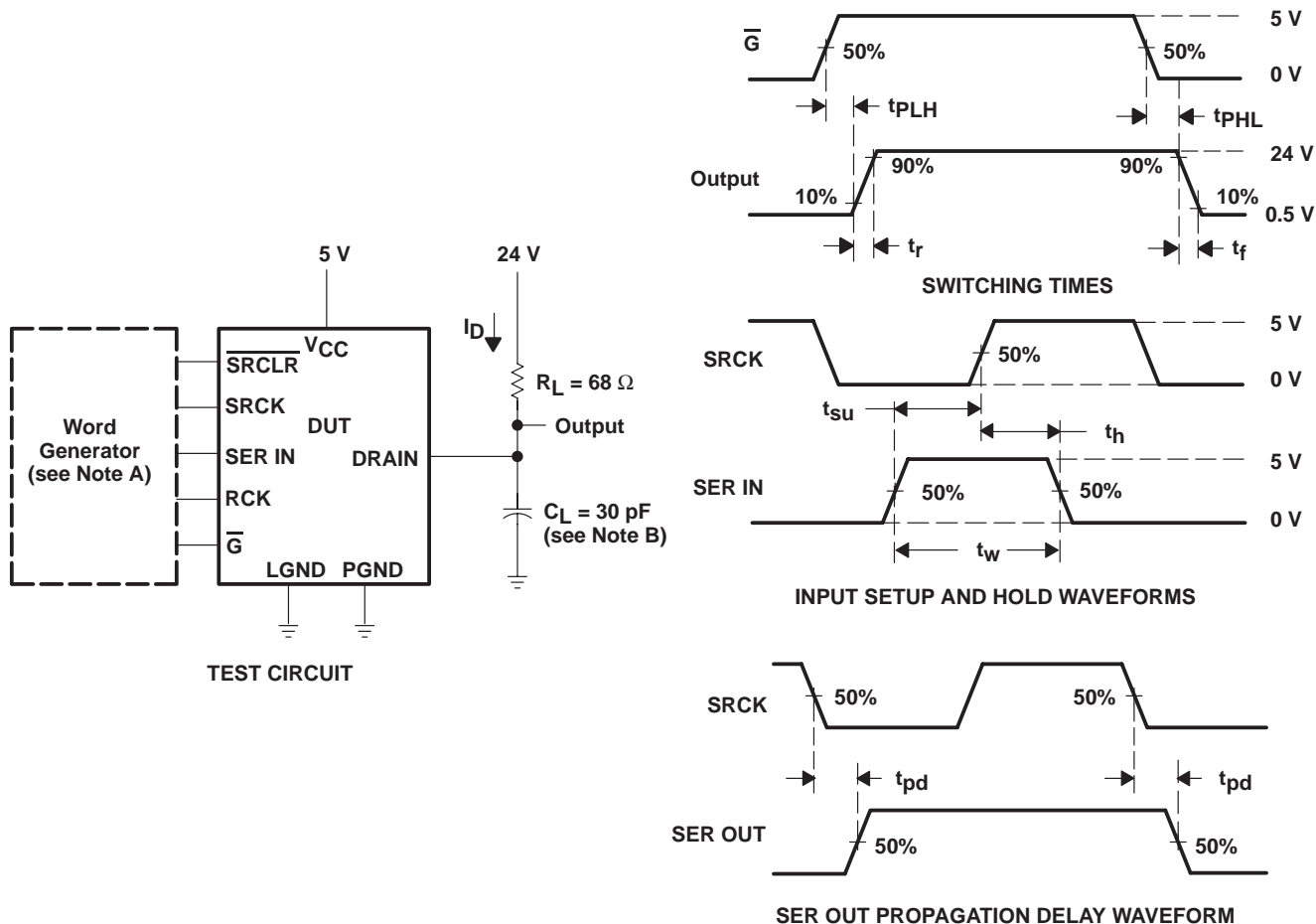


### VOLTAGE WAVEFORMS

- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ ,  $t_w = 300\text{ ns}$ , pulsed repetition rate (PRR) = 5 kHz,  $Z_O = 50\ \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 1. Resistive Load Operation

PARAMETER MEASUREMENT INFORMATION



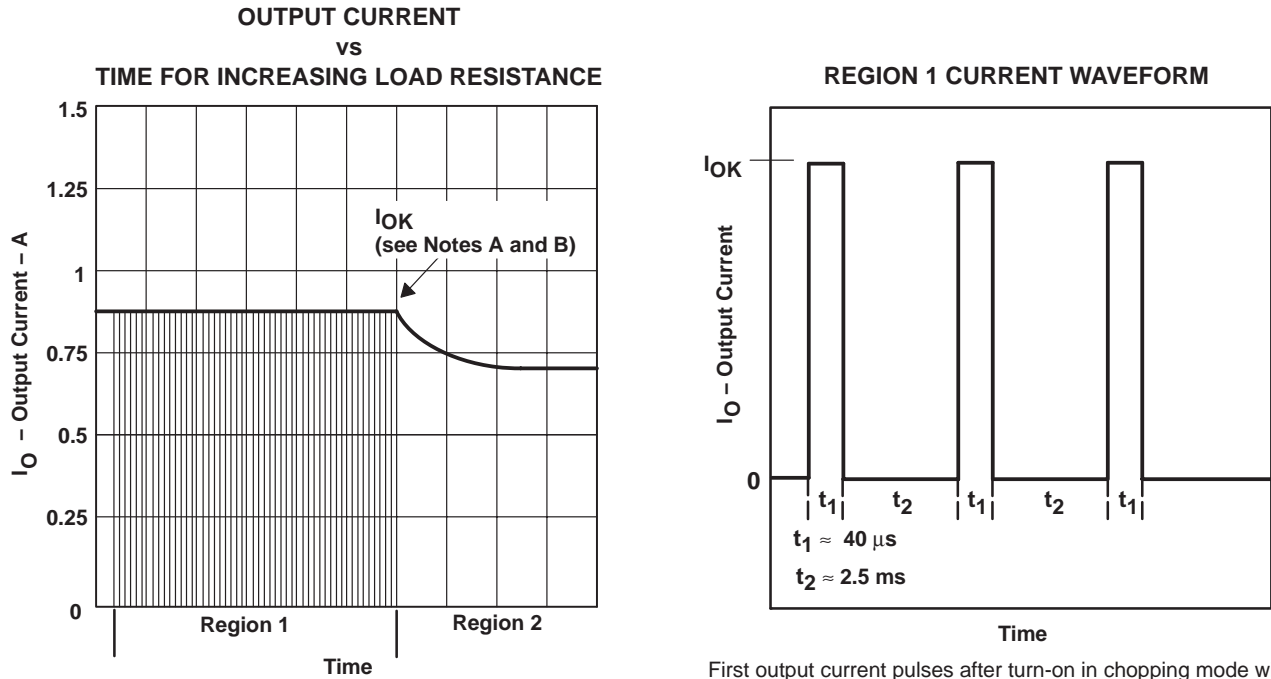
- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $t_w = 300 \text{ ns}$ , pulsed repetition rate (PRR) = 5 kHz,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

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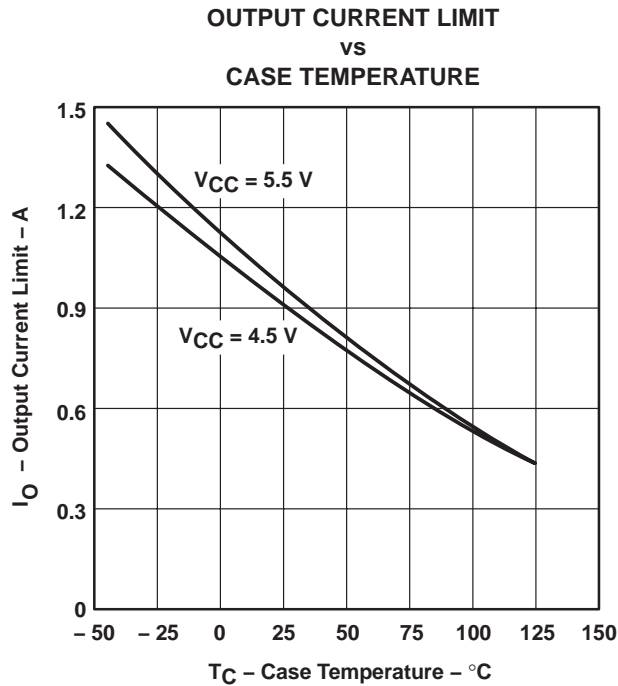
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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to  $I_{OK}$ . In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.
- B. Region 1 duty cycle is approximately 2%.

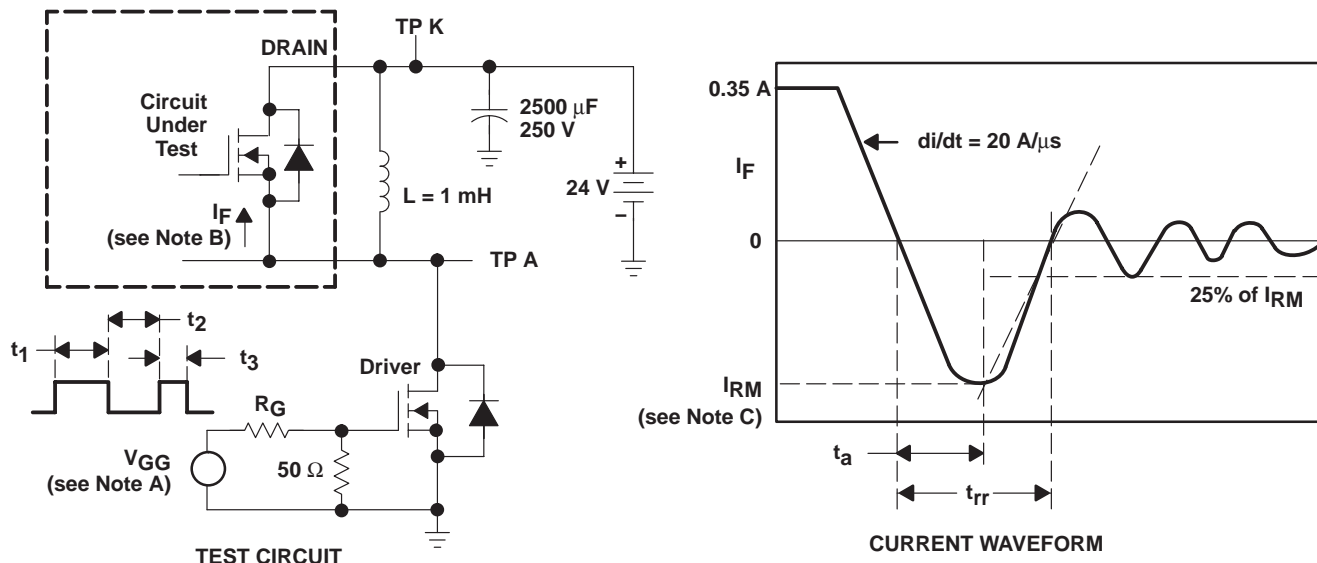
**Figure 3. Chopping-Mode Characteristics**



**Figure 4**

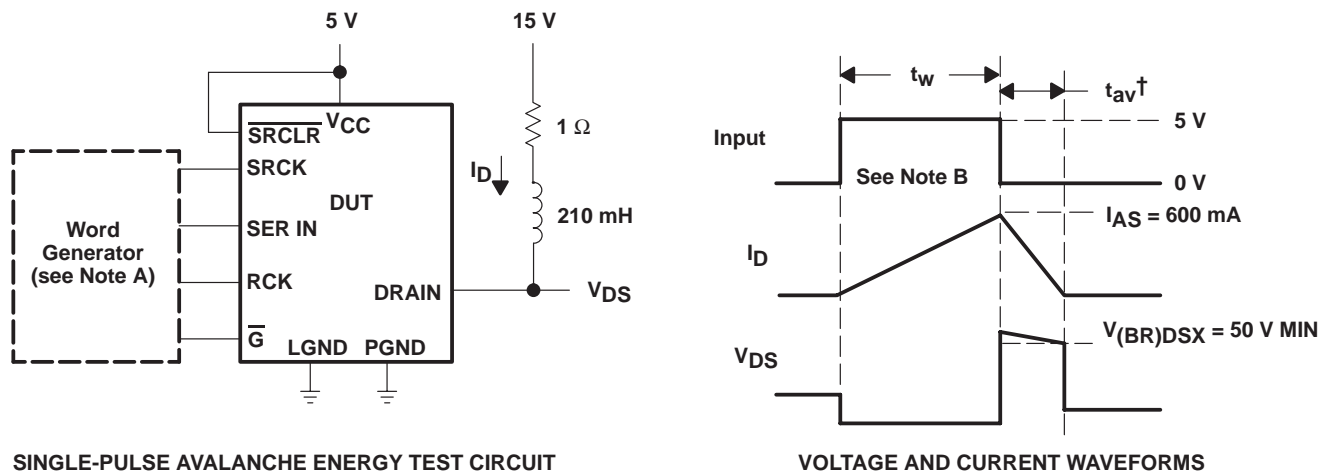


PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The  $V_{GG}$  amplitude and  $R_G$  are adjusted for  $di/dt = 20 \text{ A}/\mu\text{s}$ . A  $V_{GG}$  double-pulse train is used to set  $I_F = 0.35 \text{ A}$ , where  $t_1 = 10 \mu\text{s}$ ,  $t_2 = 7 \mu\text{s}$ , and  $t_3 = 3 \mu\text{s}$ .  
 B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.  
 C.  $I_{RM}$  = maximum recovery current

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



- † Non JEDEC symbol for avalanche time.  
 NOTES: A. The word generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $Z_0 = 50 \Omega$ .  
 B. Input pulse duration,  $t_w$ , is increased until peak current  $I_{AS} = 600 \text{ mA}$ .  
 Energy test level is defined as  $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{av})/2 = 75 \text{ mJ}$ .

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

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## TYPICAL CHARACTERISTICS

**SUPPLY CURRENT  
vs  
FREQUENCY**

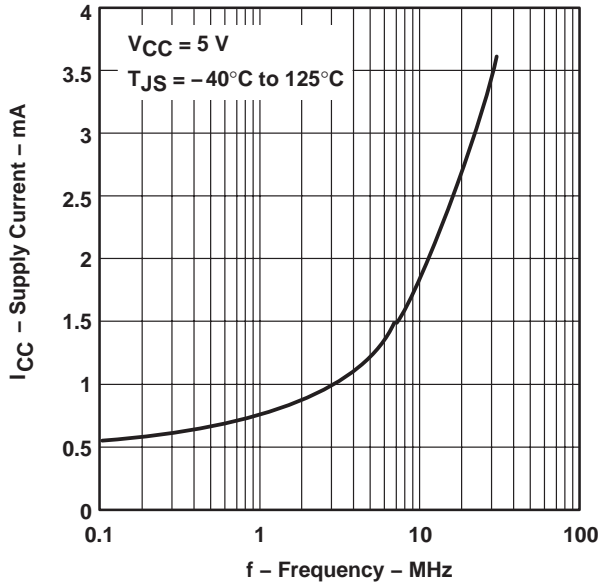


Figure 7

**MAXIMUM CONTINUOUS  
DRAIN CURRENT OF EACH OUTPUT  
vs  
NUMBER OF OUTPUTS CONDUCTING  
SIMULTANEOUSLY**

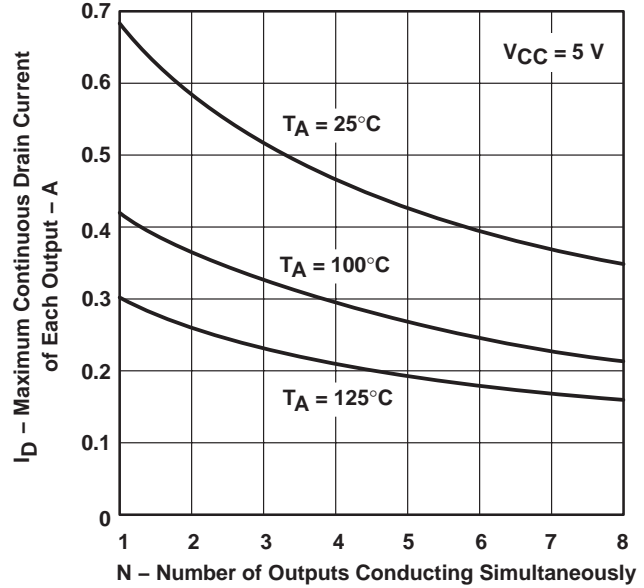


Figure 8

**MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT  
vs  
NUMBER OF OUTPUTS CONDUCTING  
SIMULTANEOUSLY**

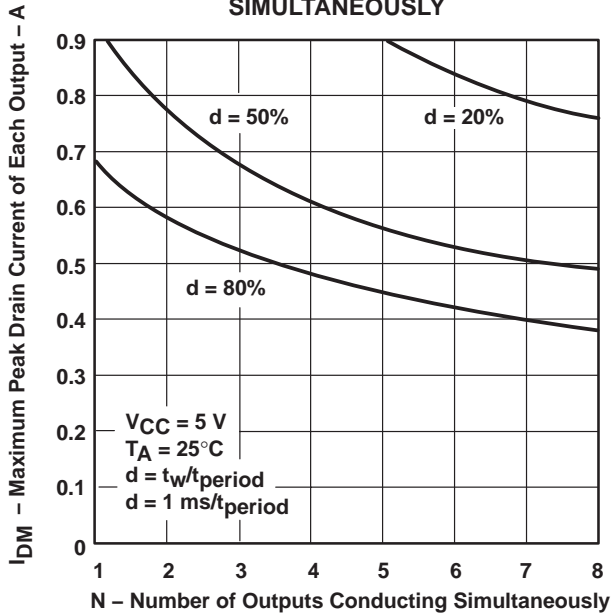


Figure 9

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE  
vs  
DRAIN CURRENT**

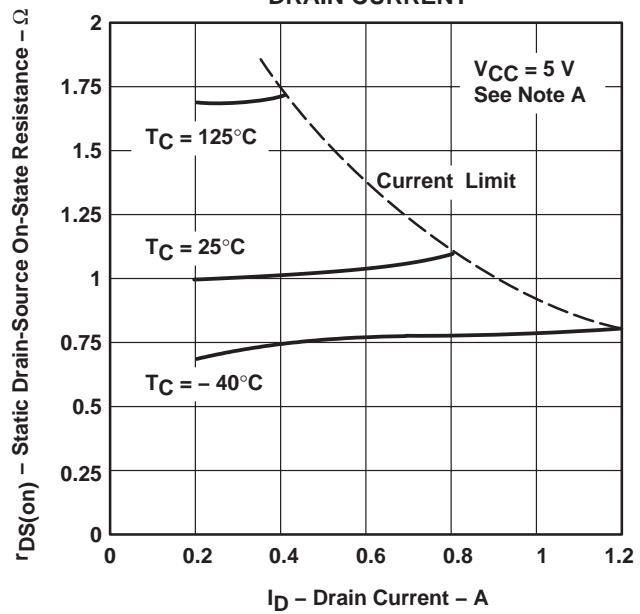


Figure 10

NOTE A: Technique should limit  $T_J - T_C$  to  $10^{\circ}\text{C}$  maximum.

TYPICAL CHARACTERISTICS

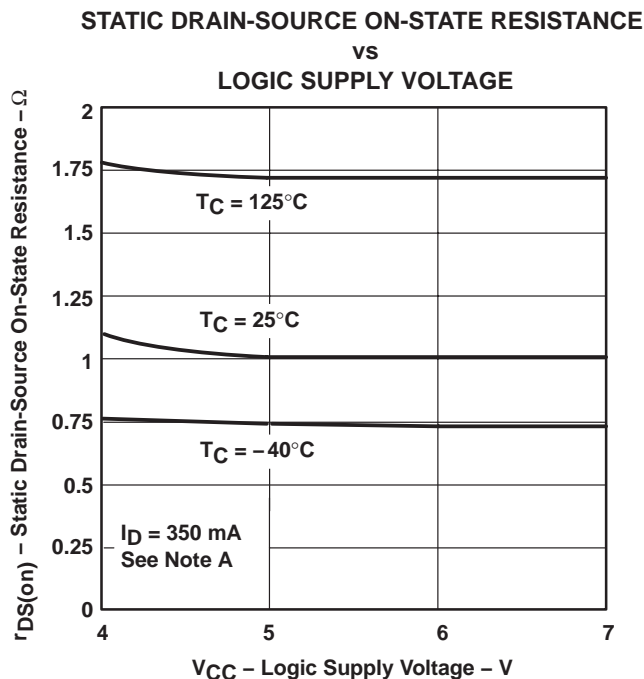


Figure 11

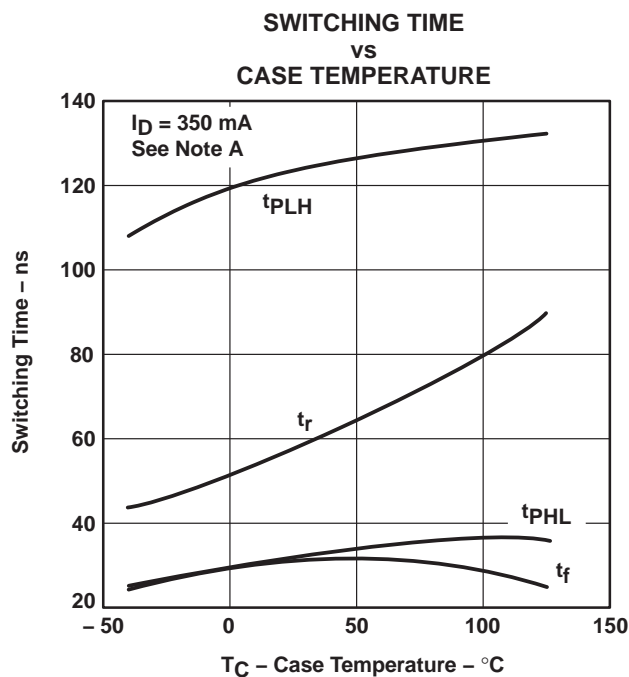


Figure 12

NOTE A: Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

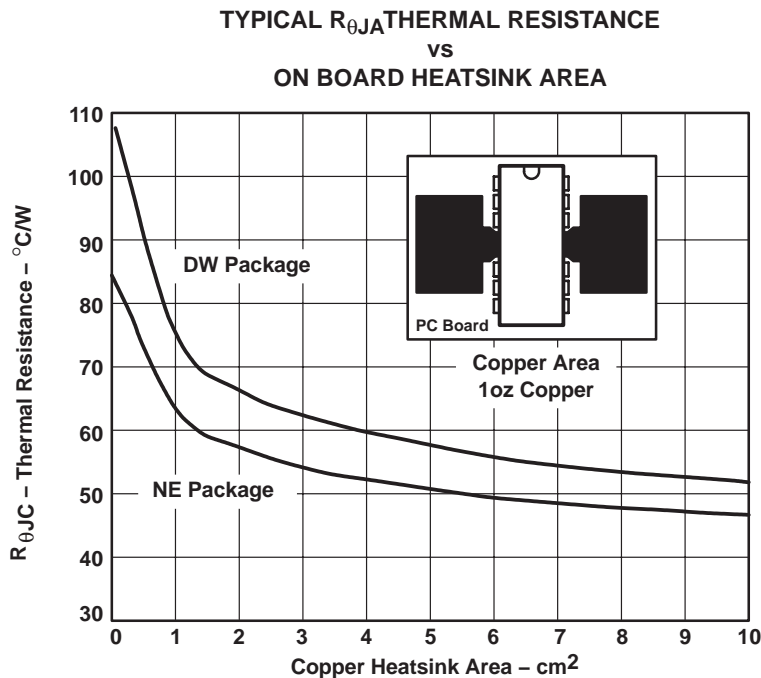
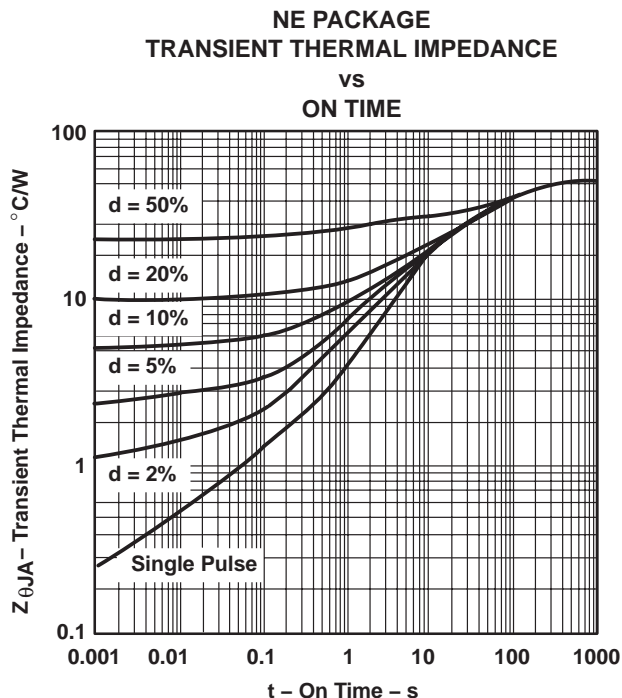


Figure 13

# TPIC6A596 POWER LOGIC 8-BIT SHIFT REGISTER

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## THERMAL INFORMATION



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_{\theta}(t_w + t_c) + Z_{\theta}(t_w) - Z_{\theta}(t_c)$$

Where:

$Z_{\theta}(t_w)$  = the single-pulse thermal impedance for  $t = t_w$  seconds

$Z_{\theta}(t_c)$  = the single-pulse thermal impedance for  $t = t_c$  seconds

$Z_{\theta}(t_w + t_c)$  = the single-pulse thermal impedance for  $t = t_w + t_c$  seconds

$$d = t_w/t_c$$

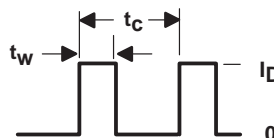


Figure 14

## Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
5/18/05	A	6	Figure 1	Changed $\overline{SRCLR}$ timing diagram and changed title on Drain timing diagrams
3/2000	*			Original reversion

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC6A596DWRG4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6A596	<a href="#">Samples</a>
TPIC6A596NE	ACTIVE	PDIP	NE	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 125	TPIC6A596NE	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

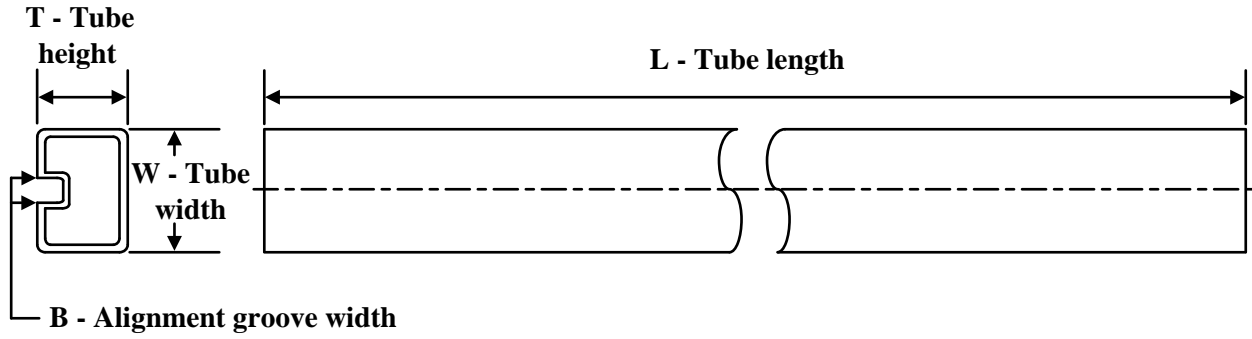

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6A596DWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TPIC6A596DWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6A596DWRG4	SOIC	DW	24	2000	350.0	350.0	43.0
TPIC6A596DWRG4	SOIC	DW	24	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPIC6A596NE	NE	PDIP	20	20	506	13.97	11230	4.32

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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