



THE DATASHEET OF TPIC6B595N



TPIC6B595 Power Logic 8-Bit Shift Register

1 Features

- Low $r_{DS(on)}$, 5 Ω (Typical)
- Avalanche Energy, 30 mJ
- Eight Power DMOS Transistor Outputs of 150-mA Continuous Current
- Output Clamp Voltage, 50 V
- Devices are Cascadable
- Low-Power Consumption

2 Applications

- Instrumentation Clusters
- Tell-Tale Lamps
- LED Illumination and Controls
- Automotive Relay or Solenoids Drivers

3 Description

The TPIC6B595 device is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively.

The storage register transfers data to the output buffer when shift-register clear (SRCLR) is high. When SRCLR is low, the input shift register is cleared. When output enable (\bar{G}) is held high, all data in the output buffers is held low and all drain outputs are off. When \bar{G} is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at $T_C = 25^\circ\text{C}$. The current limit decreases as the junction temperature increases for additional device protection.

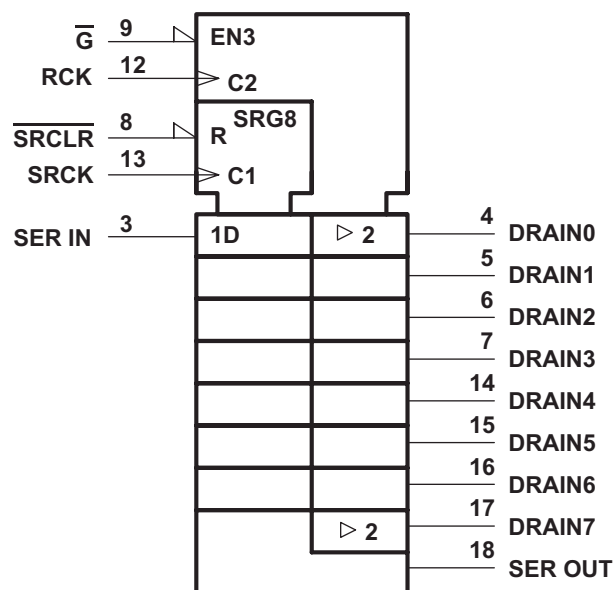
The TPIC6B595 is characterized for operation over the operating case temperature range of -40°C to 125°C .

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|--------------------|
| TPIC6B595 | SOIC (20) | 12.80 mm × 7.50 mm |
| | PDIP (20) | 24.33 mm × 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Symbol



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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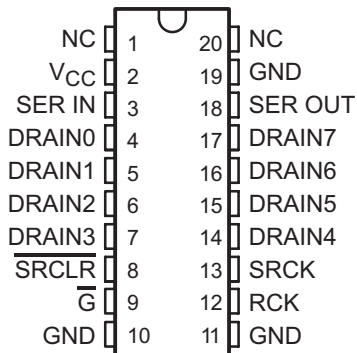
| | |
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4 Revision History

| Changes from Revision A (May 2005) to Revision B | Page |
|---|------|
| <ul style="list-style-type: none"> • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 4 | 4 |
| Changes from Original (July 1995) to Revision A | Page |
| <ul style="list-style-type: none"> • Changed SRCLR timing diagram 9 | 9 |

5 Pin Configuration and Functions

DW or N Package
20-Pin SOIC or PDIP
Top View



NC – No internal connection

Pin Functions

| PIN | | I/O | DESCRIPTION |
|--------------------|------------|-----|----------------------------------|
| NAME | NO. | | |
| DRAIN0 | 4 | O | Open-drain output |
| DRAIN1 | 5 | | |
| DRAIN2 | 6 | | |
| DRAIN3 | 7 | | |
| DRAIN4 | 14 | | |
| DRAIN5 | 15 | | |
| DRAIN6 | 16 | | |
| DRAIN7 | 17 | | |
| \overline{G} | 9 | I | Output enable, active-low |
| GND | 10, 11, 19 | — | Power ground |
| NC | 1, 20 | — | No internal connection |
| RCK | 12 | I | Register clock |
| SERIN | 3 | I | Serial data input |
| SEROUT | 18 | O | Serial data output |
| SRCK | 15 | I | Shift register clock |
| \overline{SRCLR} | 8 | I | Shift register clear, active-low |
| VCC | 2 | I | Power supply |

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|---|-----|------|
| V _{CC} | Logic supply voltage ⁽²⁾ | -0.3 | 7 | V |
| V _I | Logic input voltage | -0.3 | 7 | V |
| V _{DS} | Power DMOS drain-to-source voltage ⁽³⁾ | -0.3 | 50 | V |
| | Continuous source-to-drain diode anode current | 0 | 500 | mA |
| | Pulsed source-to-drain diode anode current ⁽⁴⁾ | 0 | 1 | A |
| I _D | Pulsed drain current, each output, all outputs ON, T _C = 25°C ⁽⁴⁾ | 0 | 500 | mA |
| I _D | Continuous drain current, each output, all outputs ON, T _C = 25°C ⁽⁴⁾ | 0 | 150 | mA |
| I _{DM} | Peak drain current single output, T _C = 25°C ⁽⁴⁾ | 0 | 500 | mA |
| E _{AS} | Single-pulse avalanche energy (see Figure 11) | 0 | 30 | mJ |
| I _{AS} | Avalanche current ⁽⁵⁾ | 0 | 500 | mA |
| | Continuous total dissipation | See Thermal Information | | |
| T _J | Operating virtual junction temperature | -40 | 150 | °C |
| T _C | Operating case temperature | -40 | 125 | °C |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Each power DMOS source is internally connected to GND.
- (4) Pulse duration ≤ 100 μs and duty cycle ≤ 2%.
- (5) DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 1.5 H, I_{AS} = 200 mA (see [Figure 11](#)).

6.2 ESD Ratings

| | | VALUE | UNIT | |
|--------------------|-------------------------|---|-----------------------------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 | |
| | | Charged-device model (CDM), per AEC Q100-011 | All pins | ±500 |
| | | | Corner pins (1, 10, 20, 11) | ±750 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------------|---|----------------------|-----|----------------------|------|
| V _{CC} | Logic supply voltage | | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 0.85 V _{CC} | | | V |
| V _{IL} | Low-level input voltage | | | 0.15 V _{CC} | V |
| | Pulsed drain output current, T _C = 25°C, V _{CC} = 5 V, all outputs on ⁽¹⁾⁽²⁾ (see Figure 7) | -500 | | 500 | mA |
| t _{su} | Setup time, SER IN high before SRCKM ↑ (see Figure 9) | 20 | | | ns |
| t _h | Hold time, SER IN high after SRCKM ↑, (see Figure 9) | 20 | | | ns |
| t _w | Pulse duration (see Figure 9) | 40 | | | ns |
| T _C | Operating case temperature | -40 | | 125 | °C |

- (1) Pulse duration ≤ 100 μs and duty cycle ≤ 2%.
- (2) Technique should limit T_J - T_C to 10°C maximum.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPIC6B595 | | UNIT |
|-------------------------------|--|-----------|----------|------|
| | | DW (SOIC) | N (PDIP) | |
| | | 20 PINS | 20 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 75.3 | 57 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 39.8 | 58.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 43.1 | 38 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 15.4 | 25.2 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 42.6 | 37.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------|---|--|---|-----|-------|-----|------|
| V _{(BR)DSX} | Drain-to-source breakdown voltage | I _D = 1 mA | | 50 | | | V |
| V _{SD} | Source-to-drain diode forward voltage | I _F = 100 mA | | | 0.85 | 1 | V |
| V _{OH} | High-level output voltage, SER OUT | I _{OH} = -20 μA, V _{CC} = 4.5 V | | 4.4 | 4.49 | | V |
| | | I _{OH} = -4 mA, V _{CC} = 4.5 V | | 4 | 4.2 | | |
| V _{OL} | Low-level output voltage, SER OUT | I _{OL} = 20 μA, V _{CC} = 4.5 V | | | 0.005 | 0.1 | V |
| | | I _{OL} = 4 mA, V _{CC} = 4.5 V | | | 0.3 | 0.5 | |
| I _{IH} | High-level input current | V _{CC} = 5.5 V, V _I = V _{CC} | | | | 1 | μA |
| I _{IL} | Low-level input current | V _{CC} = 5.5 V, V _I = 0 | | | | -1 | μA |
| I _{CC} | Logic supply current | V _{CC} = 5.5 V | All outputs OFF | | 20 | 100 | μA |
| | | | All outputs ON | | 150 | 300 | |
| I _{CC(FRQ)} | Logic supply current at frequency | f _{SRCK} = 5 MHz, All outputs off, | C _L = 30 pF, See Figure 9 and Figure 2 | | 0.4 | 5 | mA |
| I _N | Nominal current | V _{DS(on)} = 0.5 V, I _N = I _D , T _C = 85°C | See ⁽¹⁾⁽²⁾⁽³⁾ | | 90 | | mA |
| I _{DSX} | OFF-state drain current | V _{DS} = 40 V, V _{CC} = 5.5 V | | | 0.1 | 5 | μA |
| | | V _{DS} = 40 V, T _C = 125°C, V _{CC} = 5.5 V | | | 0.15 | 8 | |
| r _{DS(on)} | Static drain-source ON-state resistance | I _D = 100 mA, V _{CC} = 4.5 V | See ⁽¹⁾ and ⁽²⁾ and Figure 3 and Figure 4 | | 4.2 | 5.7 | Ω |
| | | I _D = 100 mA, T _C = 125°C, V _{CC} = 4.5 V | | | 6.8 | 9.5 | |
| | | I _D = 350 mA, V _{CC} = 4.5 V | | | 5.5 | 8 | |

(1) Technique should limit T_J - T_C to 10°C maximum.

(2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

(3) Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

TPIC6B595

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6.6 Switching Characteristics
 $V_{CC} = 5\text{ V}$, $T_C = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|---|-----|-----|-----|------|
| t_{PLH} | Propagation delay time, low-to-high-level output from \overline{G} | $C_L = 30\text{ pF}$, $I_D = 100\text{ mA}$, See Figure 5 , Figure 8 and Figure 9 | | 150 | | ns |
| t_{PHL} | Propagation delay time, high-to-low-level output from \overline{G} | | | 90 | | ns |
| t_r | Rise time, drain output | | | 200 | | ns |
| t_f | Fall time, drain output | | | 200 | | ns |
| t_a | Reverse-recovery-current rise time | $I_F = 100\text{ mA}$, $di/dt = 10\text{ A}/\mu\text{s}^{(1) (2)}$, See Figure 10 | | 100 | | ns |
| t_{rr} | Reverse-recovery time | | | 300 | | |

 (1) Technique should limit $T_J - T_C$ to 10°C maximum.

(2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

6.7 Typical Characteristics

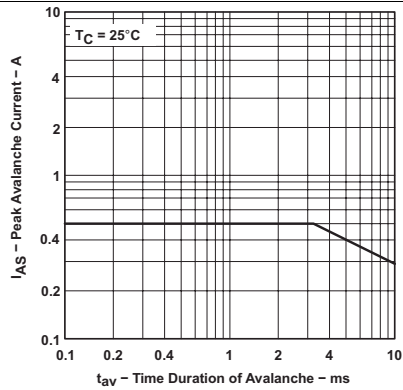


Figure 1. Peak Avalanche Current vs Time Duration of Avalanche

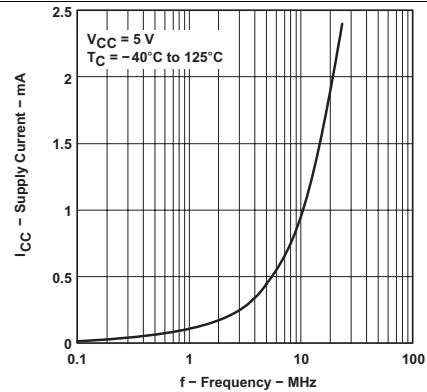
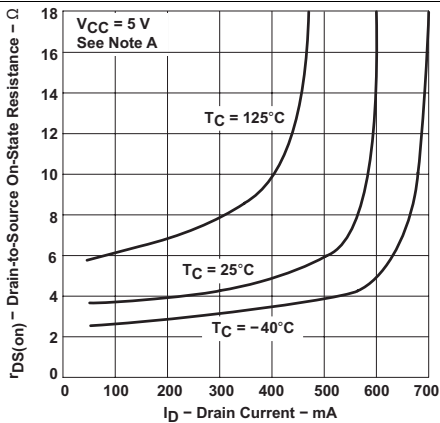
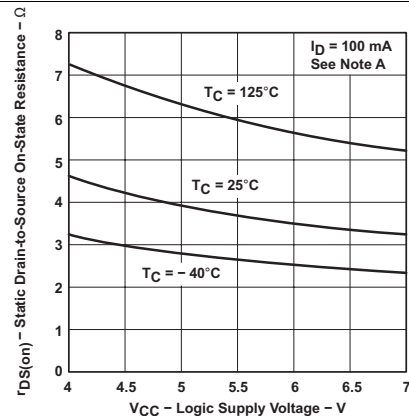


Figure 2. Supply Current vs Frequency



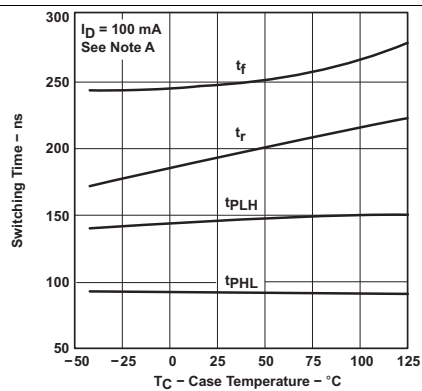
Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 3. Drain-to-Source On-State Resistance vs Drain Current



Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 4. Static Drain-to-Source On-State Resistance vs Logic Supply Voltage



Technique should limit $T_J - T_C$ to 10°C maximum

Figure 5. Switching Time vs Case Temperature

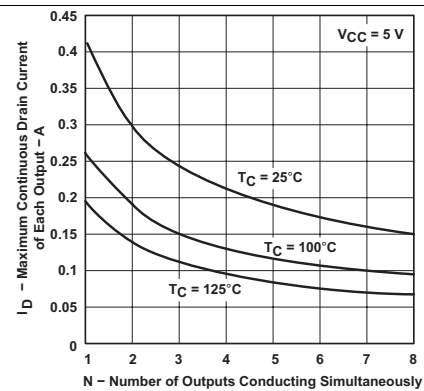


Figure 6. Maximum Continuous Drain Current of Each Output vs Number of Outputs Conducting Simultaneously

Typical Characteristics (continued)

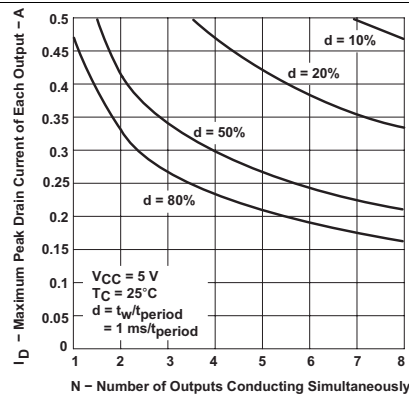
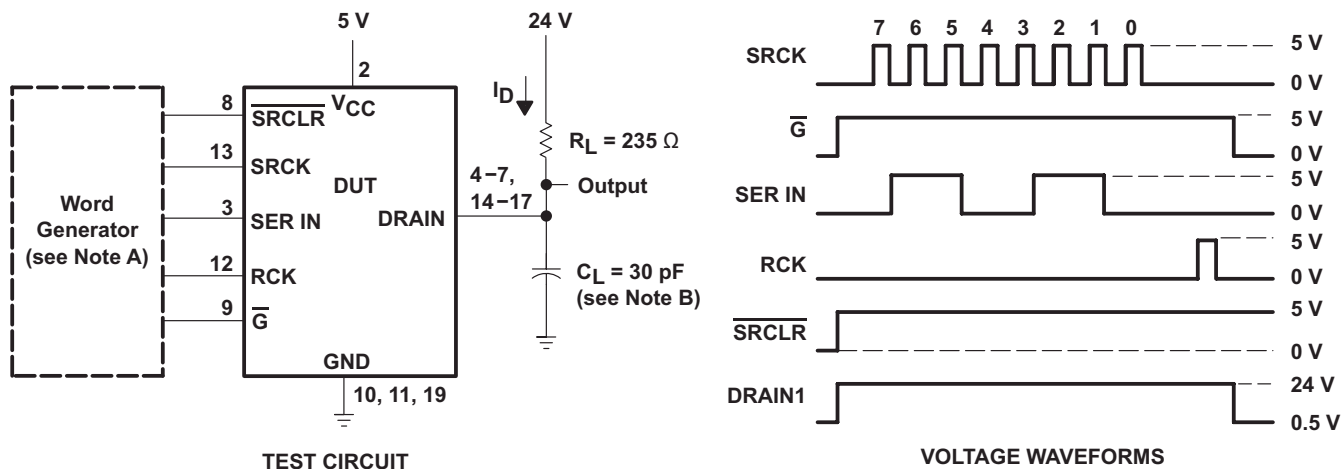


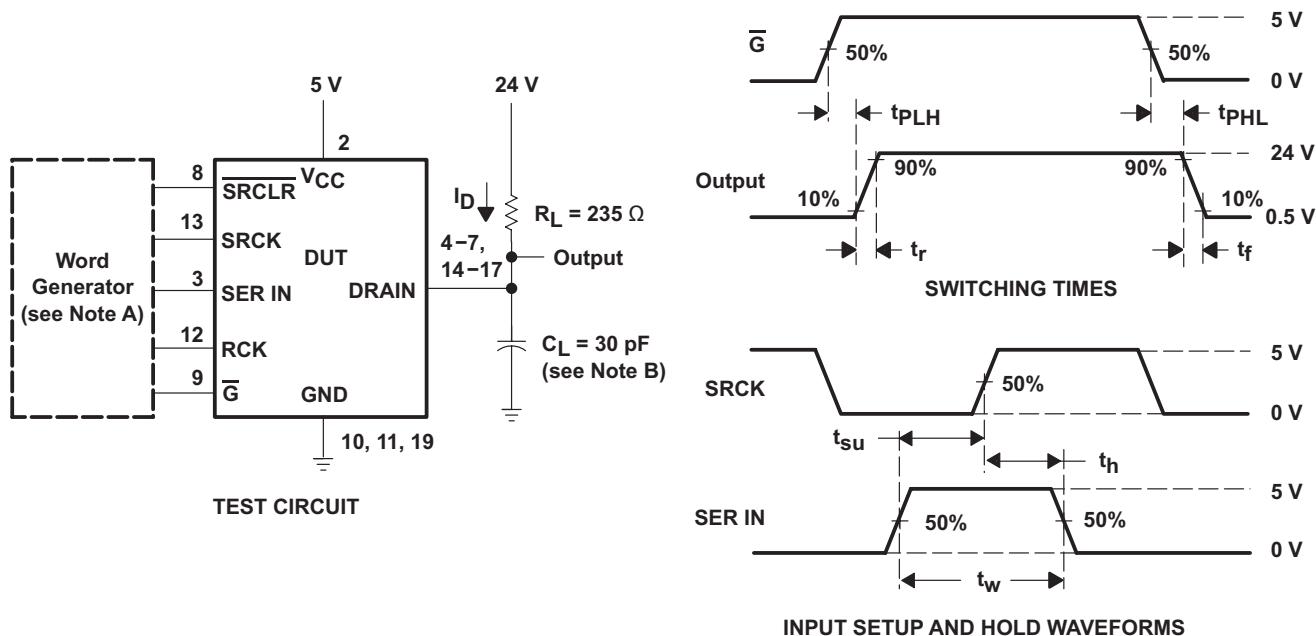
Figure 7. Maximum Peak Drain Current of Each Output vs Number of Outputs Conducting Simultaneously

7 Parameter Measurement Information



- A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

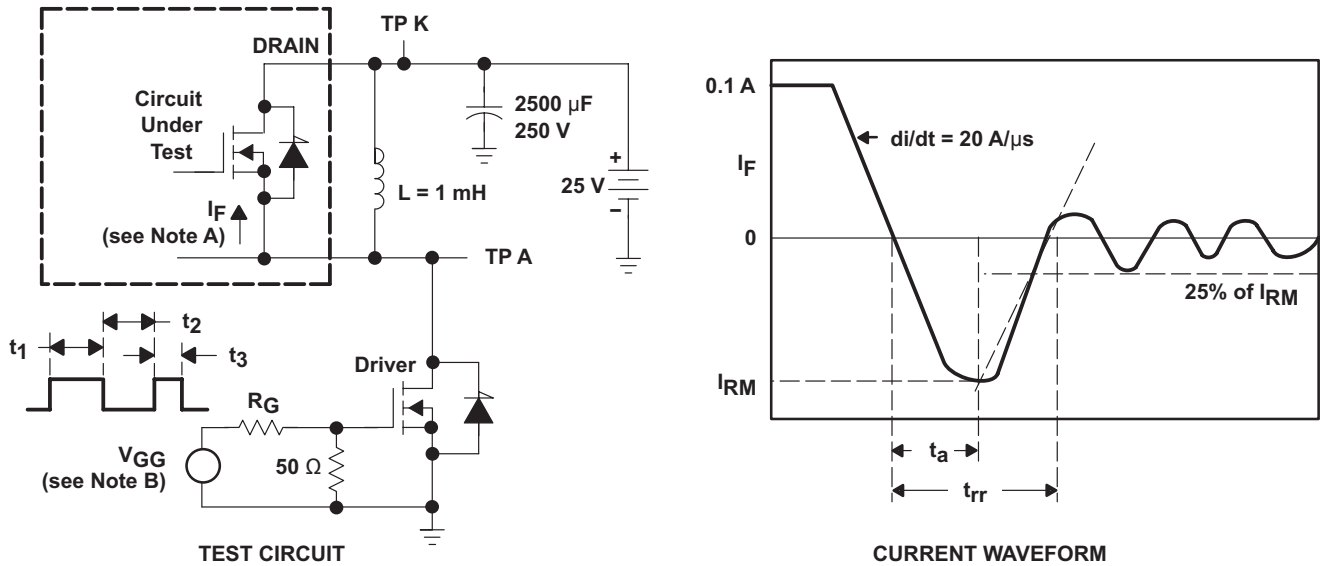
Figure 8. Resistive-Load Test Circuit and Voltage Waveforms



- A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

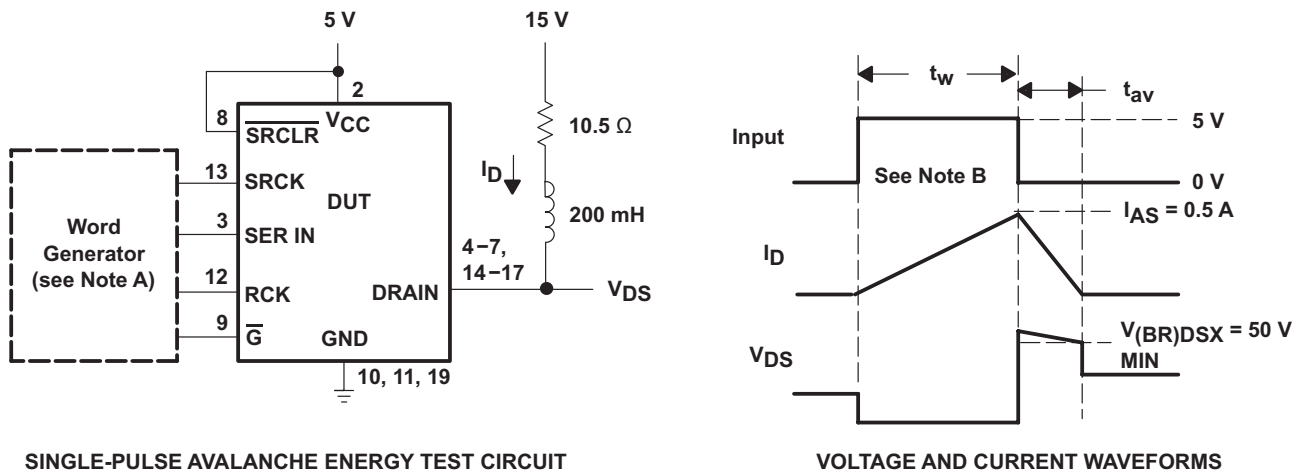
Figure 9. Test Circuit, Switching Times, and Voltage Waveforms

Parameter Measurement Information (continued)



- A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
- B. The V_{GG} amplitude and R_G are adjusted for $di/dt = 20 \text{ A}/\mu\text{s}$. A V_{GG} double-pulse train is used to set $I_F = 0.1 \text{ A}$, where $t_1 = 10 \mu\text{s}$, $t_2 = 7 \mu\text{s}$, and $t_3 = 3 \mu\text{s}$.

Figure 10. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode



- A. The word generator has the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $Z_O = 50 \Omega$.
- B. Input pulse duration, t_w , is increased until peak current $I_{AS} = 0.5 \text{ mA}$. Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30 \text{ mJ}$.

Figure 11. Single-Pulse Avalanche Energy Test Circuit and Waveforms

8 Detailed Description

8.1 Overview

The TPIC6B595 device is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection, so it can also drive relays, solenoids, and other medium-current or high-voltage loads.

8.2 Functional Block Diagram

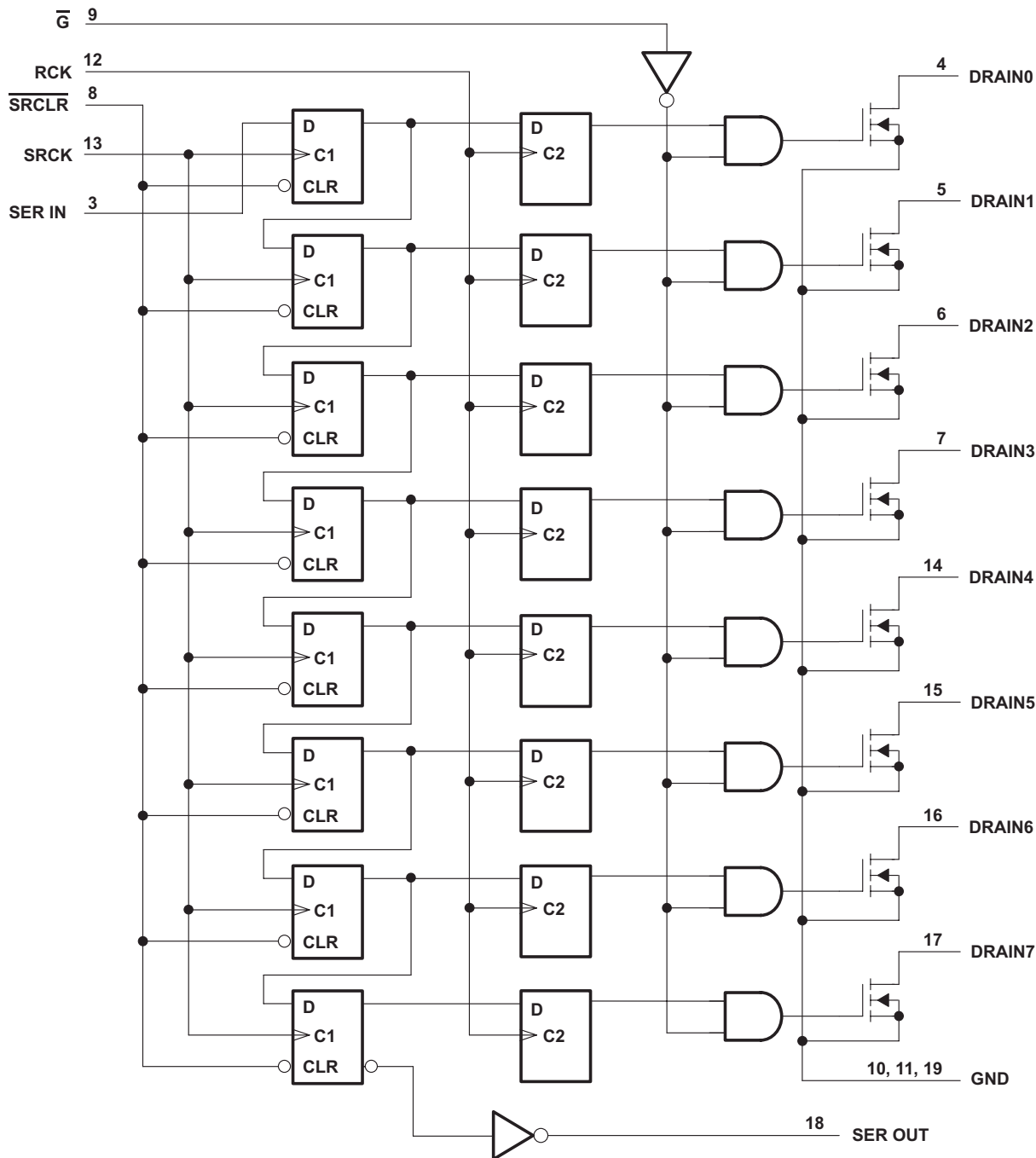


Figure 12. Logic Diagram (Positive Logic)

Functional Block Diagram (continued)

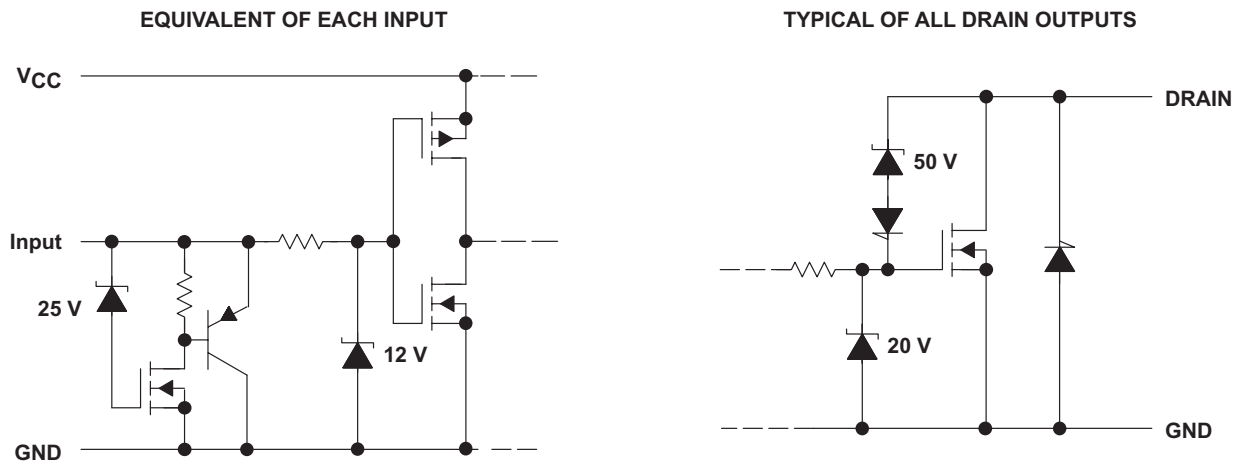


Figure 13. Schematic of Inputs

8.3 Feature Description

8.3.1 Serial-In Interface

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift register clear (SRCLR) is high.

8.3.2 Clear Register

A logical low on ($\overline{\text{SRCLR}}$) clears all registers in the device. TI suggests clearing the device during power up or initialization.

8.3.3 Output Control

Holding the output enable ($\overline{\text{G}}$) high holds all data in the output buffers low, and all drain outputs are off. Holding ($\overline{\text{G}}$) low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are OFF. When data is high, the DMOS transistor outputs have sink-current capability. This pin can also be used for global PWM dimming.

8.3.4 Cascaded Application

The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices. Connect the device (SEROUT) pin to the next device (SERIN) for daisy Chain. This provides improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

8.3.5 Current Limit Function

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink current capability. Each output provides a 500-mA typical current limit at $T_C = 25^\circ\text{C}$. The current limit decreases as the junction temperature increases for additional device protection.

8.4 Device Functional Modes

8.4.1 Operation With $V(V_{CC}) < 4.5$ (Minimum $V(V_{CC})$)

This device works normally during $4.5\text{ V} \leq V(V_{CC}) \leq 5.5\text{ V}$, when operation voltage is lower than 4.5 V. TI can't ensure the behavior of device, including communication interface and current capability.

8.4.2 Operating With $5.5\text{ V} < V(V_{CC}) < 6\text{ V}$

This device works normally during this voltage range, but reliability issues may occur while the device works for a long time in this voltage range.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPIC6B595 device is a serial-in parallel-out, Power+LogicE 8-bit shift register with low-side switch DMOS outputs rating of a 150 mA per channel. The device is designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium current or high-voltage loads. The following focuses on automotive cluster applications for the TPIC6B595 device.

9.2 Typical Application

The typical application of the TPIC6B595 device is the automotive cluster driver. In this example, two TPIC6B595 power shift registers are cascaded and used to turn on LEDs in the cluster panel. In this case, the LED must be updated after all 16 bits of data have been loaded into the serial shift registers. MCU outputs the data to the serial input (SER IN) while clocking the shift register clock (SRCK). After the 16th clock, a pulse to the register clock (RCK) transfers the data to the storage registers. If output enable (G) is low, then the LEDs are turned ON corresponding to the status word with ones being ON and zeros OFF. With this simple scheme, MCU use SPI interface can turn on 16 LEDs using only two ICs as illustrated in Figure 14.

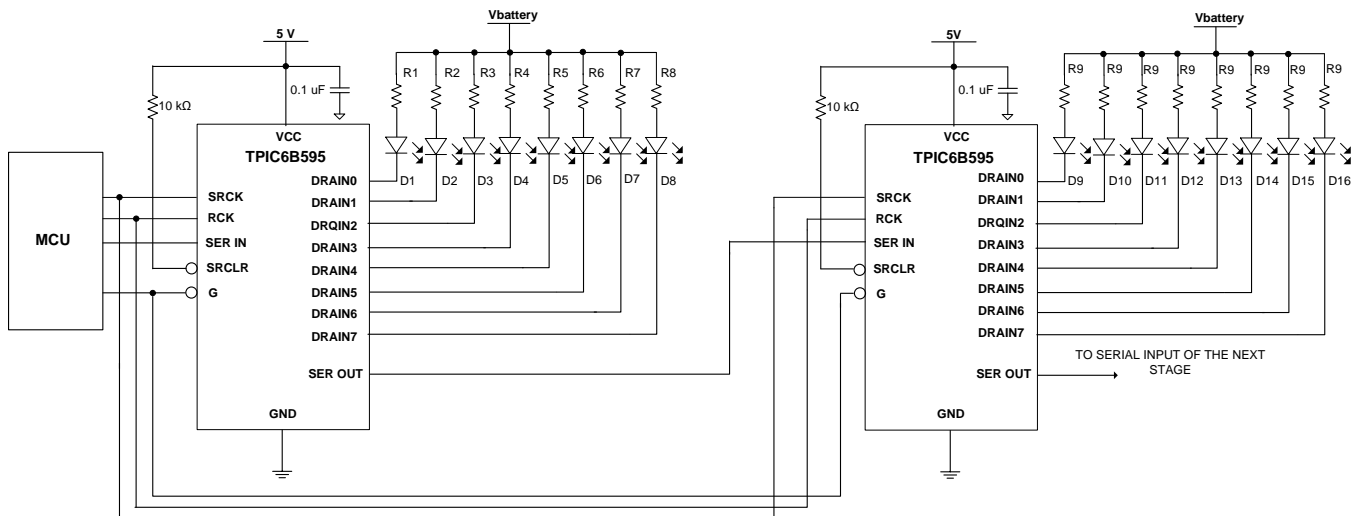


Figure 14. Typical Application Schematic

9.2.1 Design Requirements

Use the design parameters in Table 1 for this design example.

Table 1. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|----------------------------|
| VSUPPLY | 9-16 V |
| V(D1), V(D2), V(D3), V(D4), V(D5), V(D6), V(D7), V(D8) | 2 V |
| V(D9), V(D10), V(D11), V(D12), V(D13), V(D14), V(D15), V(D16) | 3.3 V |
| I(D1), I(D2), I(D3), I(D4), I(D5), I(D6), I(D7), I(D8) | 20mA When Vbattery is 12 V |
| I(D9), I(D10), I(D11), I(D12), I(D13), I(D14), I(D15), I(D16) | 30mA When Vbattery is 12 V |

9.2.2 Detailed Design Procedure

To begin the design process, one must decide on a few parameters. The designer must know the following:

- Vsupply - LED supply is connect battery directly or fix voltage, this application connect the battery directly.
- V(Dx) – LED forward voltage
- I(Dx) – LED setting current when battery is 12 V.

R1, R2, R3, R4, R5, R6, R7, R8

$$R1 = R2 = R3 = R4 = R5 = R6 = R7 = R8 = \frac{(V_{supply} - V(Dx))}{I(Dx)} = \frac{(12V - 2V)}{0.02A} = 500\Omega \quad (1)$$

When Vsupply is 9 V,

$$I(D1) = I(D2) = I(D3) = I(D4) = I(D5) = I(D6) = I(D7) = I(D8) = \frac{(V_{supply} - V(Dx))}{R_x} = 14mA \quad (2)$$

When Vsupply is 16 V,

$$I(D1) = I(D2) = I(D3) = I(D4) = I(D5) = I(D6) = I(D7) = I(D8) = \frac{(V_{supply} - V(Dx))}{R_x} = 28mA \quad (3)$$

R9, R10, R11, R12, R13, R14, R15, R16

$$R9 = R10 = R11 = R12 = R13 = R14 = R15 = R16 = \frac{(V_{supply} - V(Dx))}{I(Dx)} = \frac{(12V - 3.3V)}{0.03A} = 290\Omega \quad (4)$$

When Vsupply is 9 V,

$$I(D9) = I(D10) = I(D11) = I(D12) = I(D13) = I(D14) = I(D15) = I(D16) = \frac{(V_{supply} - V(Dx))}{R_x} = 19.7mA \quad (5)$$

When Vsupply is 16 V,

$$I(D9) = I(D10) = I(D11) = I(D12) = I(D13) = I(D14) = I(D15) = I(D16) = \frac{(V_{supply} - V(Dx))}{R_x} = 43.8mA \quad (6)$$

NOTE

If customers can accept the current variation when battery voltage is changing, they can connect to the battery directly. If customers need the less variation of current, they must use the voltage regulator as supply voltage of LED, or change to constant current LED driver directly.

9.2.3 Application Curve

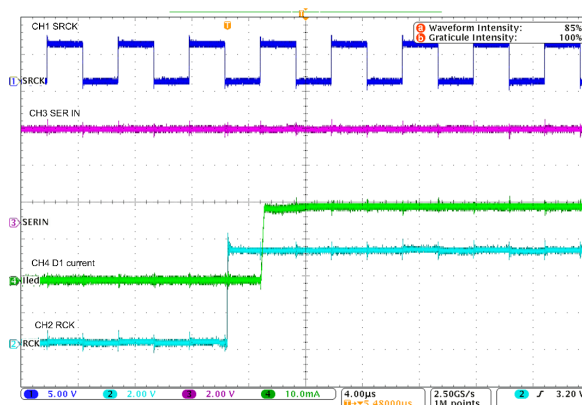


Figure 15. CH1 is SRCK, CH2 is RCK, CH3 is SER IN, CH4 is D1 current

10 Power Supply Recommendations

The TPIC6B595 device is designed to operate from an input voltage supply range from 4.5 V and 5.5 V. This input supply should be well regulated. TI recommends placing the ceramic bypass capacitors near the VCC pin.

11 Layout

11.1 Layout Guidelines

There is no special layout requirement for the digital signal pin; the only requirement is placing the ceramic bypass capacitors near the corresponding pin. Because the TPIC6B595 device does not have a thermal shutdown protection function, to prevent thermal damage, T_J must be less than 150°C. If the total sink current is high, the power dissipation might be large. The devices are currently not available in the thermal pad package, so good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device. Maximize the copper coverage on the PCB to increase the thermal conductivity of the board, because the major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when the design does not include heat sinks attached to the PCB on the other side of the package.

- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

11.2 Layout Example

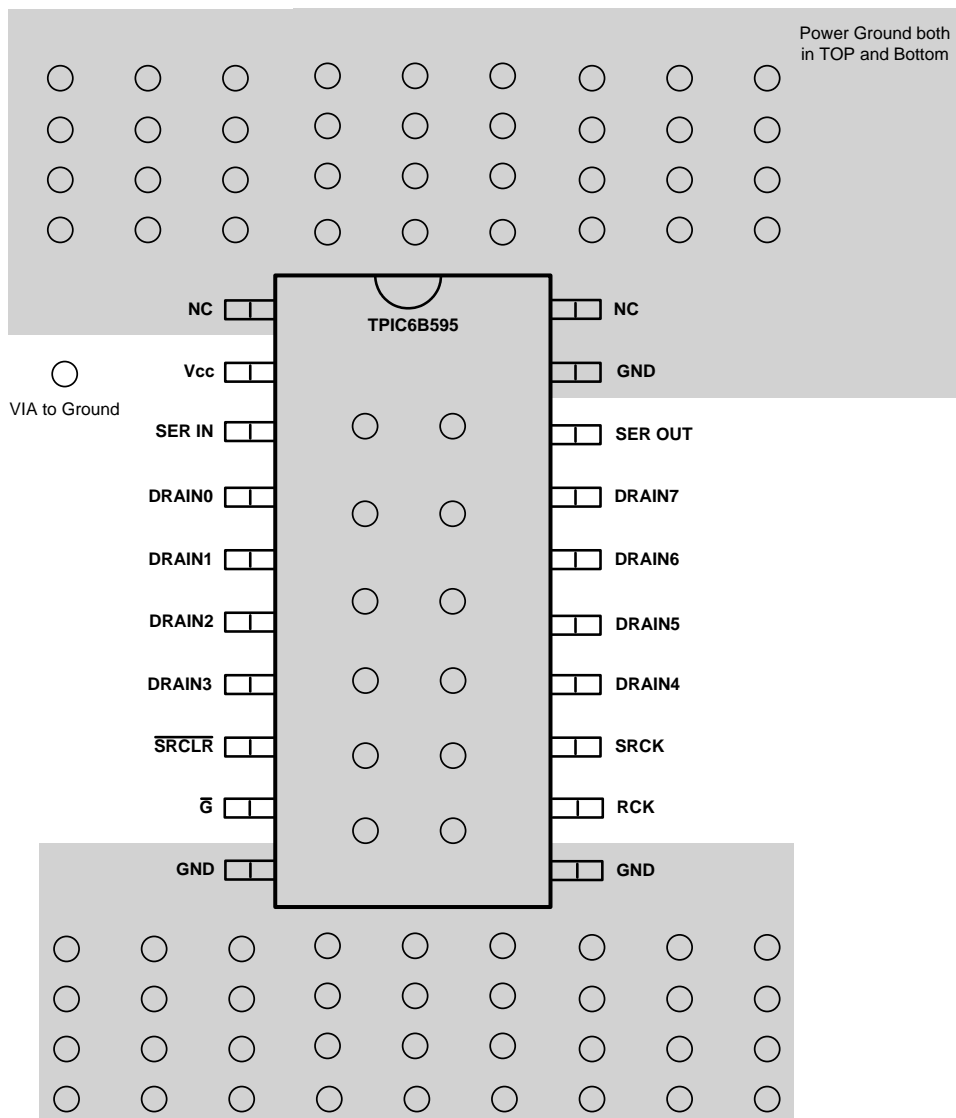


Figure 16. TPIC6B595 Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TPIC6B595DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TPIC6B595 | Samples |
| TPIC6B595N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TPIC6B595N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

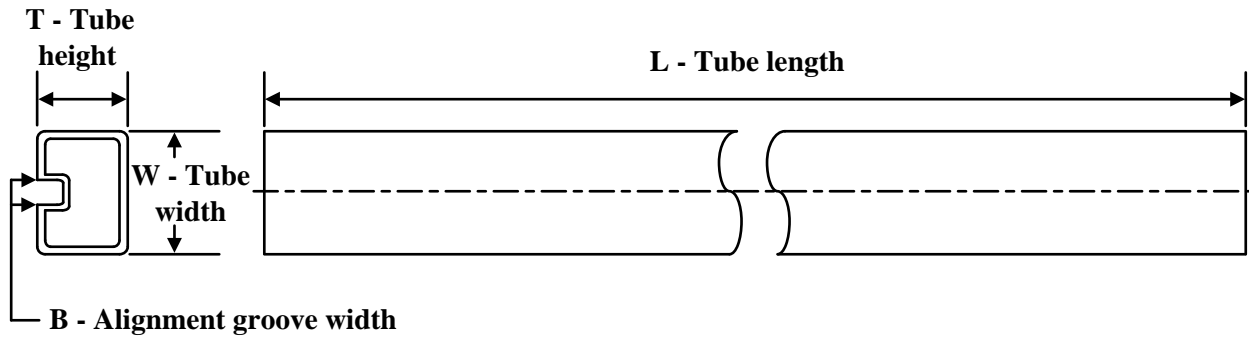

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPIC6B595DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| TPIC6B595DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPIC6B595DWR | SOIC | DW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| TPIC6B595DWR | SOIC | DW | 20 | 2000 | 350.0 | 350.0 | 43.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPIC6B595N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

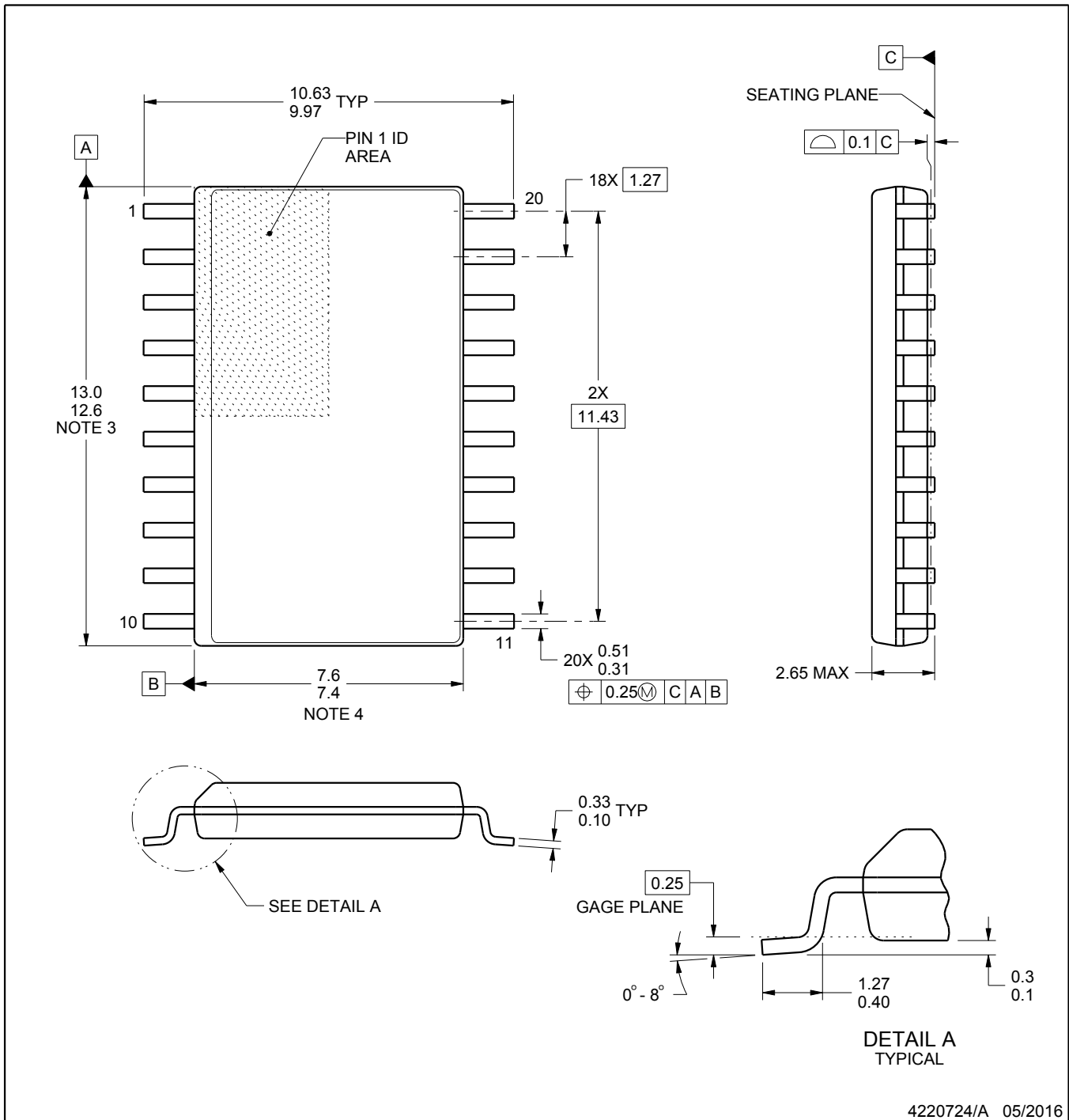
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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