



# THE DATASHEET OF TPS2052BDR



## TPS20xxB Current-Limited, Power-Distribution Switches

### 1 Features

- 70-mΩ High-Side MOSFET
- 500-mA Continuous Current
- Thermal and Short-Circuit Protection
- Accurate Current Limit (0.75 A Minimum, 1.25 A Maximum)
- Operating Range: 2.7 V to 5.5 V
- 0.6-ms Typical Rise Time
- Undervoltage Lockout
- Deglitched Fault Report ( $\overline{OC}$ )
- No  $\overline{OC}$  Glitch During Power Up
- Maximum Standby Supply Current: 1-μA (Single, Dual) or 2-μA (Triple, Quad)
- Ambient Temperature Range: -40°C to 85°C
- UL Recognized, File Number E169910
- Additional UL Recognition for TPS2042B and TPS2052B for Ganged Configuration

### 2 Applications

- Heavy Capacitive Loads
- Short-Circuit Protections

### 3 Description

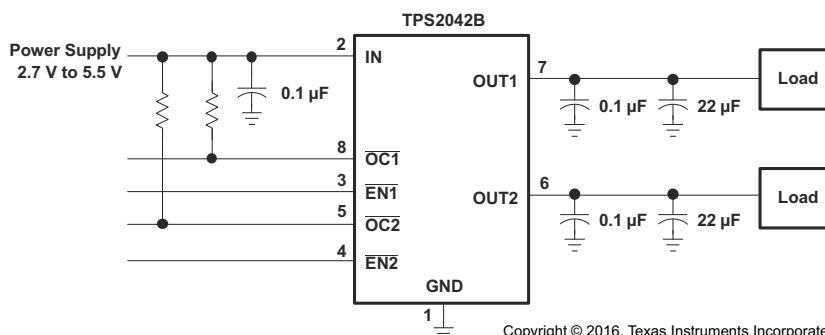
The TPS20xxB power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices incorporate 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ( $\overline{OCx}$ ) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1 A (typical).

#### Device Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)   |
|-------------|------------------------|-------------------|
| TPS20xxB    | SOIC (8)               | 4.90 mm × 3.91 mm |
|             | SOIC (16)              | 9.90 mm × 3.91 mm |
|             | SOT-23 (5)             | 2.90 mm × 1.60 mm |
|             | HVSSOP (8)             | 3.00 mm × 3.00 mm |
|             | SON (8)                | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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#### Typical Application Schematic



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






## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

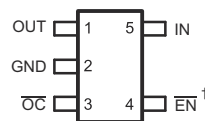
| Changes from Revision M (June 2016) to Revision N (July 2023)   | Page |
|---|------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document.....   | 1    |
| • Update TPS2051BDBV and TPS2052BD electrical characteristics, including overcurrent trip threshold, high-level output supply current and undervoltage lockout..... | 7    |
| • Updated TPS2051BDBV and TPS2052BD Typical Characteristics.....  | 14   |
| • Moved overcurrent description from Application and Implementation section to Detailed Description section.....  | 22   |
| • Added TPS2051BDBV and TPS2052BD overcurrent description.....  | 22   |

| Changes from Revision L (June 2011) to Revision M (June 2016)  | Page |
|--|------|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | 6    |

## 5 General Switch Catalog

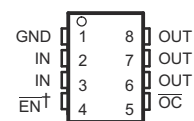
| GENERAL SWITCH CATALOG  |   |  |   |  |  |   |
|---|---|--|---|--|--|---|
| <p>33 mΩ, Single</p>  <p>TPS201xA 0.2 A to 2 A<br/>TPS202x 0.2 A to 2 A<br/>TPS203x 0.2 A to 2 A</p> | <p>80 mΩ, Single</p>  <p>TPS2014 600 mA<br/>TPS2015 1 A<br/>TPS2041B 500 mA<br/>TPS2051B 500 mA<br/>TPS2045A 250 mA<br/>TPS2049 100 mA<br/>TPS2055A 250 mA<br/>TPS2061 1 A<br/>TPS2065 1 A<br/>TPS2068 1.5 A<br/>TPS2069 1.5 A</p> | <p>80 mΩ, Dual</p>  <p>TPS2042B 500 mA<br/>TPS2052B 500 mA<br/>TPS2046B 250 mA<br/>TPS2056 250 mA<br/>TPS2062 1 A<br/>TPS2066 1 A<br/>TPS2060 1.5 A<br/>TPS2064 1.5 A</p> | <p>80 mΩ, Dual</p>  <p>TPS2080 500 mA<br/>TPS2081 500 mA<br/>TPS2082 500 mA<br/>TPS2090 250 mA<br/>TPS2091 250 mA<br/>TPS2092 250 mA</p> | <p>80 mΩ, Triple</p>  <p>TPS2043B 500 mA<br/>TPS2053B 500 mA<br/>TPS2047B 250 mA<br/>TPS2057A 250 mA<br/>TPS2063 1 A<br/>TPS2067 1 A</p> | <p>80 mΩ, Quad</p>  <p>TPS2044B 500 mA<br/>TPS2054B 500 mA<br/>TPS2048A 250 mA<br/>TPS2058 250 mA</p> | <p>80 mΩ, Quad</p>  <p>TPS2085 500 mA<br/>TPS2086 500 mA<br/>TPS2087 500 mA<br/>TPS2095 250 mA<br/>TPS2096 250 mA<br/>TPS2097 250 mA</p> |

## 6 Pin Configuration and Functions



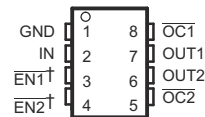
† All enable outputs are active high for the TPS205xB series.

**Figure 6-1. TPS2041B and TPS2051B: DBV Package 5-Pin SOT-23 Top View**



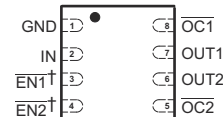
† All enable outputs are active high for the TPS205xB series.

**Figure 6-2. TPS2041B and TPS2051B: D and DGN Packages 8-Pin SOIC and HVSSOP Top View**



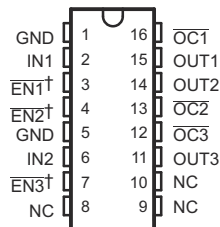
† All enable outputs are active high for the TPS205xB series.

**Figure 6-3. TPS2042B and TPS2052B: D and DGN Packages 8-Pin SOIC and HVSSOP Top View**



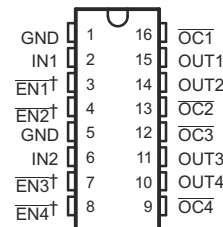
† All enable outputs are active high for the TPS205xB series.

**Figure 6-4. TPS2042B and TPS2052B: DRB Package 8-Pin SON Top View**



† All enable outputs are active high for the TPS205xB series.

**Figure 6-5. TPS2043B and TPS2053B: D Package 16-Pin SOIC Top View**



† All enable outputs are active high for the TPS205xB series.

**Figure 6-6. TPS2044B and TPS2054B: D Package 16-Pin SOIC Top View**

**Table 6-1. Pin Functions (TPS2041B and TPS2051B)**

| NAME | PIN          |          |          |          | I/O | DESCRIPTION                                    |
|------|--------------|----------|----------|----------|-----|--|
|      | TPS2041B     | TPS2051B | TPS2041B | TPS2051B |     |  |
|      | SOIC AND DGN |          | SOT-23   |          |     |  |
| EN   | 4            | —        | 4        | —        | I   | Enable input, logic low turns on power switch  |
| EN   | —            | 4        | —        | 4        | I   | Enable input, logic high turns on power switch |
| GND  | 1            | 1        | 2        | 2        | —   | Ground   |
| IN   | 2, 3         | 2, 3     | 5        | 5        | I   | Input voltage                                  |
| OC   | 5            | 5        | 3        | 3        | O   | Overcurrent open-drain output, active-low      |
| OUT  | 6, 7, 8      | 6, 7, 8  | 1        | 1        | O   | Power-switch output                            |

**Table 6-2. Pin Functions (TPS2042B and TPS2052B)**

| NAME      | PIN               |          | I/O | DESCRIPTION  |
|-----------|-------------------|----------|-----|--|
|           | TPS2042B          | TPS2052B |     |  |
|           | SOIC, HVSSOP, SON |          |     |  |
| EN1       | 3                 | —        | I   | Enable input, logic low turns on power switch IN-OUT1  |
| EN2       | 4                 | —        | I   | Enable input, logic low turns on power switch IN-OUT2  |
| EN1       | —                 | 3        | I   | Enable input, logic high turns on power switch IN-OUT1   |
| EN2       | —                 | 4        | I   | Enable input, logic high turns on power switch IN-OUT2   |
| GND       | 1                 | 1        | —   | Ground   |
| IN        | 2                 | 2        | I   | Input voltage  |
| OC1       | 8                 | 8        | O   | Overcurrent, open-drain output, active low, IN-OUT1  |
| OC2       | 5                 | 5        | O   | Overcurrent, open-drain output, active low, IN-OUT2  |
| OUT1      | 7                 | 7        | O   | Power-switch output, IN-OUT1   |
| OUT2      | 6                 | 6        | O   | Power-switch output, IN-OUT2   |
| PowerPAD™ | —                 | —        | —   | Internally connected to GND; used to heat-sink the part to the circuit board traces. Should be connected to GND pin. |

**Table 6-3. Pin Functions (TPS2043B and TPS2053B)**

| NAME | PIN      |          | I/O | DESCRIPTION   |
|------|----------|----------|-----|---|
|      | TPS2043B | TPS2053B |     |   |
|      | SOIC     |          |     |   |
| EN1  | 3        | —        | I   | Enable input, logic low turns on power switch IN1-OUT1  |
| EN2  | 4        | —        | I   | Enable input, logic low turns on power switch IN1-OUT2  |
| EN3  | 7        | —        | I   | Enable input, logic low turns on power switch IN2-OUT3  |
| EN1  | —        | 3        | I   | Enable input, logic high turns on power switch IN1-OUT1 |
| EN2  | —        | 4        | I   | Enable input, logic high turns on power switch IN1-OUT2 |
| EN3  | —        | 7        | I   | Enable input, logic high turns on power switch IN2-OUT3 |
| GND  | 1, 5     | 1, 5     | —   | Ground  |
| IN1  | 2        | 2        | I   | Input voltage for OUT1 and OUT2                         |
| IN2  | 6        | 6        | I   | Input voltage for OUT3                                  |
| NC   | 8, 9, 10 | 8, 9, 10 | —   | No connection   |
| OC1  | 16       | 16       | O   | Overcurrent, open-drain output, active low, IN1-OUT1    |
| OC2  | 13       | 13       | O   | Overcurrent, open-drain output, active low, IN1-OUT2    |
| OC3  | 12       | 12       | O   | Overcurrent, open-drain output, active low, IN2-OUT3    |
| OUT1 | 15       | 15       | O   | Power-switch output, IN1-OUT1                           |
| OUT2 | 14       | 14       | O   | Power-switch output, IN1-OUT2                           |
| OUT3 | 11       | 11       | O   | Power-switch output, IN2-OUT3                           |

**Table 6-4. Pin Functions (TPS2044B and TPS2054B)**

| NAME | PIN      |          | I/O | DESCRIPTION   |
|------|----------|----------|-----|---|
|      | TPS2044B | TPS2054B |     |   |
|      | SOIC     |          |     |   |
| EN1  | 3        | —        | I   | Enable input, logic low turns on power switch IN1-OUT1  |
| EN2  | 4        | —        | I   | Enable input, logic low turns on power switch IN1-OUT2  |
| EN3  | 7        | —        | I   | Enable input, logic low turns on power switch IN2-OUT3  |
| EN4  | 8        | —        | I   | Enable input, logic low turns on power switch IN2-OUT4  |
| EN1  | —        | 3        | I   | Enable input, logic high turns on power switch IN1-OUT1 |
| EN2  | —        | 4        | I   | Enable input, logic high turns on power switch IN1-OUT2 |

**Table 6-4. Pin Functions (TPS2044B and TPS2054B) (continued)**

| NAME             | PIN      |          | I/O | DESCRIPTION   |
|------------------|----------|----------|-----|---|
|                  | TPS2044B | TPS2054B |     |   |
|                  | SOIC     | SOIC     |     |   |
| EN3              | —        | 7        | I   | Enable input, logic high turns on power switch IN2-OUT3 |
| EN4              | —        | 8        | I   | Enable input, logic high turns on power switch IN2-OUT4 |
| GND              | 1, 5     | 1, 5     | —   | Ground  |
| IN1              | 2        | 2        | I   | Input voltage for OUT1 and OUT2                         |
| IN2              | 6        | 6        | I   | Input voltage for OUT3 and OUT4                         |
| $\overline{OC1}$ | 16       | 16       | O   | Overcurrent, open-drain output, active low, IN1-OUT1    |
| $\overline{OC2}$ | 13       | 13       | O   | Overcurrent, open-drain output, active low, IN1-OUT2    |
| $\overline{OC3}$ | 12       | 12       | O   | Overcurrent, open-drain output, active low, IN2-OUT3    |
| $\overline{OC4}$ | 9        | 9        | O   | Overcurrent, open-drain output, active low, IN2-OUT4    |
| OUT1             | 15       | 15       | O   | Power-switch output, IN1-OUT1                           |
| OUT2             | 14       | 14       | O   | Power-switch output, IN1-OUT2                           |
| OUT3             | 11       | 11       | O   | Power-switch output, IN2-OUT3                           |
| OUT4             | 10       | 10       | O   | Power-switch output, IN2-OUT4                           |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|  |  | MIN                                     | MAX | UNIT |
|--|--|---|-----|------|
| $V_{I(IN)}$ , $V_{I(INx)}$                                       | Input voltage <sup>(2)</sup>           | -0.3                                    | 6   | V    |
| $V_{O(OUT)}$ , $V_{O(OUTx)}$ <sup>(2)</sup>                      | Output voltage                         | -0.3                                    | 6   | V    |
| $V_{I(EN)}$ , $V_{I(EN\bar{x})}$ , $V_{I(EN)}$ ,<br>$V_{I(ENx)}$ | Input voltage                          | -0.3                                    | 6   | V    |
| $V_{I(OC)}$ , $V_{I(OC\bar{x})}$                                 | Voltage range                          | -0.3                                    | 6   | V    |
| $I_{O(OUT)}$ , $I_{O(OUTx)}$                                     | Continuous output current              | Internally limited                      |     |      |
|  | Continuous total power dissipation     | See <a href="#">Dissipation Ratings</a> |     |      |
| $T_J$  | Operating virtual junction temperature | -40                                     | 125 | °C   |
| $T_{stg}$  | Storage temperature                    | -65                                     | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND.

### 7.2 ESD Ratings

|                                     |  | VALUE | UNIT |
|-------------------------------------|--|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2000 | V    |
|                                     | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | NOM | MAX | UNIT |
|--|--|-----|-----|-----|------|
| $V_{I(IN)}$ , $V_{I(INx)}$                                       | Input voltage                          | 2.7 |     | 5.5 | V    |
| $V_{I(EN)}$ , $V_{I(EN\bar{x})}$ , $V_{I(EN)}$ ,<br>$V_{I(ENx)}$ | Input voltage                          | 0   |     | 5.5 | V    |
| $I_{O(OUT)}$ , $I_{O(OUTx)}$                                     | Continuous output current              | 0   |     | 500 | mA   |
| $T_J$  | Operating virtual junction temperature | -40 |     | 125 | °C   |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | TPS2042xx and TPS2053xx                      |         |              |              |           | UNIT |      |
|-------------------------------|--|---------|--------------|--------------|-----------|------|------|
|                               | D (SOIC)                                     |         | DBV (SOT-23) | DGN (HVSSOP) | DRB (SON) |      |      |
|                               | 8 PINS                                       | 16 PINS | 5 PINS       | 8 PINS       | 8 PINS    |      |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 119.3   | 81.6         | 208.6        | 53.6      | 47.5 | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 67.6    | 42.7         | 122.9        | 58.7      | 53   | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 59.6    | 39.1         | 37.8         | 35.5      | 14.2 | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 20.3    | 10.4         | 14.6         | 2.7       | 1.2  | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 59.1    | 38.8         | 36.9         | 35.3      | 14.2 | °C/W |

## 7.4 Thermal Information (continued)

| THERMAL METRIC <sup>(1)</sup>                                     | TPS2042xx and TPS2053xx |         |              |              |           | UNIT |
|---|-------------------------|---------|--------------|--------------|-----------|------|
|   | D (SOIC)                |         | DBV (SOT-23) | DGN (HVSSOP) | DRB (SON) |      |
|   | 8 PINS                  | 16 PINS | 5 PINS       | 8 PINS       | 8 PINS    |      |
| $R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance | N/A                     | N/A     | N/A          | 6.7          | 7.3       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

over recommended operating junction temperature range,  $V_{I(IN)} = 5.5\text{ V}$ ,  $I_O = 0.5\text{ A}$ ,  $V_{I(ENx)} = 0\text{ V}$  (unless otherwise noted)

| PARAMETER                                  |  | TEST CONDITIONS <sup>(1)</sup>  |   | MIN                | TYP  | MAX  | UNIT |
|--|--|---|---|--------------------|------|------|------|
| <b>POWER SWITCH</b>                        |  |   |   |                    |      |      |      |
| $r_{DS(on)}$                               | Static drain-source on-state resistance, 5-V operation and 3.3-V operation | $V_{I(IN)} = 5\text{ V}$ or $3.3\text{ V}$ , $I_O = 0.5\text{ A}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$   | D and DGN packages  | 70                 | 135  |      | mΩ   |
|  |  |   | DBV package only  | 95                 | 140  |      |      |
|  |  | Static drain-source on-state resistance, 2.7-V operation  | $V_{I(IN)} = 2.7\text{ V}$ , $I_O = 0.5\text{ A}$ , $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | D and DGN packages | 75   | 150  |      |
|  | Static drain-source on-state resistance, 5-V operation                     | $V_{I(IN)} = 5\text{ V}$ , $I_O = 1\text{ A}$ , OUT1 and OUT2 connected, $0^\circ\text{C} \leq T_J \leq 70^\circ\text{C}$ | DGN package, TPS2042B/52B   |                    |      | 49   | mΩ   |
| $t_r$                                      | Rise time, output  | $V_{I(IN)} = 5.5\text{ V}$<br>$V_{I(IN)} = 2.7\text{ V}$  | $C_L = 1\text{ }\mu\text{F}$ ,<br>$R_L = 10\text{ }\Omega$<br>$T_J = 25^\circ\text{C}$                  | 0.6                | 1.5  |      | ms   |
| $t_f$                                      | Fall time, output  | $V_{I(IN)} = 5.5\text{ V}$<br>$V_{I(IN)} = 2.7\text{ V}$  |   | 0.05               | 0.5  |      |      |
|  |  |   |   | 0.05               | 0.5  |      |      |
|  |  |   |   |                    |      |      |      |
| <b>ENABLE INPUT EN AND ENx</b>             |  |   |   |                    |      |      |      |
| $V_{IH}$                                   | High-level input voltage   | $2.7\text{ V} \leq V_{I(IN)} \leq 5.5\text{ V}$   |   | 2                  |      |      | V    |
| $V_{IL}$                                   | Low-level input voltage  | $2.7\text{ V} \leq V_{I(IN)} \leq 5.5\text{ V}$   |   |                    | 0.8  |      |      |
| $I_I$                                      | Input current  | $V_{I(ENx)} = 0\text{ V}$ or $5.5\text{ V}$   |   | -0.5               | 0.5  |      | μA   |
| $t_{on}$                                   | Turnon time  | $C_L = 100\text{ }\mu\text{F}$ , $R_L = 10\text{ }\Omega$   |   |                    |      | 3    | ms   |
| $t_{off}$                                  | Turnoff time   | $C_L = 100\text{ }\mu\text{F}$ , $R_L = 10\text{ }\Omega$   |   |                    |      | 10   |      |
| <b>CURRENT LIMIT</b>                       |  |   |   |                    |      |      |      |
| $I_{OS}$                                   | Short-circuit output current   | $V_{I(IN)} = 5\text{ V}$ , OUT connected to GND, device enabled into short-circuit  | $T_J = 25^\circ\text{C}$  | 0.75               | 1    | 1.25 | A    |
|  |  |   | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$   | 0.7                | 1    | 1.3  |      |
|  |  | $V_{I(IN)} = 5\text{ V}$ , OUT1 and OUT2 connected to GND, device enabled into short-circuit, measure at IN               | $0^\circ\text{C} \leq T_J \leq 70^\circ\text{C}$<br>TPS2042B/52B  | 1.5                |      |      |      |
| $I_{OC}^{(2)}$                             | Overcurrent trip threshold   | $V_{IN} = 5\text{ V}$ , 100 A/s   | TPS2041B  | $I_{OS}$           | 1.5  | 1.9  | A    |
|  |  |   | TPS2051B (D and DGN packages only)  |                    |      |      |      |
|  |  |   | TPS2042B<br>TPS2052B (DGN package only)   | $I_{OS}$           | 1.55 | 2    |      |
| <b>SUPPLY CURRENT (TPS2041B, TPS2051B)</b> |  |   |   |                    |      |      |      |
| Supply current, low-level output           | No load on OUT, $V_{I(ENx)} = 5.5\text{ V}$ , or $V_{I(ENx)} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$  |   | 0.5                | 1    |      | μA   |
|  |  | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$   |   | 0.5                | 5    |      |      |

## 7.5 Electrical Characteristics (continued)

over recommended operating junction temperature range,  $V_{I(IN)} = 5.5\text{ V}$ ,  $I_O = 0.5\text{ A}$ ,  $V_{I(ENx)} = 0\text{ V}$  (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS <sup>(1)</sup>  |   | MIN   | TYP                      | MAX           | UNIT             |
|---|---|---|---|--------------------------|---------------|------------------|
| Supply current, high-level output   | No load on OUT, $V_{I(ENx)} = 0\text{ V}$ , or $V_{I(ENx)} = 5.5\text{ V}$          | TPS2041B  | $T_J = 25^\circ\text{C}$                            | 43                       | 60            | $\mu\text{A}$    |
|   |   | TPS2051B (D and DGN packages only)                  | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 43                       | 70            |                  |
|   |   |   | TPS2051BDBV   | $T_J = 25^\circ\text{C}$ | 75            |                  |
|   |   | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 75  | 95                       |               |                  |
| Leakage current   | OUT connected to ground, $V_{I(ENx)} = 5.5\text{ V}$ , or $V_{I(ENx)} = 0\text{ V}$ | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 1   |                          |               | $\mu\text{A}$    |
| Reverse leakage current   | $V_{I(OUTx)} = 5.5\text{ V}$ , IN = ground  | $T_J = 25^\circ\text{C}$                            | 0   |                          |               | $\mu\text{A}$    |
| <b>SUPPLY CURRENT (TPS2042B, TPS2052B)</b>  |   |   |   |                          |               |                  |
| Supply current, low-level output  | No load on OUT, $V_{I(ENx)} = 5.5\text{ V}$   | $T_J = 25^\circ\text{C}$                            | 0.5   | 1                        | $\mu\text{A}$ |                  |
|   |   | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 0.5   | 5                        |               |                  |
| Supply current, high-level output   | No load on OUT, $V_{I(ENx)} = 0\text{ V}$   | TPS2042B  | $T_J = 25^\circ\text{C}$                            | 50                       | 70            | $\mu\text{A}$    |
|   |   | TPS2052B (DGN package only)                         | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 50                       | 90            |                  |
|   |   |   | TPS2052BD   | $T_J = 25^\circ\text{C}$ | 95            | 120              |
|   |   | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 95  | 120                      |               |                  |
| Leakage current   | OUT connected to ground, $V_{I(ENx)} = 5.5\text{ V}$                                | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 1   |                          |               | $\mu\text{A}$    |
| Reverse leakage current   | $V_{I(OUTx)} = 5.5\text{ V}$ , IN = ground  | $T_J = 25^\circ\text{C}$                            | 0.2   |                          |               | $\mu\text{A}$    |
| <b>SUPPLY CURRENT (TPS2043B, TPS2053B)</b>  |   |   |   |                          |               |                  |
| Supply current, low-level output  | No load on OUT, $V_{I(ENx)} = 0\text{ V}$   | $T_J = 25^\circ\text{C}$                            | 0.5   | 2                        | $\mu\text{A}$ |                  |
|   |   | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 0.5   | 10                       |               |                  |
| Supply current, high-level output   | No load on OUT, $V_{I(ENx)} = 5.5\text{ V}$   | $T_J = 25^\circ\text{C}$                            | 65  | 90                       | $\mu\text{A}$ |                  |
|   |   | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 65  | 110                      |               |                  |
| Leakage current   | OUT connected to ground, $V_{I(ENx)} = 0\text{ V}$                                  | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 1   |                          |               | $\mu\text{A}$    |
| Reverse leakage current   | $V_{I(OUTx)} = 5.5\text{ V}$ , INx = ground   | $T_J = 25^\circ\text{C}$                            | 0.2   |                          |               | $\mu\text{A}$    |
| <b>SUPPLY CURRENT (TPS2044B, TPS2054B)</b>  |   |   |   |                          |               |                  |
| Supply current, low-level output  | No load on OUT, $V_{I(ENx)} = 5.5\text{ V}$ , or $V_{I(ENx)} = 0\text{ V}$          | $T_J = 25^\circ\text{C}$                            | 0.5   | 2                        | $\mu\text{A}$ |                  |
|   |   | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 0.5   | 10                       |               |                  |
| Supply current, high-level output   | No load on OUT, $V_{I(ENx)} = 0\text{ V}$ , or $V_{I(ENx)} = 5.5\text{ V}$          | $T_J = 25^\circ\text{C}$                            | 75  | 110                      | $\mu\text{A}$ |                  |
|   |   | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 75  | 140                      |               |                  |
| Leakage current   | OUT connected to ground, $V_{I(ENx)} = 5.5\text{ V}$ , or $V_{I(ENx)} = 0\text{ V}$ | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 1   |                          |               | $\mu\text{A}$    |
| Reverse leakage current   | $V_{I(OUTx)} = 5.5\text{ V}$ , INx = ground   | $T_J = 25^\circ\text{C}$                            | 0.2   |                          |               | $\mu\text{A}$    |
| <b>UNDERVOLTAGE LOCKOUT (All Devices excluding TPS2051BDBV and TPS2052BD)</b>               |   |   |   |                          |               |                  |
| Low-level input voltage, IN, INx  |   |   | 2   | 2.5                      |               | V                |
| Hysteresis, IN, INx   | $T_J = 25^\circ\text{C}$  |   | 75  |                          |               | mV               |
| <b>UNDERVOLTAGE LOCKOUT (TPS2051BDBV and TPS2052BD)</b>                                     |   |   |   |                          |               |                  |
| Low-level input voltage, IN, INx  |   |   | 2   | 2.6                      |               | V                |
| Hysteresis, IN, INx   | $T_J = 25^\circ\text{C}$  |   | 75  |                          |               | mV               |
| <b>OVERCURRENT <math>\overline{\text{OC}}</math> and <math>\overline{\text{OCx}}</math></b> |   |   |   |                          |               |                  |
| Output low voltage, $V_{OL(\overline{\text{OCx}})}$   | $I_{O(\overline{\text{OCx}})} = 5\text{ mA}$  |   |   | 0.4                      |               | V                |
| Off-state current   | $V_{O(\overline{\text{OCx}})} = 5\text{ V}$ or $3.3\text{ V}$                       |   |   | 1                        |               | $\mu\text{A}$    |
| $\overline{\text{OC}}$ deglitch   | $\overline{\text{OCx}}$ assertion or deassertion                                    |   | 4   | 8                        | 15            | ms               |
| <b>THERMAL SHUTDOWN<sup>(3)</sup></b>   |   |   |   |                          |               |                  |
| Thermal shutdown threshold  |   |   | 135   |                          |               | $^\circ\text{C}$ |

## 7.5 Electrical Characteristics (continued)

over recommended operating junction temperature range,  $V_{I(IN)} = 5.5\text{ V}$ ,  $I_O = 0.5\text{ A}$ ,  $V_{I(ENx)} = 0\text{ V}$  (unless otherwise noted)

| PARAMETER                      | TEST CONDITIONS <sup>(1)</sup> | MIN | TYP | MAX | UNIT |
|--------------------------------|--------------------------------|-----|-----|-----|------|
| Recovery from thermal shutdown |                                | 125 |     |     | °C   |
| Hysteresis                     |                                |     | 10  |     | °C   |

- (1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
- (2) TPS2051BDBV and TPS2052BD don't have overcurrent trip threshold. Current will be limited to  $I_{OS}$  under different test condition. Check [Section 9.3.7](#) for more details.
- (3) The thermal shutdown only reacts under overcurrent conditions.

## 7.6 Dissipation Ratings

| PACKAGE                       | THERMAL RESISTANCE, $\theta_{JA}$ | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$<br>POWER RATING | $T_A = 85^\circ\text{C}$<br>POWER RATING |
|-------------------------------|-----------------------------------|---|---|--|--|
| DGN-8                         |                                   | 1712.3 mW                                   | 17.123 mW/°C                                      | 941.78 mW                                | 684.93 mW                                |
| D-8                           |                                   | 585.82 mW                                   | 5.8582 mW/°C                                      | 322.20 mW                                | 234.32 mW                                |
| D-16                          |                                   | 898.47 mW                                   | 8.9847 mW/°C                                      | 494.15 mW                                | 359.38 mW                                |
| DBV-5                         |                                   | 285 mW                                      | 2.85 mW/°C  | 155 mW                                   | 114 mW                                   |
| DRB-8 (Low-K) <sup>(1)</sup>  | 270 °CW                           | 370 mW                                      | 3.71 mW/°C  | 203 mW                                   | 148 mW                                   |
| DRB-8 (High-K) <sup>(2)</sup> | 60 °CW                            | 1600 mW                                     | 16.67 mW/°C                                       | 916 mW                                   | 866 mW                                   |

- (1) Soldered PowerPAD on a standard 2-layer PCB without vias for thermal pad. See TI application note [SLMA002](#) for further details.
- (2) Soldered PowerPAD on a standard 4-layer PCB with vias for thermal pad. See TI application note [SLMA002](#) for further details.

## 7.7 Typical Characteristics (All Devices Excluding TPS2051BDBV and TPS2052BD)



Figure 7-1. Turnon Time vs Input Voltage

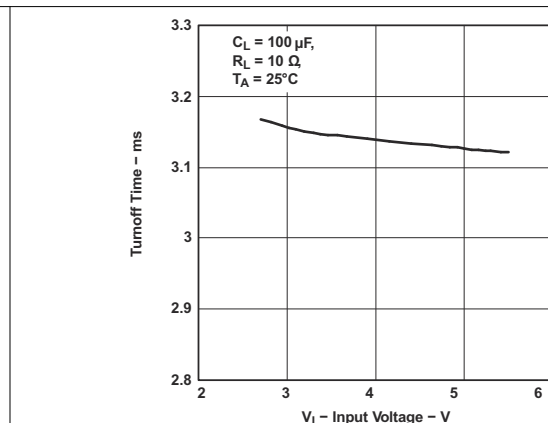


Figure 7-2. Turnoff Time vs Input Voltage

### 7.7 Typical Characteristics (All Devices Excluding TPS2051BDBV and TPS2052BD) (continued)



Figure 7-3. Rise Time vs Input Voltage



Figure 7-4. Fall Time vs Input Voltage

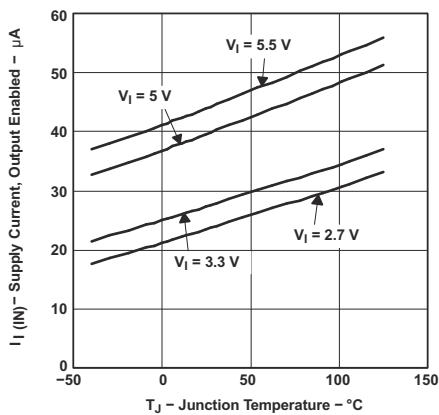


Figure 7-5. TPS2041B and TPS2051B Supply Current, Output Enabled vs Junction Temperature

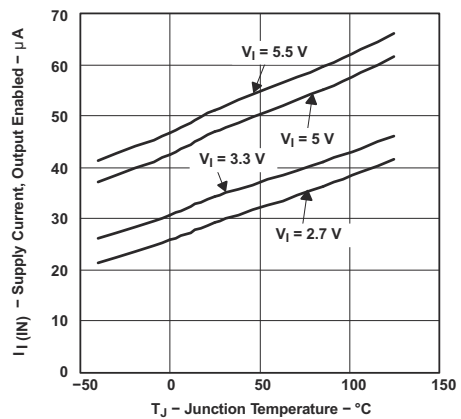


Figure 7-6. TPS2042B and TPS2052B Supply Current, Output Enabled vs Junction Temperature



Figure 7-7. TPS2043B and TPS2053B Supply Current, Output Enabled vs Junction Temperature

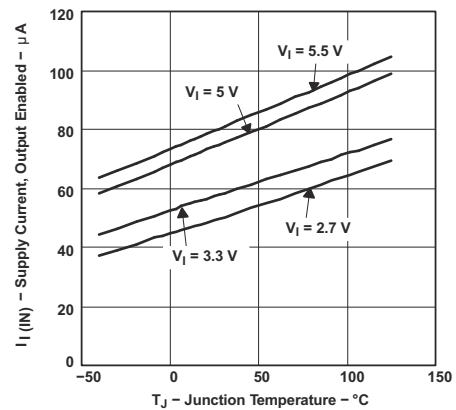


Figure 7-8. TPS2044B TPS2054B Supply Current, Output Enabled vs Junction Temperature

### 7.7 Typical Characteristics (All Devices Excluding TPS2051BDBV and TPS2052BD) (continued)

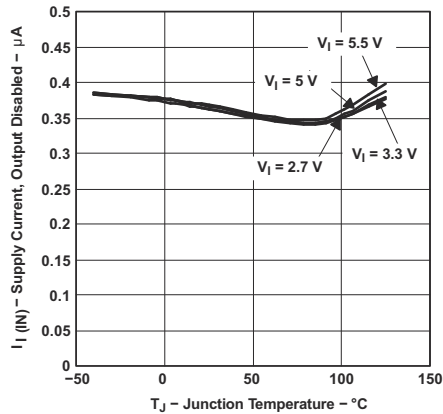


Figure 7-9. TPS2041B TPS2051B Supply Current, Output Disabled vs Junction Temperature

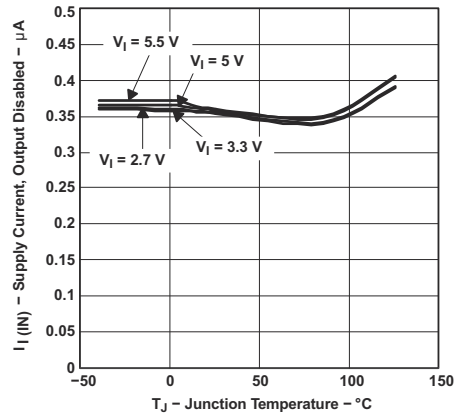


Figure 7-10. TPS2042B and TPS2052B Supply Current, Output Disabled vs Junction Temperature

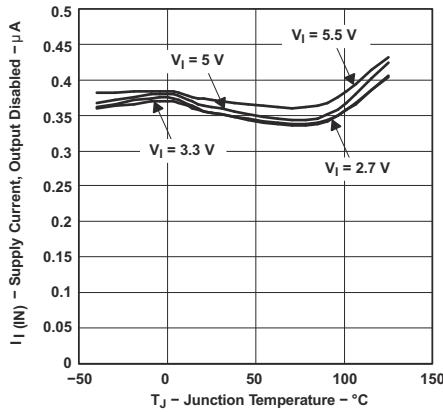


Figure 7-11. TPS2043B and TPS2053B Supply Current, Output Disabled vs Junction Temperature

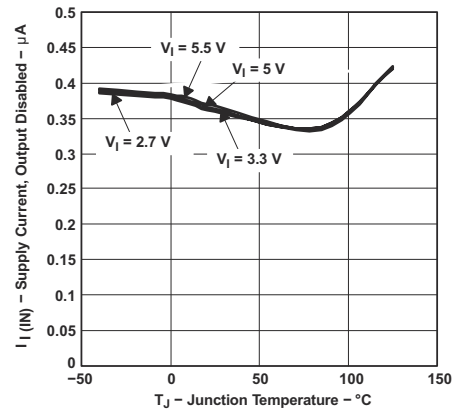


Figure 7-12. TPS2044B and TPS2054B Supply Current, Output Disabled vs Junction Temperature

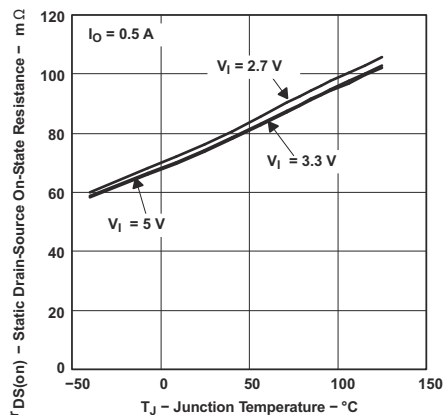


Figure 7-13. Static Drain-Source on-State Resistance vs Junction Temperature

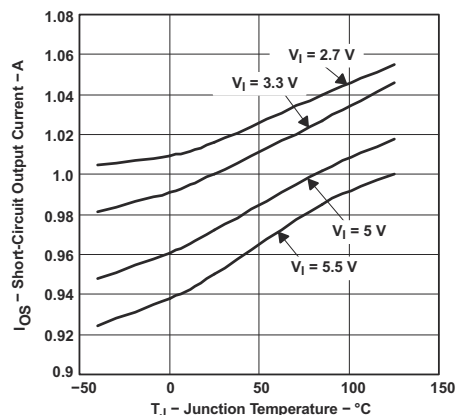


Figure 7-14. Short-Circuit Output Current vs Junction Temperature

## 7.7 Typical Characteristics (All Devices Excluding TPS2051BDBV and TPS2052BD) (continued)



Figure 7-15. Threshold Trip Current vs Input Voltage



Figure 7-16. Threshold Trip Current vs Input Voltage



Figure 7-17. Undervoltage Lockout vs Junction Temperature

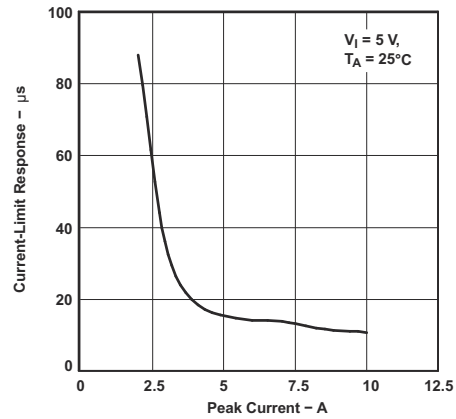


Figure 7-18. Current-Limit Response vs Peak Current

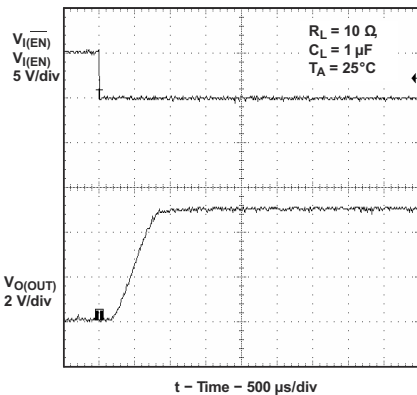


Figure 7-19. Turnon Delay and Rise Time With 1-µF Load

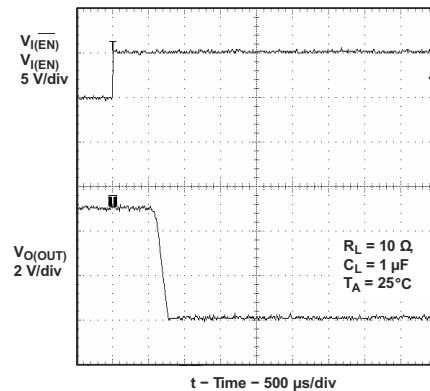


Figure 7-20. Turnoff Delay and Fall Time With 1-µF Load

### 7.7 Typical Characteristics (All Devices Excluding TPS2051BDBV and TPS2052BD) (continued)

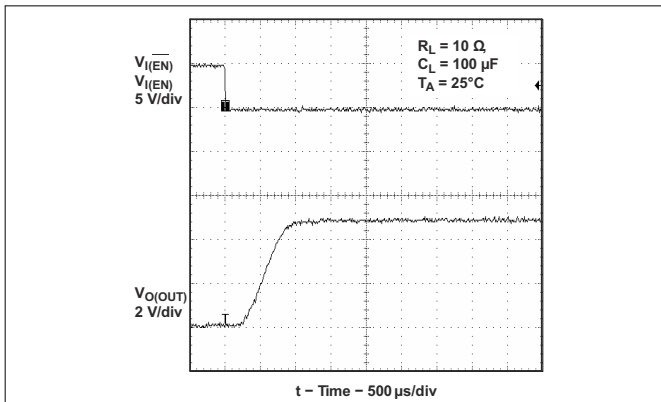


Figure 7-21. Turnon Delay and Rise Time With 100-µF Load

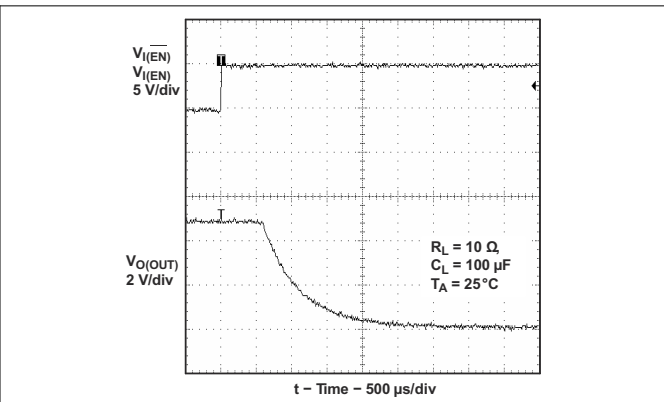


Figure 7-22. Turnoff Delay and Fall Time With 100-µF Load

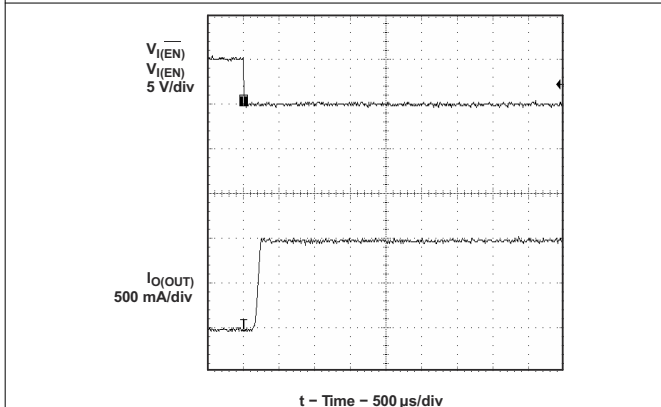


Figure 7-23. Short-Circuit Current, Device Enabled Into Short

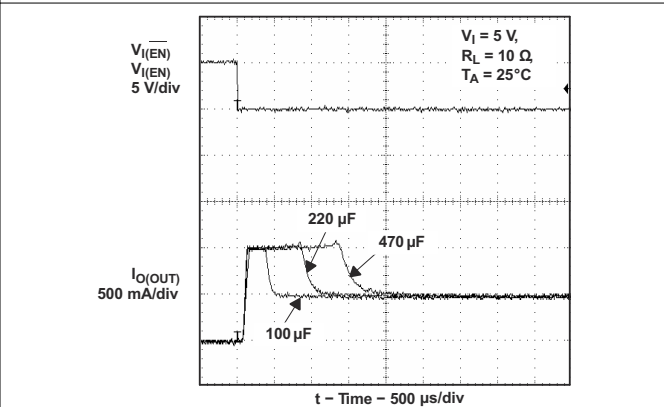


Figure 7-24. Inrush Current With Different Load Capacitance

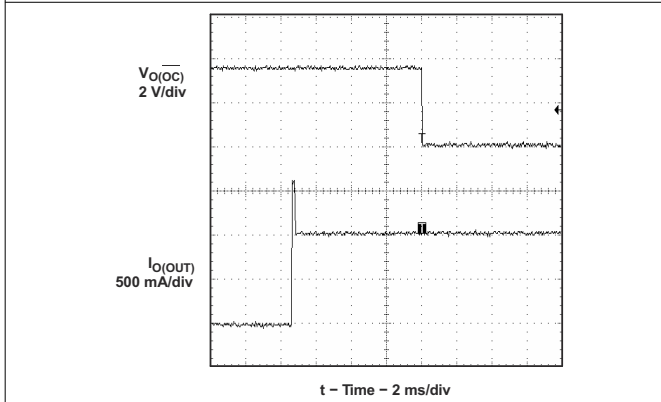


Figure 7-25. 3-Ω Load Connected to Enabled Device

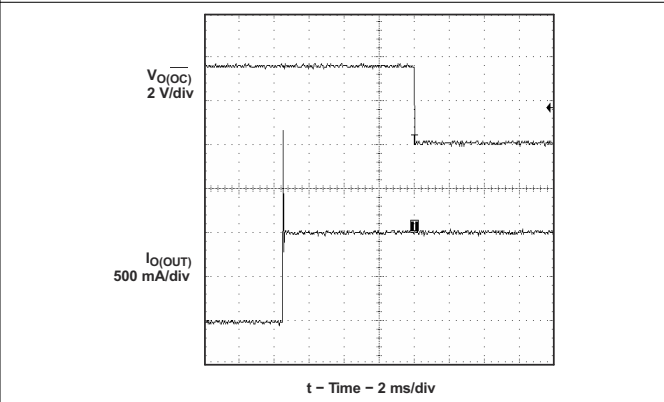


Figure 7-26. 2-Ω Load Connected to Enabled Device

## 7.8 Typical Characteristics (TPS2051BDBV and TPS2052BD)

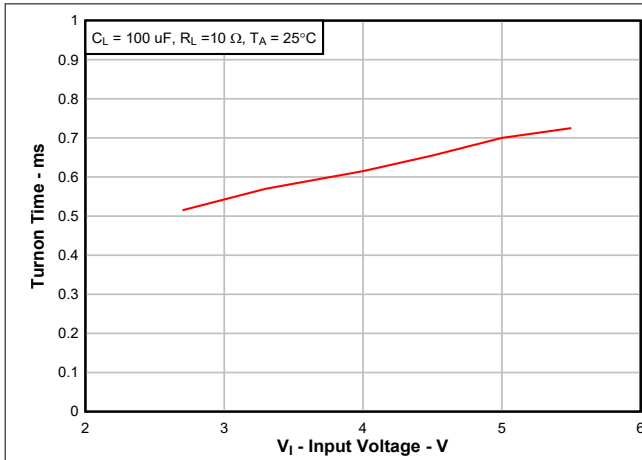


Figure 7-27. Turnon Time vs Input Voltage

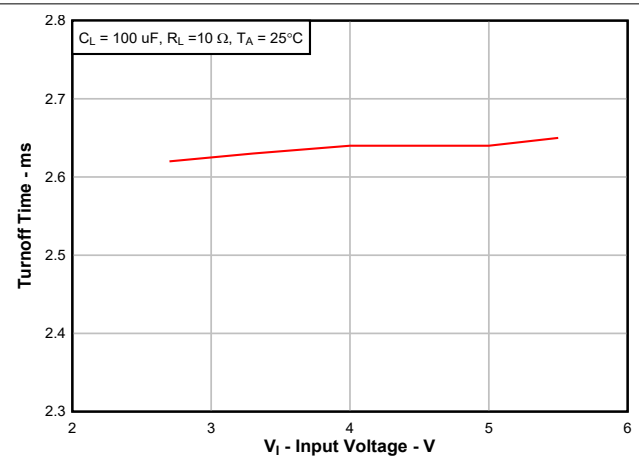


Figure 7-28. Turnoff Time vs Input Voltage



Figure 7-29. Rise Time vs Input Voltage



Figure 7-30. Fall Time vs Input Voltage

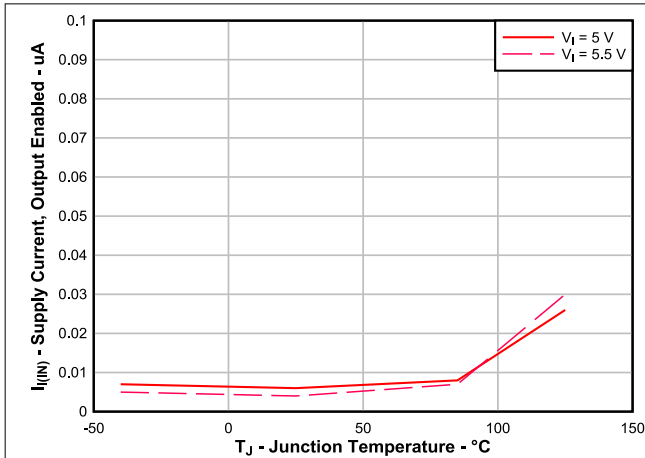


Figure 7-31. TPS2051BDBV Supply Current, Output Enabled vs Junction Temperature



Figure 7-32. TPS2052BD Supply Current, Output Enabled vs Junction Temperature

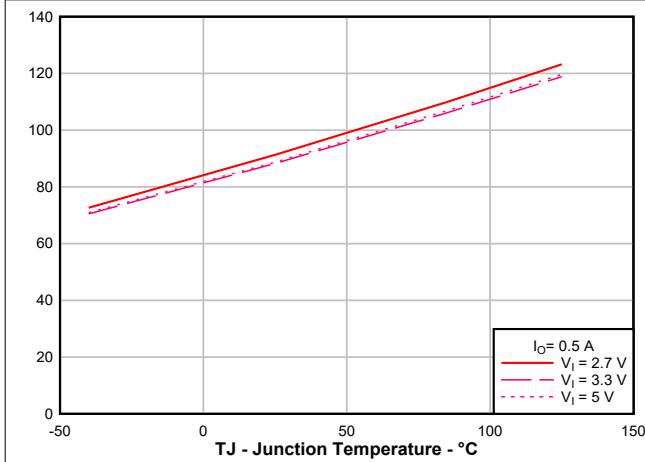
### 7.8 Typical Characteristics (TPS2051BDBV and TPS2052BD) (continued)



**Figure 7-33. TPS2051BDBV Supply Current, Output Disabled vs Junction Temperature**



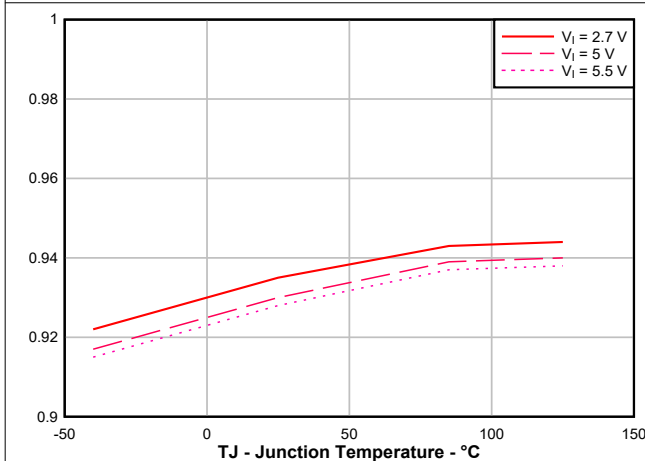
**Figure 7-34. TPS2052BD Supply Current, Output Disabled vs Junction Temperature**



**Figure 7-35. DBV Package Static Drain-Source on-State Resistance vs Junction Temperature**



**Figure 7-36. D Package Static Drain-Source on-State Resistance vs Junction Temperature**



**Figure 7-37. Short-Circuit Output Current vs Junction Temperature**



**Figure 7-38. Undervoltage Lockout vs Junction Temperature**

## 7.8 Typical Characteristics (TPS2051BDBV and TPS2052BD) (continued)

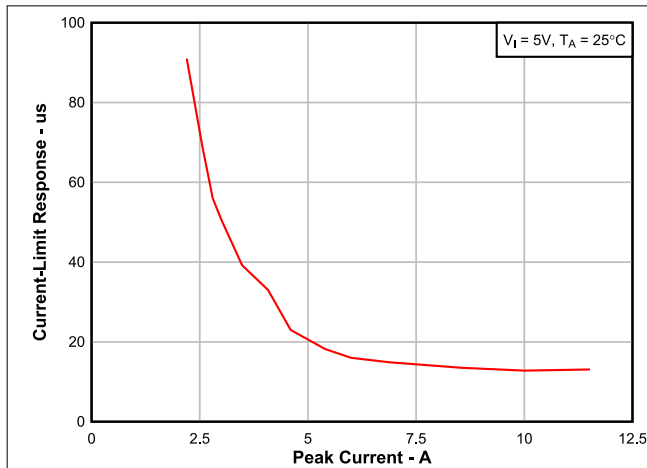


Figure 7-39. Current-Limit Response vs Peak Current

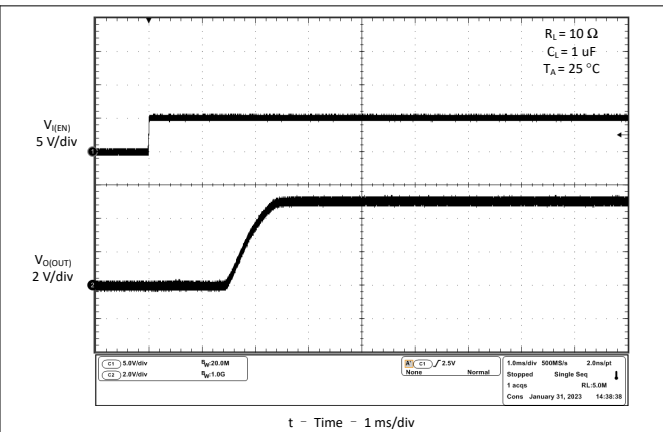


Figure 7-40. Turnon Delay and Rise Time With 1- $\mu$ F Load

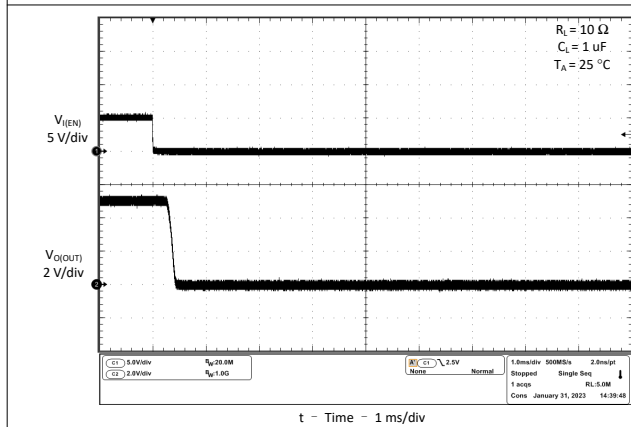


Figure 7-41. Turnoff Delay and Fall Time With 1- $\mu$ F Load

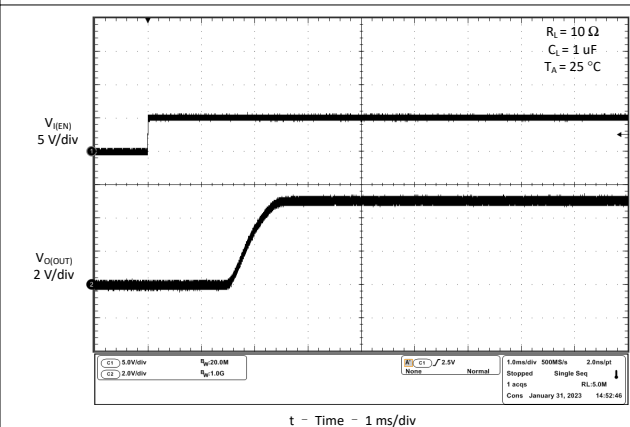


Figure 7-42. Turnon Delay and Rise Time With 100- $\mu$ F Load

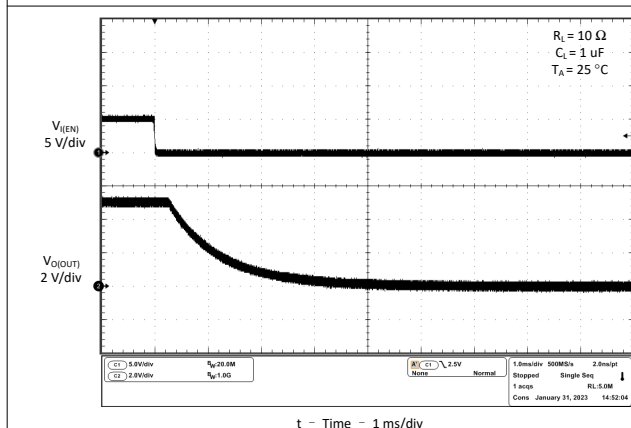


Figure 7-43. Turnoff Delay and Fall Time With 100- $\mu$ F Load

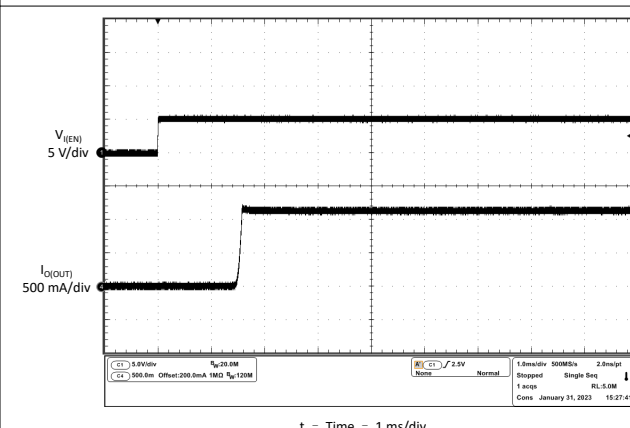
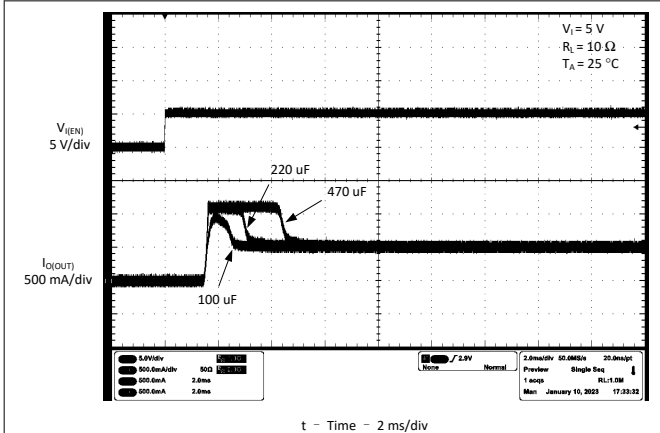
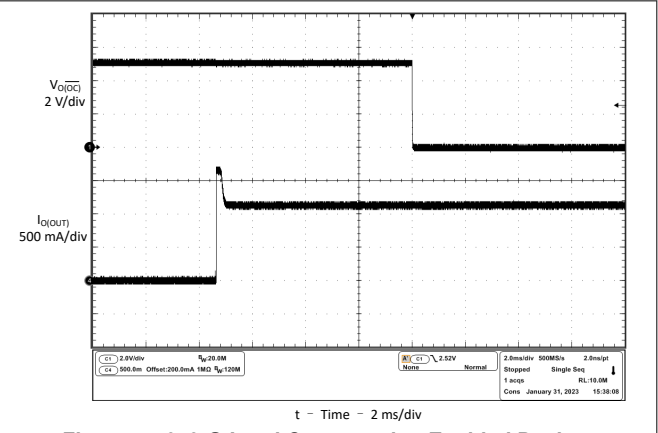


Figure 7-44. Short-Circuit Current, Device Enabled Into Short

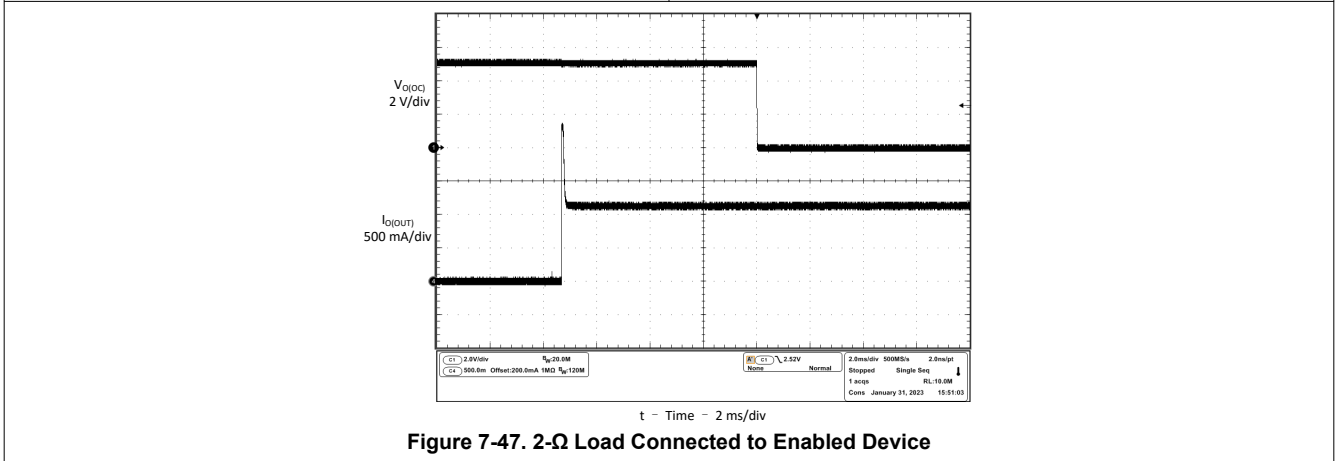
### 7.8 Typical Characteristics (TPS2051BDBV and TPS2052BD) (continued)



**Figure 7-45. Inrush Current With Different Load Capacitance**

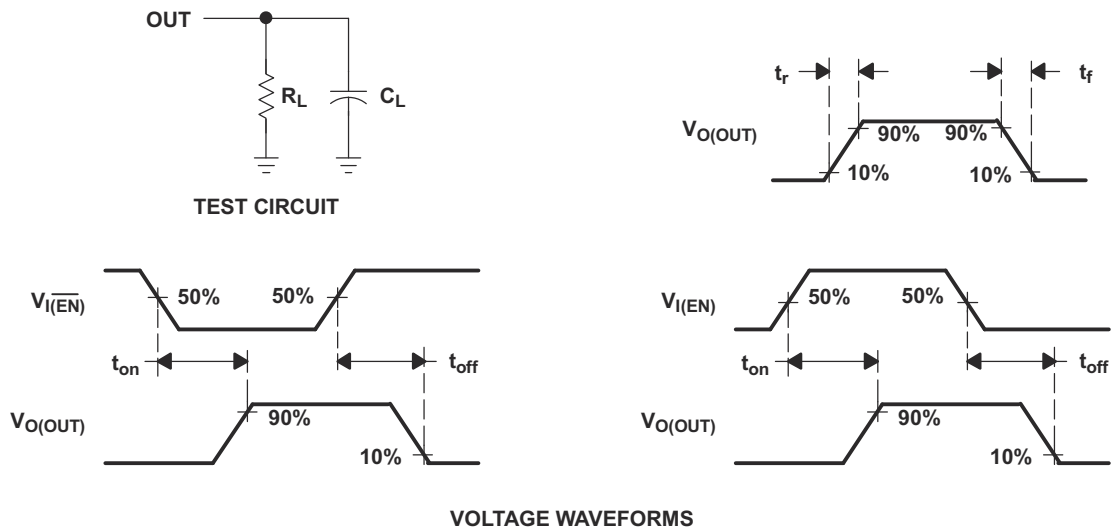


**Figure 7-46. 3-Ω Load Connected to Enabled Device**



**Figure 7-47. 2-Ω Load Connected to Enabled Device**

### 8 Parameter Measurement Information



**Figure 8-1. Test Circuit and Voltage Waveforms**

## 9 Detailed Description

### 9.1 Overview

The TPS20xxB are current-limited, power-distribution switches providing 0.5-A continuous load current. These devices incorporate 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Gate driver is provided by an internal charge pump designed to minimize current surges during switching. The charge pump requires no external components and allows operation supplies as low as 2.7 V.

### 9.2 Functional Block Diagrams



Note A: Current sense

Note B: Active low ( $\overline{\text{EN}}$ ) for TPS2041B; Active high (EN) for TPS2051B

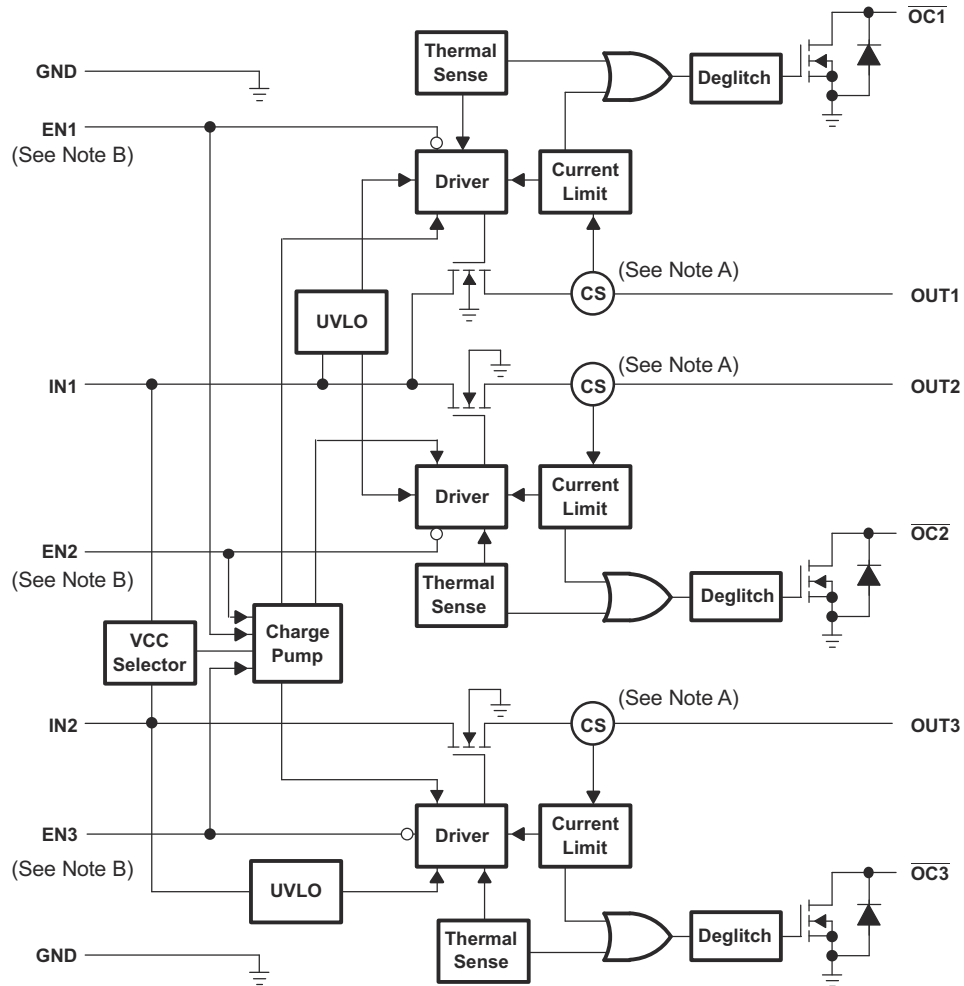
**Figure 9-1. Functional Block Diagram (TPS2041B and TPS2051B)**



Note A: Current sense

Note B: Active low ( $\overline{ENx}$ ) for TPS2042B; Active high (ENx) for TPS2052B

**Figure 9-2. Functional Block Diagram (TPS2042B and TPS2052B)**



Note A: Current sense

Note B: Active low ( $\overline{ENx}$ ) for TPS2043B; Active high (ENx) for TPS2053B

**Figure 9-3. Functional Block Diagram (TPS2043B and TPS2053B)**



Note A: Current sense  
 Note B: Active low ( $\overline{ENx}$ ) for TPS2044B; Active high ( $ENx$ ) for TPS2054B

**Figure 9-4. Functional Block Diagram (TPS2044B and TPS2054B)**

## 9.3 Feature Description

### 9.3.1 Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 500 mA.

### 9.3.2 Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

### 9.3.3 Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

### 9.3.4 Enable ( $\overline{\text{ENx}}$ )

The logic enable pin disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1  $\mu\text{A}$  or 2  $\mu\text{A}$  when a logic high is present on  $\overline{\text{EN}}$ . A logic zero input on  $\overline{\text{EN}}$  restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

### 9.3.5 Enable ( $\text{ENx}$ )

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1  $\mu\text{A}$  or 2  $\mu\text{A}$  when a logic low is present on  $\text{ENx}$ . A logic high input on  $\text{ENx}$  restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

### 9.3.6 Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

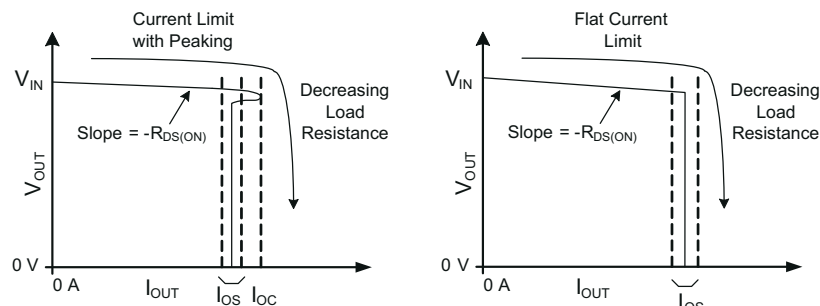
### 9.3.7 Overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

There are two kinds of current limit profiles for the TPS20xxB family of devices.

All devices (excluding TPS2051BDBV and TPS2051BD) have an output I vs V characteristic similar to the plot labeled **Current Limit with Peaking** in Figure 9-5. This type of limiting can be characterized by two parameters, the overcurrent trip threshold ( $I_{OC}$ ), and the short-circuit output current threshold ( $I_{OS}$ ).

Devices TPS2051BDBV and TPS2052BD have an output I vs V characteristic similar to the plot labeled **Flat Current Limit** in Figure 9-5. This type of limiting can be characterized by one parameters, the short circuit current ( $I_{OS}$ ).



**Figure 9-5. Current Limit Profiles**

### 9.3.7.1 Overcurrent Conditions (All Devices Excluding TPS2051BDBV, TPS2052BD)

Three possible overload conditions can occur for all devices exclude TPS2051BDBV, TPS2052BD. In the first condition, the output has been shorted before the device is enabled or before  $V_{I(IN)}$  has been applied (see [Figure 7-23](#) through [Figure 7-26](#)). The TPS20xxB senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold ( $I_{OC}$ )), the device switches into constant-current mode and current is limited at the short-circuit output current threshold ( $I_{OS}$ ).

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the overcurrent trip threshold ( $I_{OC}$ ) is reached or until the thermal limit of the device is exceeded. The TPS20xxB is capable of delivering current up to the current-limit threshold without damaging the device. Once the overcurrent trip threshold ( $I_{OC}$ ) has been reached, the device switches into its constant-current mode current is limited at the short-circuit output current threshold ( $I_{OS}$ ).

### 9.3.7.2 Overcurrent Conditions (TPS2051BDBV, TPS2052BD)

Three possible overload conditions can occur for TPS2051BDBV, TPS2052BD. In the first condition, the output has been shorted before the device is enabled or before  $V_{I(IN)}$  has been applied (see [Figure 7-44](#) through [Figure 7-47](#)). The TPS20xxB senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the short-circuit output current threshold ( $I_{OS}$ ) is reached, the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. After the short-circuit output current threshold ( $I_{OS}$ ) is reached, the device switches into constant-current mode.

### 9.3.8 Overcurrent ( $\overline{OCx}$ )

The  $\overline{OCx}$  open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the  $\overline{OCx}$  signal from oscillation or false triggering. If an overtemperature shutdown occurs, the  $\overline{OCx}$  is asserted instantaneously.

### 9.3.9 Thermal Sense

The TPS20xxB implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ( $\overline{OCx}$ ) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

### 9.3.10 Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

## 9.4 Device Functional Modes

There are no other functional modes for TPS20xxB devices.

## 10 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 10.1 Application Information

#### 10.1.1 Universal Serial Bus (USB) Applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (for example, keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts and self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS20xxB can provide power-distribution solutions to many of these classes of devices.

### 10.2 Typical Application

#### 10.2.1 Typical Application (TPS2042B)

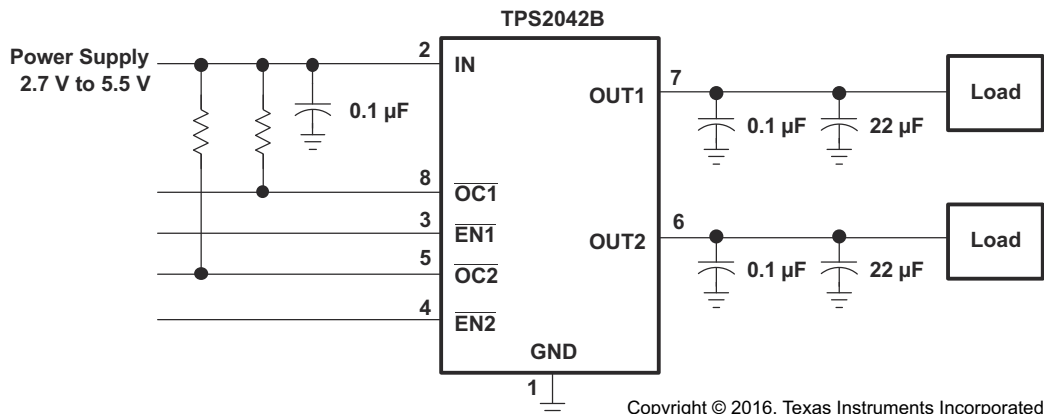


Figure 10-1. Typical Application (Example, TPS2042B)

##### 10.2.1.1 Design Requirements

Table 10-1 shows the design parameters for this application.

Table 10-1. Design Parameters

| DESIGN PARAMETER | VALUE |
|------------------|-------|
| Input voltage    | 5 V   |

**Table 10-1. Design Parameters (continued)**

| DESIGN PARAMETER | VALUE |
|------------------|-------|
| Output1 voltage  | 5 V   |
| Output2 voltage  | 5 V   |
| Output1 current  | 0.5 A |
| Output2 current  | 0.5 A |

### 10.2.1.2 Detailed Design Procedure

#### 10.2.1.2.1 Power-Supply Considerations

TI recommends placing a 0.01- $\mu$ F to 0.1- $\mu$ F ceramic bypass capacitor between IN and GND, close to the device. When the output load is heavy, TI recommends placing a high-value electrolytic capacitor on the necessary output pins. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01- $\mu$ F to 0.1- $\mu$ F ceramic capacitor improves the immunity of the device to short-circuit transients.

#### 10.2.1.2.2 $\overline{OC}$ Response

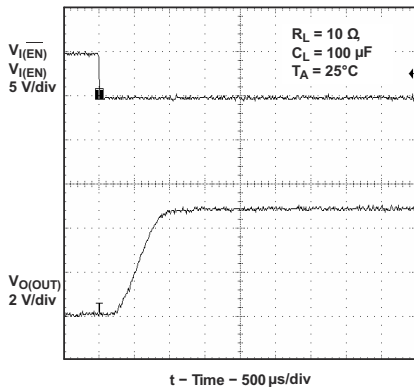
The  $\overline{OCx}$  open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on  $\overline{OCx}$  occurs due to the 10-ms deglitch circuit. The TPS20xxB is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses.  $\overline{OCx}$  is not deglitched when the switch is turned off due to an overtemperature shutdown.



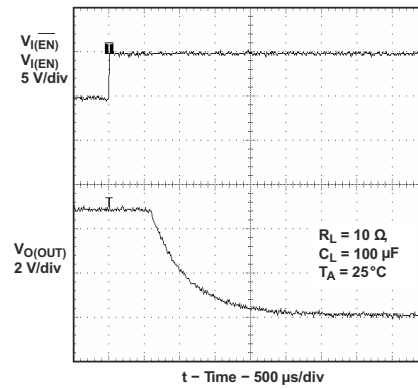
**Figure 10-2. Typical Circuit for the  $\overline{OC}$  Pin (Example, TPS2042B)**

### 10.2.1.3 Application Curves

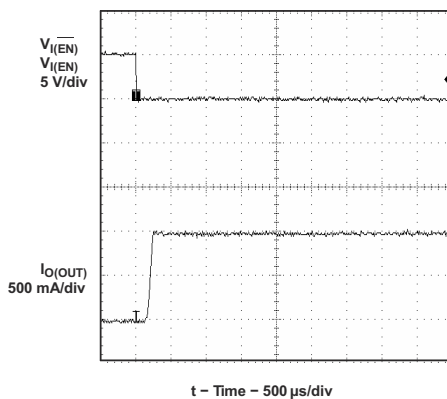




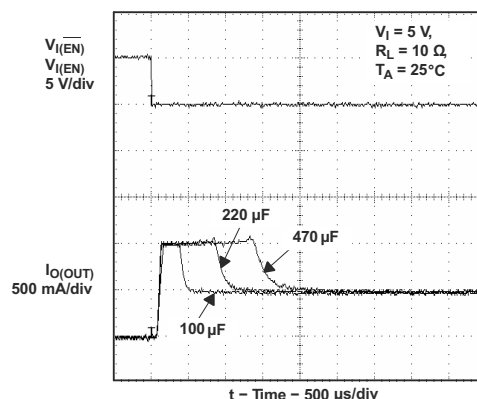
**Figure 10-5. Turnon Delay and Rise Time With 100- $\mu$ F Load**



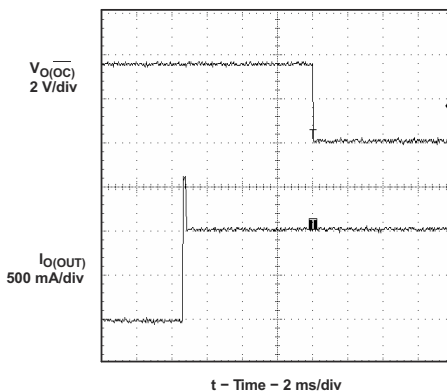
**Figure 10-6. Turnoff Delay and Fall Time With 100- $\mu$ F Load**



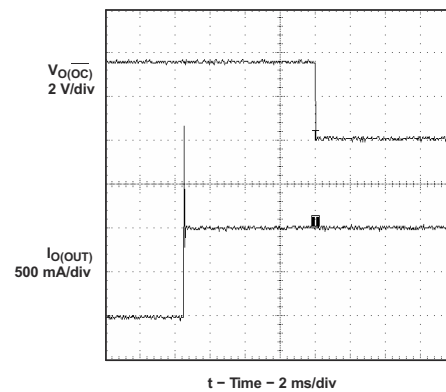
**Figure 10-7. Short-Circuit Current, Device Enabled Into Short**



**Figure 10-8. Inrush Current With Different Load Capacitance**



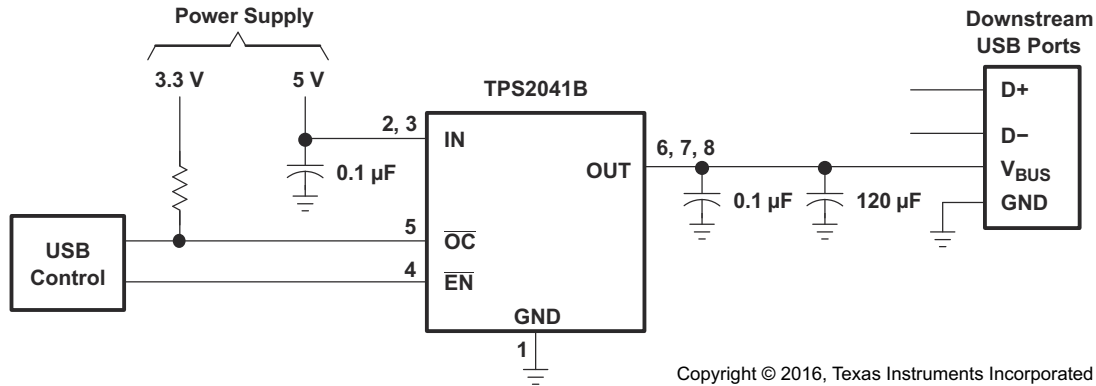
**Figure 10-9. 3- $\Omega$  Load Connected to Enabled Device**



**Figure 10-10. 2- $\Omega$  Load Connected to Enabled Device**

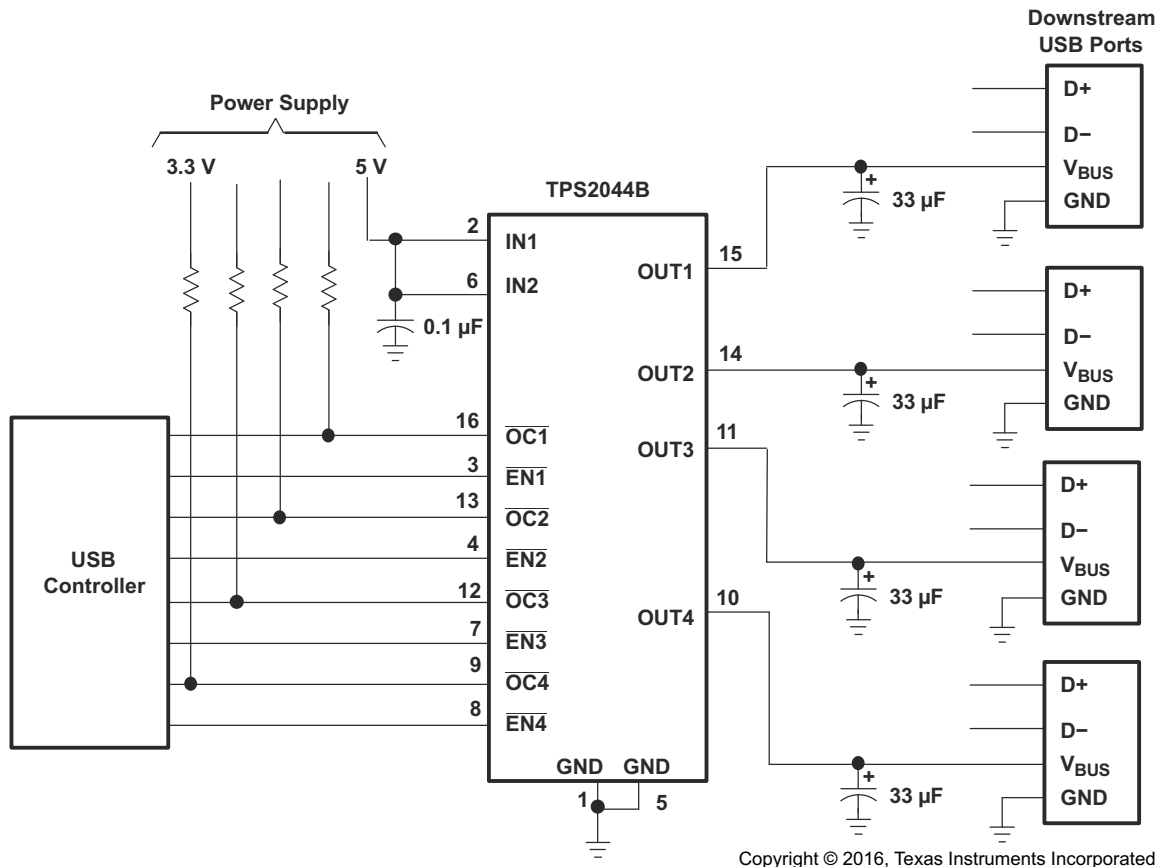
## 10.2.2 Host and Self-Powered and Bus-Powered Hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see [Figure 10-11](#) and [Figure 10-12](#)). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.



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**Figure 10-11. Typical One-Port USB Host and Self-Powered Hub**



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**Figure 10-12. Typical Four-Port USB Host and Self-Powered Hub**

### 10.2.2.1 Design Requirements

#### 10.2.2.1.1 USB Power-Distribution Requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts and self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB  $V_{BUS}$
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA

- Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

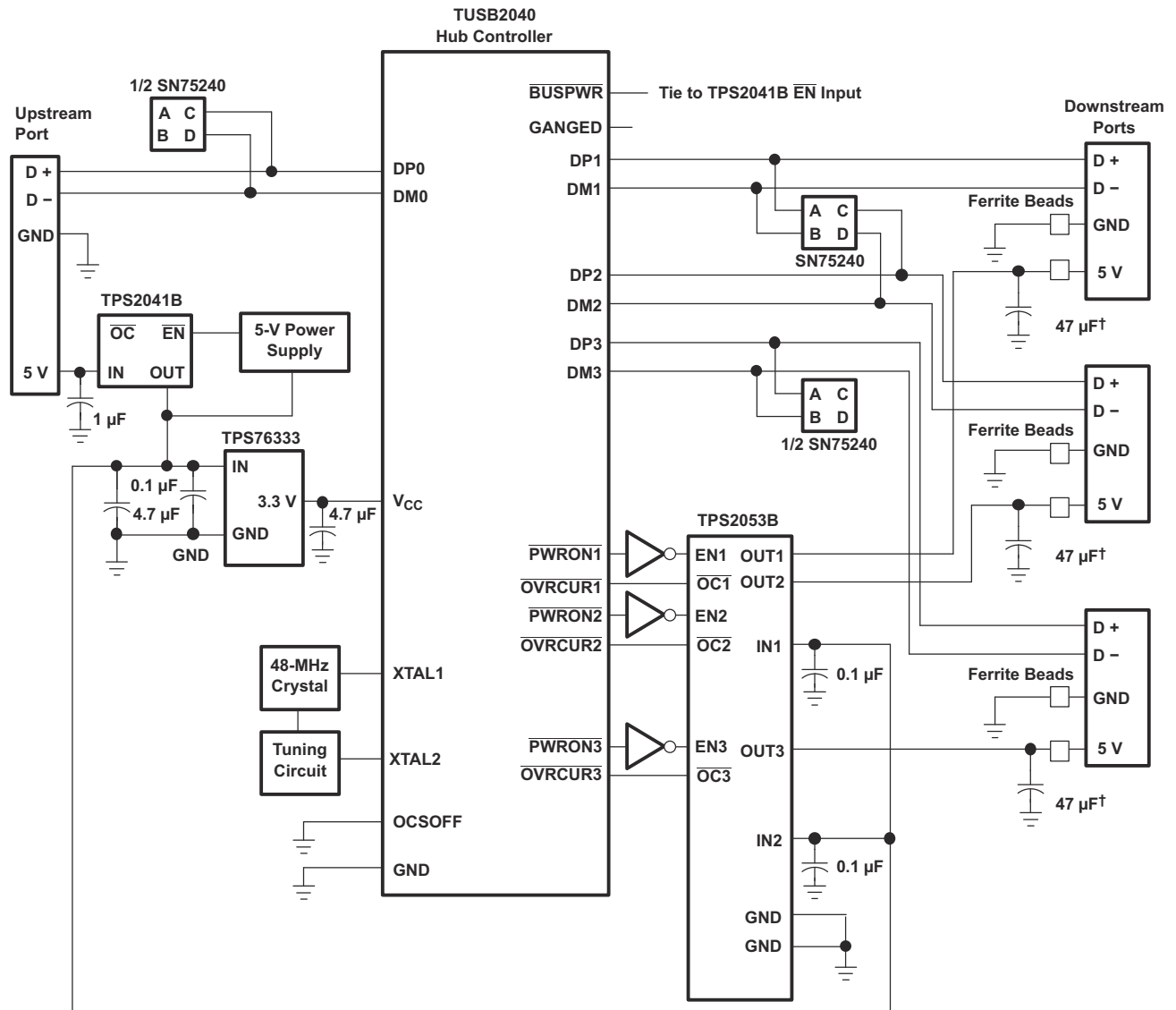
The feature set of the TPS20xxB allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see Figure 10-13 through Figure 10-16).



† USB rev 1.1 requires 120 μF per hub.

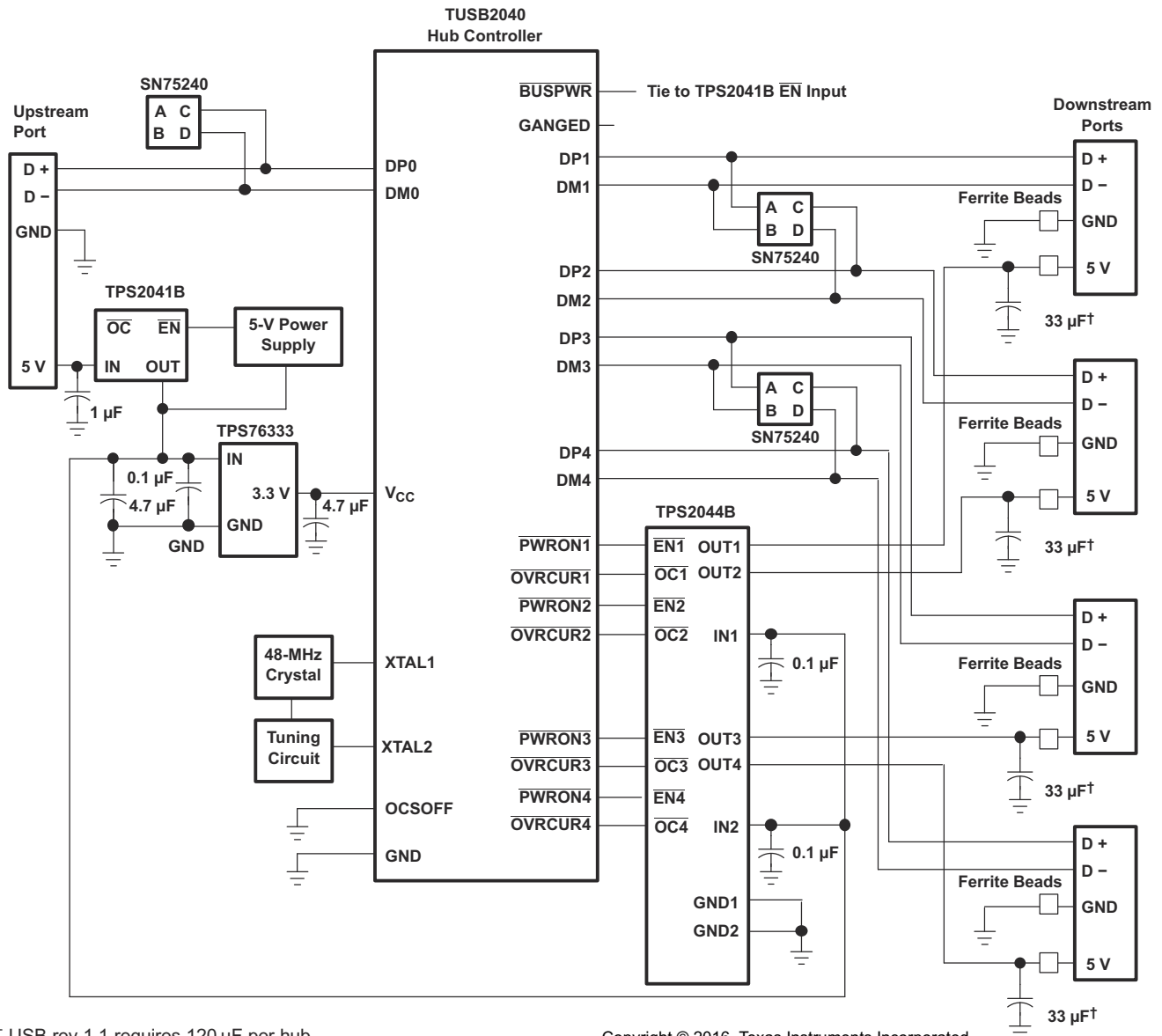
**Figure 10-13. Hybrid Self and Bus-Powered Hub Implementation, TPS2041B and TPS2051B**





† USB rev 1.1 requires 120 μF per hub.

**Figure 10-15. Hybrid Self and Bus-Powered Hub Implementation, TPS2043B and TPS2053B**



† USB rev 1.1 requires 120 µF per hub.

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**Figure 10-16. Hybrid Self and Bus-Powered Hub Implementation, TPS2044B and TPS2054B**

### 10.2.2.2 Detailed Design Procedure

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

#### 10.2.2.2.1 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 10-17).



Figure 10-17. High-Power Bus-Powered Function (Example, TPS2042B)

### 10.2.2.3 Application Curves



Figure 10-18. Turnon Delay and Rise Time With 1- $\mu$ F Load

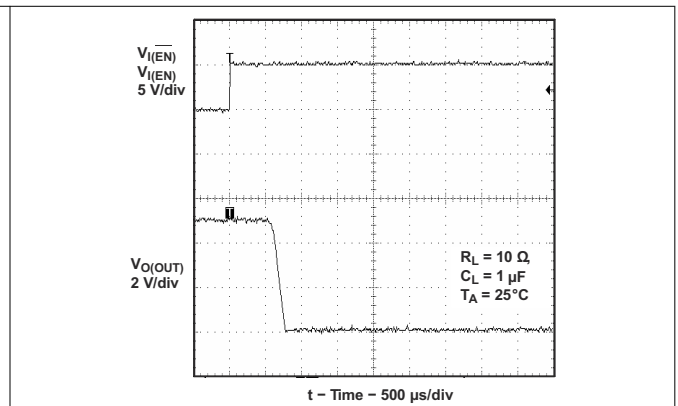


Figure 10-19. Turnoff Delay and Fall Time with 1- $\mu$ F Load



Figure 10-20. Turnon Delay and Rise Time With 100- $\mu$ F Load

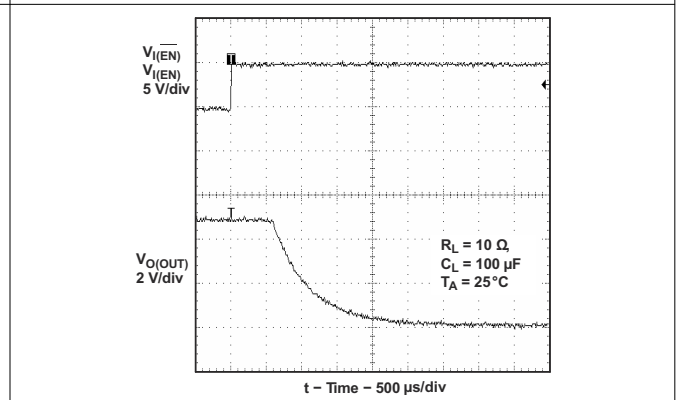
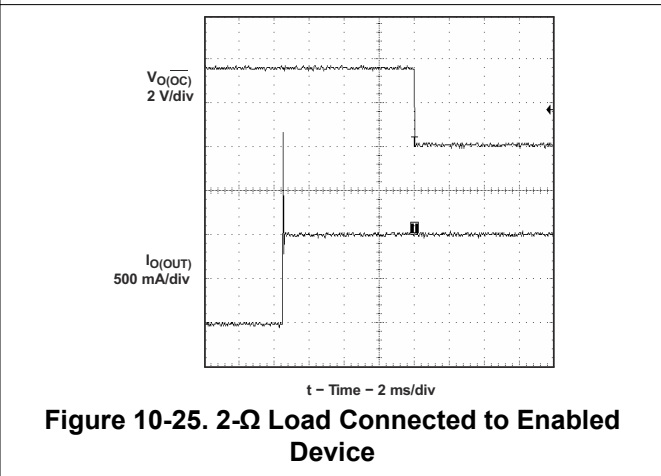
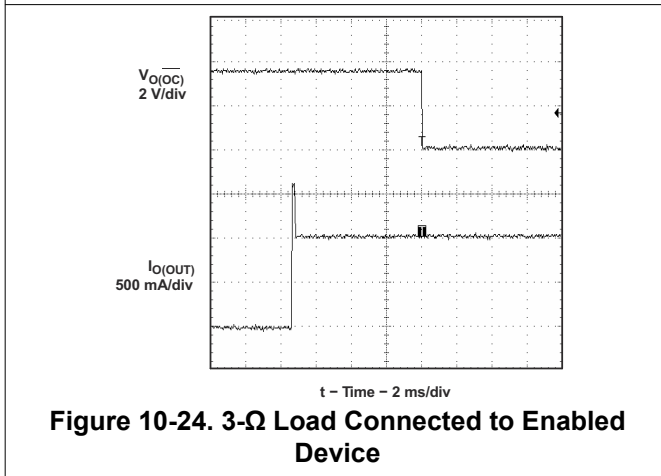
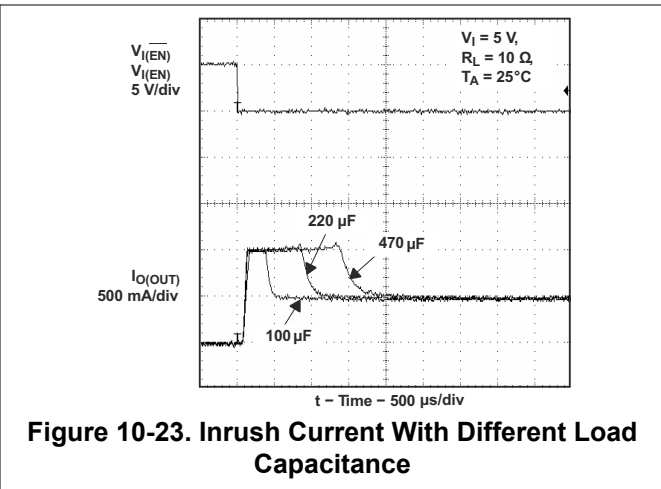
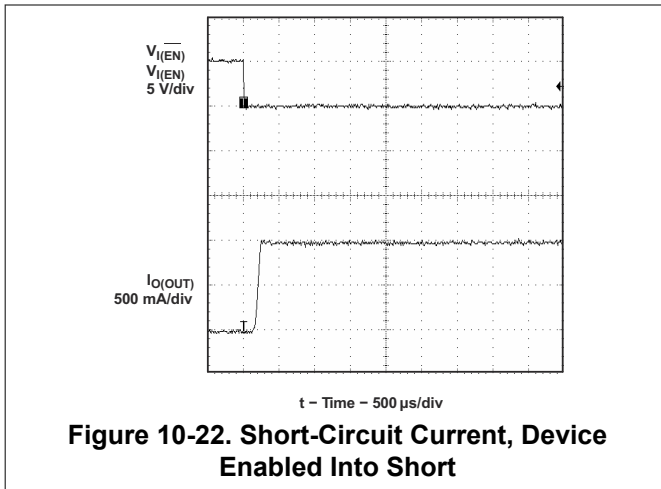


Figure 10-21. Turnoff Delay and Fall Time With 100- $\mu$ F Load



### 10.2.3 Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS20xxB, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS20xxB also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.



**Figure 10-26. Typical Hot-Plug Implementation (Example, TPS2042B)**

By placing the TPS20xxB between the  $V_{CC}$  input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

### 10.2.3.1 Design Requirements

Table 10-2 shows the design parameters for this application.

**Table 10-2. Design Parameters**

| DESIGN PARAMETER | VALUE |
|------------------|-------|
| Input voltage    | 5 V   |
| Output1 voltage  | 5 V   |
| Output2 voltage  | 5 V   |
| Output1 current  | 0.5 A |
| Output2 current  | 0.5 A |

### 10.2.3.2 Detailed Design Procedure

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

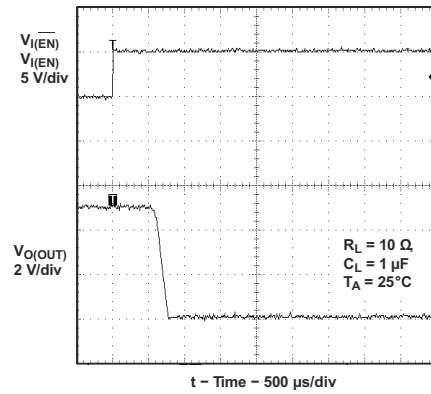
- Normal Input Operation Voltage
- Current Limit

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, TI recommends a 0.1-µF or greater ceramic bypass capacitor between IN and GND, as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage undershoot from exceeding the UVLO of other load share one power rail with TPS2042 device or overshoot from exceeding the absolute-maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply. Output capacitance is not required, but TI recommends placing a high-value electrolytic capacitor on the output pin when large transient currents are expected on the output to reduce the undershoot, which is caused by the inductance of the output power bus just after a short has occurred and the TPS2042 device has abruptly reduced OUT current. Energy stored in the inductance will drive the OUT voltage down and potentially negative as it discharges.

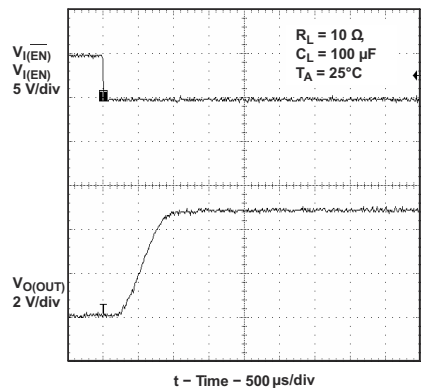
### 10.2.3.3 Application Curves



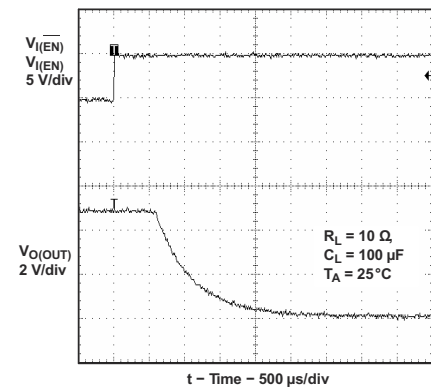
**Figure 10-27. Turnon Delay and Rise Time With 1- $\mu$ F Load**



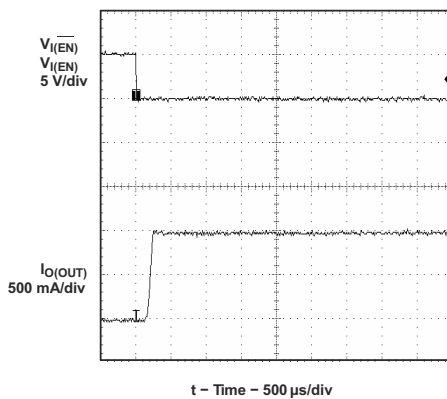
**Figure 10-28. Turnoff Delay and Fall Time With 1- $\mu$ F Load**



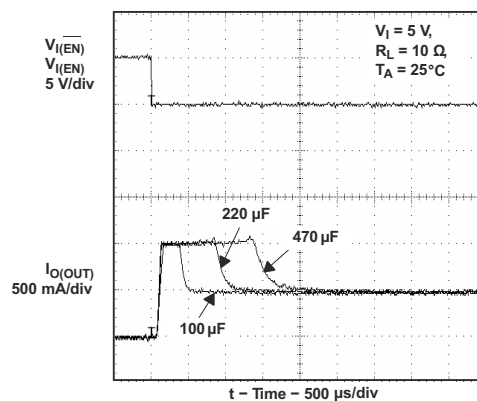
**Figure 10-29. Turnon Delay and Rise Time With 100- $\mu$ F Load**



**Figure 10-30. Turnoff Delay and Fall Time With 100- $\mu$ F Load**



**Figure 10-31. Short-Circuit Current, Device Enabled Into Short**



**Figure 10-32. Inrush Current With Different Load Capacitance**



**Figure 10-33. 3- $\Omega$  Load Connected to Enabled Device**



**Figure 10-34. 2- $\Omega$  Load Connected to Enabled Device**

## 11 Power Supply Recommendations

### 11.1 Undervoltage Lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

## 12 Layout

### 12.1 Layout Guidelines

- Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace.
- Placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin is recommended when large transient currents are expected on the output.
- The PowerPAD should be directly connected to PCB ground plane using wide and short copper trace.

### 12.2 Layout Example



**Figure 12-1. Layout Recommendation**

### 12.3 Power Dissipation

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the  $r_{DS(on)}$  of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read  $r_{DS(on)}$  from [Figure 7-13](#). Using this value, the power dissipation per switch can be calculated by [Equation](#) :

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature with [Equation](#) :

$$T_J = P_D \times R_{\theta JA} + T_A$$

where

- $T_A$  = Ambient temperature °C
- $R_{\theta JA}$  = Thermal resistance
- $P_D$  = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

### 12.4 Thermal Protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS20xxB implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature

rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The  $\overline{OCx}$  open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

## 13 Device and Documentation Support

### 13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 13-1. Related Links**

| PARTS   | PRODUCT FOLDER             | ORDER NOW                  | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TPS2041 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS2042 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS2043 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS2044 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS2051 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS2052 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS2053 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TPS2054 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 13.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
 All trademarks are the property of their respective owners.

### 13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS2041BD        | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2041B                   | <a href="#">Samples</a> |
| TPS2041BDBVR     | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | PLII                    | <a href="#">Samples</a> |
| TPS2041BDBVRG4   | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | PLII                    | <a href="#">Samples</a> |
| TPS2041BDBVT     | ACTIVE        | SOT-23       | DBV             | 5    | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | PLII                    | <a href="#">Samples</a> |
| TPS2041BDBVTG4   | ACTIVE        | SOT-23       | DBV             | 5    | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | PLII                    | <a href="#">Samples</a> |
| TPS2041BDG4      | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2041B                   | <a href="#">Samples</a> |
| TPS2041BDGN      | ACTIVE        | HVSSOP       | DGN             | 8    | 80          | RoHS & Green    | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM   | -40 to 125   | 2041B                   | <a href="#">Samples</a> |
| TPS2041BDGNG4    | ACTIVE        | HVSSOP       | DGN             | 8    | 80          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2041B                   | <a href="#">Samples</a> |
| TPS2041BDGNR     | ACTIVE        | HVSSOP       | DGN             | 8    | 2500        | RoHS & Green    | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM   | -40 to 125   | 2041B                   | <a href="#">Samples</a> |
| TPS2041BDR       | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2041B                   | <a href="#">Samples</a> |
| TPS2041BDRG4     | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2041B                   | <a href="#">Samples</a> |
| TPS2042BD        | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2042B                   | <a href="#">Samples</a> |
| TPS2042BDGN      | ACTIVE        | HVSSOP       | DGN             | 8    | 80          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2042B                   | <a href="#">Samples</a> |
| TPS2042BDGNG4    | ACTIVE        | HVSSOP       | DGN             | 8    | 80          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2042B                   | <a href="#">Samples</a> |
| TPS2042BDGNR     | ACTIVE        | HVSSOP       | DGN             | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2042B                   | <a href="#">Samples</a> |
| TPS2042BDGNRG4   | ACTIVE        | HVSSOP       | DGN             | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2042B                   | <a href="#">Samples</a> |
| TPS2042BDR       | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2042B                   | <a href="#">Samples</a> |
| TPS2042BDRBR     | ACTIVE        | SON          | DRB             | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2042                    | <a href="#">Samples</a> |
| TPS2042BDRBT     | ACTIVE        | SON          | DRB             | 8    | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2042                    | <a href="#">Samples</a> |
| TPS2042BDRG4     | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2042B                   | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS2043BD        | ACTIVE        | SOIC         | D               | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2043B                   | <a href="#">Samples</a> |
| TPS2043BDR       | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2043B                   | <a href="#">Samples</a> |
| TPS2043BDRG4     | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2043B                   | <a href="#">Samples</a> |
| TPS2044BD        | ACTIVE        | SOIC         | D               | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2044B                   | <a href="#">Samples</a> |
| TPS2044BDG4      | ACTIVE        | SOIC         | D               | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2044B                   | <a href="#">Samples</a> |
| TPS2044BDR       | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2044B                   | <a href="#">Samples</a> |
| TPS2044BDRG4     | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2044B                   | <a href="#">Samples</a> |
| TPS2051BD        | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2051B                   | <a href="#">Samples</a> |
| TPS2051BDBVR     | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | PLJI                    | <a href="#">Samples</a> |
| TPS2051BDG4      | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2051B                   | <a href="#">Samples</a> |
| TPS2051BDGN      | ACTIVE        | HVSSOP       | DGN             | 8    | 80          | RoHS & Green    | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM   | -40 to 125   | 2051B                   | <a href="#">Samples</a> |
| TPS2051BDGNG4    | ACTIVE        | HVSSOP       | DGN             | 8    | 80          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2051B                   | <a href="#">Samples</a> |
| TPS2051BDGNR     | ACTIVE        | HVSSOP       | DGN             | 8    | 2500        | RoHS & Green    | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM   | -40 to 125   | 2051B                   | <a href="#">Samples</a> |
| TPS2051BDGNRG4   | ACTIVE        | HVSSOP       | DGN             | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2051B                   | <a href="#">Samples</a> |
| TPS2051BDR       | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2051B                   | <a href="#">Samples</a> |
| TPS2051BDRG4     | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2051B                   | <a href="#">Samples</a> |
| TPS2052BDGN      | ACTIVE        | HVSSOP       | DGN             | 8    | 80          | RoHS & Green    | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM   | -40 to 125   | 2052B                   | <a href="#">Samples</a> |
| TPS2052BDGNG4    | ACTIVE        | HVSSOP       | DGN             | 8    | 80          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2052B                   | <a href="#">Samples</a> |
| TPS2052BDGNR     | ACTIVE        | HVSSOP       | DGN             | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2052B                   | <a href="#">Samples</a> |
| TPS2052BDGNRG4   | ACTIVE        | HVSSOP       | DGN             | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2052B                   | <a href="#">Samples</a> |
| TPS2052BDR       | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2052B                   | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS2052BDRBR     | ACTIVE        | SON          | DRB             | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2052                    | <a href="#">Samples</a> |
| TPS2052BDRBT     | ACTIVE        | SON          | DRB             | 8    | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 2052                    | <a href="#">Samples</a> |
| TPS2053BD        | ACTIVE        | SOIC         | D               | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2053B                   | <a href="#">Samples</a> |
| TPS2053BDR       | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2053B                   | <a href="#">Samples</a> |
| TPS2054BD        | ACTIVE        | SOIC         | D               | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2054B                   | <a href="#">Samples</a> |
| TPS2054BDR       | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | 2054B                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS2041B, TPS2042B, TPS2051B :**

- Automotive : [TPS2041B-Q1](#), [TPS2042B-Q1](#), [TPS2051B-Q1](#)
- Enhanced Product : [TPS2041B-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS2041BDBVR | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| TPS2041BDBVR | SOT-23       | DBV             | 5    | 3000 | 179.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TPS2041BDBVT | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| TPS2041BDBVT | SOT-23       | DBV             | 5    | 250  | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TPS2041BDGNR | HVSSOP       | DGN             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.3     | 1.3     | 8.0     | 12.0   | Q1            |
| TPS2041BDGNR | HVSSOP       | DGN             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TPS2041BDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TPS2042BDGNR | HVSSOP       | DGN             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.3     | 1.3     | 8.0     | 12.0   | Q1            |
| TPS2042BDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TPS2042BDRBR | SON          | DRB             | 8    | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| TPS2042BDRBT | SON          | DRB             | 8    | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| TPS2043BDR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| TPS2044BDR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| TPS2051BDBVR | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| TPS2051BDGNR | HVSSOP       | DGN             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TPS2051BDGNR | HVSSOP       | DGN             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.3     | 1.3     | 8.0     | 12.0   | Q1            |

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS2051BDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TPS2052BDGNR | HVSSOP       | DGN             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.3     | 1.3     | 8.0     | 12.0   | Q1            |
| TPS2052BDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TPS2052BDRBR | SON          | DRB             | 8    | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| TPS2052BDRBT | SON          | DRB             | 8    | 250  | 180.0              | 12.4               | 3.3     | 3.3     | 1.0     | 8.0     | 12.0   | Q2            |
| TPS2053BDR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| TPS2054BDR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS2041BDBVR | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| TPS2041BDBVR | SOT-23       | DBV             | 5    | 3000 | 200.0       | 183.0      | 25.0        |
| TPS2041BDBVT | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| TPS2041BDBVT | SOT-23       | DBV             | 5    | 250  | 200.0       | 183.0      | 25.0        |
| TPS2041BDGNR | HVSSOP       | DGN             | 8    | 2500 | 346.0       | 346.0      | 35.0        |
| TPS2041BDGNR | HVSSOP       | DGN             | 8    | 2500 | 364.0       | 364.0      | 27.0        |
| TPS2041BDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TPS2042BDGNR | HVSSOP       | DGN             | 8    | 2500 | 346.0       | 346.0      | 35.0        |
| TPS2042BDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TPS2042BDRBR | SON          | DRB             | 8    | 3000 | 346.0       | 346.0      | 35.0        |
| TPS2042BDRBT | SON          | DRB             | 8    | 250  | 200.0       | 183.0      | 25.0        |
| TPS2043BDR   | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| TPS2044BDR   | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| TPS2051BDBVR | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| TPS2051BDGNR | HVSSOP       | DGN             | 8    | 2500 | 364.0       | 364.0      | 27.0        |
| TPS2051BDGNR | HVSSOP       | DGN             | 8    | 2500 | 346.0       | 346.0      | 35.0        |
| TPS2051BDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TPS2052BDGNR | HVSSOP       | DGN             | 8    | 2500 | 346.0       | 346.0      | 35.0        |

---

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS2052BDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TPS2052BDRBR | SON          | DRB             | 8    | 3000 | 346.0       | 346.0      | 35.0        |
| TPS2052BDRBT | SON          | DRB             | 8    | 250  | 200.0       | 183.0      | 25.0        |
| TPS2053BDR   | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| TPS2054BDR   | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS2041BD     | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| TPS2041BDG4   | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| TPS2041BDGN   | DGN          | HVSSOP       | 8    | 80  | 330    | 6.55   | 500    | 2.88   |
| TPS2041BDGN   | DGN          | HVSSOP       | 8    | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS2041BDGNG4 | DGN          | HVSSOP       | 8    | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS2041BDGNG4 | DGN          | HVSSOP       | 8    | 80  | 330    | 6.55   | 500    | 2.88   |
| TPS2042BD     | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| TPS2042BDGN   | DGN          | HVSSOP       | 8    | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS2042BDGNG4 | DGN          | HVSSOP       | 8    | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS2043BD     | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |
| TPS2044BD     | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |
| TPS2044BDG4   | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |
| TPS2051BD     | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| TPS2051BDG4   | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| TPS2051BDGN   | DGN          | HVSSOP       | 8    | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS2051BDGN   | DGN          | HVSSOP       | 8    | 80  | 330    | 6.55   | 500    | 2.88   |
| TPS2051BDGNG4 | DGN          | HVSSOP       | 8    | 80  | 330    | 6.55   | 500    | 2.88   |
| TPS2051BDGNG4 | DGN          | HVSSOP       | 8    | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS2052BDGN   | DGN          | HVSSOP       | 8    | 80  | 330    | 6.55   | 500    | 2.88   |
| TPS2052BDGN   | DGN          | HVSSOP       | 8    | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS2052BDGNG4 | DGN          | HVSSOP       | 8    | 80  | 322    | 6.55   | 1000   | 3.01   |
| TPS2052BDGNG4 | DGN          | HVSSOP       | 8    | 80  | 330    | 6.55   | 500    | 2.88   |
| TPS2053BD     | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |
| TPS2054BD     | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |

## GENERIC PACKAGE VIEW

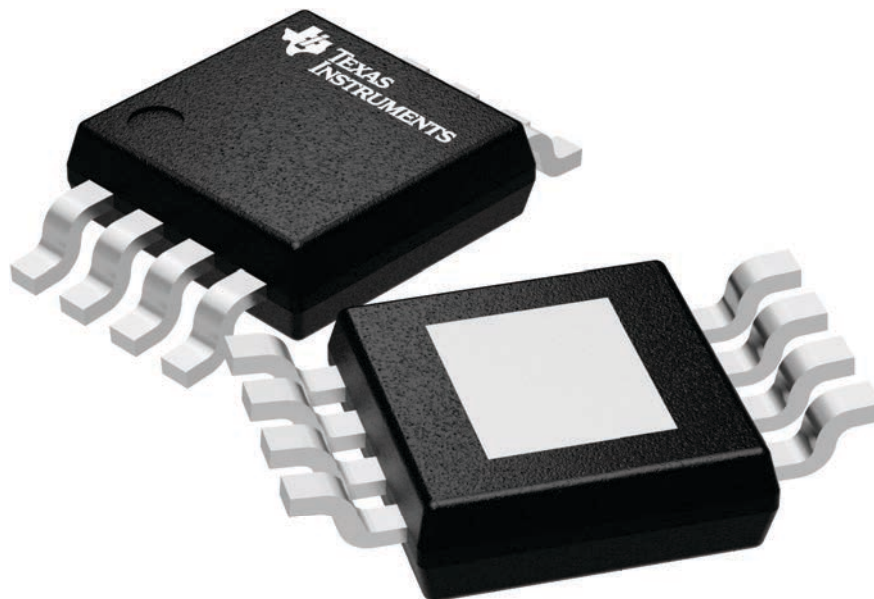
**DGN 8**

**PowerPAD VSSOP - 1.1 mm max height**

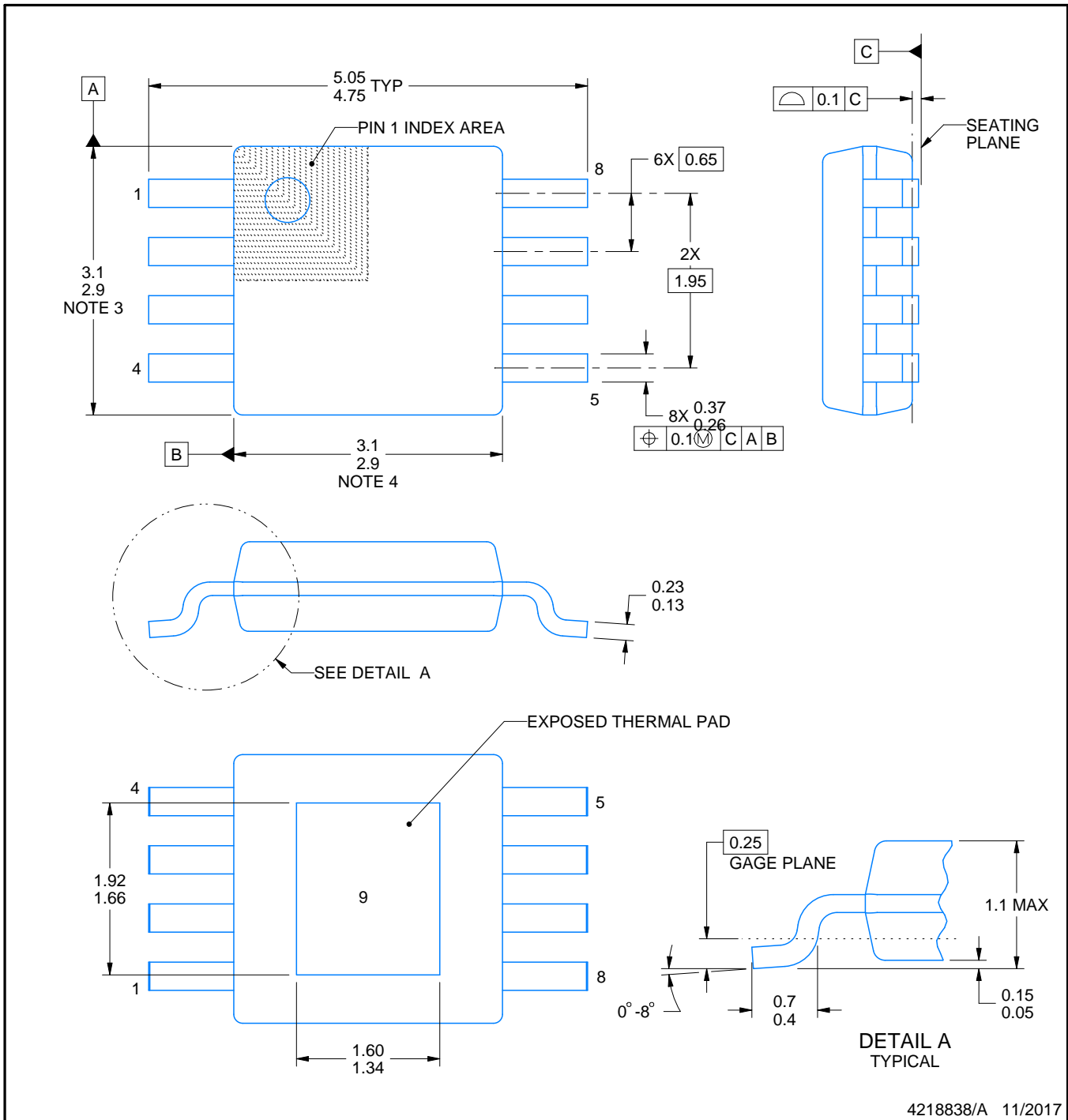
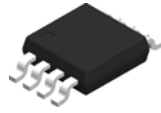
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225482/A



4218838/A 11/2017

NOTES:

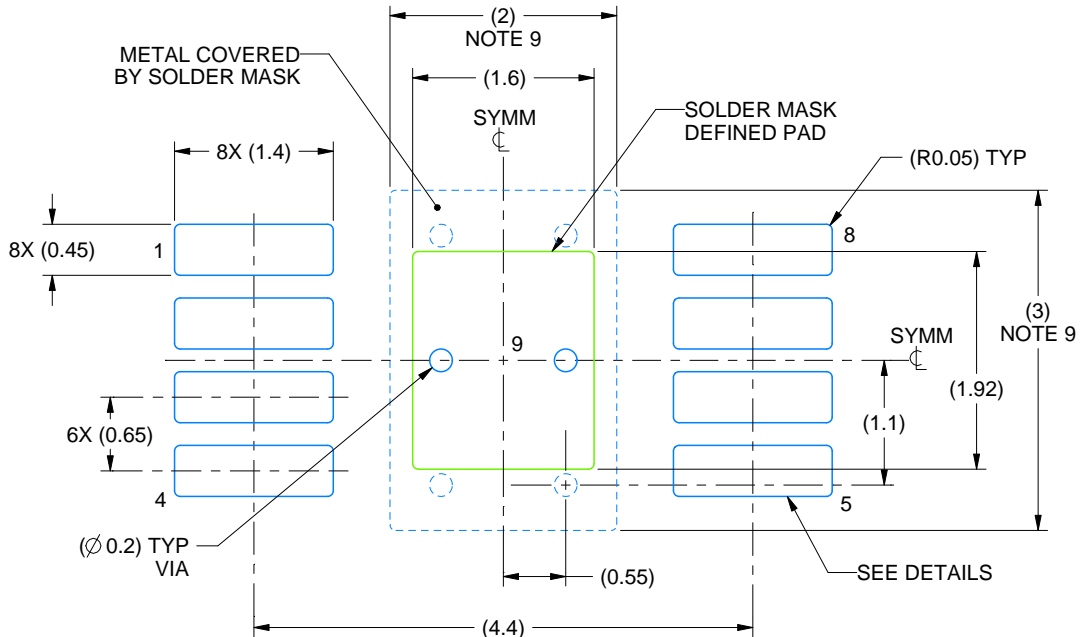
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

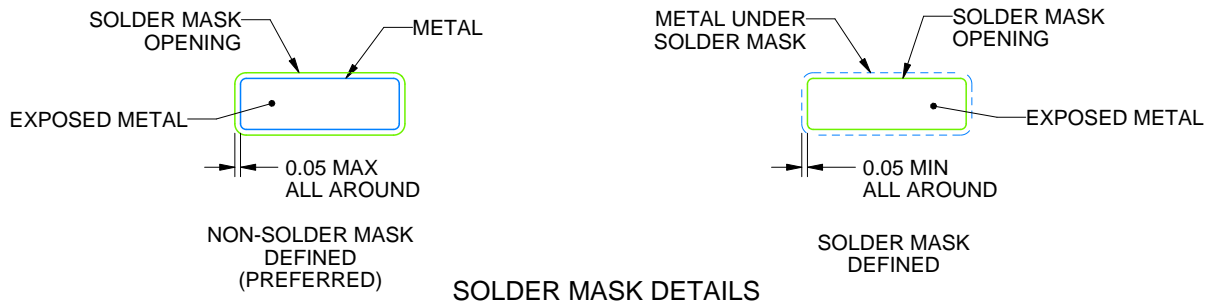
DGN0008C

HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4218838/A 11/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGN0008C

HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



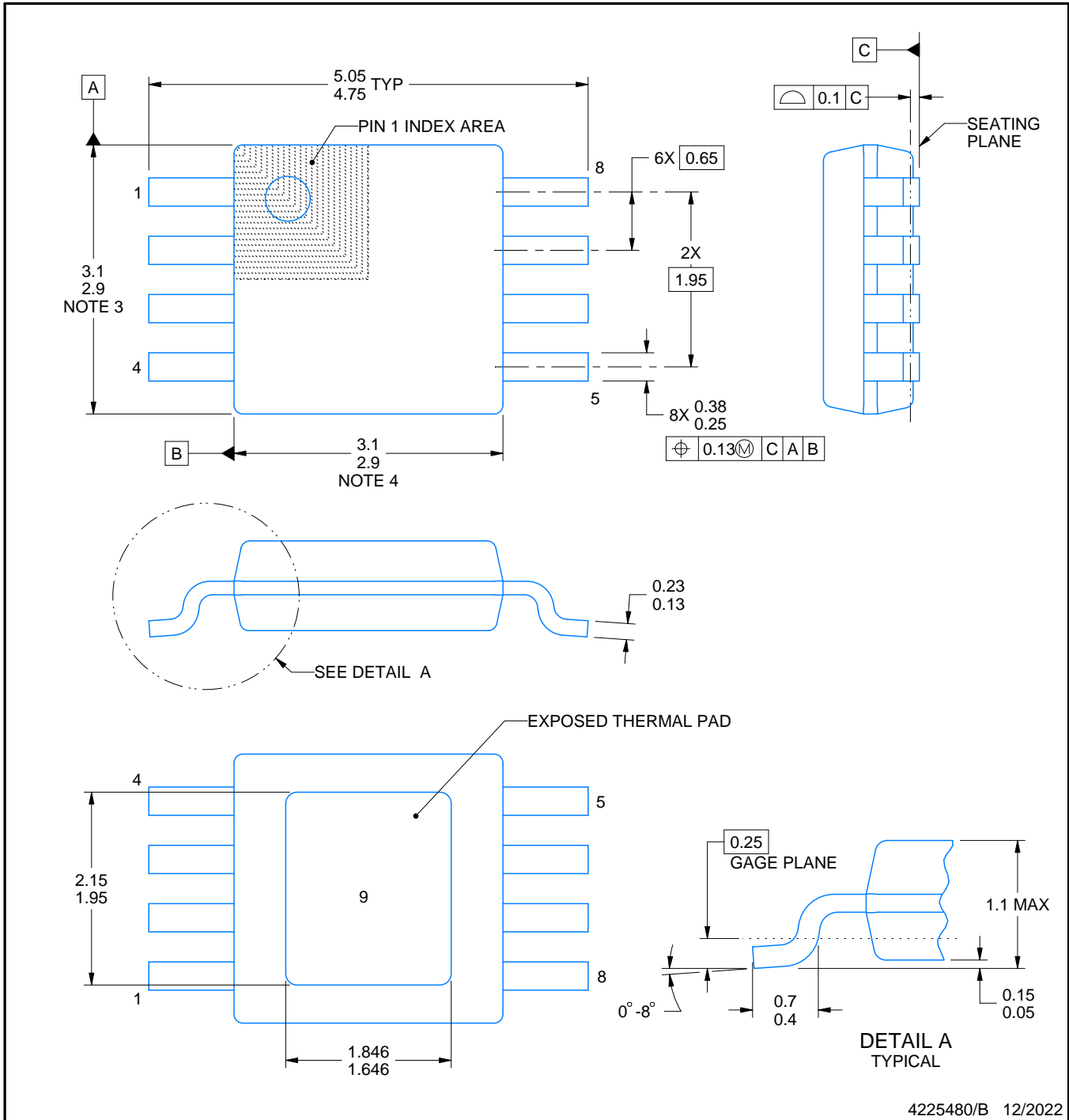
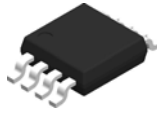
**SOLDER PASTE EXAMPLE**  
 EXPOSED PAD 9:  
 100% PRINTED SOLDER COVERAGE BY AREA  
 SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 1.79 X 2.15            |
| 0.125             | 1.60 X 1.92 (SHOWN)    |
| 0.15              | 1.46 X 1.75            |
| 0.175             | 1.35 X 1.62            |

4218838/A 11/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



4225480/B 12/2022

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

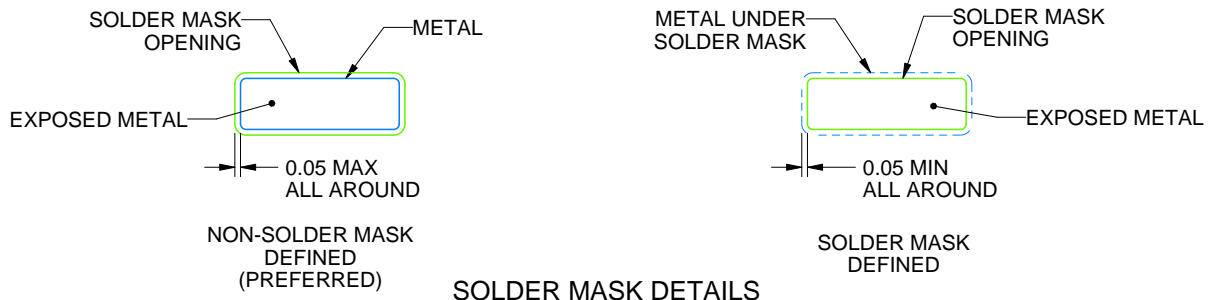
DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

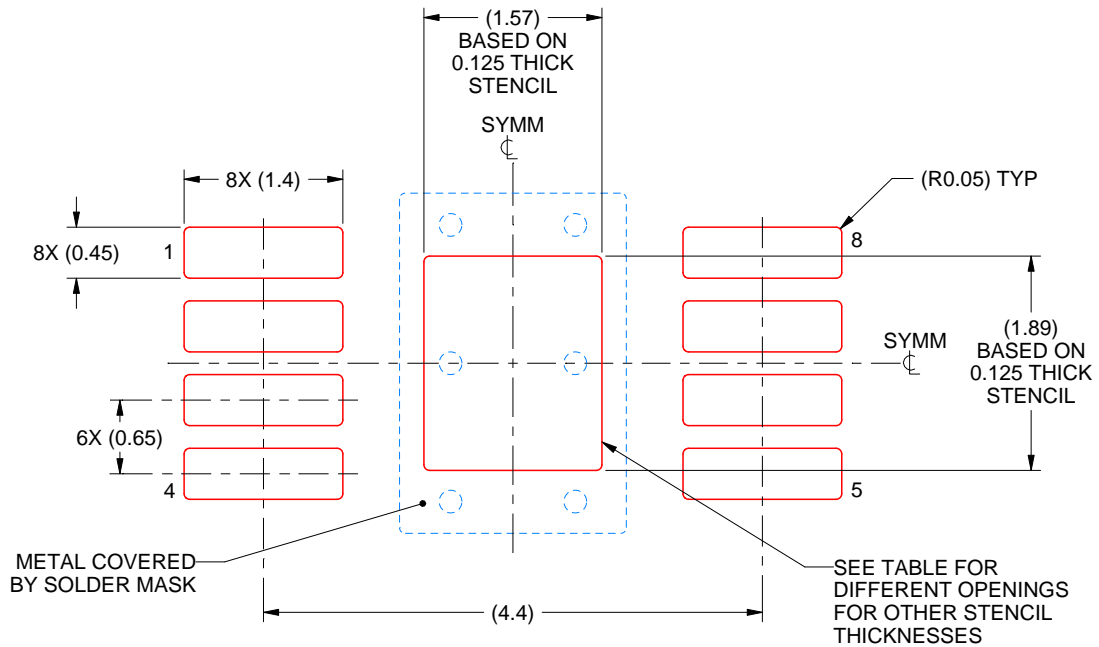
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD 9:  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 1.76 X 2.11            |
| 0.125             | 1.57 X 1.89 (SHOWN)    |
| 0.15              | 1.43 X 1.73            |
| 0.175             | 1.33 X 1.60            |

4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



# EXAMPLE BOARD LAYOUT

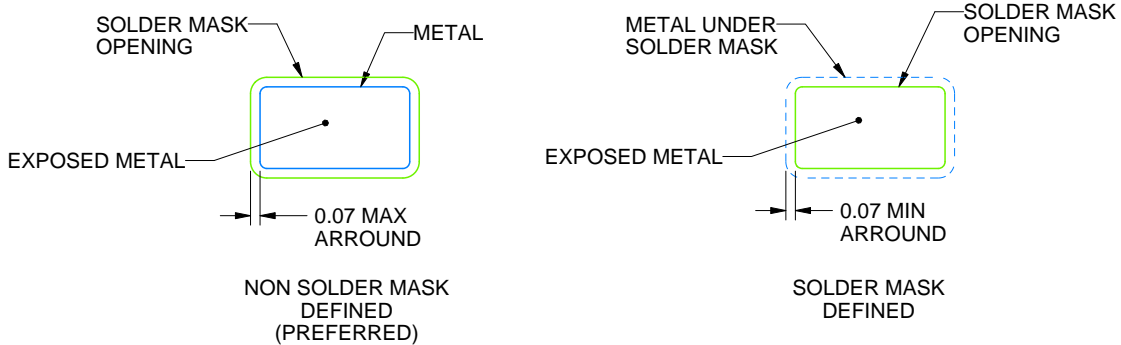
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

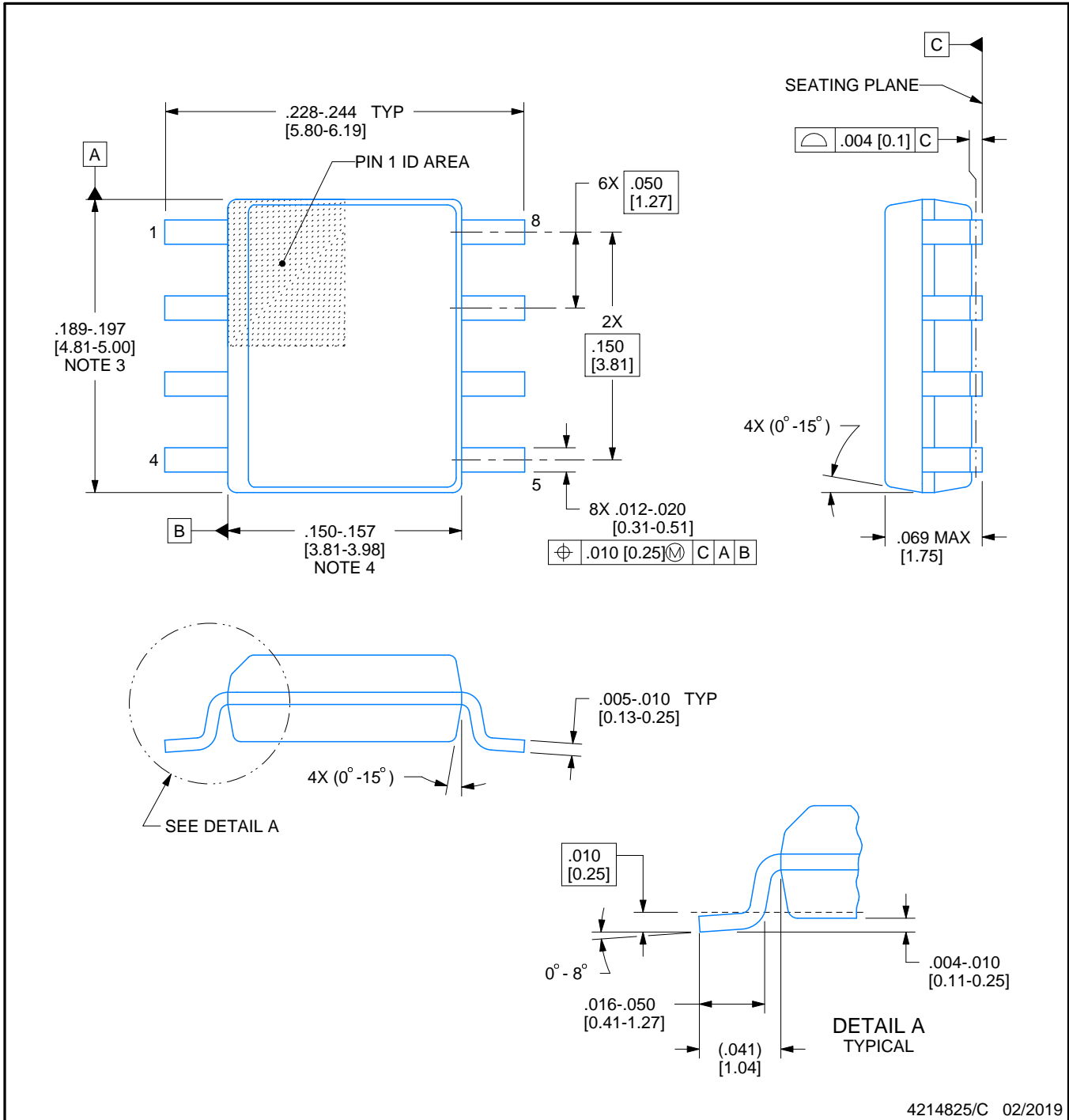


D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**DRB 8**

**GENERIC PACKAGE VIEW**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203482/L

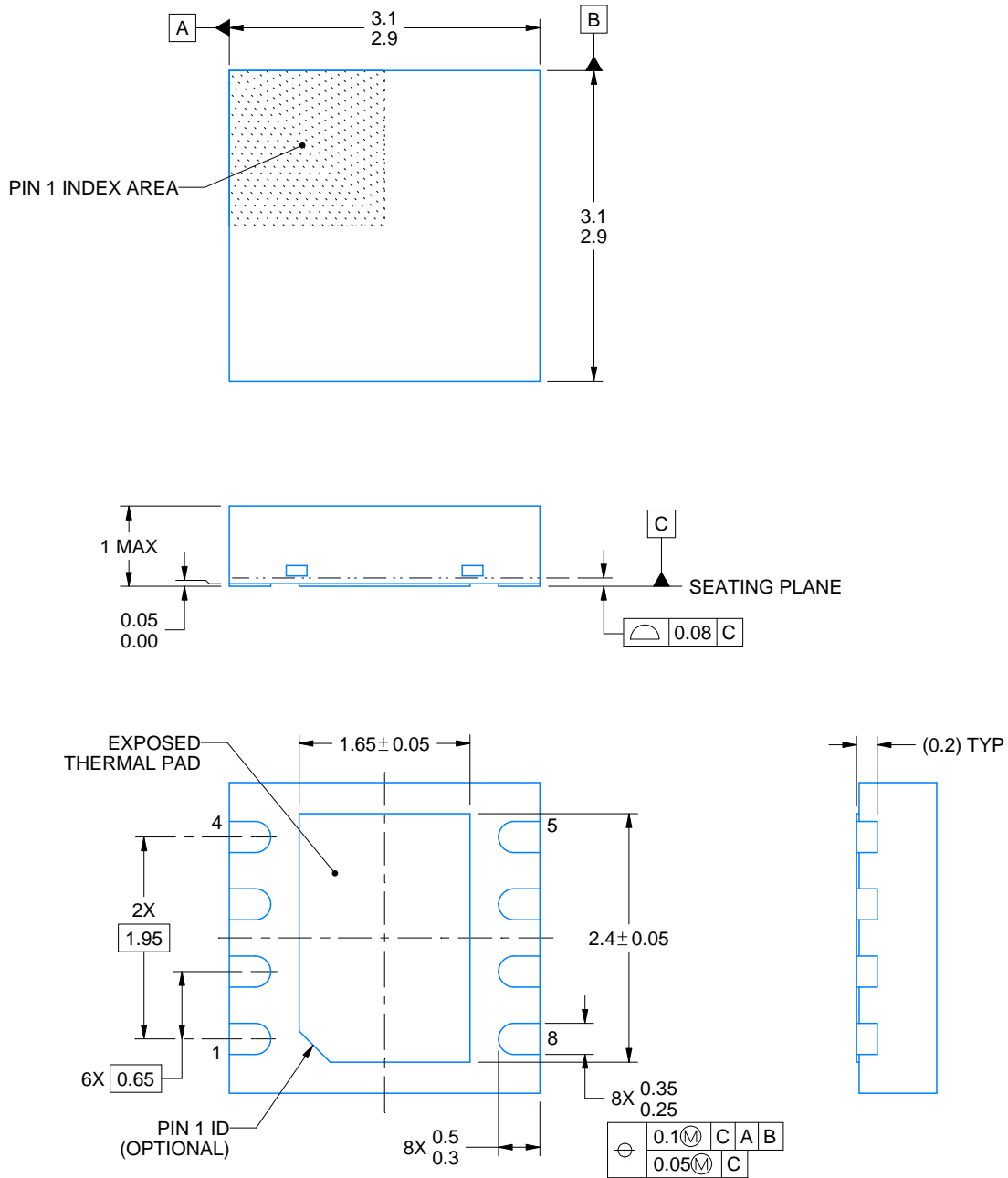
DRB0008B



# PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218876/A 12/2017

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
81% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4218876/A 12/2017

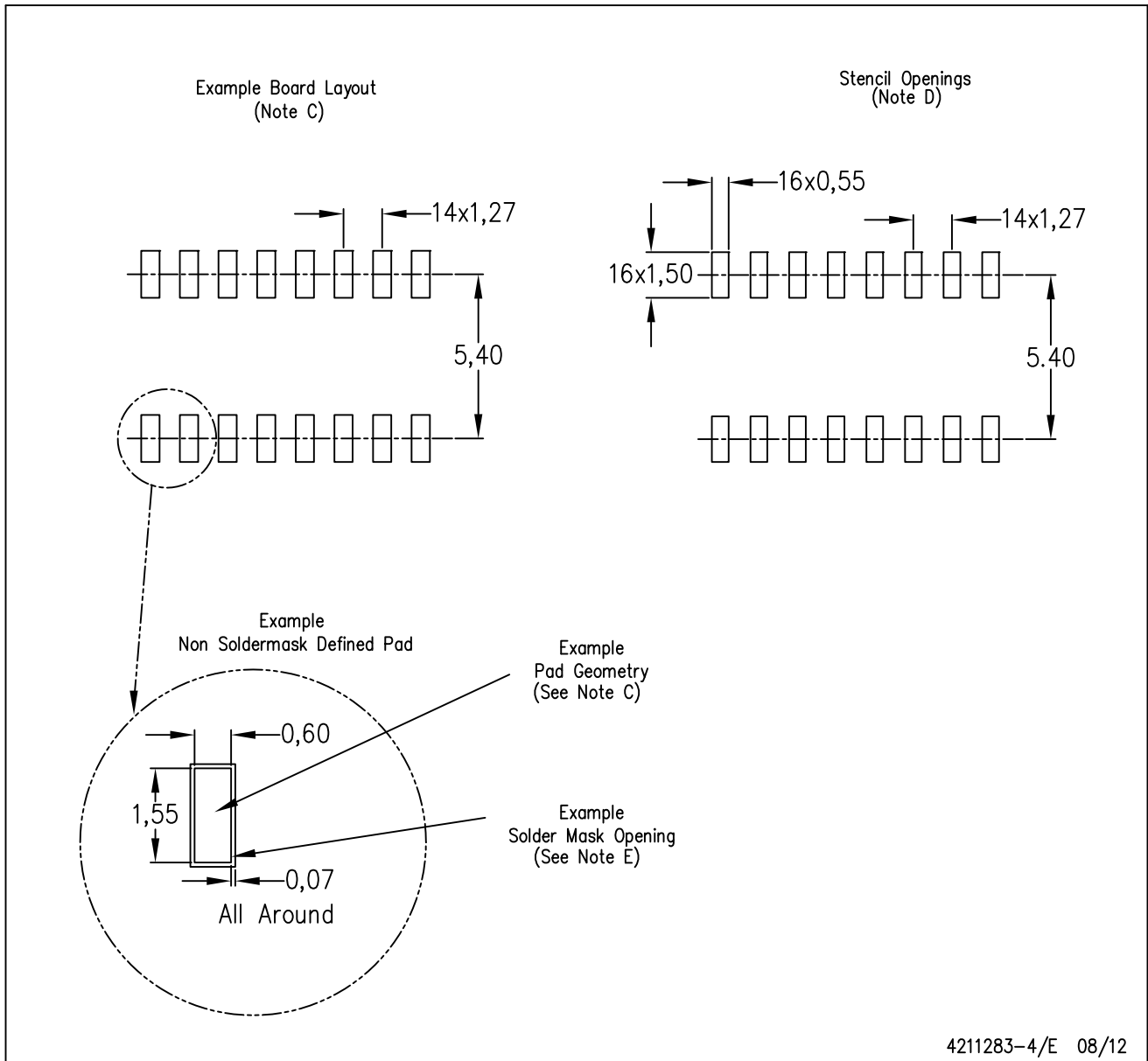
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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