THE DATASHEET OF

TPS65040ZQER

Actual Size
5 mm x 5 mm

CLOCK- AND POWER-MANAGEMENT IC FOR RF SYSTEM

FEATURES

- **High Efficiency, 550-mA, Adjustable-Output Buck Boost DC-DC Converter**
- **6 High Performance LDO With Low Power Mode**
- **2 Analog Switches**
- **2 High Performance LDO**
- **3-Channel Selectable Output, 8-Bit Resolution D/A Converter**
- **12-Bit Resolution D/A Converter**
- **3-Channel Clock Buffer of 26 MHz VCTCXO For Clock Reference**
- **2 Serial Interface With 3-Wire**
- **Thermal Shut Down Protection**
- **Hot-Die Detection For Die Temperature Alert**
- **5 mm × 5 mm, 0.5 mm Pitch MicroStar Junior™ Package**

APPLICATIONS

- **UMTS/WCDMA/GSM Cellular Phone**
- **Smart Phones**
- **Wireless Modems**

DESCRIPTION

The TPS65040 is an advanced RF power management chip for cellular phones, providing a highly optimized solution for UMTS/WCDMA/GSM power amplifier applications. This solution improves efficiency by voltage control of the power amplifiers, saving power to prolong battery life. The TPS65040 features buck boost DC/DC converters suited for applications requiring up to 550-mA output current while dynamically adjusting output voltage from 0.8 V to 4.2 V with a fast settling time, high performance 8-channel LDO regulators, 8bit DAC, 12bit ADC and clock distribution buffers of 26 MHz VCTCXO. Each block can be controlled by serial interface and external pins. The TPS65040 offers material cost savings and small size, using a compact 5 mm × 5 mm MicroStar Junior™ package.

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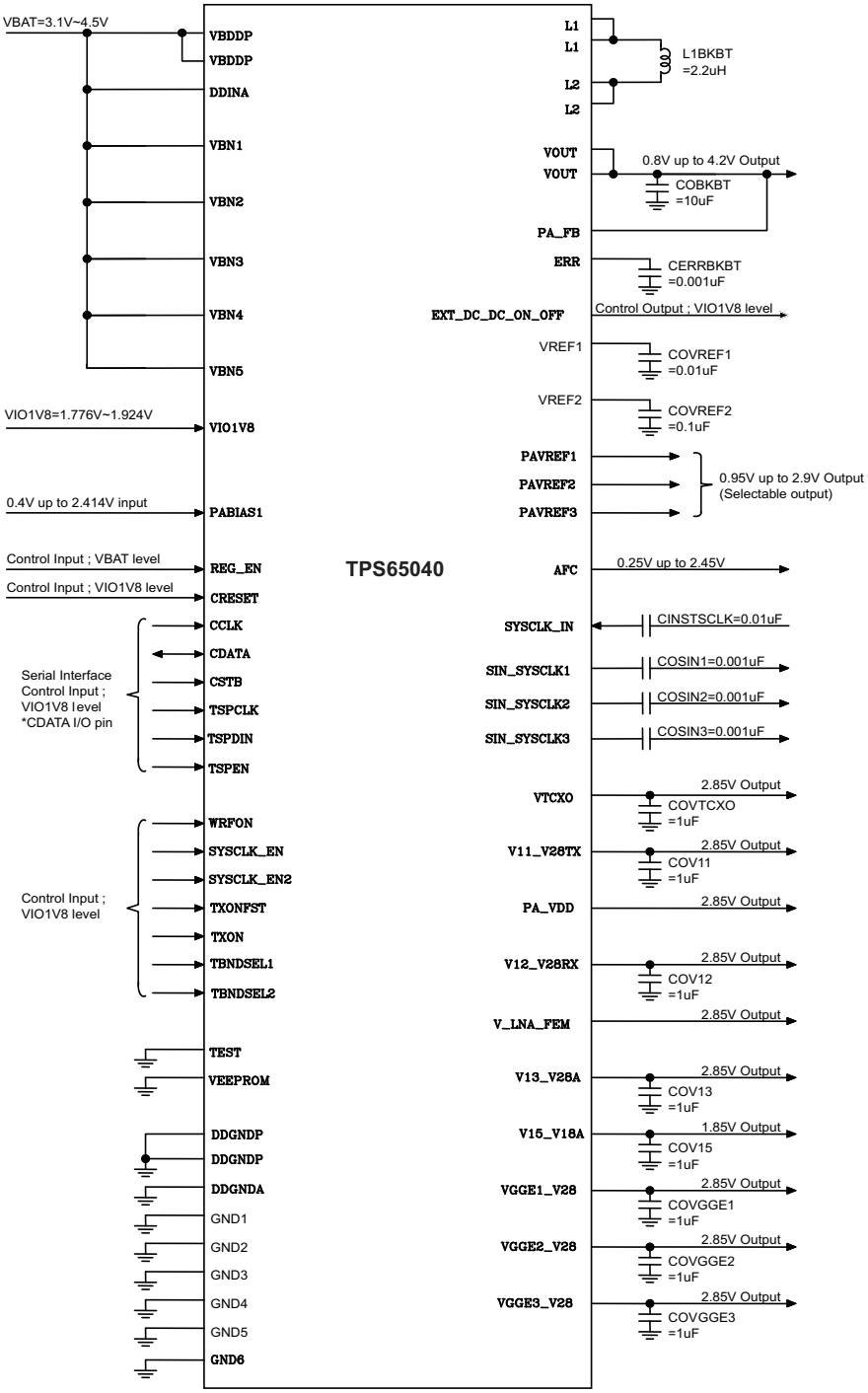
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TPS65040 OUTPUT(1) AND OPERATIONAL RANGE

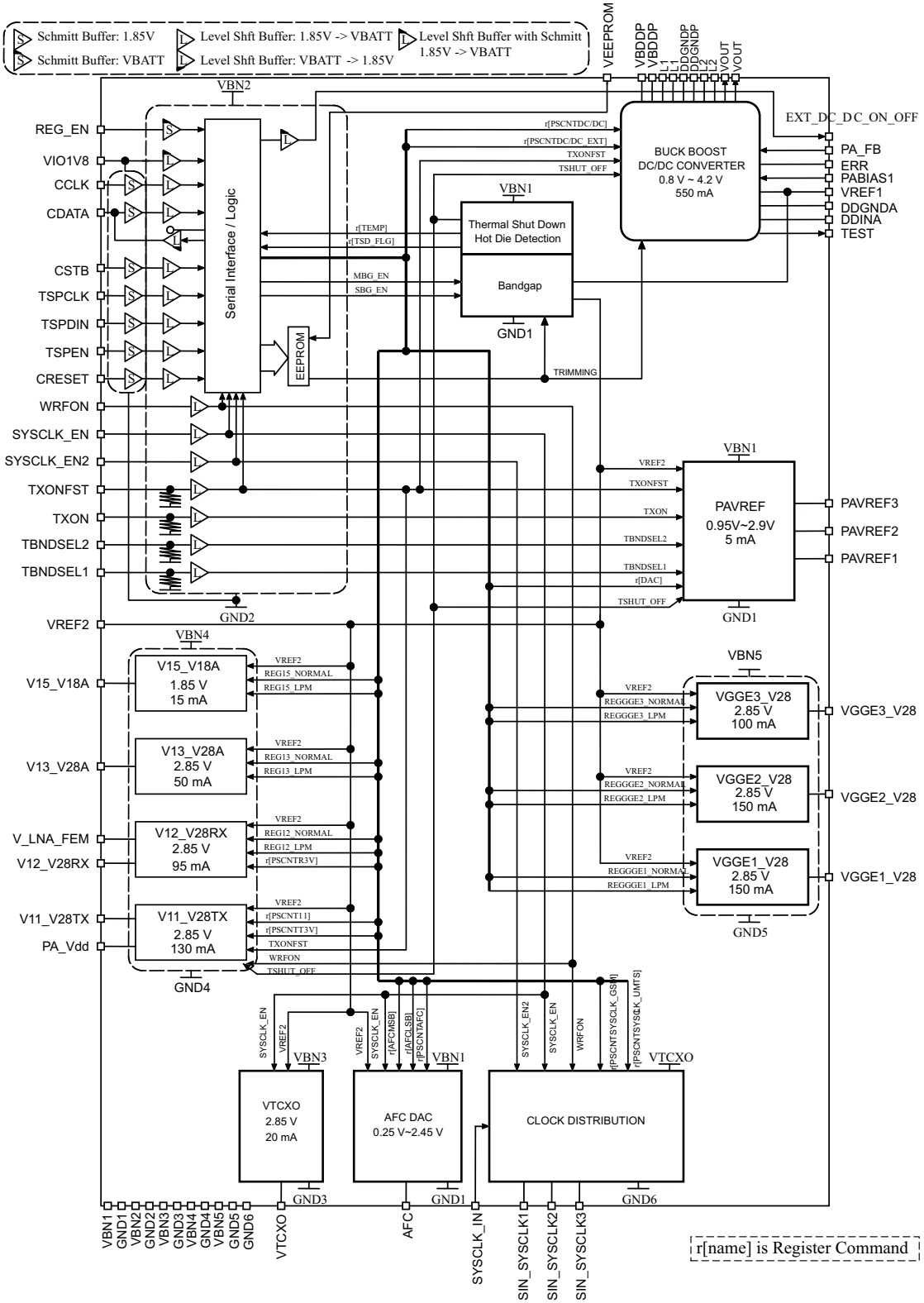
PIN NAME	PIN NO.	TYPE	V_{OUT} (V)	I_{OUT}MAX (mA)
VOUT	A8, B8	Buck boost DC/DC converter	0.8~4.2	550
V11_V28TX	G1	Normal mode (high PSRR LDO)	2.85	130(2)
PA_VDD	F2	Switch output of V11_V28TX	2.85	20
V12_V28RX	E1	Low power mode/normal mode (high PSRR LDO)	2.85	95(3)
V_LNA_FEM	E2	Switch output of V12_V28RX	2.85	30
V13_V28A	D1	Low power mode/normal mode (high PSRR LDO)	2.85	50
V15_V18A	C2	Low power mode/normal mode (high PSRR LDO)	1.85	15
VGGE1_V28	H9	Low power mode/normal mode (high PSRR LDO)	2.85	150
VGGE2_V28	G9	Low power mode/normal mode (high PSRR LDO)	2.85	150
VGGE3_V28	F9	Low power mode/normal mode (high PSRR LDO)	2.85	100
VTCXO	J2	Normal mode (high PSRR LDO)	2.85	20
PAVREF1	A3	8-bit DAC output	0.95~2.9	5
PAVREF2	A2	8-bit DAC output	0.95~2.9	5
PAVREF3	B1	8-bit DAC output	0.95~2.9	5
AFC	J3	12-bit DAC output	0.25~2.45	0.025
SIN_SYSCLK1	J5	Clock distribution with –3 dB gain		—
SIN_SYSCLK2	J6	Clock distribution with –1 dB gain		—
SIN_SYSCLK3	J7	Clock distribution with –1 dB gain		—

(1) All outputs can be controlled by serial interface, except VTCXO, PAVREF1, PAVREF2 and PAVREF3.
(2) When the PA_VDD has load current, the maximum load current of V11_V28TX is decreased from 130 mA by the value of I_{OUT} of PA_VDD.
(3) When the V_LNA_FEM has load current, the maximum load current of V12_V28RX is decreased from 95 mA by the value of I_{OUT} of V_LNA_FEM.

APPLICATION CIRCUIT



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	T_A	PACKAGE(1)	ORDERING	PACKAGE MARKING
TPS65040	–30°C to 85°C	71-pin MicroStar Junior™	TPS65040ZQE	PS65040

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Supply voltage	VIO1V8 pin with respect to GND2	–0.3 to 3.3	V
	VBN1 pin with respect to GND1	–0.3 to 5.5	V
	VBN2 pin with respect to GND2	–0.3 to 5.5	V
	VBN3 pin with respect to GND3	–0.3 to 5.5	V
	VBN4 pin with respect to GND4	–0.3 to 5.5	V
	VBN5 pin with respect to GND5	–0.3 to 5.5	V
	VBDDP(2) pin with respect to DDGNDP(2)	–0.3 to 5.5	V
	DDINA pin with respect to DDGNDA	–0.3 to 5.5	V
Input voltage range on REG_EN pin with respect to GND2		–0.3 to 5.5	V
Input voltage range on PABIAS1, PA_FB and ERR pins with respect to DDGNDA		–0.3 to 5.5	V
Input voltage range(2) on L1 and L2 pins with respect to DDGNDP		–0.3 to 5.5	V
Input voltage range on other pins(3)		–0.3 to 5.5	V
Input voltage range on SYSCLK_IN pin with respect to GND6		–0.3 to 3.3	V
Input voltage range on other input pins(4)		–0.3 to 3.3	V
Input voltage range on other pins(5)		–0.3 to 3.3	V
Peak LDO and SW output current(6)		Internally Limited	
Peak current of power path(2) on VBDDP, L1, L2 pins with respect to DDGNDP		5	A
Storage temperature		–40 to 150	°C
Maximum junction temperature		125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) VBDDP is A4 and B4 pins, L1 is A5 and B5 pins, L2 is A7 and B7 pins, and DDGNDP is A6 and B6 pins.
(3) Pin is *VTCXO* with respect to GND3. Pins are *VGGE1_V28*, *VGGE2_V28*, and *VGGE3_V28* with respect to GND5. Pin is *VOUT* with respect to DDGNDP. Pin is *TEST* with respect to DDGNDA.
(4) Pins are *CCLK*, *CDATA*, *CSTB*, *TSPCLK*, *TSPDIN*, *TSPEN*, *CRESET*, *WRFON*, *TXON*, *TXONFST*, *TBNDSEL1*, *TBNDSEL2*, *SYSCLK_EN* and *SYSCLK_EN2* with respect to GND2.
(5) Pins are *AFC*, *PAVREF1*, *PAVREF2*, and *PAVREF3* with respect to GND1. Pins are *SIN_SYSCLK1*, *SIN_SYSCLK2* and *SIN_SYSCLK3* with respect to GND6.
(6) LDO and SW OUTPUT are *V11_V28TX*, *PA_VDD*, *V12_V28RX*, *V_LNA_FEM*, *V15_V18A* , *V13_V28A*, *VTCXO*, *VGGE1_V28*, *VGGE2_V28* and *VGGE3_V28*.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$	MAX POWER DISSIPATION AT T_A = 25°C	DERATING FACTOR T_A < 25°C
ZQE	51.23°C/W	1.95 W	19.52 mW/°C

(1) Test board conditions
- JEDEC High-K (2S2P) board used
- 3x3 inch, 4 layer
- 1 oz copper ground/power trace in the PCB
- 2 oz copper trace on the top/bottom of the PCB

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{VIO}	Supply voltage to VIO1V8 input	1.746		1.924	V
VBAT(1)	Supply voltage to VBN1 input	3.1		4.5	V
	Supply voltage to VBN2 input	3.1		4.5	V
	Supply voltage to VBN3 input	3.1		4.5	V
	Supply voltage to VBN4 input	3.1		4.5	V
	Supply voltage to VBN5 input	3.1		4.5	V
	Supply voltage to VBDDP input	3.1		4.5	V
	Supply voltage to DDINA input	3.1		4.5	V
VROM	Supply voltage to VEEPROM input (EEPROM WRITE VOLTAGE)	13	14	15	V
NROM	Acceptable number of EEPROM writings(2)			10	times
C_{OVREF1}(3)	Output capacitor at VREF1		0.01		µF
C_{OVREF2}(3)	Output capacitor at VREF2		0.1		µF
$C_{OUTBKBT}$(3)	Output capacitor at VOUT		10		µF
L_{I2BKBT}	Inductor at L1 and L2		2.2		µH
$C_{ERRBKBT}$(3)	Phase compensation at ERR		0.001		µF
C_{OV11}(3)	Output capacitor at V11_V28TX		1		µF
C_{OV12}(3)	Output capacitor at V12V28R		1		µF
C_{OV13}(3)	Output capacitor at V13_V28A		1		µF
C_{OV15}(3)	Output capacitor at V15_V28A		1		µF
C_{OVGGE1}(3)	Output capacitor at VGGE1_V28		1		µF
C_{OVGGE2}(3)	Output capacitor at VGGE2_V28		1		µF
C_{OVGGE3}(3)	Output capacitor at VGGE3_V28		1		µF
C_{OVTCXO}(3)	Output capacitor at VTCXO		1		µF
$C_{INSYSCLK}$(3)	Input capacitor at SYSCLK_IN		0.01		µF
C_{OSIN1}(3)	Output capacitor at SIN_SYSCLK1		0.001		µF
C_{OSIN2}(3)	Output capacitor at SIN_SYSCLK2		0.001		µF
C_{OSIN3}(3)	Output capacitor at SIN_SYSCLK3		0.001		µF
T_A	Operating ambient temperature	–30		85	°C
T_J	Operating junction temperature	–30		125	°C

(1) VBN1, VBN2, VBN3, VBN4, VBN5, VBDDP and DDINA are the same supply voltage range for VBAT.
(2) This defines the number of customer's writings after shipment from TI.
(3) B characteristics capacitor

ELECTRICAL CHARACTERISTICS

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK BOOST DC/DC CONVERTER						
$V_{O(BKBT)}$	Output voltage	PABIAS1 pin = 2.414 V		0.8		V
		PABIAS1 pin = 1.407 V		2.5		
		PABIAS1 pin = 0.400 V		4.2		
$I_{O(BKBT)}$	Maximum output current(1)				550	mA
$V_{O(BKBT_ACC)}$	Output voltage accuracy	VBAT = 3.8 V, I_{LOAD} = 10 µA, PABIAS1 pin voltage accuracy = ±0 mV at T_A = 25°C	–50		50	mV
		VBAT = 3.8 V, I_{LOAD} = 10 µA, PABIAS1 pin voltage accuracy = ±0 mV(2)	–80		80	
$I_{SD(BKBT)}$	Shutdown current	VBDDP pin and DDINA pin at T_A = 25°C			1	µA
$I_{Q(BKBT)}$	Quiescent current	DDINA pin, I_{LOAD}= 0 mA, PABIAS1 pin = 1.4 V, No External Component, device is not switching		0.8	3	mA
VREG	Line Regulation(2)	VBAT = 3.1 V to 4.5 V, I_{LOAD} = 400 mA		20	40	mV
IREG	Load Regulation(2)	I_{LOAD} = 10 µA to 400 mA		20	40	mV
	Efficiency(2)	VBAT ≥ 4.0 V, $V_{O(BKBT)}$ = 3.5 V, I_{LOAD} = 270 mA		93%		
		VBAT ≥ 3.1 V, $V_{O(BKBT)}$ = 4.0 V, I_{LOAD} = 270 mA		90%		
		VBAT ≥ 3.1 V, $V_{O(BKBT)}$ = 2.5 V, I_{LOAD} = 150 mA		90%		
		VBAT ≥ 3.1 V, $V_{O(BKBT)}$ = 1.6 V, I_{LOAD} = 90 mA		80%		
		VBAT ≥ 3.1 V, $V_{O(BKBT)}$ = 1.0 , I_{LOAD} = 65 mA		70%		
f_S	Switching frequency		1.2	1.5	1.8	MHz
	Max Duty	Boost Mode	40%	50%	60%	
$R_{DS(on)P}$	P-channel MOSFET on resistance(2)			150		mΩ
$R_{DS(on)N}$	N-channel MOSFET on resistance(2)			150		mΩ
	Output ripple voltage(2)	$V_{O(BKBT)}$ = 0.8 V ~ 4.2 V, I_{LOAD} = 10 mA ~ 400 mA			100	mVpp
	Output voltage settling time of buck mode(2)(3)	VBAT = 4.2 V, $V_{O(BKBT)}$ = 1 V to 4 V, I_{LOAD} = 100 mA		25	50	µs
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 4 V to 1 V, I_{LOAD} = 400 mA to 20 mA		25	50	µs
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 1 V to 1.5 V, I_{LOAD} = 20 mA		25	50	µs
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 2 V to 2.5 V, I_{LOAD} = 50 mA		25	50	µs
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 3.5 V to 4 V, I_{LOAD} = 150 mA		25	50	µs
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 1.5 V to 1 V, I_{LOAD} = 150 mA to 20 mA		25	50	µs
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 2.5 V to 2 V, I_{LOAD} = 200 mA to 50 mA		25	50	µs
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 4 V to 3.5 V, I_{LOAD} = 400 mA to 150 mA		25	50	µs

(1) Using the reference EVM.
(2) Not production tested. Specified by using the reference EVM.
(3) Settling time measures ±0.2 V of the target $V_{O(BKBT)}$ voltage

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output voltage settling time of boost mode(2)(3)	VBAT = 3.1 V, $V_{O(BKBT)}$ = 1 V to 4.2 V, I_{LOAD}= 100 mA			50	µs
		VBAT = 3.1 V, $V_{O(BKBT)}$ = 4.2 V to 1 V, I_{LOAD} = 400 mA to 20 mA			50	µs
		VBAT = 3.1 V, $V_{O(BKBT)}$ = 3.5 V to 4.2 V, I_{LOAD} = 400 mA			50	µs
		VBAT = 3.1 V, $V_{O(BKBT)}$ = 4.2 V to 3.5 V, I_{LOAD} = 400 mA to 150 mA			50	µs
	Output voltage shift peak voltage value (changed load current)(2)	VBAT = 4.2 V, $V_{O(BKBT)}$ = 1 V, I_{LOAD} = 0 mA to 100 mA, I_{TR}/I_{TF} = 1 µs			200	mV
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 2 V, I_{LOAD} = 0 mA to 400 mA, I_{TR}/I_{TF} = 1 µs			200	mV
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 3.5 V, I_{LOAD} = 0 mA to 400 mA, I_{TR}/I_{TF} = 1 µs			200	mV
		VBAT = 3.1 V, $V_{O(BKBT)}$ = 4.2 V, I_{LOAD} = 0 mA to 400 mA, I_{TR}/I_{TF} = 1 µs			250	mV
	Output voltage shift convergence time (changed load current)(4)(5)	VBAT = 4.2 V, $V_{O(BKBT)}$ = 1 V, I_{LOAD} = 0 mA to 100 mA, I_{TR}/I_{TF} = 1 µs			35	µs
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 2 V, I_{LOAD} = 0 mA to 400 mA, I_{TR}/I_{TF} = 1 µs			35	µs
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 3.5 V, I_{LOAD} = 0 mA to 400 mA, I_{TR}/I_{TF} = 1 µs			35	µs
		VBAT = 4.2 V, $V_{O(BKBT)}$ = 4 V, I_{LOAD} = 0 mA to 400 mA, I_{TR}/I_{TF} = 1 µs			35	µs
		VBAT = 3.1 V, $V_{O(BKBT)}$ = 4.2 V, I_{LOAD} = 0 mA to 400 mA, I_{TR}/I_{TF} = 1 µs			35	µs
		VBAT = 3.1 V, $V_{O(BKBT)}$ = 4.2 V, I_{LOAD} = 0 mA to 400 mA, I_{TR}/I_{TF} = 1 µs			35	µs
		VBAT = 3.1 V, $V_{O(BKBT)}$ = 3.4 V, I_{LOAD} = 0 mA to 400 mA, I_{TR}/I_{TF} = 1 µs			35	µs
$R_{PABIAS1}$	PABIAS1 input impedance		100	200		kΩ
V_{SCP}	Short circuit protection voltage(6)	$V_{O(BKBT)}$× 80% detection	$V_{O(BKBST)}$ × 70%	$V_{O(BKBST)}$ × 80%	$V_{O(BKBST)}$ × 90%	V
t_{SCP}	SCP monitor mode count time	$V_{O(BKBT)}$ < $V_{O(BKBT)}$× 80%		0.5		ms
	SCP mode count time	Output P-channel MOSFETs are OFF, $V_{O(BKBT)}$ force to 0 V		8		ms
$I_{CL(BKBT)}$	Current limit protection(4)	VBAT = 3.8 V, C_{OBKBT} = 10 µF, L_{1BKBT} = 2.2 µH, $C_{ERRBKBT}$ = 1 nF, T_A = 25°C		1.5		A
t_{SS}	Soft start ramp up time(4)	$V_{O(BKBT)}$ = 0.8 V ~ 4.2 V, I_{LOAD} = 400 mA, r[PSCNTDC/DC](7)= 1, TXONFST pin = 0 V to V_{VIO}, VOUT ±0.2 V			500	µs
		$V_{O(BKBT)}$ = 0.8 V ~ 4.2 V, I_{LOAD} = 400 mA, TXONFST pin = V_{VIO}, r[PSCNTDC/DC] = 0 to 1, VOUT ±0.2 V			660	µs

(4) Not production tested. Specified by using the reference EVM.
(5) Convergence time measures ±0.1 V of the target $V_{O(BKBT)}$ voltage
(6) Tested at $V_{O(BKBT)}$ = 2.5 V
(7) r[PSCNTDC/DC] is a name of register command by serial interface.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V11_V28TX (LOW DROPOUT OUTPUT)						
$V_{O(V11)}$	Output voltage	$I_{LOAD(V11)}$ = 10 mA	2.79	2.85	2.92	V
$I_{O(V11)}$	Maximum output current	PA_VDD is off			130	mA
		PA_VDD is on, $I_{LOAD(PA_VDD)}$ = 20 mA			110	
$V_{O(V11_ACC)}$	Total output accuracy(1)		–4%		4%	
$I_{CL(V11)}$	Current limit protection	$V_{O(V11)}$ = 0 V		170	280	mA
$V_{SAT(V11)}$	Output saturation voltage				0.3	V
$I_{SD(V11)}$	Shutdown current(2)	VBN4 pin at T_A = 25°C			1	µA
$I_{Q(V11)}$	Quiescent current	VBN4 pin, $I_{LOAD(V11)}$ = 0 mA at T_A = 25°C V12_V28RX, V13_V28A and V15_V18A are off		40	60	µA
$V_{REG(V11)}$	Line regulation	VBAT = 3.1 V ~ 4.5 V, $I_{LOAD(V11)}$ = 130 mA, PA_VDD is off		0.1	0.4	%/V
$I_{REG(V11)}$	Load regulation(3)	$I_{LOAD(V11)}$ = 10 µA to 130 mA PA_VDD is off		50	100	mV
$I_{TR(V11)}$	Load Transient(3)(4)	$I_{LOAD(V11)}$ = 10 µA to 130 mA, I_{TR} = 1 µs		135	165	mV
		$I_{LOAD(V11)}$ = 130 mA to 10 µA, I_{TF} = 1 µs		135	210	
$PSRR_{(V11)}$	Power supply ripple rejection(3)(5)	VBAT = 3.8 V, F_{RIPPLE} = 1 kHz, $I_{LOAD(V11)}$ = 130 mA, PA_VDD is off		60		dB
		VBAT = 3.8 V, F_{RIPPLE} = 100 kHz, $I_{LOAD(V11)}$ = 130 mA, PA_VDD is off		45		dB
$V_{ON(V11)}$	Output noise(3)	$I_{LOAD(V11)}$ = 5 mA, PA_VDD is off, 10 Hz to 100 kHz		30		µVrms
$t_{ST(V11)}$	Startup time(3)	$V_{O(V11)}$ > 90%, $I_{LOAD(V11)}$ = 10 µA to 130 mA r[PSCNT11](6) = 1 and WRFON pin = 0 V to V_{VIO} or WRFON pin = V_{VIO} and r[PSCNT11] = 0 to 1			500	µs
$t_{F(V11)}$	Output voltage falling time(3)	$V_{0(V11)}$ > 10%, $I_{LOAD(V11)}$ = 10 mA r[PSCNT11](6) = 1 and WRFON pin = V_{VIO} to 0 V or WRFON pin = V_{VIO} and r[PSCNT11] = 1 to 0			5	ms
PA_VDD						
$V_{O(PA_VDD)}$	Output voltage	V11_V28TX is on, $I_{LOAD(PA_VDD)}$ = 20 mA, $I_{LOAD(V11)}$ = 0 mA	2.74	2.84	2.9	V
$I_{O(PA_VDD)}$	Maximum output current	V11_V28TX is on			20	mA
$t_{ST(PA_VDD)}$	Startup time	$V_{O(PA_VDD)}$ > 90%, $I_{LOAD(PA_VDD)}$ = 0 mA , VIO1V8 pin = V_{VIO} and WRFON pin = V_{VIO} r[PSCNTT3V](7) = 1 and TXONFST pin = 0 V to V_{VIO}, or TXONFST pin = V_{VIO} and r[PSCNTT3V] = 0 to 1(3)			5	µs
$t_{F(PA_VDD)}$	Output voltage falling time	$V_{O(PA_VDD)}$ < 10%, $I_{LOAD(PA_VDD)}$ = 0 mA, TXONFST pin = V_{VIO} to 0 V, or WRFON pin = V_{VIO} to 0 V(3), or r[PSCNTT3V] = 1 to 0(3)			1.5	ms

(1) Total accuracy includes line and load regulation, temperature and process condition. It does not include load and line transients
(2) Shutdown current include V12_V28RX, V13_V28A and V15_V18A2
(3) Not Production tested. Specified by using the reference EVM.
(4) The margin up to 2.7 V extends to the output voltage if COV11 is changed into 4.7 µ F. Specified by using the reference EVM.
(5) Ripple voltage = 0.1 V_{PP}
(6) r[PSCNT11] is the name of a register command by serial interface.
(7) r[PSCNTT3V] is the name of a register command by serial interface. The name of the switch is a T3V, and the name of the output pin is PA_VDD.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V12_V28RX (LOW DROPOUT OUTPUT)						
$V_{O(V12)}$	Normal mode output voltage	$I_{LOAD(V12)}$ = 10 mA	2.79	2.85	2.92	V
	Low power mode output voltage	$I_{LOAD(V12)}$= 1 mA	2.79	2.85	2.91	
$I_{O(V12)}$	Normal mode Maximum output current	V_LNA_FEM is off			95	mA
		V_LNA_FEM is on, $I_{LOAD(V_LNA_FEM)}$ = 30 mA			65	mA
	Low power mode maximum output current	V_LNA_FEM is off			5	mA
$V_{O(V12_ACC)}$	Total output accuracy(1)		–4%		4%	
$I_{CL(V12)}$	Current limit protection(2)	$V_{O(V12)}$ = 0 V		160	270	mA
$V_{SAT(V12)}$	Output saturation voltage(2)				0.3	V
$I_{SD(V12)}$	Shutdown current(3)	VBN4 pin at T_A = 25°C			1	µA
$I_{Q(V12)}$	Normal mode quiescent current	VBN4 pin, $I_{LOAD(V12)}$ = 0 mA at T_A = 25°C V11_V28TX, V13_V28A and V15_V18A are off		40	60	µA
	Low power mode quiescent current	VBN4 pin, $I_{LOAD(V12)}$ = 0 mA at T_A = 25°C V11_V28TX, V13_V28A and V15_V18A are off		1.2	3	
$V_{REG(V12)}$	Line regulation(2)	VBAT = 3.1 V ~ 4.5 V, $I_{LOAD(V12)}$ = 95 mA, V_LNA_FEM is off		0.1	0.4	%/V
$I_{REG(V12)}$	Load regulation(2)(4)	$I_{LOAD(V12)}$ = 10 µA to 95 mA, V_LNA_FEM is off		50	100	mV
$I_{TR(V12)}$	Load Transient(2)(4)(5)	$I_{LOAD(V12)}$ = 10 µA to 95 mA, I_{TR} = 1 µs		130	160	mV
		$I_{LOAD(V12)}$ = 95 mA to 10 µA, I_{TF} = 1 µs		130	160	mV
$PSRR_{(V12)}$	Power supply ripple rejection(2)(4)(6)	VBAT = 3.8 V, F_{RIPPLE} = 1 kHz, $I_{LOAD(V12)}$ = 95 mA, V_LNA_FEM is off		60		dB
		VBAT = 3.8 V, F_{RIPPLE} = 100 kHz, $I_{LOAD(V12)}$ = 95 mA, V_LNA_FEM is off		45		dB
$V_{ON(V12)}$	Output noise(2)(4)	$I_{LOAD(V12)}$ = 5 mA, V_LNA_FEM is off, 10 Hz to 100 kHz		30		µVrms
$t_{ST(V12)}$	Startup time(2)(4)	$V_{O(V12)}$ > 90%, $I_{LOAD(V12)}$ = 10 µA to 95 mA VIO1V8 pin = 0 V to V_{VIO}, or VIO1V8 pin = V_{VIO} and WRFON pin = V_{VIO} and r[PSCNT12](7) = 0 to 1			500	µs
$t_{F(V12)}$	Output voltage falling time(4)	$V_{O(V12)}$ < 10%, $I_{LOAD(V12)}$ = 0 mA, DVIO1V8 pin = V_{VIO} to 0 V, or r[PSCNT12] = 1 to 0			5	ms
V_LNA_FEM						
$V_{O(V_LNA_FEM)}$	Output voltage(2)	V12_V28RX is on $I_{LOAD(V_LNA_FEM)}$ = 30 mA, $I_{LOAD(V12)}$ = 0 mA	2.71	2.83	2.89	V
$I_{O(V_LNA_FEM)}$	Maximum output current(2)	V12_V28RX is on			30	mA
$T_{ST(V_LNA_FEM)}$	Startup time(2)(4)	$V_{O(V_LNA_FEM)}$ > 90%, $I_{LOAD(V_LNA_FEM)}$ = 0 mA, r[PSCNT12] = 1 and r[PSCNTR3V](5) = 1 and WRFON pin = 0 V to V_{VIO}			5	µs
$T_{F(V_LNA_FEM)}$	Output voltage falling time(2)	$V_{O(V_LNA_FEM)}$ < 10%, $I_{LOAD(V_LNA_FEM)}$ = 0 mA ,VIO1V8 pin = V_{VIO} to 0 V, or r[PSCNT12] = 1 to 0(4), or r[PSCNTR3V] = 1 to 0(4)			1.5	ms

(1) Total accuracy includes line and load regulation, temperature and process condition. It does not include load and line transients
(2) Normal mode operation
(3) Shutdown current include V11_V28TX, V13_V28A and V15_V18A
(4) Not Production tested. Specified by using the reference EVM.
(5) The margin up to 2.7 V extends to the output voltage if COV12 is changed to 4.7 µF. Specified by using the reference EVM.
(6) Ripple voltage = 0.1 V_{PP}
(7) r[PSCNT12] is a name of register command by serial interface. r[PSCNTR3V] is a name of register command by serial interface. The name of switch is a R3V and the name of output pin is V_LNA_FEM.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V13_V28A (LOW DROPOUT OUTPUT)						
$V_{O(V13)}$	Normal mode output voltage	I_{LOAD} = 10 mA	2.79	2.85	2.92	V
	Low power mode output voltage	I_{LOAD} = 1 mA	2.79	2.85	2.91	
$I_{O(V13)}$	Normal mode maximum output current				50	mA
	Low power mode maximum output current				2	mA
$V_{O(V13_ACC)}$	Total output accuracy(1)		–4%		4%	
$I_{CL(V13)}$	Current limit protection(2)	$V_{O(V13)}$ = 0 V		100	210	mA
$V_{SAT(V13)}$	Output saturation voltage(2)				0.3	V
$I_{SD(V13)}$	Shutdown current(3)	VBN4 pin at T_A = 25°C			1	µ A
$I_{Q(V13)}$	Normal mode quiescent current	VBN4 pin, I_{LOAD} = 0 mA at T_A = 25°C V11_V28TX, V12_V28RX and V15_V18A are off		40	60	µA
	Low power mode quiescent current	VBN4 pin, I_{LOAD} = 0 mA at T_A = 25°C V11_V28TX, V12_V28RX and V15_V18A are off		1.2	3	
$V_{REG(V13)}$	Line regulation(2)	VBAT = 3.1 V ~ 4.5 V, I_{LOAD} = 50 mA		0.1	0.4	%/V
$I_{REG(V13)}$	Load regulation(2)(4)	I_{LOAD} = 10 µA to 50 mA		50	100	mV
$I_{TR(V13)}$	Load transient(2)(4)	I_{LOAD} = 10 µA to 50 mA, I_{TR} = 1 µs		110	150	mV
		I_{LOAD} = 50 mA to 10 µA, I_{TF} = 1 µs		110	150	mV
$PSRR_{(V13)}$	Power supply ripple rejection(2)(4)(5)	VBAT = 3.8 V, F_{RIPPLE} = 1 kHz, I_{LOAD} = 50 mA		60		dB
		VBAT = 3.8 V, F_{RIPPLE} = 100 kHz, I_{LOAD} = 50 mA		45		dB
$V_{ON(V13)}$	Output noise(2)(4)	I_{LOAD} = 5 mA, 10 Hz to 100 kHz		30		µVrms
$t_{ST(V13)}$	Startup time(2)(4)	$V_{O(V13)}$ > 90%, I_{LOAD} = 10 µA to 50 mA , VIO1V8 pin = 0 V to V_{VIO}, or VIO1V8 pin = V_{VIO} and WRFON pin = V_{VIO} and r[PSCNT13](6) = 0 to 1			500	µs
$t_{F(V13)}$	Output voltage falling time(4)	$V_{O(V13)}$ < 10%, I_{LOAD} = 0 mA, VIO1V8 pin = V_{VIO} to 0 V, or r[PSCNT13] = 1 to 0			5	ms

(1) Total accuracy includes line and load regulation, temperature and process condition. It does not include load and line transients
(2) Normal mode operation
(3) Shutdown current include V11_V28TX, V12_V28RX and V15_V18A1
(4) Not production tested. Specified by using the reference EVM.
(5) Ripple voltage = 0.1 V_{PP}
(6) r[PSCNT13] is a name of register command by serial interface.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V15_V18A (LOW DROPOUT OUTPUT)						
$V_{O(V15)}$	Normal mode output voltage	I_{LOAD} = 5 mA	1.81	1.85	1.89	V
	Low power mode output voltage	I_{LOAD} = 1 mA	1.81	1.85	1.89	
$I_{O(V15)}$	Normal mode maximum output current				15	mA
	Low power mode maximum output current				2	mA
$V_{O(V15_ACC)}$	Total output accuracy(1)		–4%		4%	
$I_{CL(V15)}$	Current limit protection(2)	$V_{O(V15)}$ = 0 V		60	170	mA
$V_{SAT(V15)}$	Output saturation voltage(2)				0.3	V
$I_{SD(V15)}$	Shutdown current(3)	VBN4 pin at T_A = 25°C			1	µ A
$I_{Q(V15)}$	Normal mode quiescent current	VBN4 pin, I_{LOAD} = 0 mA at T_A = 25°C V11_V28TX, V12_V28RX and V13_V18A are off		40	60	µA
	Low power mode quiescent current	VBN4 pin, I_{LOAD} = 0 mA at T_A = 25°C V11_V28TX, V12_V28RX and V13_V18A are off		1.3	3	
$V_{REG(V15)}$	Line regulation(2)	VBAT = 3.1 V ~ 4.5 V, I_{LOAD} = 15 mA		0.1	0.4	%/V
$I_{REG(V15)}$	Load regulation(2)(4)	I_{LOAD} = 10 µA to 15 mA		50	100	mV
$I_{TR(V15)}$	Load transient(2)(4)	I_{LOAD} = 10 µA to 15 mA, I_{TR} = 1 µs		70	100	mV
		I_{LOAD} = 15 mA to 10 µA, I_{TF} = 1 µs		70	100	mV
$PSRR_{(V15)}$	Power supply ripple rejection(2)(4)(5)	VBAT = 3.8 V, F_{RIPPLE} = 1 kHz, I_{LOAD} = 15 mA		60		dB
		VBAT = 3.8 V, F_{RIPPLE} = 100 kHz, I_{LOAD} = 15 mA		45		dB
$V_{ON(V15)}$	Output noise(2)(4)	I_{LOAD} = 5 mA, 10 Hz to 100 kHz		30		µVrms
$t_{ST(V15)}$	Startup time(2)(4)	$V_{O(V15)}$ > 90%, I_{LOAD} = 10 µA to 15 mA , VIO1V8 pin = 0 V to V_{VIO}, or VIO1V8 pin = V_{VIO} and WRFON pin = V_{VIO} and r[PSCNT15](6) = 0 to 1			500	µs
$t_{F(V15)}$	Output voltage falling time(4)	$V_{O(V15)}$ < 10%, I_{LOAD} = 0 mA, VIO1V8 pin = V_{VIO} to 0 V, or r[PSCNT15] = 1 to 0			5	ms
VBAT UNDERVOLTAGE ELECTRICAL CHARACTERISTICS(7)						
$V_{O(V15)}$	Normal mode output voltage	2.7 V < VBAT < 3.1		1.85		V
	Low power mode output voltage			1.85		V

(1) Total accuracy includes line and load regulation, temperature and process condition. It does not include load and line transients
(2) Normal mode operation
(3) Shutdown current includes V11_V28TX, V12_V28RX, and V13_V28A
(4) Not production tested. Specified by using the reference EVM.
(5) Ripple voltage = 0.1 V_{PP}
(6) r[PSCNT15] is a name of register command by serial interface.
(7) V15 LDO is the only functional operation. The electrical characteristics are typical, but not specified.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VGGE1_V28 (LOW DROPOUT OUTPUT)						
$V_{O(VG1)}$	Normal mode output voltage	I_{LOAD} = 10 mA	2.79	2.85	2.92	V
	Low power mode output voltage	I_{LOAD} = 1 mA	2.79	2.85	2.91	
$I_{O(VG1)}$	Normal mode maximum output current				150	mA
	Low power mode maximum output current				2	mA
$V_{O(VG1_ACC)}$	Total output accuracy(1)		–4%		4%	
$I_{CL(VG1)}$	Current limit protection(2)	$V_{O(VG1)}$ = 0 V		230	320	mA
$V_{SAT(VG1)}$	Output saturation voltage(2)				0.3	V
$I_{SD(VG1)}$	Shutdown current(3)	VBN5 pin at T_A = 25°C			1	µ A
$I_{Q(VG1)}$	Normal mode quiescent current	VBN5 pin, I_{LOAD} = 0 mA at T_A = 25°C VGGE2_V28, and VGGE3_V28 are off		40	60	µA
	Low power mode quiescent current	VBN5 pin, I_{LOAD} = 0 mA at T_A = 25°C VGGE2_V28, and VGGE3_V28 are off		1.2	3	
$V_{REG(VG1)}$	Line regulation(2)	VBAT = 3.1 V ~ 4.5 V, I_{LOAD} = 150 mA		0.1	0.4	%/V
$I_{REG(VG1)}$	Load regulation(2)(4)	I_{LOAD} = 10 µA to 150 mA		50	100	mV
$I_{TR(VG1)}$	Load transient(2)(4)(5)	I_{LOAD} = 10 µA to 150 mA, I_{TR} = 1 µs		145	180	mV
		I_{LOAD} = 150 mA to 10 µA, I_{TF} = 1 µs		145	230	mV
$PSRR_{(VG1)}$	Power supply ripple rejection(2)(4)(6)	VBAT = 3.8 V, F_{RIPPLE} = 1 kHz, I_{LOAD} = 150 mA		60		dB
		VBAT = 3.8 V, F_{RIPPLE} = 100 kHz, I_{LOAD} = 150 mA		45		dB
$V_{ON(VG1)}$	Output noise(2)(4)	I_{LOAD} = 5 mA, 10 Hz to 100 kHz		30		µVrms
$t_{ST(VG1)}$	Startup time(2)(4)	$V_{0(VG1)}$ > 90%, I_{LOAD} = 10 µA to 150 mA , REG_EN pin = 0 V to VBAT			850	µs
		$V_{0(VG1)}$ > 90%, I_{LOAD} = 10 µA to 150 mA , REG_EN pin = VBAT and r[PSCNTGGE1](7) = 0 to 1			500	µs
$t_{F(VG1)}$	Output voltage falling time(4)	$V_{0(VG1)}$ < 10%, I_{LOAD} = 0 mA, REG_EN pin = VBAT to 0 V, or REG_EN pin = VBAT and r[PSCNTGGE1] = 1 to 0			5	ms
VBAT UNDER VOLTAGE ELECTRICAL CHARACTERISTICS(8)						
$V_{O(VG1)}$	Normal mode output voltage	3 V < VBAT < 3.1		2.85		V
	Low power mode output voltage			2.85		V

(1) Total accuracy includes line and load regulation, temperature and process condition. It does not include load and line transients
(2) Normal mode operation
(3) Shutdown current include VGGE2_V28 and VGGE3_V28.
(4) Not Production tested. Specified by using the reference EVM.
(5) The margin up to 2.7 V extends to the output voltage if COVGGE1 is changed to 4.7 µF. Specified by using the reference EVM.
(6) Ripple voltage = 0.1 V_{PP}
(7) r[PSCNTGGE1] is a name of register command by serial interface.
(8) VGGE1_V28 LDO is the only functional operation. The electrical characteristics are typical, but not specified.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VGGE2_V28 (LOW DROPOUT OUTPUT)						
$V_{O(VG2)}$	Normal mode output voltage	I_{LOAD} = 10 mA	2.79	2.85	2.92	V
	Low power mode output voltage	I_{LOAD} = 1 mA	2.79	2.85	2.91	
$I_{O(VG2)}$	Normal mode maximum output current				150	mA
	Low power mode maximum output current				2	mA
$V_{O(VG2_ACC)}$	Total output accuracy(1)		–4%		4%	
$I_{CL(VG2)}$	Current limit protection(2)	$V_{(VG2)}$ = 0 V		230	320	mA
$V_{sat(VG2)}$	Output saturation voltage(2)				0.3	V
$I_{SD(VG2)}$	Shutdown current(3)	VBN5 pin at T_A = 25°C			1	µ A
$I_{Q(VG2)}$	Normal mode quiescent current	VBN5 pin, I_{LOAD} = 0 mA at T_A = 25°C VGGE1_V28, and VGGE3_V28 are off		40	60	µA
	Low power mode quiescent current	VBN5 pin, I_{LOAD} = 0 mA at T_A = 25°C VGGE1_V28, and VGGE3_V28 are off		1.2	3	
$V_{REG(VG2)}$	Line regulation(2)	VBAT = 3.1 V ~ 4.5 V, I_{LOAD} = 150 mA		0.1	0.4	%/V
$I_{REG(VG2)}$	Load regulation(2)(4)	I_{LOAD} = 10 µA to 150 mA		50	100	mV
$I_{TR(VG2)}$	Load transient(2)(4)(5)	I_{LOAD} = 10 µA to 150 mA, I_{TR} = 1 µs		145	180	mV
		I_{LOAD} = 150 mA to 10 µA, I_{TF} = 1 µs		145	230	mV
$PSRR_{(VG2)}$	Power supply ripple rejection(2)(4)(6)	VBAT = 3.8 V, F_{RIPPLE} = 1 kHz, I_{LOAD} = 150 mA		60		dB
		VBAT = 3.8 V, F_{RIPPLE} = 100 kHz, I_{LOAD} = 150 mA		45		dB
$V_{ON(VG2)}$	Output noise(2)(4)	I_{LOAD} = 5 mA, 10 Hz to 100 kHz		30		µVrms
$t_{ST(VG2)}$	Startup time(2)(4)	$V_{O(VG2)}$ > 90%, I_{LOAD} = 10 µA to 150 mA, REG_EN pin = 0 V to VBAT			850	µs
		$V_{O(VG2)}$ > 90%, I_{LOAD} = 10 µA to 150 mA, REG_EN pin = VBAT and r[PSCNTGGE2](7) = 0 to 1			500	
$t_{F(VG2)}$	Output voltage falling time(4)	$V_{O(VG2)}$ < 10%, I_{LOAD} = 0 mA, REG_EN pin = VBAT to 0 V, or REG_EN pin = VBAT and r[PSCNTGGE2] = 1 to 0			5	ms
VBAT UNDER VOLTAGE ELECTRICAL CHARACTERISTICS(8)						
$V_{O(VG2)}$	Normal mode output voltage	3 V < VBAT < 3.1		2.85		V
	Low power mode output voltage			2.85		V

(1) Total accuracy includes line and load regulation, temperature and process condition. It does not include load and line transients.
(2) Normal mode operation
(3) Shutdown current includes VGGE1_V28 and VGGE3_V28.
(4) Not Production tested. specified by using the reference EVM.
(5) The margin up to 2.7 V extends to the output voltage if COVGGE2 is changed to 4.7 µF. Specified by using the reference EVM.
(6) Ripple voltage = 0.1 V_{PP}
(7) r[PSCNTGGE2] is a name of register command by serial interface.
(8) VGGE2_V28 LDO is the only functional operation. The electrical characteristics are typical, but not specified.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VGGE3_V28 (LOW DROPOUT OUTPUT)						
$V_{O(VG3)}$	Normal mode output voltage	I_{LOAD} = 10 mA	2.79	2.85	2.92	V
	Low power mode output voltage	I_{LOAD} = 1 mA	2.79	2.85	2.91	
$I_{O(VG3)}$	Normal mode maximum output current				100	mA
	Low power mode maximum output current				2	mA
$V_{O(VG3_ACC)}$	Total output accuracy(1)		–4%		4%	
$I_{CL(VG3)}$	Current limit protection(2)	$V_{(VG3)}$ = 0 V		170	260	mA
$V_{SAT(VG3)}$	Output saturation voltage(2)				0.3	V
$I_{SD(VG3)}$	Shutdown current(3)	VBN5 pin at T_A = 25°C			1	µ A
$I_{Q(VG3)}$	Normal mode quiescent current	VBN5 pin, I_{LOAD} = 0 mA at T_A = 25°C VGGE1_V28, and VGGE2_V28 are off		40	60	µA
	Low power mode quiescent current	VBN5 pin, I_{LOAD} = 0 mA at T_A = 25°C VGGE1_V28, and VGGE2_V28 are off		1.2	3	
$V_{REG(VG3)}$	Line regulation(2)	VBAT = 3.1 V ~ 4.5 V, I_{LOAD} = 100 mA		0.1	0.4	%/V
$I_{REG(VG3)}$	Load regulation(2)(4)	I_{LOAD} = 10 µA to 100 mA		50	100	mV
$I_{TR(VG3)}$	Load transient(2)(4)	I_{LOAD} = 10 µA to 100 mA, I_{TR} = 1 µs		140	170	mV
		I_{LOAD} = 100 mA to 10 µA, I_{TF} = 1 µs		140	230	mV
$PSRR_{(VG3)}$	Power supply ripple rejection(2)(4)(5)	VBAT = 3.8 V, F_{RIPPLE} = 1 kHz, I_{LOAD} = 100 mA		60		dB
		VBAT = 3.8 V, F_{RIPPLE} = 100 kHz, I_{LOAD} = 100 mA		45		dB
$V_{ON(VG3)}$	Output noise(2)(4)	I_{LOAD} = 5 mA, 10 Hz to 100 kHz		30		µVrms
$t_{ST(VG3)}$	Startup time(2)(4)	$V_{O(VG3)}$ > 90%, I_{LOAD} = 10 µA to 100 mA, REG_EN pin = 0 V to VBAT			850	µs
		$V_{O(VG3)}$ > 90%, I_{LOAD} = 10 µA to 100 mA, REG_EN pin = VBAT and r[PSCNTGGE3](6) = 0 to 1			500	
$t_{F(VG3)}$	Output voltage falling time(4)	$V_{O(VG3)}$ < 10%, I_{LOAD} = 0 mA, REG_EN pin = VBAT to 0 V, or REG_EN pin = VBAT and r[PSCNTGGE3] = 1 to 0			5	ms
VBAT UNDERVOLTAGE ELECTRICAL CHARACTERISTICS(7)						
$V_{O(VG3)}$	Normal mode output voltage	3.0 V < VBAT < 3.1		2.85		V
	Low power mode output voltage			2.85		V

(1) Total accuracy includes line and load regulation, temperature and process condition. It does not include load and line transients.
(2) Normal mode operation
(3) Shutdown current includes VGGE1_V28 and VGGE2_V28.
(4) Not production tested. Assured by using the reference EVM.
(5) Ripple voltage = 0.1 V_{PP}
(6) r[PSCNTGGE3] is the name of register command by serial interface.
(7) VGGE3_V28 LDO is the only functional operation. The electrical characteristics are typical, but not specified.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VTCXO (LOW DROPOUT OUTPUT)						
$V_{O(VXO)}$	Output voltage	I_{LOAD} = 5 mA	2.79	2.85	2.92	V
$I_{O(VXO)}$	Maximum output current				20	mA
$V_{O(VXO_ACC)}$	Total output accuracy(1)		–4%		4%	
$I_{CL(VXO)}$	Current limit protection	$V_{O(VXO)}$ = 0 V		30	90	mA
$V_{SAT(VXO)}$	Output saturation voltage				0.3	V
$I_{SD(VXO)}$	Shutdown current	VBN3 pin at T_A = 25°C			1	µA
$I_{Q(VXO)}$	Quiescent current	VBN3 pin, I_{LOAD} = 0 mA at T_A = 25°C		40	60	µA
$V_{REG(VXO)}$	Line regulation	I_{LOAD} = 20 mA		0.1	0.4	%/V
$I_{REG(VXO)}$	Load regulation(2)	I_{LOAD} = 10 µA to 20 mA		50	100	mV
$I_{TR(VXO)}$	Load transient(2)	I_{LOAD} = 10 µA to 20 mA, I_{TR} = 1 µs		100	110	mV
		I_{LOAD} = 20 mA to 10 µA, I_{TF} = 1 µs		100	110	mV
$PSRR_{(VXO)}$	Power supply ripple rejection(2)(3)	VBAT = 3.8 V, F_{RIPPLE} = 1 kHz, I_{LOAD} = 20 mA		60		dB
		VBAT = 3.8 V, F_{RIPPLE} = 100 kHz, I_{LOAD} = 20 mA		45		dB
$V_{ON(VXO)}$	Output noise(2)	I_{LOAD} = 5 mA, 10 Hz to 100 kHz		30		µ Vrms
$t_{ST(VXO)}$	Startup time(2)	$V_{O(VXO)}$ > 90%, I_{LOAD} = 10 µA to 20 mA SYSCLK_EN pin = 0 V to V_{VIO}			400	µs
$t_{F(VXO)}$	Output voltage falling time(2)	$V_{O(VXO)}$ < 10%, I_{LOAD} = 0 mA, SYSCLK_EN pin = V_{VIO} to 0 V			5	ms
VBAT UNDERVOLTAGE ELECTRICAL CHARACTERISTICS(4)						
$V_{O(VXO)}$	Output voltage	3.0 V < VBAT < 3.1		2.85		V
		2.7 V < VBAT < 3.0		VBAT $-V_{SAT(VXO)}$		V

(1) Total accuracy includes line and load regulation, temperature and process condition. It does not include load and line transients.
(2) Not production tested. Specified by using the reference EVM.
(3) Ripple voltage = 0.1 V_{PP}
(4) VTCXO LDO is the only functional operation. The electrical characteristics are typical, but not specified.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PAVREF (D/A CONVERTER)(1)						
	Resolution			8		bit
DNL	Differential non-linearity error(2)		–			LSB
INL	Integral non-linearity error(2)		–			LSB
	Monotony Increase(2)	Specified				
$V_{O(PAVREF)}$	Output voltage	Full scale code digital input, I_{LOAD} = 5 mA	2.85	2.90	2.95	V
		Zero scale code digital input, I_{LOAD} = 5 mA	0.90	0.95	1.0	
		Input code = F8h, I_{LOAD} = 5 mA	2.80	2.85	2.90	
$I_{O(PAVREF)}$	Maximum output current				5	mA
$I_{SD(PAVREF)}$	Shutdown current(3)	VBN1 pin at T_A = 25°C			1	µA
$I_{Q(PAVREF)}$	Quiescent current(4)	VBN1 pin, I_{LOAD} = 0 mA at T_A = 25°C, Default code set		900	1500	µA
$t_{SET(PAVREF)}$	Settling time1(2)	TXONFST pin = V_{VIO}, TXON pin = V_{VIO}, C_L = 130 pF, Zero scale code to full scale code (95%)			5	µs
	Settling time2(2)	TXONFST pin = V_{VIO}, TXON pin = V_{VIO}, C_L = 130 pF, Full scale code to zero scale code (5%)			5	µs
$t_{ST(PAVREF)}$	Startup time	TXONFST pin = V_{VIO} and TXON pin = 0 V to V_{VIO}, Full scale code (95%)			5	µ s
$t_{F(PAVREF)}$	Output voltage falling time	TXON pin = V_{VIO} to 0 V			15	µs
$V_{ON(PAVREF)}$	Output noise(2)	Default code, I_{LOAD} = 0 mA		80		µVrms
$PSRR_{(PAVREF)}$	Power supply ripple rejection(2)(5)	F_{RIPPLE} = 100 Hz, I_{LOAD} = 5 mA, Full scale code		75		dB
$R_{O(PAVREF)}$	Output impedance	TXONFST pin = V_{VIO}, TXON pin = V_{VIO}			20	Ω
$R_{PD(PAVREF)}$	Pull down resistance	TXON pin = 0 V			100	Ω
C_L	Capacitance load				130	pF

(1) Output pin is PAVREF1, PAVREF2 or PAVREF3. Output pin can be selected by TBNDSEL1 and TBNDSE2 pin. More detail is given in PAVREF section.
(2) Not production tested. Specified by using the reference EVM.
(3) REG_EN pin = Low, includes reference block and AFCDAC
(4) Includes power consumption of the reference block.
(5) Ripple voltage = 0.1 V_{PP}

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AFCDAC (D/A CONVERTER)						
	Resolution			12		bit
DNL	Differential non-linearity error(1)		–1		1	LSB
	Monotony increase	Specified				
$V_{O(AFC)}$	Output voltage	Full scale code digital input	2.4	2.45	2.5	V
		Zero scale code digital input	0.2	0.25	0.3	V
		Input code = 80h	1.3	1.35	1.4	V
$I_{SD(AFC)}$	Shutdown current(2)	VBN1 pin at T_A = 25°C			1	µA
$I_{Q(AFC)}$	Quiescent current(3)	VBN1 pin, I_{LOAD} = 0 mA at T_A = 25°C, Default code set		220	260	µA
$t_{SET(AFC)}$	Settling time1(1)	r[PSCNTAFC] (4) = 1 and SYSCLK_EN pin = V_{VIO}, Zero scale code to full scale code (95%) or full scale code to zero scale code (95%) R_L = 100 kΩ, R_S = 1 kΩ, C = 0.01 µF			100	µs
	Settling time2(1)	r[PSCNTAFC] = 1 and SYSCLK_EN pin = V_{VIO}, Zero scale code to full scale code (95%) or full scale code to zero scale code (95%) R_L = 100 kΩ, R_S = 10 kΩ, C= 0.1 µF			3.0	ms
$t_{ST(AFC)}$	Startup time1	r[PSCNTAFC] = 1 and SYSCLK_EN pin = 0V to V_{VIO}, or SYSCLK_EN pin = V_{VIO} and r[PSCNTAFC] = 0 to 1(1), Default scale code (95%) R_L = 100 kΩ, R_S = 1 kΩ, C = 0.01 µF			600	µs
	Startup time2	r[PSCNTAFC] = 1 and SYSCLK_EN pin = 0V to V_{VIO}, or SYSCLK_EN pin = V_{VIO} and r[PSCNTAFC] = 0 to 1(1), Default scale code (95%) R_L = 100 kΩ, R_S = 10 kΩ, C = 0.1 µF			3.5	ms
$R_{O(AFC)}$	Output impedance	r[PSCNTAFC] = 1 and SYSCLK_EN pin =V_{VIO}			20	Ω
R_L	Resistance load		100			kΩ
C_L	Capacitance load				15	pF
VBAT UNDERVOLTAGE ELECTRICAL CHARACTERISTICS(5)						
$V_{O(AFC)}$	Output voltage	2.7 < VBAT < 3.1, Full scale code digital input		2.45		V
		2.7 < VBAT < 3.1, Zero scale code digital input		0.25		
		2.7 < VBAT < 3.1, Input code = 80h		1.35		

(1) Not production tested. Assured by using the reference EVM.
(2) REG_EN pin = Low, includes reference block and PAVREF.
(3) Includes power consumption of the reference block.
(4) r[PSCNTAFC] is the name of a register command by serial interface.
(5) AFC DAC is the only functional operation. The electrical characteristics are typical, but not specified.

ELECTRICAL CHARACTERISTICS

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK DISTRIBUTION						
	Input voltage(1)		0.75	1		V_{PP}
f_{OUT}	Output frequency(2)			26		MHz
$V_{O1(CLKD)}$	Output gain level(2)	SYSCLK_IN pin to SIN_SYSCLK1 pin	–3.5	–3	–2.5	dB
$V_{O2(CLKD)}$		SYSCLK_IN pin to SIN_SYSCLK2 pin	–1.5	–1	–0.5	dB
$V_{O3(CLKD)}$		SYSCLK_IN pin to SIN_SYSCLK3 pin	–1.5	–1	–0.5	dB
$I_{SD(CLKD)}$	Shutdown current	VBN3 pin at T_A = 25°C			1	µA
$I_{Q(CLKD)}$	Quiescent current	VBN3 pin, SIN_SYSCLK1 pin with C_{L1} = 15 pF, R_{L1} = 3 kΩ at T_A = 25°C		2.3	4	mA
		VBN3 pin, SIN_SYSCLK1 pin with C_{L1} = 15 pF, R_{L1} = 3 kΩ and SIN_SYSCLK2 pin with C_{L2} = 10 pF, R_{L2} = 10 kΩ at T_A = 25°C		4.4	6.5	mA
		VBN3 pin, SIN_SYSCLK1 pin with C_{L1} = 15 pF, R_{L1} =3 kΩ and SIN_SYSCLK3 pin with C_{L3} = 10 pF, R_{L3} = 10 kΩ at T_A = 25°C		4.4	6.5	mA
	Duty cycle	SIN_SYSCLK1 pin with C_{L1} = 15 pF, R_{L1} = 3 kΩ	40%		60%	
		SIN_SYSCLK2 pin with C_{L2} = 10 pF, R_{L2} = 10 kΩ SIN_SYSCLK3 pin with C_{L3} = 10 pF, R_{L3} = 10 kΩ	40%		60%	
	Phase noise(1)(3) SIN_SYSCLK1 pin	1 kHz offset with C_{L1} = 15 pF, R_{L1} = 3 kΩ		134		dBc/Hz
		12.5 kHz offset with C_{L1} = 15 pF, R_{L1} = 3 kΩ		146		dBc/Hz
		100 kHz offset with C_{L1} = 15 pF, R_{L1} = 3 kΩ		147		dBc/Hz
	Phase noise(1)(3) SIN_SYSCLK2 pin	1 kHz offset with C_{L2} = 10 pF, R_{L2} = 10 kΩ		135		dBc/Hz
		12.5 kHz offset with C_{L2} = 10 pF, R_{L2} = 10 kΩ		147		dBc/Hz
		100 kHz offset with C_{L2} = 10 pF, R_{L2} = 10 kΩ		149		dBc/Hz
	Phase noise(1)(3) SIN_SYSCLK3 pin	1 kHz offset with C_{L3} = 10 pF, R_{L3} = 10 kΩ		135		dBc/Hz
		12.5 kHz offset with C_{L3} = 10 pF, R_{L3} = 10 kΩ		147		dBc/Hz
		100 kHz offset with C_{L3} = 10 pF, R_{L3} = 10 kΩ		149		dBc/Hz
$t_{ST2(CLKD)}$	Startup time(4)	SIN_SYSCLK2 pin with C_{L2} = 10 pF, R_{L2} = 10 kΩ, SIN_SYSCLK2 pin > 90% of final voltage SYSCLK_EN pin = V_{VIO} and r[PSCNTSYSCLK_GSM](5) = 1 and SYSCLK_EN2 pin = 0V to V_{VIO}, or SYSCLK_EN pin = V_{VIO}, SYSCLK_EN2 pin = V_{VIO} and r[PSCNTSYSCLK_GSM] = 0 to 1 (2)			10	µs
$t_{ST3(CLKD)}$		SIN_SYSCLK3 pin with C_{L3} = 10 pF, R_{L3} = 10 kΩ, SIN_SYSCLK3 pin > 90% of final voltage SYSCLK_EN pin = V_{VIO} and r[PSCNTSYSCLK_UMTS](6) = 1 and WRFON pin = 0V to V_{VIO}, or SYSCLK_EN pin = V_{VIO}, WRFON pin = V_{VIO} and r[PSCNTSYSCLK_UMTS] = 0 to 1(2)			10	µs
R_{IN}	Input impedance(2)	SYSCLK_IN pin		3	4	pF
			14	18	22	kΩ
C_{L1}	Capacitive load	SIN_SYSCKL1 pin			15	pF
C_{L2}		SIN_SYSCKL2 pin			10	pF
C_{L3}		SIN_SYSCKL3 pin			10	pF

(1) Not production tested. Specified by using the reference EVM. Using the external VCTCXO: TCO-5870 [TOYOCOM]
(2) Not production tested. Specified by using the reference EVM.
(3) Buck boost DC/DC converter is OFF
(4) SIN_SYSCLK1 pin startup time depends on the VTCXO LDO startup time.
(5) r[PSCNTSYSCLK_GSM] is a name of register command by serial interface.
(6) r[PSCNTSYSCLK_UMTS] is the name of a register command by serial interface.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{L1}	Resistive load	SIN_SYSCKL1 pin	3			kΩ
R_{L2}		SIN_SYSCKL2 pin	10			kΩ
R_{L3}		SIN_SYSCKL3 pin	10			kΩ
VBAT UNDERVOLTAGE ELECTRICAL CHARACTERISTICS(7)						
f_{OUT}	Output frequency			26		MHz
V_{OG1}	Output voltage gain level	2.7 V < VBAT < 3.1, SYSCLK_IN pin to SIN_SYSCLK1		–3		dB
V_{OG2}		2.7 V < VBAT < 3.1, SYSCLK_IN pin to SIN_SYSCLK2		–1		dB
V_{OG3}		2.7 V < VBAT < 3.1, SYSCLK_IN pin to SIN_SYSCLK3		–1		dB

(7) Clock distribution is the only functional operation. The electrical characteristics are typical, but not specified.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC SIGNAL						
V_{VIO} Input logic (Schmitt trigger input)(1)						
V_{IH}	High-level input voltage		V_{VIO}×0.8		V_{VIO}	V
V_{IL}	Low-level input voltage		0		V_{VIO}×0.2	V
V_{HYS}	Hysteresis range(2)			0.5		V
I_{IH}	High-level input current	Input = V_{VIO}	–1		1	µA
I_{IL}	Low-level input current	Input = 0 V	–1		1	µA
V_{VIO} Input logic (CMOS input)(3)						
V_{IH}	High-level input voltage		V_{VIO}×0.8		V_{VIO}	V
V_{IL}	Low-level input voltage		0		V_{VIO}×0.2	V
I_{IH}	High-level input current	Input = V_{VIO}	–1		1	µA
I_{IL}	Low-level input current	Input = 0 V	–1		1	µA
V_{VIO} Input logic with pull-down resistance (CMOS input)(4)						
V_{IH}	High-level input voltage		V_{VIO}×0.8		V_{VIO}	V
V_{IL}	Low-level input voltage		0		V_{VIO}×0.2	V
R_{PD}	Pull down resistance		70	100	130	kΩ
I_{IH}	High-level input current	Input = V_{VIO}	10	18.5	30	µA
I_{IL}	Low-level input current	Input = 0 V	–1		1	µA
VBAT Input logic (Schmitt trigger input)(5)						
V_{IH}	High-level input voltage		VBAT×0.8		VBAT	V
V_{IL}	Low-level input voltage		0		VBAT×0.2	V
V_{HYS}	Hysteresis range(2)			1		V
I_{IH}	High-level input current	Input = VBAT	–1		1	µA
I_{IL}	Low-level input current	Input = 0 V	–1		1	µA
VIO1V8 Input logic (Schmitt trigger input)(6)						
V_{IH}	High-level input voltage		1.4		V_{VIO}	V
V_{IL}	Low-level input voltage		0		0.3	V
V_{HYS}	Hys range(2)		0.15	0.2	0.28	V
V_{VIO} Output logic(7)						
V_{OH}	High-level output voltage	I_{OUT} = 2 mA	V_{VIO}×0.8		V_{VIO}	V
V_{OL}	Low-level output voltage	I_{OUT} = –2 mA	0		V_{VIO}×0.2	V

(1) CCLK, CDATA, CSTB, TSPCLK, TSPDIN, TSPEN and CRESET pins.
(2) Not production tested. Specified by using the reference EVM.
(3) WRFON, SYSCLK_EN and SYSCLK_EN2 pins
(4) TXON, TXONFST, TBNDSEL1 and TBNDSEL2 pins
(5) REG_EN pin.
(6) VIO1V8 pin. Note that VIO1V8 is supplies as IO buffer voltage supply, but it works as an enable signal in the start up sequence.
(7) EXT_DC_DC_ON_OFF and CDATA(READ Operation) pin

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL INTERFACE TIMING(1)						
CSPI (2)						
t_{cymc}	CCLK cycle time (3)		90			ns
t_{whmc}	CCLK high level time		20			ns
t_{wlmc}	CCLK low level time		20			ns
t_{DS}	CDATA setup time		20			ns
t_{DH}	CDATA hold time		20			ns
t_{SD}	CSTB input delay time		20			ns
t_{whms}	CSTB high level time(3)		1.5×tcycm			ns
t_{PSLH}	CDATA transmission delay time (3) CSTB fall edge to CDATA rise edge	C_{LOAD} = 30 pF			26	ns
t_{PSHL}	CDATA transmission delay time (3) CSTB fall edge to CDATA fall edge	C_{LOAD} = 30 pF			26	ns
t_{PLH}	CDATA transmission delay time CCLK fall edge to CDATA rise edge	C_{LOAD} = 30 pF			26	ns
t_{PHL}	CDATA transmission delay time CCLK fall ledge to CDATA fall edge	C_{LOAD} = 30 pF			26	ns
TSP(4)						
t_{cw}	TSPCLK cycle time(3)		76.9			ns
t_{cwh}	TSPCLK high level time		15			ns
t_{cwl}	TSPCLK low level time		15			ns
t_{su}	TSPDIN setup time		10			ns
t_h	TSPDIN delay time		10			ns
t_{cs}	TSPEN setup time		10			ns
t_{ch}	TSPEN hold time		10			ns
t_{rt}	TSPEN rest time(3)		1×tcw			ns

(1) Internal logic is able to operate between 2.7 V and 3.1 V. But the buck boost DC/DC Converter, PAVREF and V11_V28TX should be OFF. Also V12_V28RX, V13_V28A, V15_V18A, VGGE1_V28, VGGE2_V28 and VGGE3_V28 should be OFF or Low-power mode.
(2) See Figure 88 to show the setup/hold time and pulse width on CSPI interface.
(3) Not Production tested. Specified by using the reference EVM.
(4) See Figure 90 to show the setup/hold time and pulse width on TSP interface.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VREF1, VREF2(1)						
$V_{O(REF1)}$	Output voltage of VREF1 pin	Sub bandgap on, Main bandgap on(2)	1.235	1.242	1.248	V
$V_{O(REF2)}$	Output voltage of VREF2 pin	Sub bandgap on, Main bandgap on(2)	1.235	1.242	1.248	V
		Sub bandgap on , Main bandgap off(3)	1.233	1.246	1.258	V
I_{SD}	Shutdown current(4)	VBN1 pin at T_A = 25°C			1	µA
I_Q	Quiescent current	Sub bandgap on, Main bandgap on(2), VBN1 pin at T_A = 25°C		53	87	µA
		Sub bandgap on, Main bandgap off(3), VBN1 pin at T_A = 25°C		17	42	µA
$t_{ST(REF1)}$	Startup time	REG_EN pin = 0V to VBAT(5), C_{OVREF1} = 0.01 µF		150	250	µs
		Power up from low power mode to normal mode or r[PSCNTDC/DC] = 0 to 1(6), C_{OVREF1} = 0.01 µF		60	160	µs
$t_{ST(REF2)}$		REG_EN pin = 0V to VBAT(5), C_{OVREF2} = 0.1 µF		200	350	µs
VBAT UNDERVOLTAGE ELECTRICAL CHARACTERISTICS (2.7 V < VBAT < 3.1 V)						
$V_{O(REF1)}$	Output voltage of VREF1 pin	Sub bandgap on , Main bandgap on(2)		1.242		V
$V_{O(REF2)}$	Output voltage of VREF2 pin	Sub bandgap on , Main bandgap on(2)		1.242		V
		Sub bandgap on , Main bandgap off(3)		1.246		V
$t_{ST(REF1)}$	Startup time	REG_EN pin = 0V to VBAT(5), C_{OVREF1} = 0.01 µF			300	µs
		Power up from Low Power Mode to Normal Mode or r[PSCNTDC/DC] = 0 to 1(6), C_{OVREF1} = 0.01 µF			200	µs
$t_{ST(REF2)}$		REG_EN pin = 0V to VBAT(5), C_{OVREF2} = 0.1 µF			450	µs
THERMAL SHUTDOWN(7)						
THD	Shutdown temperature	Increasing junction temperature	145	160	175	°C
THD_{rel}	Releasing temperature	Decreasing junction temperature	135	150	165	°C
THD_{HYS}	Temperature hysteresis			10		°C
HOT DIE DETECTION(7)						
HDD1	Hot-die detection1		95	110	125	°C
HDD2	Hot-die detection2		105	120	135	°C
HDD3	Hot-die detection3		115	130	145	°C
HDD4	Hot-die detection4		125	140	155	°C
HDD5	Hot-die detection5		135	150	165	°C
HDD_{HYS}	Temperature hysteresis			10		°C

(1) VREF1 pin and VREF2 pin must not connect to other devices.
(2) Some block is powered up by a register command which is written from serial interface, or SYSCLK_EN pin, or TXONFST pin is VVIO. If r[PSCNTDC/DC]=0, VREF1 pin is 0 V. More detail is provided in the VREF1, VREF2 Section.
(3) All blocks are powered down by register commands which are written from serial interface and SYSCLK_EN, TXONFST and TXON pins are 0V. Or V12_V28RX, V13_V28A, V15_V18A, VGGE1_V28, VGGE2_V28 and VGGE3_V28 are Low Power Mode, and other blocks are powered down by register command which is written from serial interface and SYSCLK_EN, TXONFST and TXON pins are 0V. More detail is given in the VREF1, VREF2 Section.
(4) REG_EN pin = Low, include PAVREF and AFCDAC
(5) Power up sequence by starting from REG_EN pin = 0 V to VBAT. More detail is given in the VREF1, VREF2 Section.
(6) When the Low Power Mode or r[PSCNTDC/DC] = 0, VREF1 pin is powered down. More detail is given in VREF1, VREF2 Section. The start up of the r[PSCNTDC/DC] control is not production tested.
(7) Not production tested. Specified by using the reference EVM.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended input conditions, T_A = –30°C to 85°C, typical values are VBAT = 3.8 V, VIO1V8 = 1.85 V at T_A = 25°C (unless otherwise noted)

QUIESCENT CURRENT												
		TEST CONDITIONS							MIN	TYP	MAX	UNIT
		REG_EN	VIO1V8	WRFON	SYSCLK_EN	SYSCLK_EN2	TXONFST	TXON				
IOFF	OFF Mode, TA = 25°C	Low	Low	Low	Low	Low	Low	Low		1	2	µA
ILPM	Low Power Mode, TA = 25°C	Hi	Hi	Low	Low	Low	Low	Low		30	40	µA
I2G	2G Mode	Hi	Hi	Low	Hi	Hi	Low	Low		5	8	mA
I3G	3G Mode	Hi	Hi	Hi	Hi	Low	Hi	Hi		14	18	mA
INC	No communication mode	Hi	Hi	Low	Hi	Low	Low	Low		3	6	mA

BLOCK CONDITION FOR EACH MODE																
	VOUT(BKBT DCDC)	PAVREF	V11_V28TX	V12_V28RX	V13_V28A	V15_V18A	VGGE1_V28	VGGE2_V28	VGGE3_VE8	VTCXO	AFC	SIN_SYSCLK1	SIN_SYSCLK2	SIN_SYSCLK3	SERIAL I/F	TSD/HDD
OFF Mode	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Power Up Mode	OFF	OFF	OFF	LPM	LPM	LPM	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	ON
Low Power Mode	OFF	OFF	OFF	LPM	LPM	LPM	LPM	LPM	LPM	OFF	OFF	OFF	OFF	OFF	ON	ON
2G Mode	OFF	OFF	OFF	LPM	LPM	LPM	ON	ON	ON	ON	ON	ON	ON	OFF	ON	ON
3G Mode	ON	ON	ON	ON	ON	ON	LPM	LPM	LPM	ON	ON	ON	OFF	ON	ON	ON
No communication Mode	OFF	OFF	OFF	LPM	LPM	LPM	LPM	LPM	LPM	ON	ON	ON	OFF	OFF	ON	ON

PIN ASSIGNMENT

(BOTTOM VIEW)

	1	2	3	4	5	6	7	8	9
J	NC	VTCXO	AFC	SYSCLK_IN	SIN_SYSCLK1	SIN_SYSCLK2	SIN_SYSCLK3	VBN5	NC
H	VBN3	NC	GND3	GND6	TBNDSEL 2	GND2	GND5	TSPEN	VGGE1 _V28
G	V11_ V28TX	GND4	TXONFST	TBNDSEL1	NC	TSPDIN	CSTB	CCLK	VGGE2 _V28
F	VBN4	PA_VDD	TXON				CDATA	VBN2	VGGE3 _V28
E	V12_ V28RX	V_LNA_ FEM	REG_EN				TSPCLK	DDGNDA	VIO1V8
D	V13_ V28A	VREF2	SYSCLK _EN2				TEST	VREF1	DDINA
C	GND1	V15_V18A		CRESET	EXT_DC_DC_O N _OFF	SYSCLK _EN	VEEPROM	ERR	PABIAS1
B	PAVREF3	VBN1	WRFON	VBDDP	L1	DDGNDP	L2	VOUT	PA_FB
A	NC	PAVREF2	PAVREF1	VBDDP	L1	DDGNDP	L2	VOUT	NC

TERMINAL FUNCTIONS

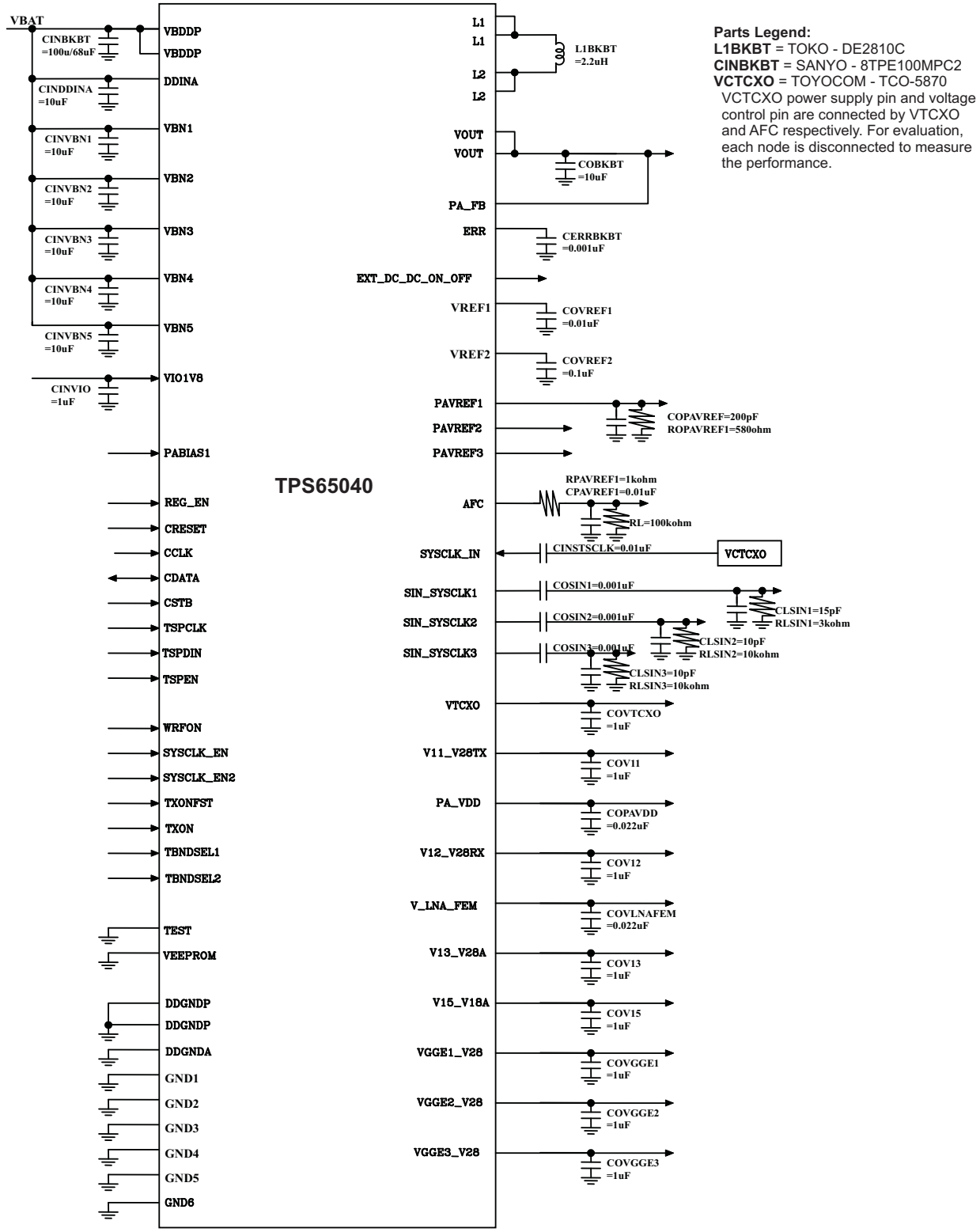
TERMINAL NO.	TERMINAL PIN ADDRESS	NAME[1]	I/O	DESCRIPTION
1	B3	WRFON	I	V12_V28RX, V13_V28A and V15_V18A mode control input V11_V28TX, PA_VDD, V_LNA_FEM and SIN_SYSCLK3 enable input
2	C6	SYSCLK_EN	I	VTCXO, AFCDAC, CLOCK DISTRIBUTION enable input
3	B1	PAVREF3	O	PAVREF output3
4	B2	VBN1	I	Power supply of VREF1/VREF2, PAVREF and AFCDAC
5	D3	SYSCLK_EN2	I	VGGE1_V28, VGGE2_V28, VGGE3_V28 mode control input SIN_SYSCLK2 enable input
6	C1	GND1	I	GND of VREF1/VREF2, PAVREF and AFCDAC
7	C2	V15_V18A	O	V15_V18A LDO output
8	D1	V13_V28A	O	V13_V28A LDO output
9	D2	VREF2	O	Bandgap buffer output
10	E2	V_LNA_FEM	O	Output through MOS switch from V12_V28RX LDO
11	E1	V12_V28RX	O	V12_V28RX LDO output
12	F1	VBN4	I	Power supply of V11_V28TX, V12_V28RX, V13_V28A and V15_V18A
13	G1	V11_V28TX	O	V11_V28TX LDO output
14	F2	PA_VDD	O	Output through MOS switch from V11_V28TX LDO
15	G2	GND4	I	GND of V11_V28TX, V12_V28RX, V13_V28A and V15_V18A
16	H1	VBN3	I	Power supply of VTCXO
17	H2	NC	–	No connection (recommended to be GND)
18	J2	VTCXO	O	VTCXO LDO output
19	G3	TXONFST	I	Buck boost DC/DC converter and PAVREF enable input
20	H3	GND3	I	GND of VTCXO
21	J3	AFC	O	AFCDAC output
22	F3	TXON	I	PAVREF output buffer enable input
23	E3	REG_EN	I	Enable input
24	J4	SYSCLK_IN	I	Clock input
25	H4	GND6	I	GND of CLOCK DISTRIBUTION
26	J5	SIN_SYSCLK1	O	Clock output1 of CLOCK DISTRIBUTION
27	H5	TBNDSEL2	I	PAVREF switch select 2
28	J6	SIN_SYSCLK2	O	Clock output2 of CLOCK DISTRIBUTION

(1) GND1, GND2, GND3, GND4, GND5 and DDGNDA are internally connected. GND6 and DDGNDP are separated from these ground pins. VBN1, VBN2, VBN3, VBN4, VBN5 and DDINA are separated each other.

TERMINAL FUNCTIONS (continued)

TERMINAL		NAME[1]	I/O	DESCRIPTION
NO.	PIN ADDRESS			
29	G4	TBNDSEL1	I	PAVREF switch select 1
30	H6	GND2	I	GND of SERIAL INTERFACE, EEPROM and logic
31	J7	SIN_SYSCLK3	O	Clock output3 of CLOCK DISTRIBUTION
32	H7	GND5	I	GND of VGGE1_V28, VGGE2_V28, VGGE3_V28
33	J8	VBN5	I	Power supply of VGGE1_V28, VGGE2_V28, VGGE3_V28
34	H8	TSPEN	I	TSP enable input
35	G6	TSPDIN	I	TSP data input
36	H9	VGGE1_V28	O	VGGE1_V28 LDO output
37	G7	CSTB	I	CSPI strobe input
38	G9	VGGE2_V28	O	VGGE2_V28 LDO output
39	G8	CCLK	I	CSPI clock input
40	F7	CDATA	IO	CSPI data input/output
41	F9	VGGE3_V28	O	VGGE3_V28 LDO output
42	F8	VBN2	I	Power supply of SERIAL INTERFACE, EEPROM and logic
43	E7	TSPCLK	I	TSP clock input
44	E9	VIO1V8	I	Power supply of IO buffer and enable input
45	E8	DDGNDA	I	GND of buck boost DC/DC CONVERTER analog
46	D9	DDINA	I	Power supply of buck boost DC/DC CONVERTER analog
47	D8	VREF1	O	Bandgap buffer output for buck boost DC/DC CONVERTER
48	C8	ERR	IO	Buck boost DC/DC converter phase compensation terminal
49	C9	PABIAS1	I	Buck boost DC/DC converter output voltage control input
50	D7	TEST	O	Test mode output (recommended to be GND)
51	C7	VEEPROM	I	Power supply of EEPROM write mode (recommended to be GND)
52	B9	PA_FB	I	Buck boost DC/DC converter output voltage feed back input
53	B8(=A8)	VOUT	O	Buck boost DC/DC converter output (same pin as NO54. A8)
54	A8(=B8)	VOUT	O	Buck boost DC/DC converter output (same pin as NO53. B8)
55	B7(=A7)	L2	IO	VOUT side pin of coil (same as NO56. A7)
56	A7(=B7)	L2	IO	VOUT side pin of coil (same as NO55. B7)
57	B6(=A6)	DDGNDP	I	Power GND of buck boost DC/DC CONVERTER (same as NO58. A6)
58	A6(=B6)	DDGNDP	I	Power GND of buck boost DC/DC CONVERTER (same as NO57. B6)
59	B5(=A5)	L1	IO	VBDDP side pin of coil (same as NO60. A5)
60	A5(=B5)	L1	IO	VBDDP side pin of coil (same as NO59. B5)
61	B4(=A4)	VBDDP	I	Power supply of buck boost DC/DC converter (same as NO62. A4)
62	A4(=B4)	VBDDP	I	Power supply of buck boost DC/DC converter (same as NO61. B4)
63	C4	CRESET	I	SERIAL INTERFACE reset input
64	A3	PAVREF1	O	PAVREF output1
65	C5	EXT_DC_DC_ON_OFF	O	Logic output
66	A2	PAVREF2	O	PAVREF output2
67	G5	NC	–	No connection (recommended to be GND)
68	A1	NC	–	No connection (recommended to be GND)
69	A9	NC	–	No connection (recommended to be GND)
70	J1	NC	–	No connection (recommended to be GND)
71	J9	NC	–	No connection (recommended to be GND)

TYPICAL CHARACTERISTICS MEASUREMENT CIRCUIT



Parts Legend:
L1BKBT = TOKO - DE2810C
CINBKBT = SANYO - 8TPE100MPC2
VCTCXO = TOYOCOM - TCO-5870
VCTCXO power supply pin and voltage control pin are connected by VTCXO and AFC respectively. For evaluation, each node is disconnected to measure the performance.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
BUCK BOOST DCDC CONVERTER	EFFICIENCY	vs OUTPUT CURRENT (VOUT = 0.8 V)	1
		vs OUTPUT CURRENT (VOUT = 2.5 V)	2
		vs OUTPUT CURRENT (VOUT = 3.5 V)	3
		vs OUTPUT CURRENT (VOUT = 4.2 V)	4
	WAVEFORMS	OUTPUT VOLTAGE SETTLING TIME	5
		OUTPUT VOLTAGE SETTLING TIME	6
		LOAD TRANSIENT	7
		SOFTSTARTS	8
	OSCILLATOR	SWITCHING FREQUENCY	9
V11_V28TXV	OUTPUT VOLTAGE	LINE REGULATION	10
		LOAD REGULATION	11
		CURRENT LIMIT	12
	WAVEFORMS	LOAD TRANSIENT	13
		LOAD TRANSIENT	14
		LOAD TRANSIENT	15
	RIPPLE REJECTION	PSRR	16
PA_VDD	OUTPUT VOLTAGE	LOAD REGULATION	17
	WAVEFORMS	STARTUP TIME	18
		FALLING TIME	19
VGGE1_V28TX	OUTPUT VOLTAGE	LINE REGULATION	20
		LOAD REGULATION	21
		CURRENT LIMIT	22
	WAVEFORMS	LOAD TRANSIENT	23
		LOAD TRANSIENT	24
		LOAD TRANSIENT	25
	RIPPLE REJECTION	PSRR	26
PAVREF	WAVEFORMS	PAVREF1 SETTLING TIME	27
		PAVREF1 FALLING TIME	28
		PAVREF1 STARTUP TIME	29
		PAVREF1 FALLING TIME	30
	RIPPLE REJECTION	PSRR	31
	LINEARITY	DNL	32
		INL	33
AFCDAC	WAVEFORMS	SETTLING TIME	34
		FALLING TIME	35
		STARTUP TIME	36
	LINEARITY	DNL	37

TYPICAL CHARACTERISTICS (continued)

			FIGURE
CLOCK DISTRIBUTION	WAVEFORMS	SIN_SYSCLK1 STARTUP TIME	38
		SIN_SYSCLK1 INPUT vs OUTPUT	39
		SIN_SYSCLK2 STARTUP TIME	40
		SIN_SYSCLK2 INPUT vs OUTPUT	41
		SIN_SYSCLK3 STARTUP TIME	42
		SIN_SYSCLK3 INPUT vs OUTPUT	43
	PHASE NOISE	SYSCLK_IN (VCTCXO output) Reference PHASE NOISE	44
		SIN_SYSCLK1 PHASE NOISE	45
		SIN_SYSCLK2 PHASE NOISE	46
		SIN_SYSCLK3 PHASE NOISE	47

BUCK BOOST/EFFICIENCY vs OUTPUT CURRENT

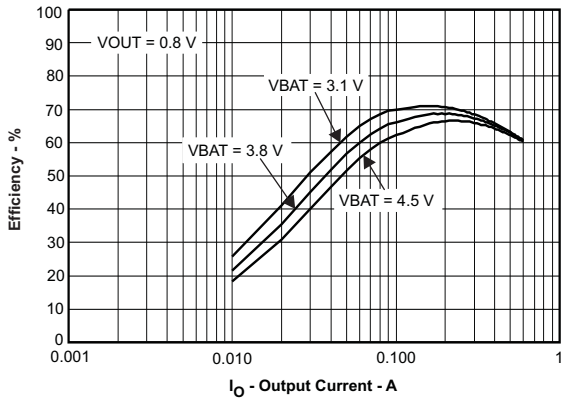


Figure 1.

BUCK BOOST/EFFICIENCY vs OUTPUT CURRENT

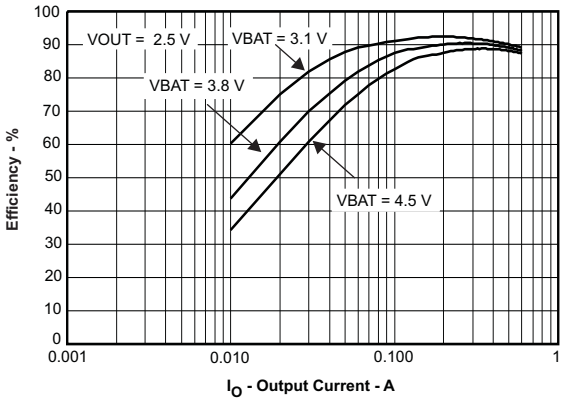


Figure 2.

BUCK BOOST/EFFICIENCY vs OUTPUT CURRENT

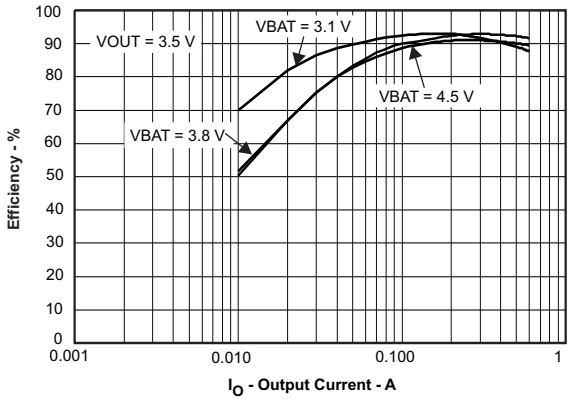


Figure 3.

BUCK BOOST/EFFICIENCY vs OUTPUT CURRENT

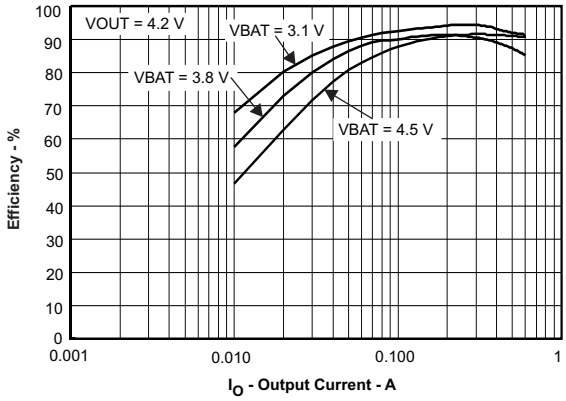


Figure 4.

BUCK BOOST/OUTPUT VOLTAGE SETTLING TIME

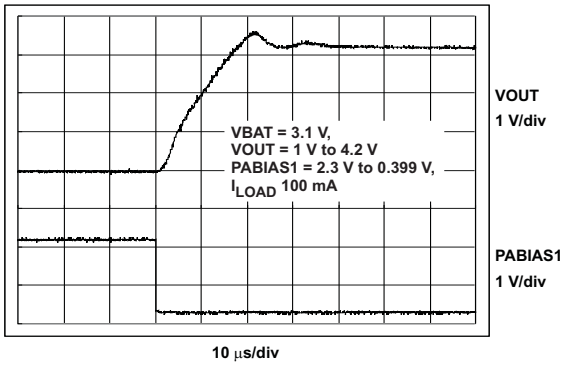


Figure 5.

BUCK BOOST/OUTPUT VOLTAGE SETTLING TIME

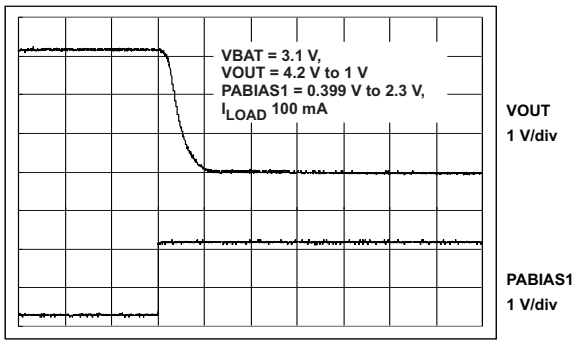


Figure 6.

BUCK BOOST/LOAD TRANSIENT

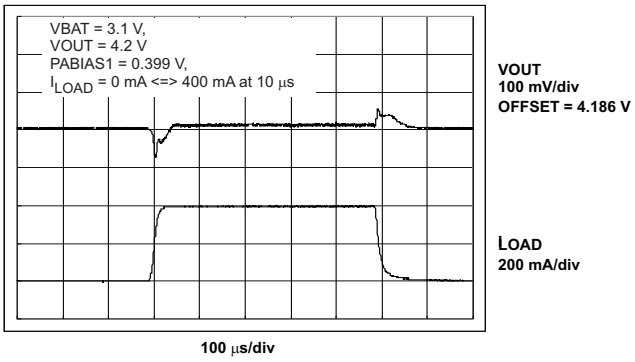


Figure 7.

BUCK BOOST/SOFTSTART

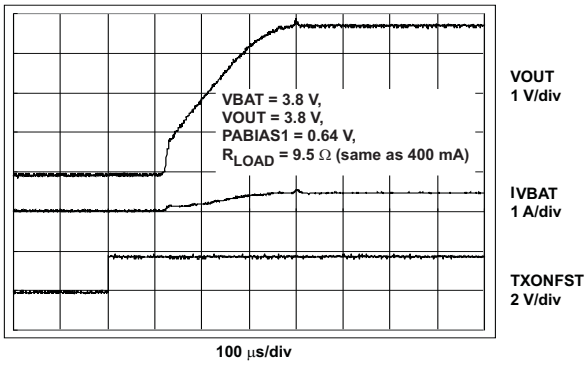


Figure 8.

BUCK BOOST/SWITCHING FREQUENCY

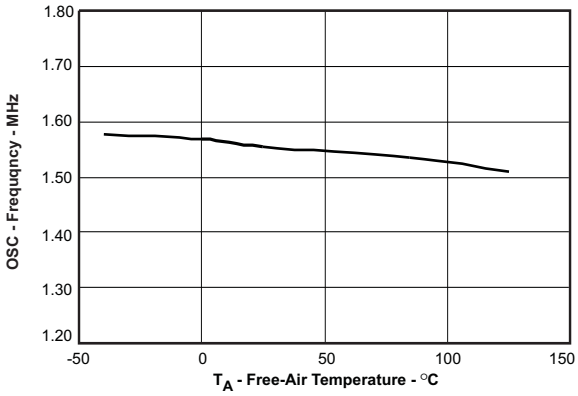


Figure 9.

V11_V28TX/LINE REGULATION

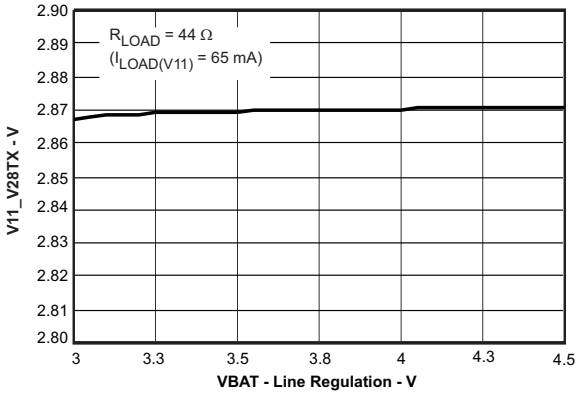


Figure 10.

V11_V28TX/LOAD REGULATION

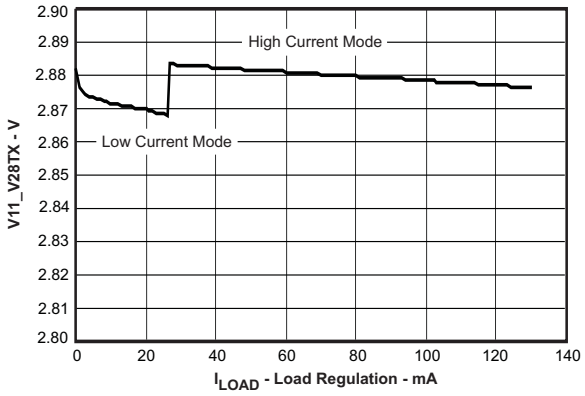


Figure 11.

V11_V28TX/CURRENT LIMIT

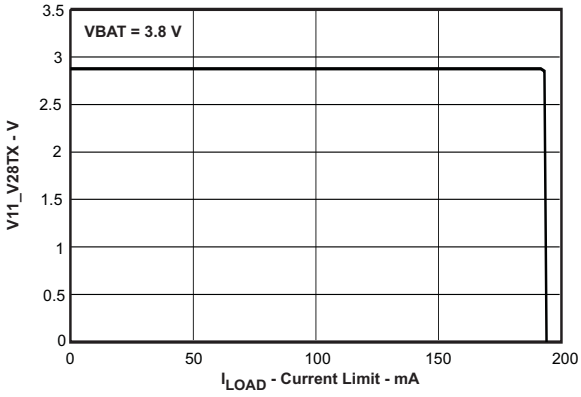


Figure 12.

V11_V28TX/LOAD TRANSIENT

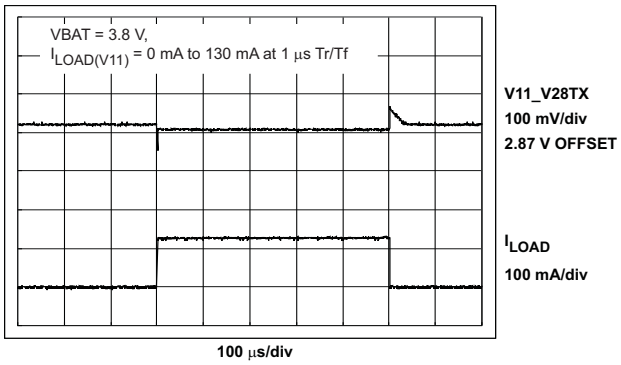


Figure 13.

V11_V28TX/LOAD TRANSIENT (CONTINUED)

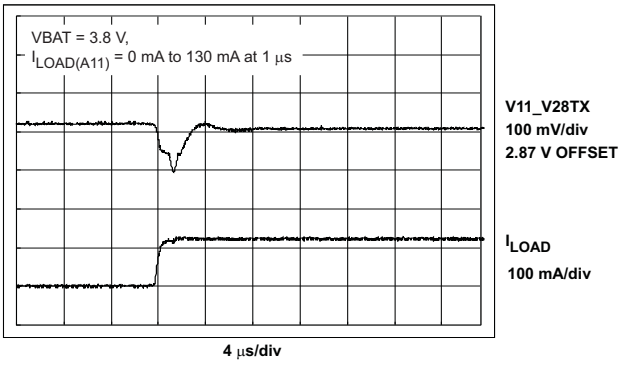


Figure 14.

V11_V28TX/LOAD TRANSIENT (CONTINUED)

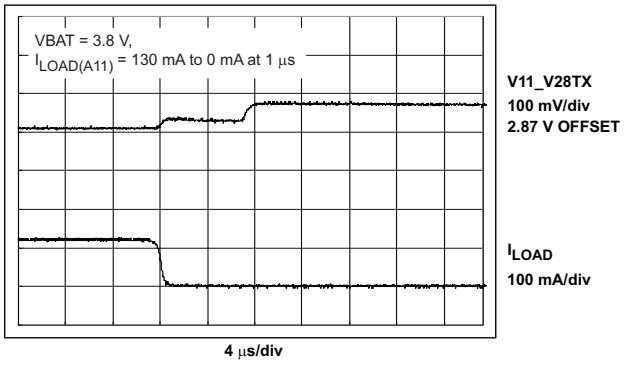


Figure 15.

V11_V28TX/PSRR

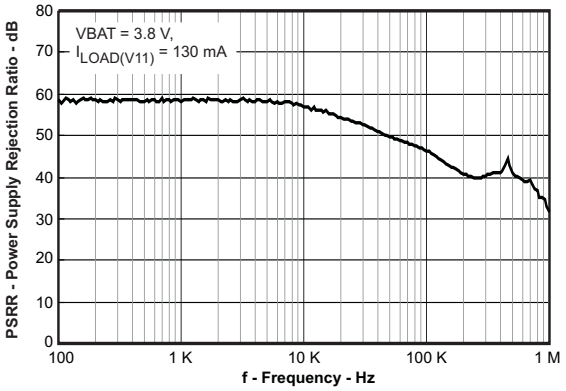


Figure 16.

PA_VDD/LOAD REGULATION

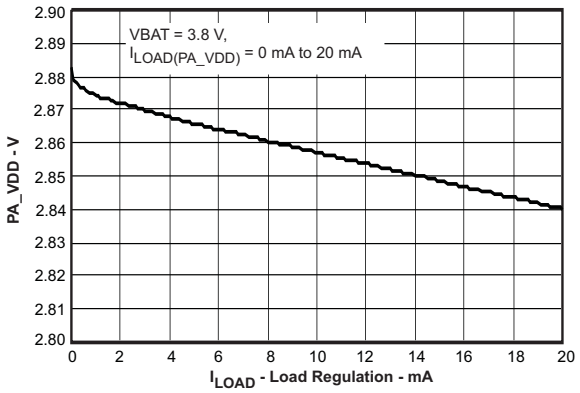


Figure 17.

PA_VDD/STARTUP TIME

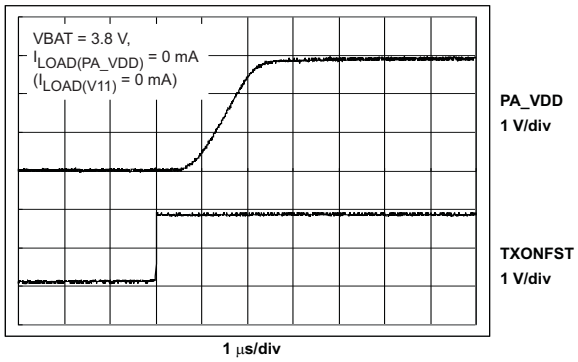


Figure 18.

PA_VDD/FALLING TIME

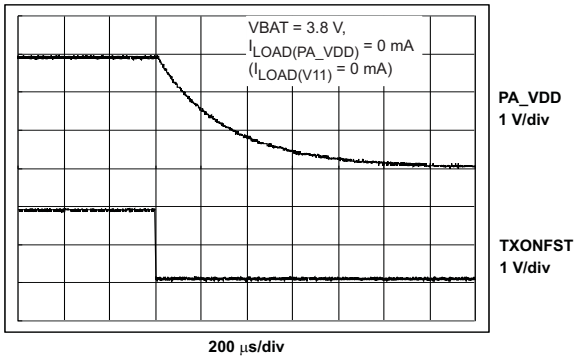


Figure 19.

VGGE1_V28A/LINE REGULATION

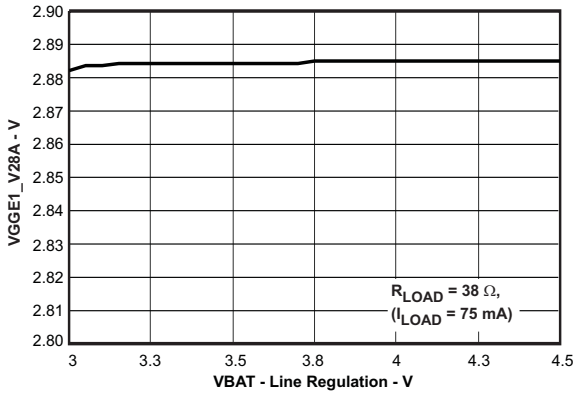


Figure 20.

VGGE1_V28A/LOAD REGULATION

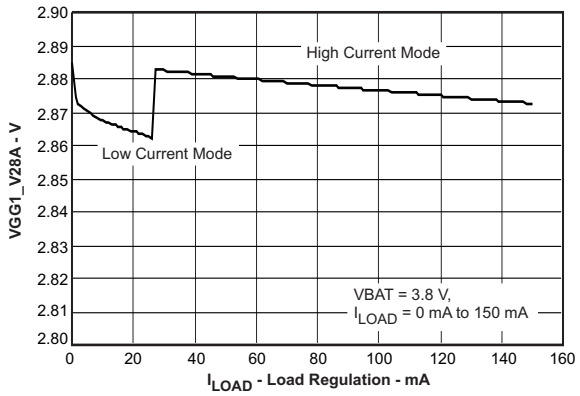


Figure 21.

VGGE1_V28A/CURRENT LIMIT

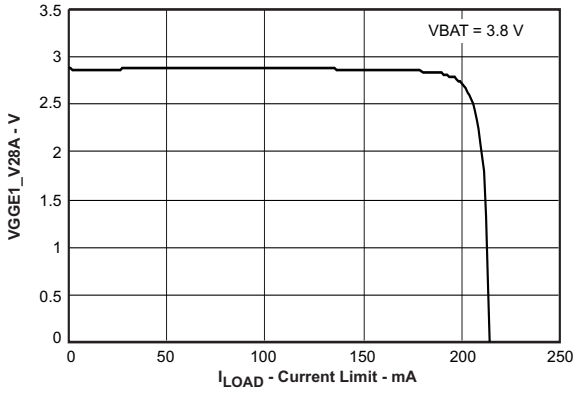


Figure 22.

VGGE1_V28A/LOAD TRANSIENT

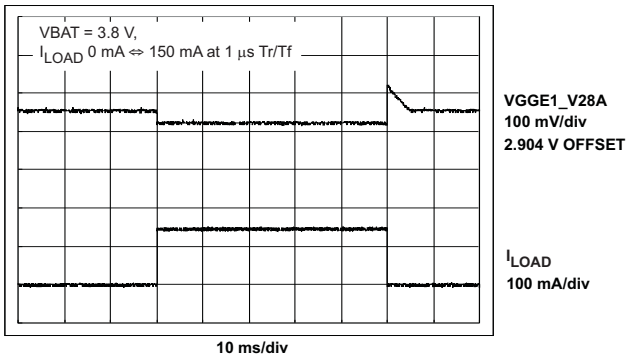


Figure 23.

VGGE1_V28A/LOAD TRANSIENT (CONTINUED)

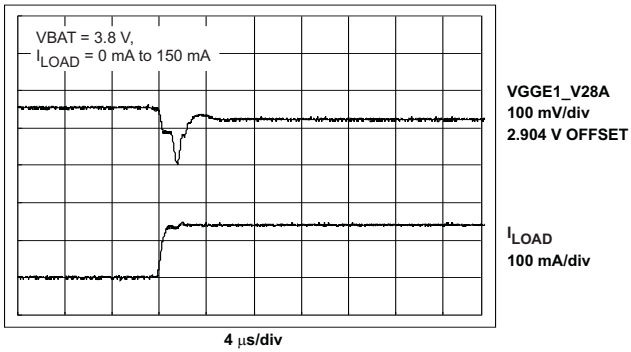


Figure 24.

VGGE1_V28A/LOAD TRANSIENT (CONTINUED)

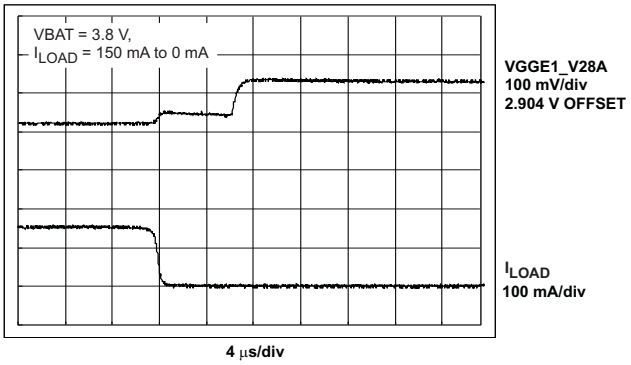


Figure 25.

VGGE1_V28A/PSRR

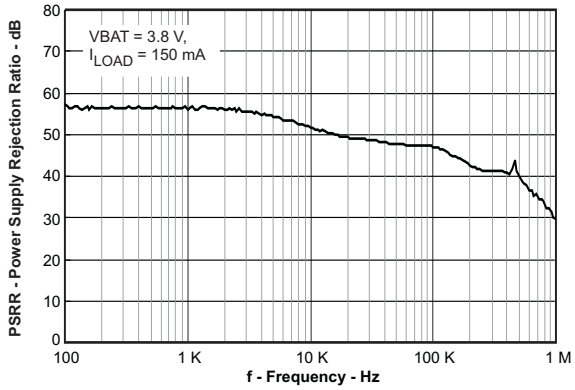


Figure 26.

PAVREF1/SETTLING TIME

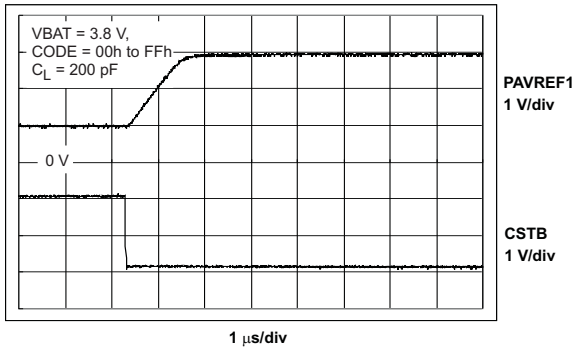


Figure 27.

PAVREF1/SETTLING TIME (CONTINUED)

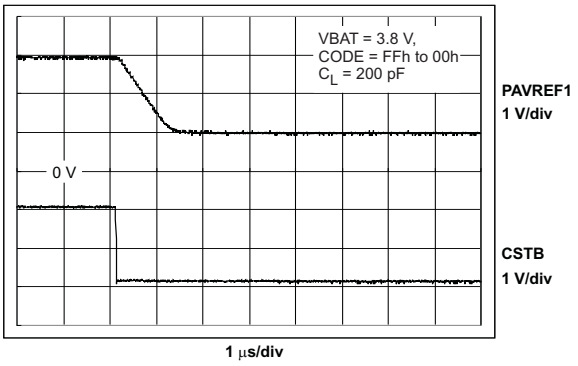


Figure 28.

PAVREF1/STARTUP TIME

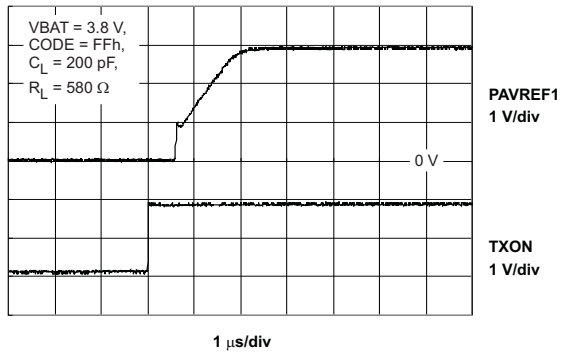


Figure 29.

PAVREF1/FALLING TIME

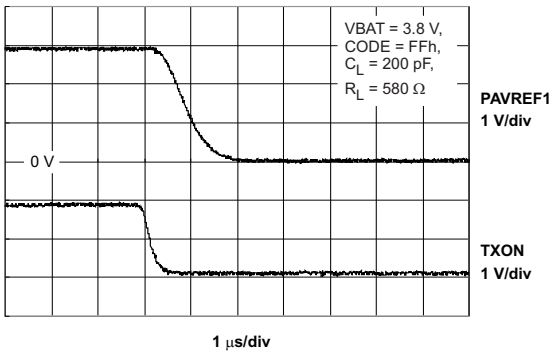


Figure 30.

PAVREF1/PSRR

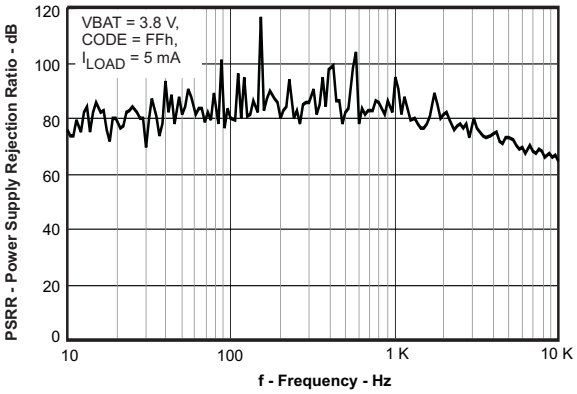


Figure 31.

PAVREF1/DNL

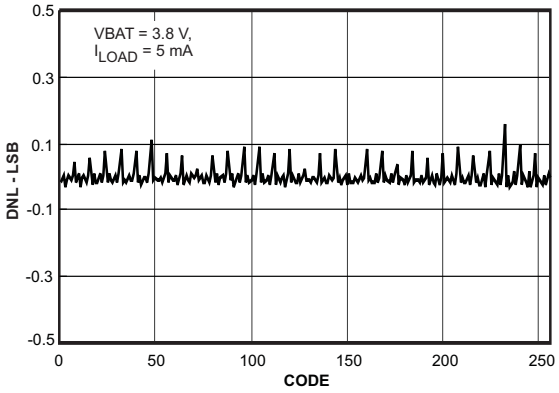


Figure 32.

PAVREF1/INL

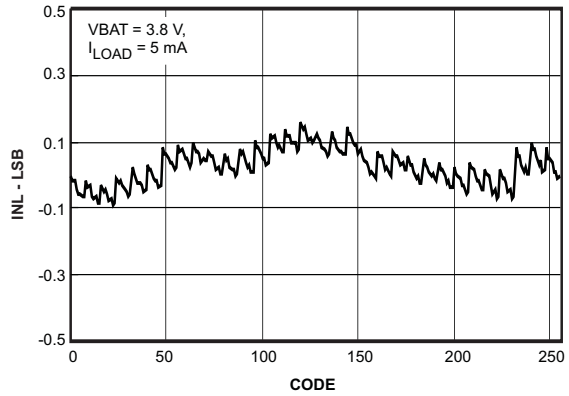


Figure 33.

AFCDAC/SETTLING TIME

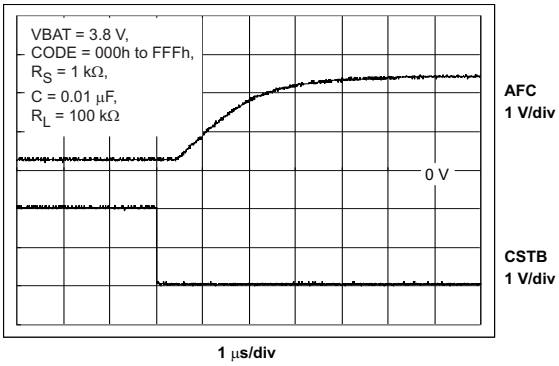


Figure 34.

AFCDAC/FALLING TIME

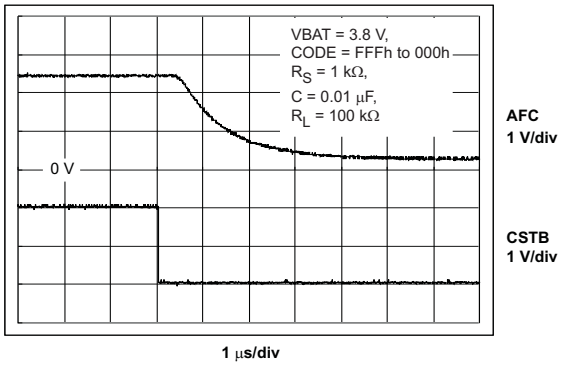


Figure 35.

AFCDAC/STARTUP TIME

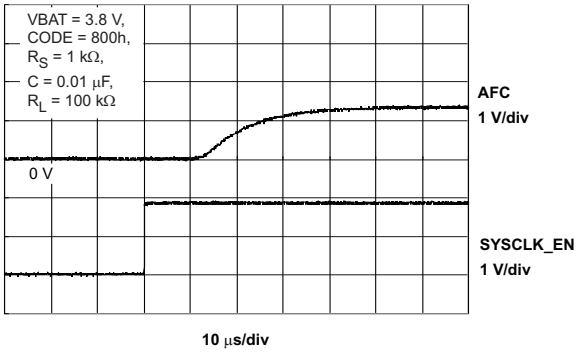


Figure 36.

AFCDAC/DNL

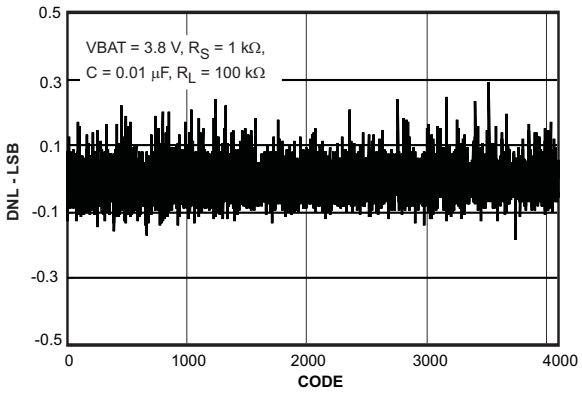


Figure 37.

CLOCK DISTRIBUTION/SIN_SYSCLK1 STARTUP TIME

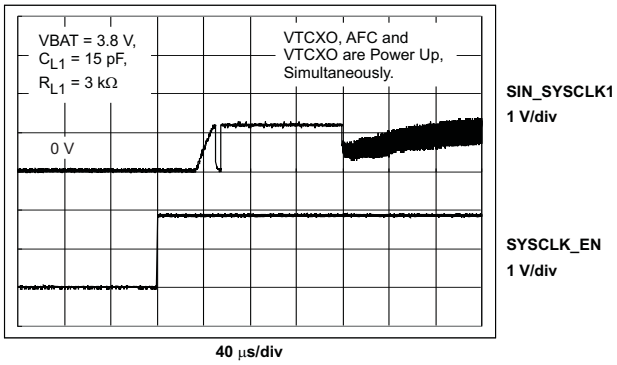


Figure 38.

CLOCK DISTRIBUTION/SIN_SYSCLK1 INPUT vs OUTPUT (–3 dB TYP)

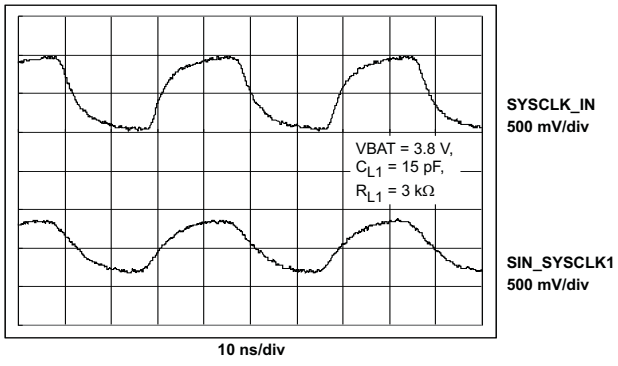


Figure 39.

CLOCK DISTRIBUTION/SIN_SYSCLK2 STARTUP TIME

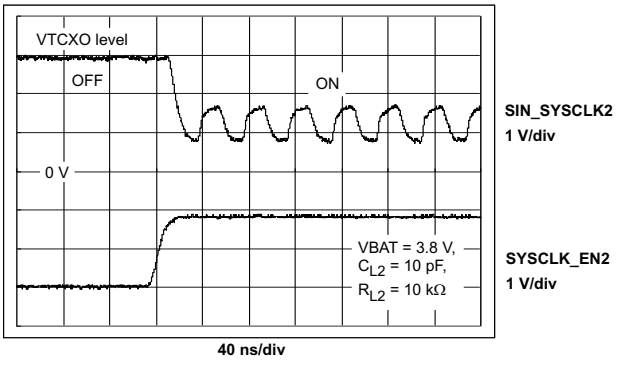


Figure 40.

CLOCK DISTRIBUTION/SIN_SYSCLK2 INPUT VS OUTPUT (–1 dB TYP)

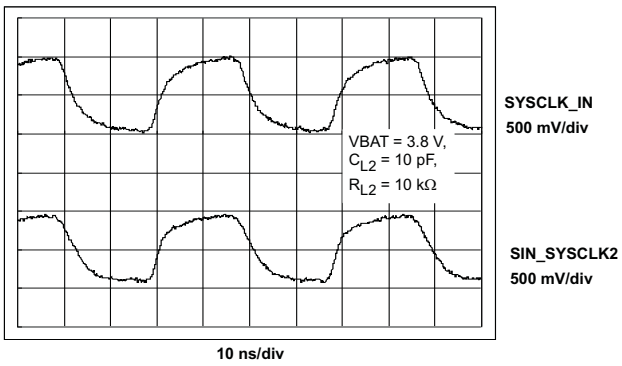


Figure 41.

CLOCK DISTRIBUTION/SIN_SYSCLK3 STARTUP TIME

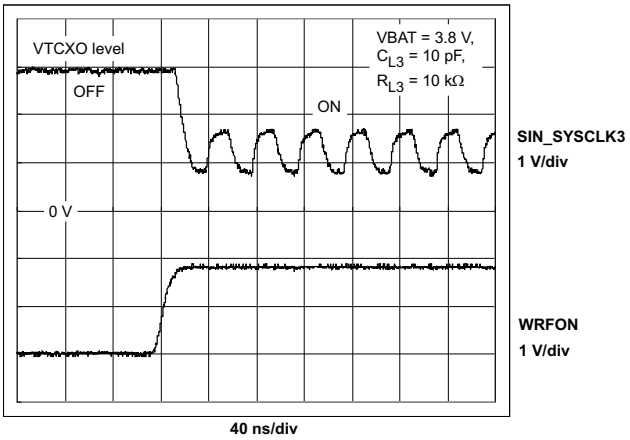


Figure 42.

CLOCK DISTRIBUTION/SIN_SYSCLK3 INPUT VS OUTPUT (–1 dB TYP)

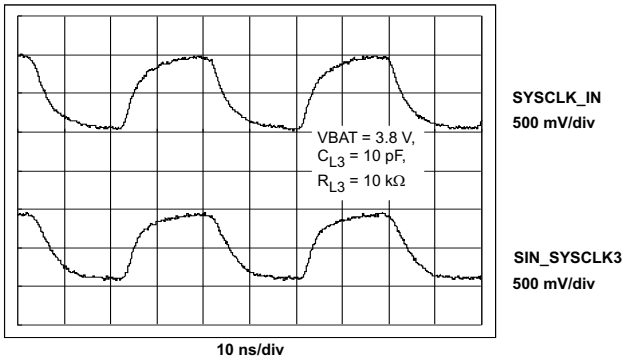


Figure 43.

SYSCLK_IN (VCTCXO OUTPUT) INPUT PHASE NOISE

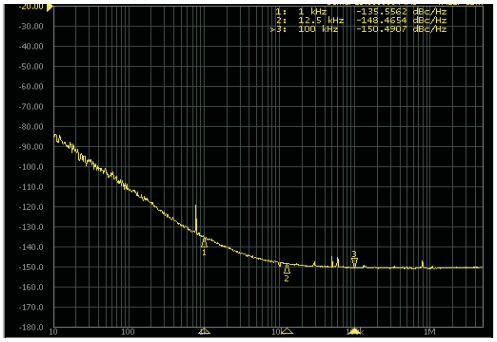


Figure 44.

CLOCK DISTRIBUTION/SIN_SYSCLK1 OUTPUT PHASE NOISE

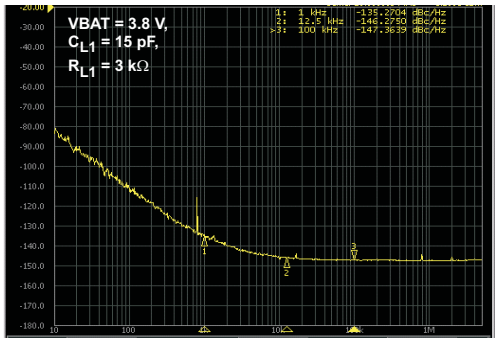


Figure 45.

CLOCK DISTRIBUTION/SIN_SYSCLK2 OUTPUT PHASE NOISE

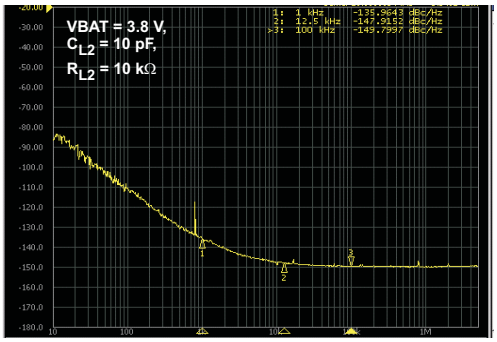


Figure 46.

CLOCK DISTRIBUTION/SIN_SYSCLK3 OUTPUT PHASE NOISE

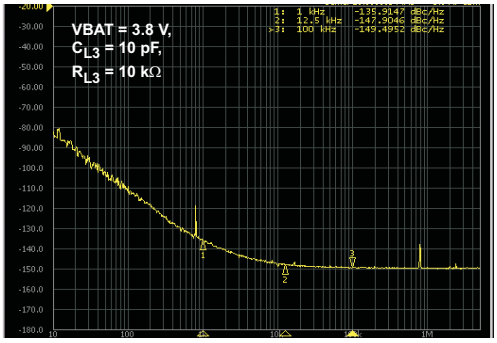


Figure 47.

PARAMETER MEASUREMENT INFORMATION

EQUIVALENT INPUT/OUTPUT CIRCUIT DIAGRAMS

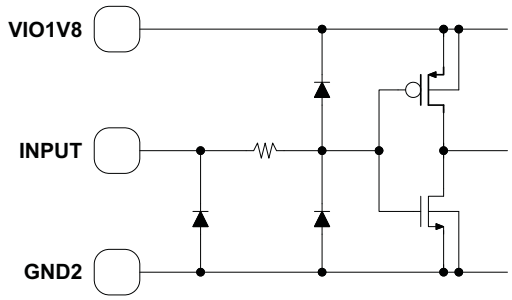


Figure 48. WRFON, SYSCLK_EN, SYSCLK_EN2

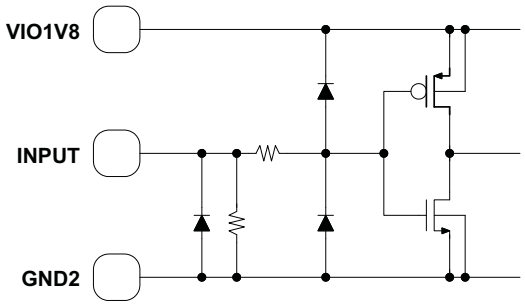


Figure 49. TXONFST, TXON, TBNDSEL2, TBNDSEL1

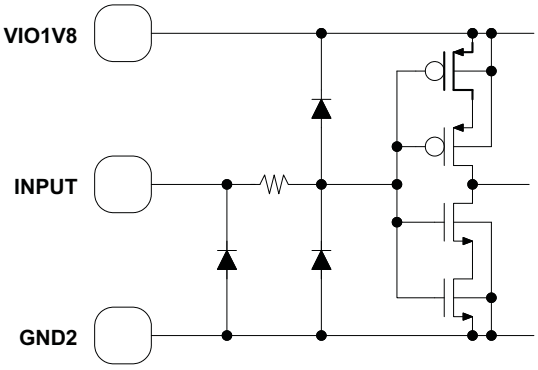


Figure 50. TSPCLK, TSPDIN, TSPEN, CCLK, CSTB, CRESET

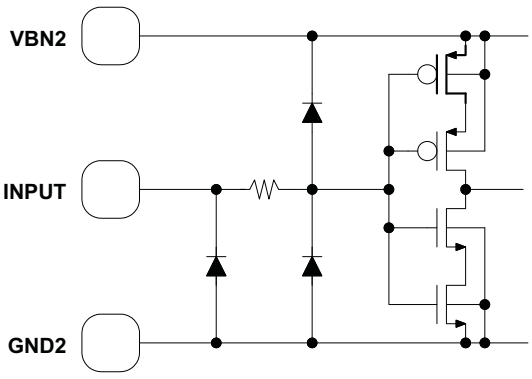


Figure 51. REG_EN

PARAMETER MEASUREMENT INFORMATION (continued)

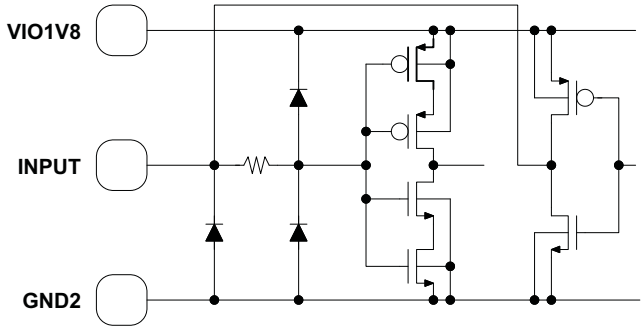


Figure 52. CDATA

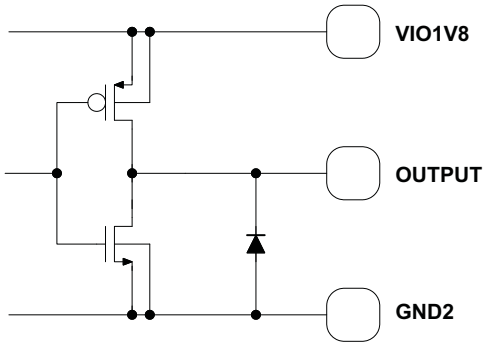


Figure 53. EXT_DC_DC_ON_OFF

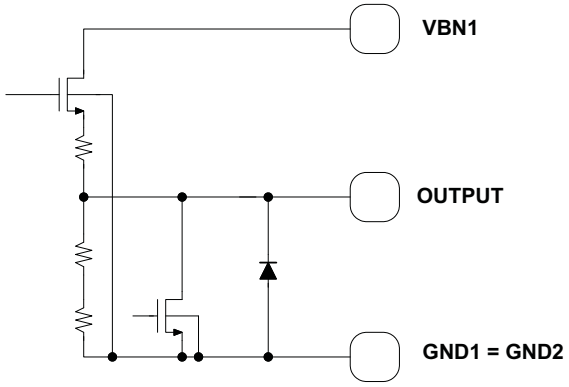


Figure 54. VREF1/VREF2

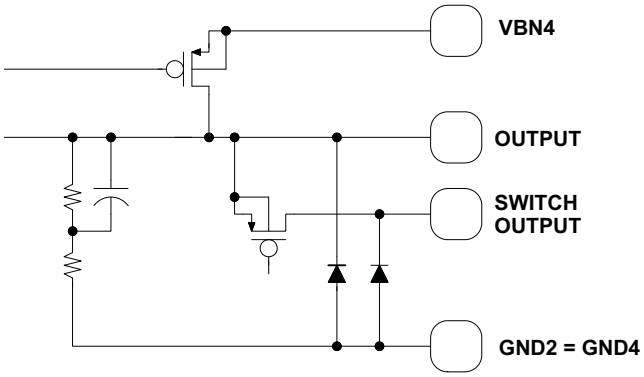


Figure 55. V11_V28TX, V12_V28RX, PA_VDD, L_LNA_FEM

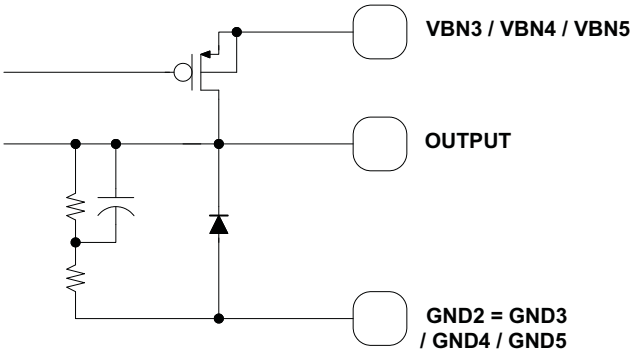


Figure 56. V13_V28A, V15_V18A, VGGE1_V28, VGGE2_V28, VGGE3_V28

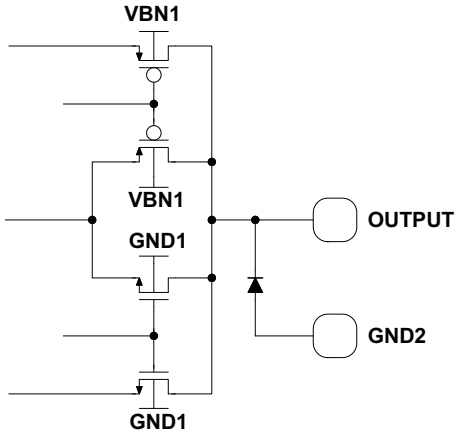


Figure 57. PAVREF1, PAVREF2, PAVREF3

PARAMETER MEASUREMENT INFORMATION (continued)

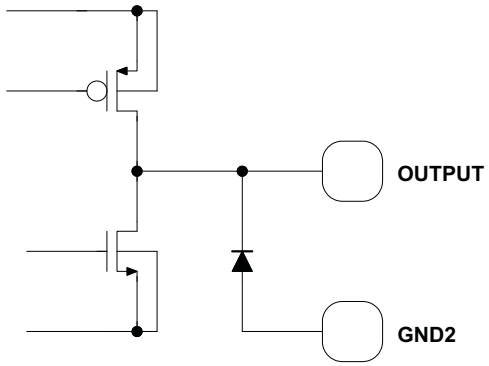


Figure 58. AFC

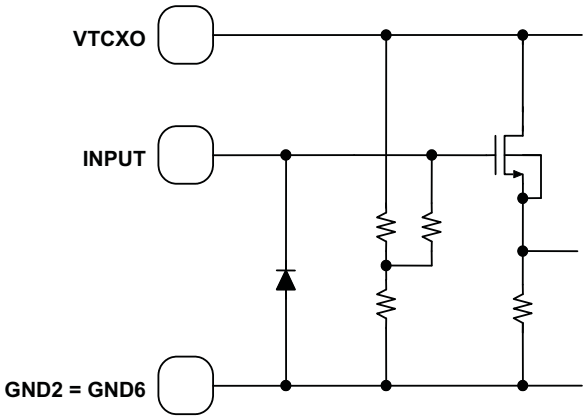


Figure 59. SYSCLK_IN

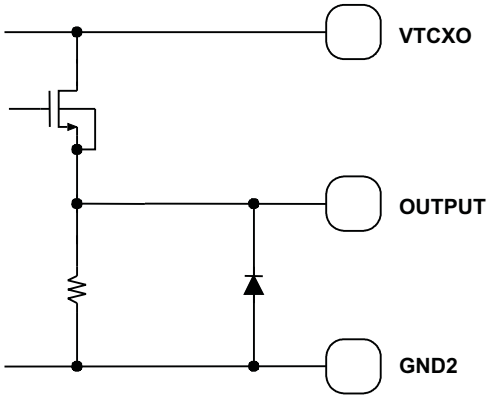


Figure 60. SIN_SYSCLK1, SIN_SYSCLK2, SIN_SYSCLK3

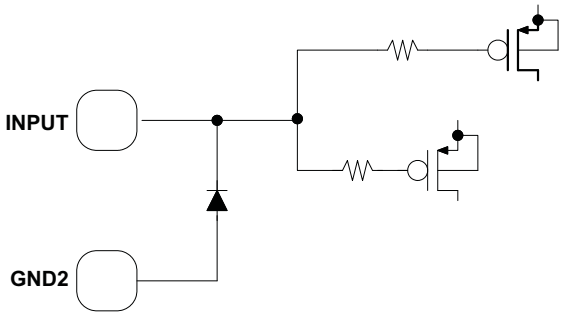


Figure 61. PABIAS1

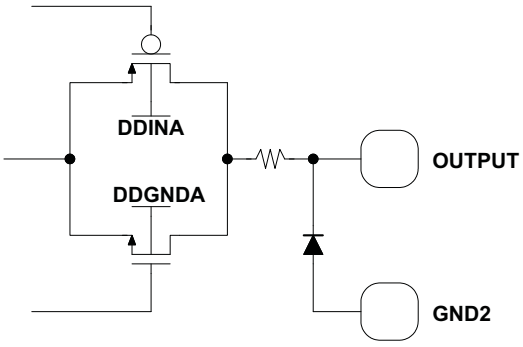


Figure 62. ERR

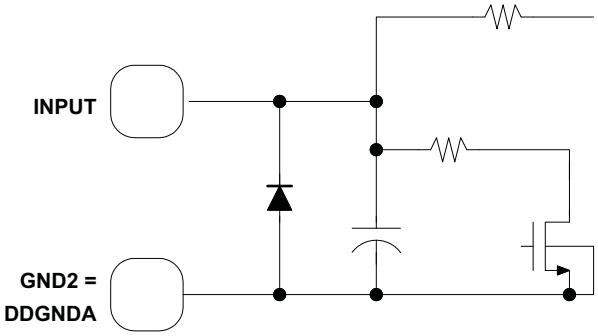


Figure 63. PA_FB

PARAMETER MEASUREMENT INFORMATION (continued)

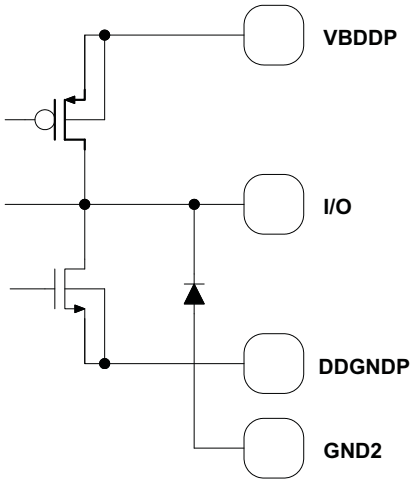


Figure 64. L1

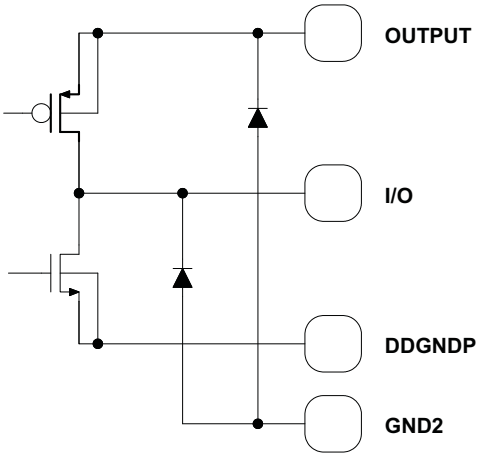


Figure 65. VOUT, L2

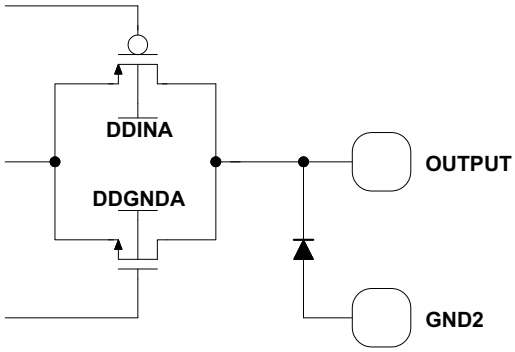


Figure 66. TEST

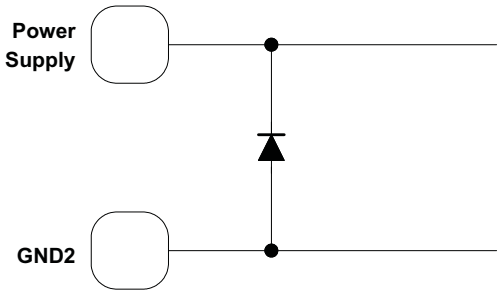


Figure 67. VBN1, VBN2, VBN3, VBN4, VBN5, DDINA, VBDDP, VIO1V8

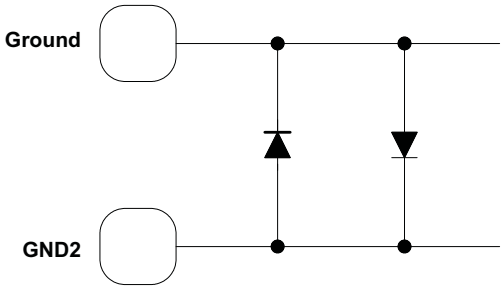


Figure 68. GND1, GND2, GND3, GND4, GND5, GND6, DDGNDA, DDGNDP

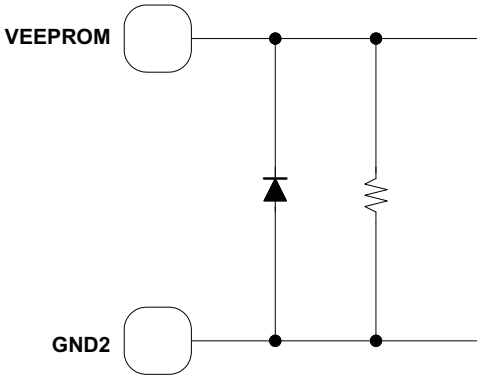


Figure 69. VEEPROM

DETAILED DESCRIPTION

DC/DC converter

The TPS65040 is a buck/boost PWM converter optimized for cellular phone power amplifier applications. Switching frequency is internally set at 1.5 MHz, allowing the use of small inductors and capacitors. The internal synchronous switch increases efficiency and provides fast transient response. Figure 70 is a block diagram of the device.

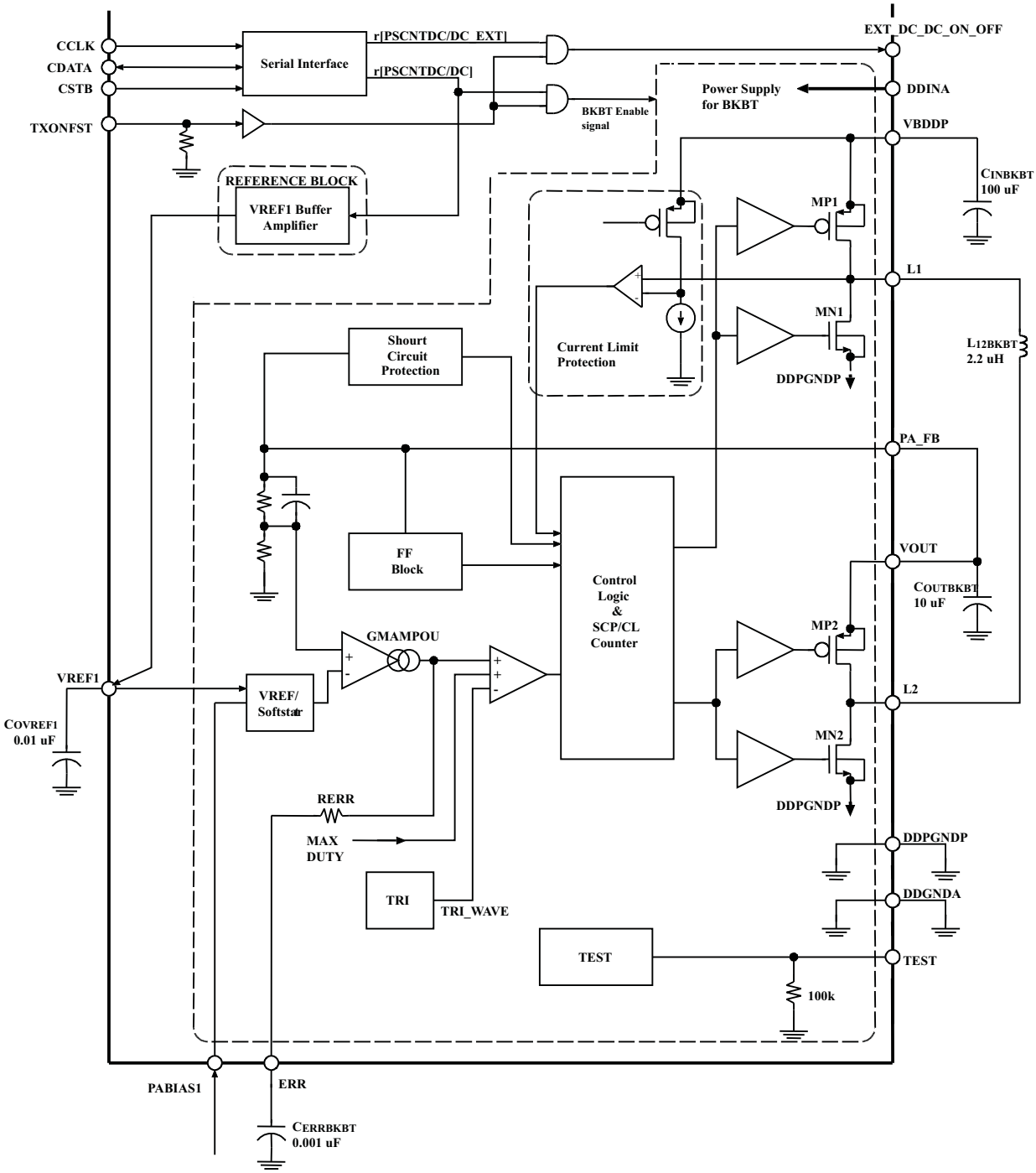


Figure 70. DC/DC converter Block Diagram

DETAILED DESCRIPTION (continued)

Because the DC/DC converter operates in buck/boost mode using only one external inductor, the output voltage can be programmed from 0.8 V to 4.2 V by an analog input voltage applied to terminal PABIAS1. The VOUT voltage is determined by:

VOUT (V) = -1.688 × PABIAS1 (V) + 4.874

Figure 71 shows VOUT voltage vs PABIAS1 input.

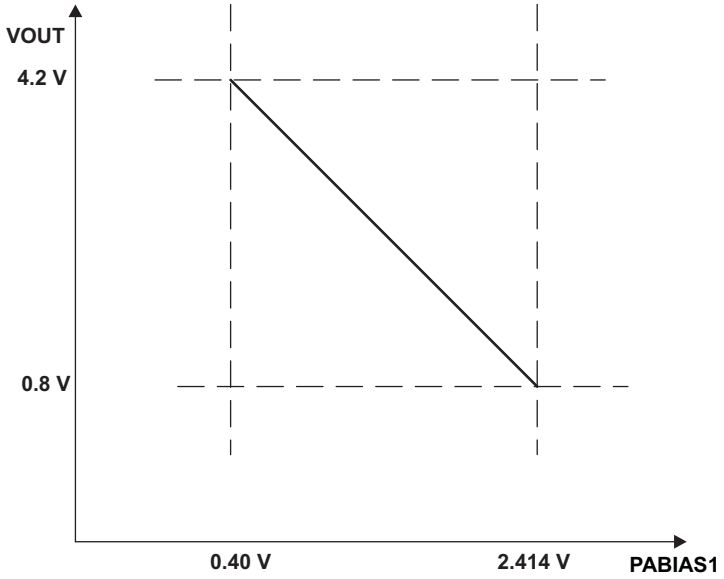


Figure 71. VOUT Voltage vs PABIAS1 Input

The DC/DC converter output is enabled or disabled by TXONFST pin and the r[PSNCNTDC/DC] register bit (accessed via the serial I/F, default value = 1). When r[PSNCNTDC/DC] = 1, a high level on the TXONFST pin powers up the DC/DC converter. The output then rises to the voltage selected by the input voltage on the PABIAS1 pin. Note: At VBAT values outside the range specified in the recommended operating conditions table, the DC/DC converter must be turned off. The DC/DC converter ON/OFF options are shown in Table 1.

Table 1. DC/C Converter (BKBT) ON/OFF Control

REG_EN(1)	VIO1V8(1)	TXONFST	r[PSCNTDC/DC]	OUTPUT
1	1	1	1	**ON**
1	1	0	1	**OFF**
1	1	1	0	**OFF**
1	1	0	0	**OFF**
0	0	Don't Care	Don't Care	**OFF**
1	0	Don't Care	Don't Care	**OFF**

(1) REG_EN and VIO1V8 sequence is described in the Sequence Control section.

The *EXT_DC_DC_ON_OFF* pin can control an external DC/DC converter based on the states of the TXONFST pin, and r [PSCNTDC/DC_EXT]. r [PSCNTDC/DC_EXT] is 0 by default. The detail is described in the *SERIAL INTERFACE Section*. Table 2 shows Low/High control for an external DC/DC converter.

Table 2. Low/High Control for External DC/DC Converter

REG_EN(1)	VIO1V8(1)	TXONFST	r[PSCNTDC/DC_EXT]	EXT_DC_DC_ON_OFF
1	1	1	1	**High**
1	1	0	1	**Low**

(1) REG_EN and VIO1V8 sequence is described in the Sequence Control section.

Table 2. Low/High Control for External DC/DC Converter (continued)

REG_EN(1)	VIO1V8(1)	TXONFST	r[PSCNTDC/DC_EXT]	EXT_DC_DC_ON_OFF
1	1	1	0	**Low**
1	1	0	0	**Low**
0	0	Don't Care	Don't Care	**Low**
1	0	Don't Care	Don't Care	**Low**

BUCK-BOOST DC/DC CONVERTER POWER-UP SEQUENCE AND MODE STATE DESCRIPTION

Power-Up Sequence

Pin PABIAS1 controls the output voltage and must have an input to set the output voltage before power up of the DC/DC converter. If PABIAS1 pin has an unknown voltage, the DC/DC converter can not regulate the output voltage; and, the device or peripheral components may be damaged. Figure 72 shows the power-up sequence for the DC/DC converter: (a) via an external pin controlled by TXONFST, and (b) via a register command control. Figure 72 shows each mode from OFF (Disable Mode) to ON (Normal Operation Mode). The following paragraphs give more details.

PABIAS1 Pin Input Voltage Range

The input voltage range of PABIAS1 pin is from 0.4 V to 2.414 V. This range keeps the output voltage of the DC/DC converter at the proper level. Also, it must be input before power-up of the DC/DC converter.

Disable Mode

Table 1 shows the buck-boost DC/DC converter is disabled when TXONFST = Low, or r[PSCNTDC/DC] = Low. Then the analog circuit of Figure 70 is disabled and the logic circuit is reset. Also, current-limit protection and short-circuit protection are disabled.

Active Discharge When Disable Mode

VOUT output is pulled down to 0V when the buck-boost DC/DC converter is disabled. Then MN1, MP2 = ON and MP1, MN2 = OFF in Figure 70. VOUT pin is pulled down to 0V via the coil, but when VOUT is below 0.6 V, the discharging speed is at a gentle slope. Because the power supply of the MN2 and its gate driver buffer in Figure 70 are supplied from VOUT, the MN2 cannot discharge the VOUT to 0V.

Idle Mode

Table 1 shows the DC/DC converter is enabled when TXONFST = High and r[PSCNTDC/DC] = High. Figure 72 shows each mode during power-up sequence. Since the analog circuit is unstable, output transistors (MP1, MN1, MP2, MN2) operate after 50µs (typ), counted by an internal oscillator. After the count-up it shifts to softstart mode. Current-limit protection and short-circuit protection are disabled. Figure 72 shows the same sequence; that is, TXONFST turns from low to high at r[PSCNTDC/DC] = High, and r[PSCNTDC/DC] turns low to high at TXONFST = High.

Softstart Mode

Softstart mode operates to avoid rush current when the buck-boost DC/DC converter activates the output transistor via idle mode. Internal VREF_SS ramps up within 500µs (max) by counter, when idle mode shifts to softstart mode. Output voltage is set by PABIAS1 pin. The time of softstart mode depends on the value of the output voltage. SS_OK = High finishes softstart mode when VREF_SS is counted up. After completing softstart mode, current-limit protection and short-circuit protection start operation simultaneously.

Normal Operation Mode

Normal operation mode provides line regulation, load regulation, and fast transient response control by the analog input of PABIAS1 pin. Current-limit and short-circuit protection are enabled continuously.

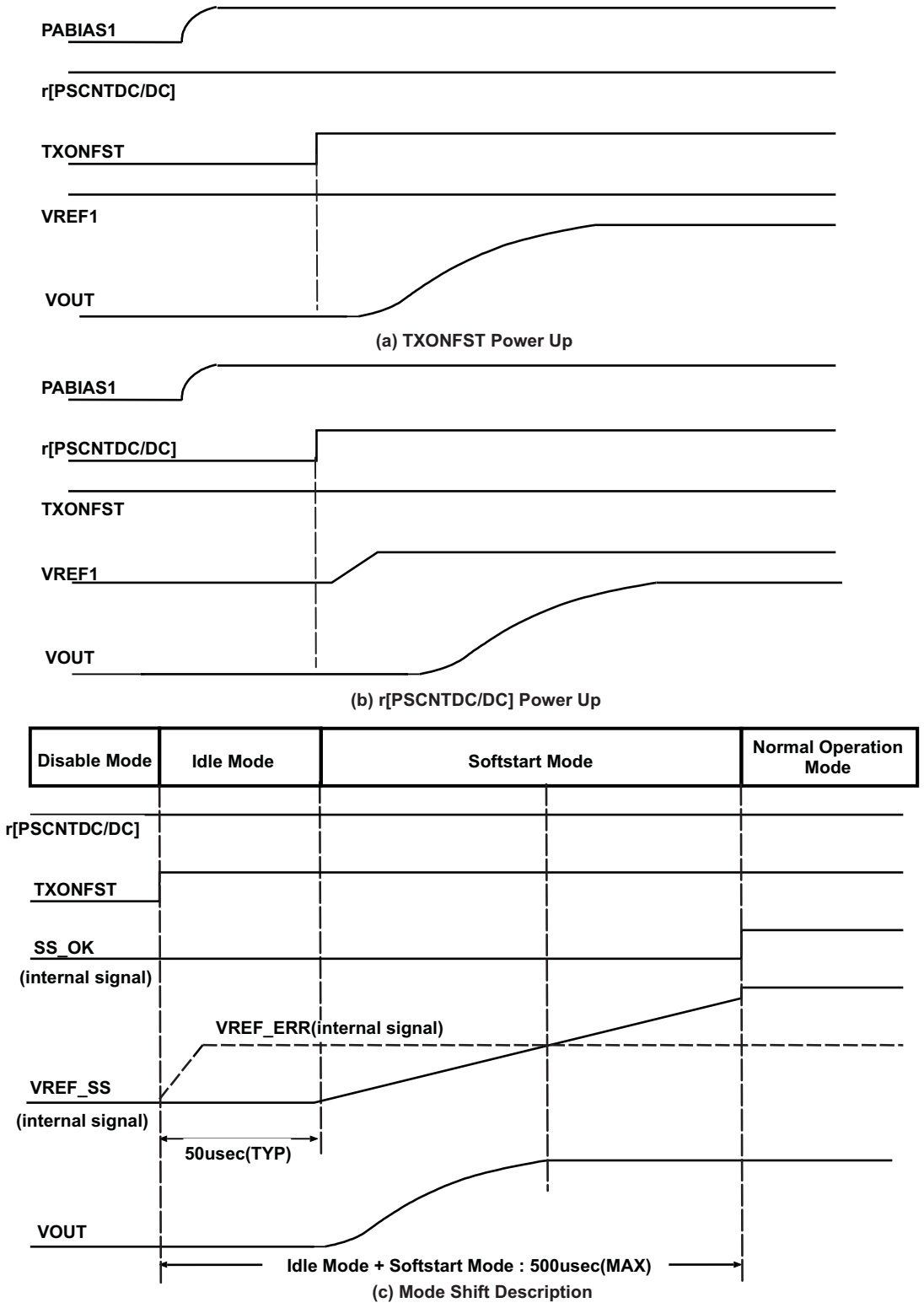


Figure 72. DC/DC converter Power Up Sequence

Buck-Boost Mode Operation

The DC/DC converter is able to regulate the output voltage at all possible input voltages. The buck mode, buck-boost mode, and boost mode are automatically switched in the analog circuit. It operates as buck mode when the input voltage of VBDDP is higher than the output voltage of VOUT, and as boost mode when the input voltage of VBDDP is lower than the output voltage of VOUT. It operates as buck-boost mode when the input voltage of VBDDP is close to the output voltage of VOUT. In buck mode, MP1 and MN1 on the L1 side, shown in Figure 70, are switching continuously. MP2 on the L2 side, shown in Figure 70 is always on, and MN2 on the L2 side is always off. When the voltage difference between input voltage of VBDDP and output voltage of VOUT is 0.5 V or less, MP2 and MN2 on the L2 side start switching. Therefore, the mode is switched from buck mode to buck-boost mode. In boost mode, MP2 and MN2 on the L2 side are switching continuously. MP1 on the L1 side is always on, and MN1 on the L1 side is always off. When the voltage difference between the output voltage of VOUT and the input voltage of VBDDP is 0.5 V or less, MP1 and MN1 on the L1 side start switching. Therefore the mode is switched from boost mode to buck-boost mode.

Current-Limit Protection

Figure 73 and Figure 74 show coil current, VOUT output voltage, PABIAS1 input voltage operations, and current-limit protection mode. Current-limit protection has a limit value of 4 A and 1.5 A detected peak current. Figure 73(a) shows PABIAS1 input voltage, VOUT output voltage regulation, and coil current. VOUT output voltage begins to ramp to target value based on the reducing PABIAS1 input voltage. Then, coil current increases for fast transient response. Current-limit value in the current-limit protection circuit shifts from 1.5 A to 4 A, after the 1.5 A current limit value is detected twice in normal mode operation. This is the current-limit 4-A detection mode, which keeps within 50 µs (typ) counted internal oscillator. Coil current is decreased when settling of the output voltage reaches completion in current-limit 4-A detection mode. When 50 µs (typ) of current-limit 4-A detection mode ending, the current-limit protection circuit shifts to current-limit 1.5-A detection mode automatically, and detects the coil current by 1.5-A current limit value between 5 µs (typ) counted by internal oscillator. When the current limit protection circuit does not detect 1.5-A coil current between 5 µs (typ), it shifts from current-limit 1.5-A detection mode to normal operation mode. Thereafter, while the current limit protection circuit continuously monitors the peak current of the coil, and a 1.5-A current limit condition is detected twice continuously, it shifts to current-limit 4-A detection mode again. This describes the operation for continuous coil current flow.

Figure 73(b) shows the operation when the coil current flows continuously. When the current-limit protection circuit detects 1.5 A continuously twice, it shifts to the current-limit 4-A detection mode. Even if 4 A keeps flowing after mode shifting, it shifts from the current-limit 4-A detection mode, to the current-limit 1.5-A detection mode after 50 µs (typ). However, when 1.5 A keeps flowing for a specific cause for more than 5 µs (typ), the current-limit protection circuit keeps operating in the current-limit 1.5-A detection mode. The output voltage decreases when DC/DC converter can not drive the low impedance load because of current limit conditions. The short-circuit protection circuit operates when the output voltage falls to 80% or less. See the *SHORT-CIRCUIT PROTECTION* Section for details.

While 1.5 A is flowing continuously, the current-limit protection circuit is operating in the current-limit 1.5-A detection mode. When the coil current falls to 1.5 A or less, 5 µs (typ) is counted again.

Figure 74 shows the operation when the coil current is decreasing from current-limit 1.5-A detection mode, and the mode shifts to normal mode operation. It is waited that Coil current becomes 1.5 A or less continuing after 1.5 A kept flowing between 5 µs (typ) by Current-limit 1.5-A detection mode. When the coil current falls to 1.5 A or less, another 5 µs (typ) is counted. Meanwhile, the current-limit protection circuit shifts from current-limit 1.5-A detection mode to normal operation mode if the current-limit protection circuit does not detect a 1.5 A current-limit value. But if the current limit value of 1.5 A is detected again within this 5 µs (typ) interval, it remains in the current-limit 1.5-A detection mode, and waits for the coil current to fall to 1.5 A, or less.

Current-limit protection not only detects output transient response by PABIAS1, but it also detects heavy load conditions during stable output conditions.

Note that the detection time is counted by an internal oscillator which generates the switching frequency (fs) of the DC/DC converter.

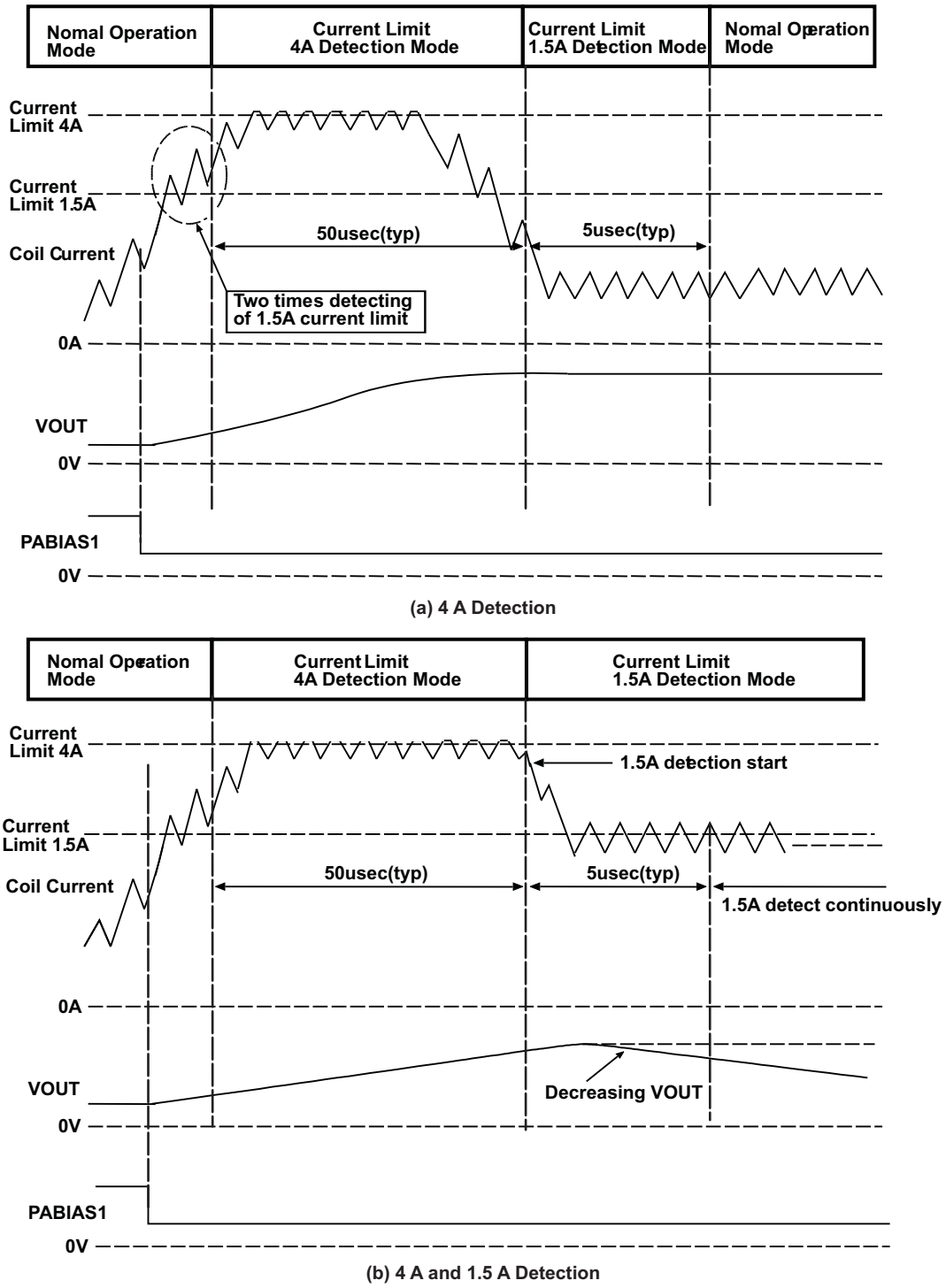


Figure 73. Current Limit Protection - View (a) and (b)

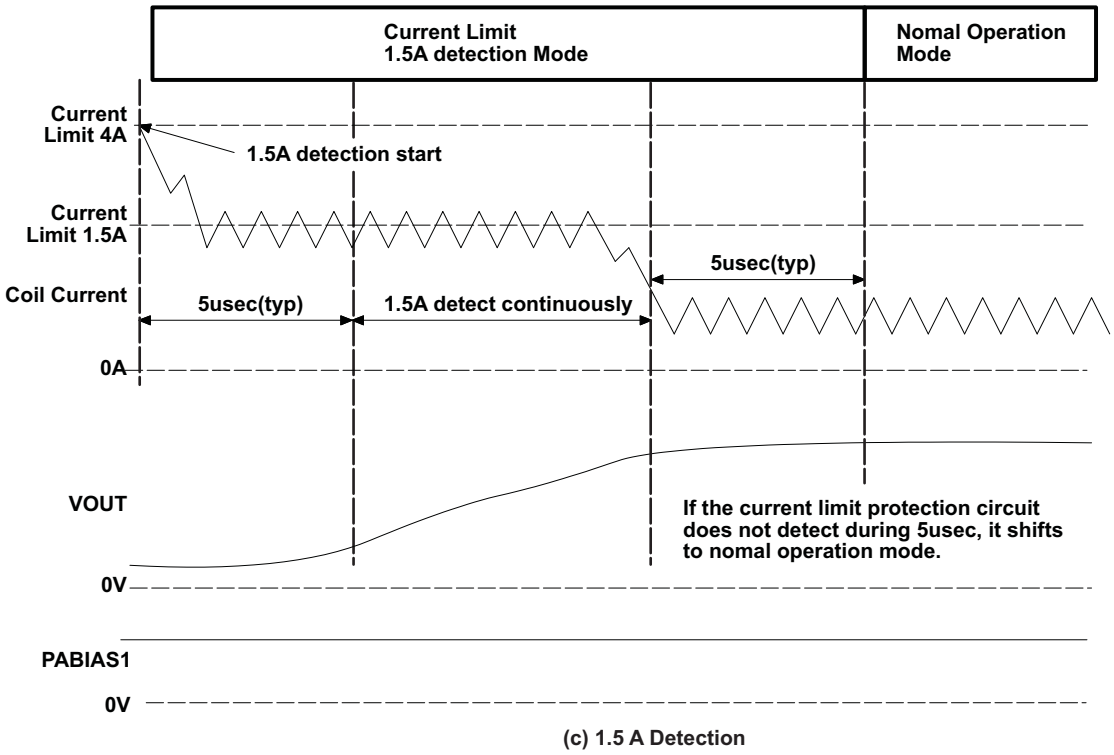


Figure 74. Current Limit Protection - View

Short-Circuit Protection

The DC/DC converter incorporates short-circuit protection (SCP) in addition to current-limit protection (CLP) circuitry. The current-limit protection circuit applies to the peak current detection of the coil, while the short-circuit protection circuit detects the level of the output voltage. Figure 75 (a) shows the operation of short-circuit protection. The output voltage of VOUT decreases when current-limit operates, limiting the current through the coil. Short-circuit protection occurs when 80% or less of the target output voltage value is detected while in the normal operation mode, thereby shifting from normal operation mode to SCP monitor mode. An internal oscillator provides the timing for a 0.5 msec (typ) delay before shifting to SCP-monitor mode. The two protection circuits (current-limit protection and short-circuit protection) operate in this manner, shifting to SCP mode when the output voltage of VOUT does not exceed the target value for 0.5 msec (typ), even if passing, and the VOUT pin is adjusted to 0V for 8 msec (typ). The analog circuit of the DC/DC converter is enabled for the 8-msec (typ) period, after which the DC/DC converter powers up from soft-start mode. If the output voltage of VOUT exceeds 80% of the target value after soft-start mode ends, it operates in normal operation mode. The short-circuit protection circuit continuously monitors the output voltage value of VOUT. It transitions from soft-start mode to normal-operation mode once, after power up, as shown in Figure 75 (b), and then if the output voltage of VOUT does not achieve 80% of the target output voltage, it again shifts to SCP-monitor mode. It shifts to SCP mode when the output voltage of VOUT does not exceed the target value for 0.5 msec (typ), even if passing, and the VOUT pin is adjusted to 0V for 8 msec (typ). The DC/DC converter keeps repeating this intermittent operation as long as there is no setting change from the host. Figure 75 (c) shows the image chart for intermittent operation. Note that the detection time is counted by an internal oscillator, which generates the switching frequency (fs) of the DC/DC converter.

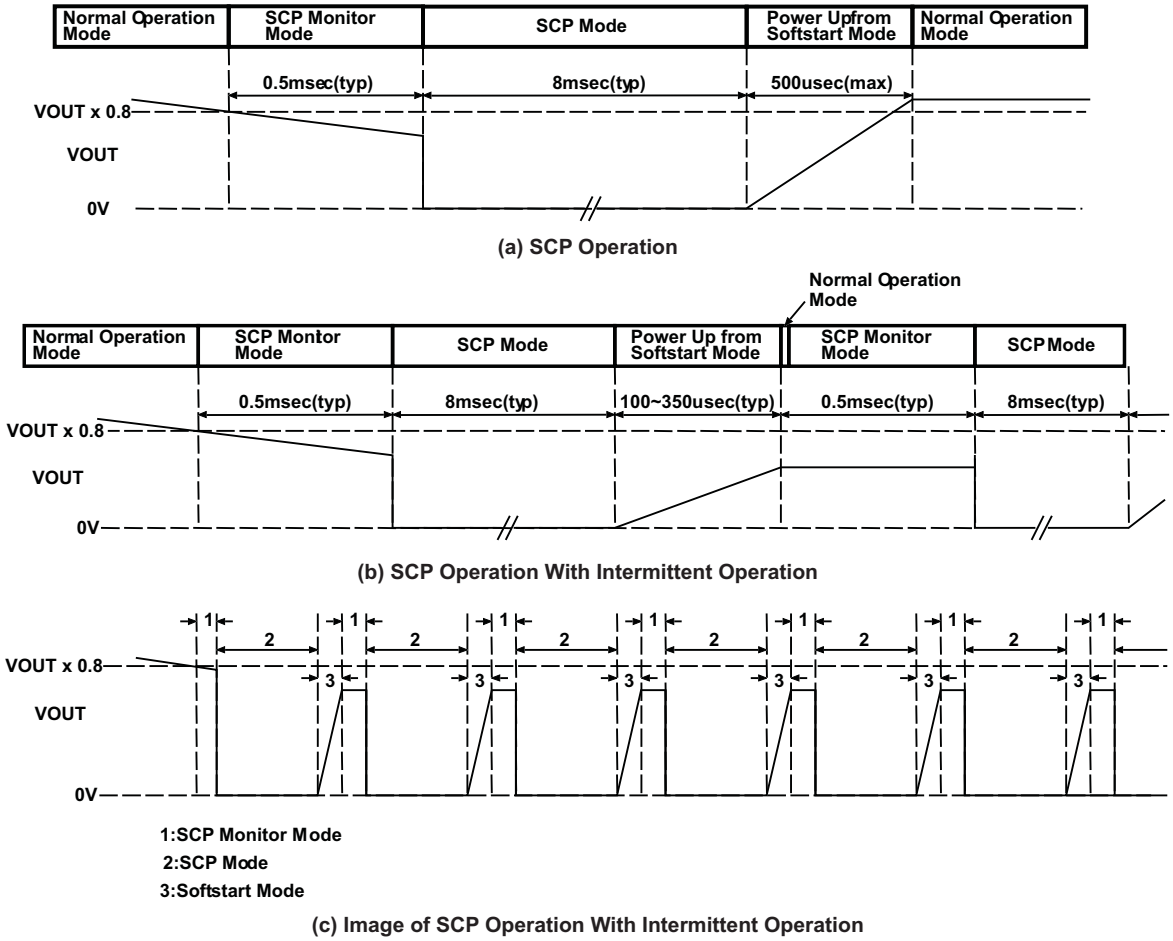


Figure 75. Short Circuit Protection

LOW DROPOUT OUTPUT

Figure 76 shows the block diagram of V11_V28TX, V12_V28RX, V13_V28A and V15_V18A. Also Figure 77 shows the block diagram of VGGE1_V28, VGGE2_V28 and VGGE3_V28 which have different control signals.

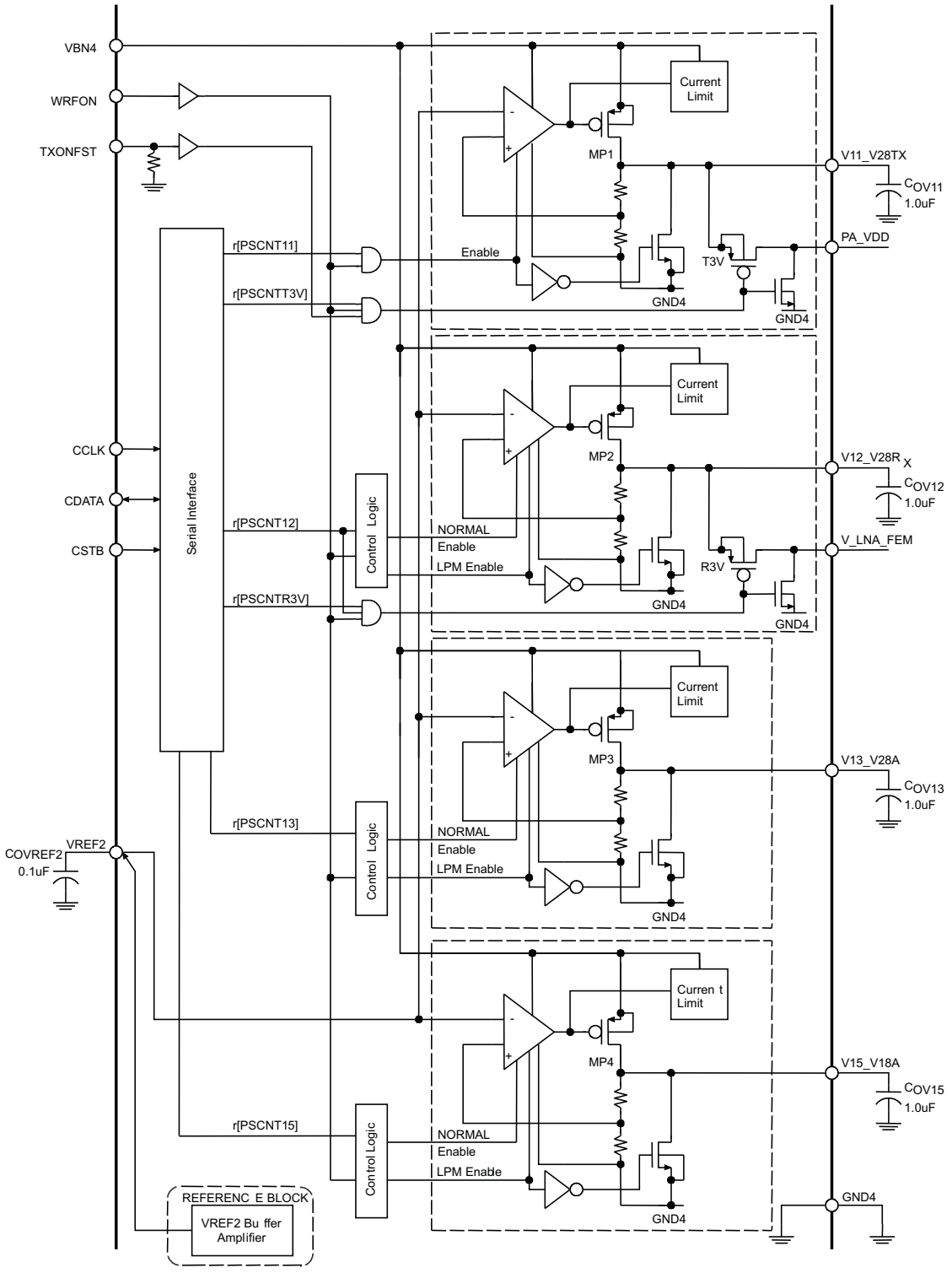


Figure 76. BLOCK DIAGRAM OF V11_V28TX, V12_V28RX, V13_V28A and V15_V18A

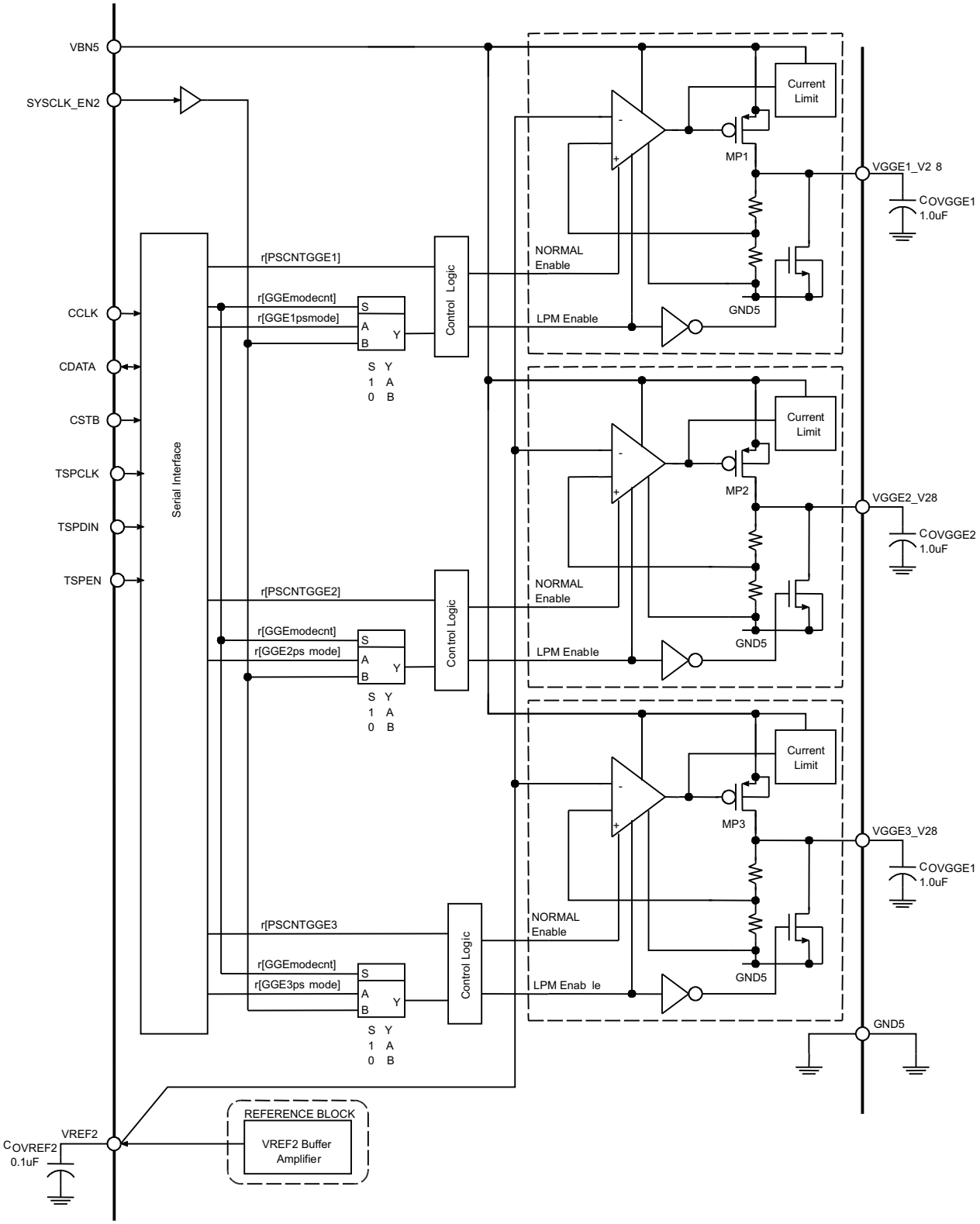


Figure 77. BLOCK DIAGRAM OF VGGE1_V28, VGGE2_V28 and VGGE3_V288

V11_28TX

V11_V28TX is a high-performance LDO having a 2.85-V output voltage. The output PMOS of the LDO turns off when the load current exceeds the limit value of the current-limit protection circuit and stops the power supply. When the load current falls to under-the-limit values, the current-limit state is released. This LDO has a low-current mode and a high-current mode, corresponding to light-load and heavy-load conditions, respectively. The mode is changed automatically. The LDO on/off is controlled by the WRFON pin and r[PSCNT11]. Register command r[PSCNT11] can be controlled through the serial interface; the default is 0. Note: Turn off this LDO when VBAT < 3.1 V. The *SERIAL INTERFACE Section* explains this in detail. On/off control of V11_V28TX is shown in Table 3.

Table 3. V11_V28TX ON/OFF Control

REG_EN(1)	VIO1V8(1)	WRFON	r[PSCNT11]	V11_V28TX
1	1	1	1	**ON**
1	1	1	0	**OFF**
1	1	0	1	**OFF**
1	1	0	0	**OFF**
0	0	Don't Care	Don't Care	**OFF**
1	0	Don't Care	Don't Care	**OFF**

(1) REG_EN and VIO1V8 sequence is described in *SEQUENCE CONTROL*.

PA_VDD

PA_VDD is output from V11_V28TX through the T3V switch. On/off of the T3V switch is controlled by WRFON pin, TXONFST pin, and r[PSCNTT3V]. Register command r[PSCNTT3V] can be controlled through the serial interface; default is 0. Note: PA_VDD is output only when V11_V28TX has been turned on. More detail is given in the *SERIAL INTERFACE Section*. On/off control of PA_VDD is shown in Table 4.

Table 4. PA_VDD ON/OFF Control

REG_EN(1)	VIO1V8(1)	WRFON	TXONFSTS	r[PSCNTT3V]	PA_VDD
1	1	1	1	1	**ON**
1	1	1	0	1	**OFF**
1	1	1	1	0	**OFF**
1	1	1	0	0	**OFF**
1	1	0	1	1	**OFF**
1	1	0	0	1	**OFF**
1	1	0	1	0	**OFF**
1	1	0	0	0	**OFF**
0	0	Don't Care	Don't Care	Don't Care	**OFF**
1	0	Don't Care	Don't Care	Don't Care	**OFF**

(1) REG_EN and VIO1V8 sequence is described in *SEQUENCE CONTROL*.

V12_V28RX

V12_V28RX is an LDO that outputs 2.85 V, and is enabled during the power-up sequence of the TPS65040. The *SEQUENCE CONTROL Section* gives more detail. Normal mode and low-power mode can be selected. Normal mode provides high performance, and low-power mode provides low current consumption. Normal-mode performance is much better than low-power mode. The output PMOS is stopped when the load current exceeds the limit value of the current-limit protection in the normal mode, shutting down the power supply. When the load current falls to less than the limit values, current limit is released. Current-limit protection is not available in low-power mode. This LDO has low-current mode and high-current mode in normal mode. When in a light-load condition, the mode is low-current mode. When in a heavy-load condition, the mode is high-current mode. The

mode is changed automatically. On/off for this LDO is controlled by register command r[PSCNT12], and switching from normal mode to low-power mode is controlled with the WRFON pin. Register command r[PSCNT12] can be controlled through the serial interface; the default is 1. Note: Turn off this LDO, or use low-power mode when VBAT < 3.1 V. The *SERIAL INTERFACE Section* explains in more detail. The switch control of normal mode/low-power mode, and V12_V28RX ON/OFF control is shown in Table 5.

Table 5. V12_V28RX ON/OFF and Normal Mode/Low Power Mode Control

REG_EN(1)	VIO1V8(1)	CRESET(1)	WRFON	r[PSCNT12]	V12_V28RX
1	1	1	1	1	**Normal Mode**
1	1	1	0	1	**Low Power Mode**
1	1	1	1	0	**OFF**
1	1	1	0	0	**OFF**
0	0	Don't Care	Don't Care	Don't Care	**OFF**
1	0	Don't Care	Don't Care	Don't Care	**OFF**
1	1	0	Don't Care	1	**Normal Mode**

(1) REG_EN and VIO1V8 sequence is described in *SEQUENCE CONTROL*.

V_LNA_FEM

V_LNA_FEM is output from V12_V28RX through the R3V switch. Switch R3V controls on/off by the WRFON pin, TXONFST pin, and r[PSCNTR3V]. Register command r[PSCNTR3V] can be controlled through the serial interface; default is 0. The *SERIAL INTERFACE Section* provides more detail. On/off control of V_LNA_FEM is shown in Table 6.

Table 6. V_LNA_FEM ON/OFF Control

REG_EN(1)	VIO1V8(1)	WRFON	r[PSCNT12]	r[PSCNTR3V]	V_LNA_FEM
1	1	1	1	1	**ON**
1	1	1	0	1	**OFF**
1	1	1	1	0	**OFF**
1	1	1	0	0	**OFF**
1	1	0	1	1	**OFF**
1	1	0	0	1	**OFF**
1	1	0	1	0	**OFF**
1	1	0	0	0	**OFF**
0	0	Don't Care	Don't Care	Don't Care	**OFF**
1	0	Don't Care	Don't Care	Don't Care	**OFF**

(1) REG_EN, VIO1V8 and CRESET sequence is described in *SEQUENCE CONTROL*.

V13_V28A

V13_V28A outputs 2.85 V. This LDO is enabled during the power-up sequence of the TPS65040. The *SEQUENCE CONTROL Section* provides more detail. Normal mode and low-power mode can be selected. Normal mode provides high performance, and low-power mode provides low current consumption. The output PMOS is stopped when the load current exceeds the limit value of the current-limit protection circuit in normal mode, shutting down the power supply. When the load current falls to less than the limit values, current limit is released. Current-limit protection is not available in low-power mode. This LDO has a low-current mode and a high-current mode in normal mode. Under light-load conditions the mode is low-current. When under heavy-load conditions, the mode is high current. Mode is changed automatically. This LDO on/off is controlled by r[PSCNT13], and switches from normal mode to low-power mode with the WRFON pin. Register command r[PSCNT13] can be controlled through the serial interface; default is 1. Note: Turn off this LDO, or use low-power mode when VBAT < 3.1V. The *SERIAL INTERFACE Section* explains in greater detail. The switch control of normal mode / low-power mode, and V13_V28A on/off control is shown in Table 7.

Table 7. V13_V28A ON/OFF and Normal Mode/Low Power Mode Control

REG_EN(1)	VIO1V8(1)	CRESET(1)	WRFON	r[PSCNT13]	V13_V28A
1	1	1	1	1	**Normal Mode**
1	1	1	0	1	**Low Power Mode**
1	1	1	1	0	**OFF**
1	1	1	0	0	**OFF**
0	0	Don't Care	Don't Care	Don't Care	**OFF**
1	0	Don't Care	Don't Care	Don't Care	**OFF**
1	1	0	Don't Care	1	**Normal Mode**

(1) REG_EN, VIO1V8 and CRESET sequence is described in *SEQUENCE CONTROL*.

V15_V18A

V15_V18A is an LDO that outputs 1.85 V, and is powered up during the power-up sequence of the TPS65040. The *SEQUENCE CONTROL Section* provides more detail. Normal mode and low-power mode can be selected. Normal mode provides high performance, and low-power mode provides low current consumption. The output PMOS is stopped when the load current exceeds the limit value of the current-limit protection circuit in normal mode; the power supply is shut down. When the load current falls below the limit values, current limit is released. Current-limit protection is not available in the low-power mode. This LDO has a low-current mode and a high-current mode in normal mode. The low-current mode and high-current mode correspond to light-load and heavy-load conditions, respectively. The modes are changed automatically. This LDO on/off is controlled by r[PSCNT15], and switches from normal mode to low-power mode with the WRFON pin. Register command r[PSCNT15] can be controlled through the serial interface; default is 1. The *SERIAL INTERFACE Section* provides greater detail. Note that the electrical characteristics of this LDO are not assured for the range of 2.7V < VBAT < 3.1V function. When not used, turn it off or to the low-power mode. On/off control of V15_V18A and switch control for normal mode/low-power mode are shown in Table 8.

Table 8. V15_V18A ON/OFF and Normal Mode/Low Power Mode Control

REG_EN(1)	VIO1V8(1)	CRESET(1)	WRFON	r[PSCNT15]	V15_V18A
1	1	1	1	1	**Normal Mode**
1	1	1	0	1	**Low Power Mode**
1	1	1	1	0	**OFF**
1	1	1	0	0	**OFF**
0	0	Don't Care	Don't Care	Don't Care	**OFF**
1	0	Don't Care	Don't Care	Don't Care	**OFF**
1	1	0	Don't Care	1	**Normal Mode**

(1) REG_EN, VIO1V8 and CRESET sequence is described in *SEQUENCE CONTROL*.

VGGE1_V28

VGGE1_V28 is an LDO that outputs 2.85 V, and is one of the LDOs enabled during the power-up sequence of the TPS65040. More detail is given in the *SEQUENCE CONTROL Section*. The normal mode and low-power mode can be selected, where normal mode provides high performance, and low-power mode provides low current consumption. The output PMOS is stopped when the load current exceeds the limit value for the current-limit protection circuit in normal mode, and the power supply is shut down. When the load current falls below the limit value, current limit is released. Current-limit protection is not available in the low-power mode. This LDO has a low-current mode and a high-current mode in normal mode. The low-current mode and high-current mode correspond to light-load and heavy-load conditions, respectively. The modes are changed automatically. LDO on/off is controlled by register command r[PSCNTGGE1]. Normal mode and low-power mode are switched using register command r[GGE1psmode] at r[GGEmodecnt]=High, SYSCLK_EN2 pin at r[GGEmodecnt]=Low. Register commands r[PSCNTGGE1], r[GGEmodecnt], and r[GGE1psmode] can be controlled through the serial interface; the default is 1. More detail is provided in the *SERIAL INTERFACE Section*. Note that the electrical characteristics for this LDO are not assured within the range of 3.0V<VBAT<3.1V function. Moreover, the output voltage also decreases by VBAT–VSAT, when VBAT decreases. Turn off this LDO, or use the low-power mode, when in the VBAT<3 V condition. On/off control of VGGE1_V28 and the switch control of normal mode/low-power mode are shown in Table 9.

Table 9. VGGE1_V28 ON/OFF and Normal Mode/Low Power Mode Control

REG_EN(1)	r[PSCNTGGE1]	r[GGEmodecnt]	r[GGE1psmode]	SYSCLK_EN2	VGGE1_V28
1	VIO1V8 is off	Don't Care	Don't Care	Don't Care	**Normal Mode**
1	1	1	1	Don't Care	**Normal Mode**
1	1	1	0	Don't Care	**Low Power Mode**
1	1	0	Don't Care	1	**Normal Mode**
1	1	0	Don't Care	0	**Low Power Mode**
0	1	Don't Care	Don't Care	Don't Care	**OFF**
1	0	Don't Care	Don't Care	Don't Care	**OFF**
0	0	Don't Care	Don't Care	Don't Care	**OFF**

(1) REG_EN sequence is described in *SEQUENCE CONTROL*.

VGGE2_V28

VGGE2_V28 is an LDO that outputs 2.85 V, and is one of the LDOs enabled during the power-up sequence of the TPS65040. More detail is given in the *SEQUENCE CONTROL Section*. Normal mode and low-power mode can be selected, with normal mode being the high-performance mode, and low-power mode for low current consumption. The output PMOS is stopped when the load current exceeds the limit value for the current-limit protection circuit in normal mode, and the power supply is shut down. When the load current falls below the limit value, current limit is released. Current limit protection is not available in low-power mode. This LDO has a low-current mode and a high-current mode in normal mode. The low-current mode and high-current mode correspond to light-load and heavy-load conditions, respectively. The modes are changed automatically. LDO on/off is controlled by register command r[PSCNTGGE2]. Normal mode and low-power mode are switched using register command r[GGE2psmode] at r[GGEmodecnt]=High , SYSCLK_EN2 pin at r[GGEmodecnt]=Low. Register commands r[PSCNTGGE2], r[GGEmodecnt], and r[GGE2psmode] are controlled through the serial interface; the default is 1. Note that the electrical characteristics of this LDO are not assured within the range of 3 V <VBAT<3.1V function. Moreover, the output voltage also decreases by VBAT–VSAT when VBAT decreases. Turn off this LDO, or use the low-power mode ,when in the VBAT<3 V condition. On/off control of VGGE2_V28A, and the switch control of normal mode/low-power mode are shown in Table 10.

Table 10. VGGE2_V28 ON/OFF and Normal Mode/Low Power Mode Control

REG_EN(1)	r[PSCNTGGE2]	r[GGEmodecnt]	r[GGE2psmode]	SYSCLK_EN2	VGGE2_V28
1	VIO1V8 is off	Don't Care	Don't Care	Don't Care	**Normal Mode**
1	1	1	1	Don't Care	**Normal Mode**
1	1	1	0	Don't Care	**Low Power Mode**
1	1	0	Don't Care	1	**Normal Mode**
1	1	0	Don't Care	0	**Low Power Mode**
0	1	Don't Care	Don't Care	Don't Care	**OFF**
1	0	Don't Care	Don't Care	Don't Care	**OFF**
0	0	Don't Care	Don't Care	Don't Care	**OFF**

(1) REG_EN sequence is described in *SEQUENCE CONTROL*.

VGGE3_V28

VGGE3_V28 is an LDO that outputs 2.85 V, and powers up with the power-up sequence of the TPS65040. More detail is found in the *SEQUENCE CONTROL Section*. Normal mode and low-power mode can be selected. Normal mode provides high performance, and low-power mode offers low current consumption. Output PMOS is stopped when the load current exceeds the limit value of the current limit protection circuit in normal mode, and the power supply is shut down. When the load current falls below the limit values, current limit is released. Current-limit protection is not available in low-power mode. This LDO has a low-current mode and a high-current mode in normal mode. The low-current mode and high-current mode correspond to light-load and heavy-load conditions, respectively. The modes are changed automatically. The LDO on/off is controlled by register command r[PSCNTGGE3]. Normal mode and low-power mode are switched using register command r[GGE3psmode] at r[GGEmodecnt]=High , SYSCLK_EN2 pin at r[GGEmodecnt]=Low. Register commands that

can be controlled through the serial interface are r[PSCNTGGE3], r[GGEmodecnt], r[GGE3psmode]; the default is 1. Note that the electrical characteristics of this LDO are not assured within the range of 3 V < VBAT< 3.1 V function. Moreover, the output voltage decreases by VBAT–VSAT when VBAT decreases. Turn off this LDO, or use the low-power mode in the condition where VBAT<3 V. On/off control of VGGE3_V28A and the switch control of normal mode/low-power mode are shown in Table 11.

Table 11. VGGE3_V28 ON/OFF and Normal Mode/Low Power Mode Control

REG_EN(1)	r[PSCNTGGE3]	r[GGEmodecnt]	r[GGE3psmode]	SYSCLK_EN2	VGGE3_V28
1	VIO1V8 is off	Don't Care	Don't Care	Don't Care	**Normal Mode**
1	1	1	1	Don't Care	**Normal Mode**
1	1	1	0	Don't Care	**Low Power Mode**
1	1	0	Don't Care	1	**Normal Mode**
1	1	0	Don't Care	0	**Low Power Mode**
0	1	Don't Care	Don't Care	Don't Care	**OFF**
1	0	Don't Care	Don't Care	Don't Care	**OFF**
0	0	Don't Care	Don't Care	Don't Care	**OFF**

(1) REG_EN sequence is described in *SEQUENCE CONTROL*.

VTCXO

VTCXO is a high-performance LDO that outputs 2.85 V. This LDO provides the power supply for the clock distribution circuit in TPS65040, and VCTCXO is external. This LDO stops output PMOS when the load current exceeds the limit value of the current-limit protection circuit, and then the power supply is shut down. When the load current falls below the limit values current limit is released. This LDO has two modes which are low-current mode and high-current mode in normal mode. The low-current mode and high-current mode correspond to light-load and heavy-load conditions, respectively. The modes are changed automatically. This LDO on/off is controlled with the SYSCLK_EN pin. Note that the electrical characteristics of this LDO are not assured within the range of 2.7 V < VBAT < 3.1 V function. Moreover, the output voltage decreases by VBAT–VSAT when VBAT decreases. Turn off this LDO when not using it. On/Off control of VTCXO is shown in Table 12. Figure 78 shows a block diagram.

Table 12. VTCXO ON/OFF Control

REG_EN(1)	SYSCLK_EN	VTCXO
1	1	**ON**
1	0	**OFF**
0	Don't Care	**OFF**

(1) REG_EN sequence is described in *SEQUENCE CONTROL*.

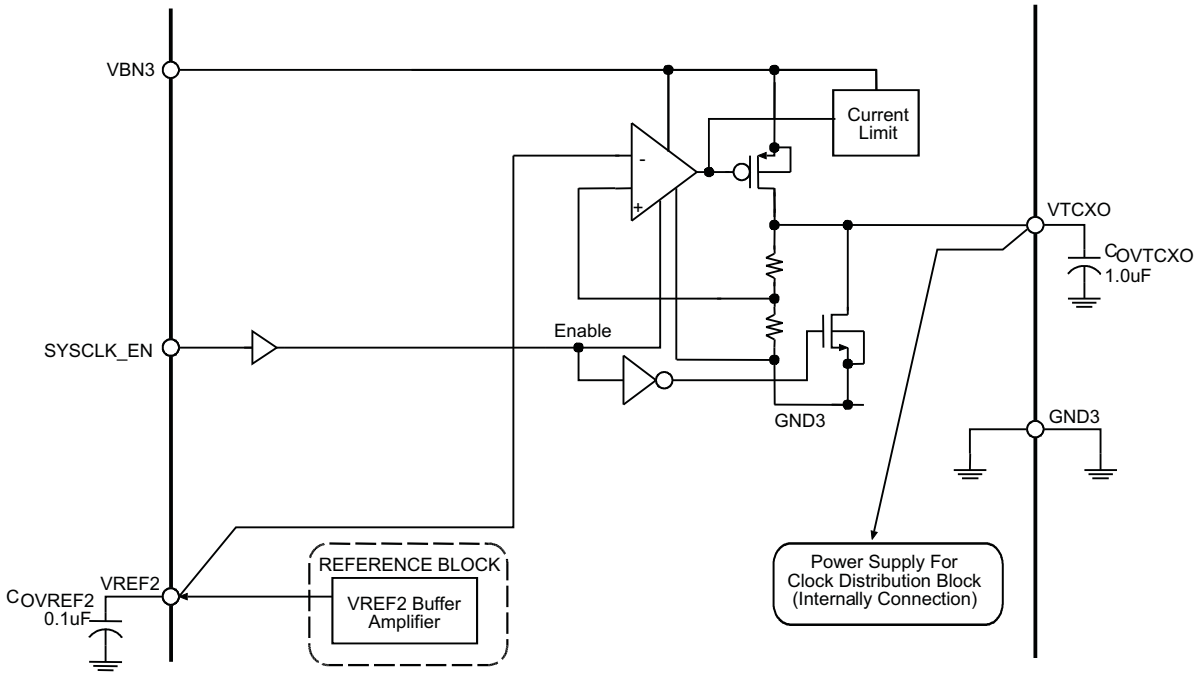


Figure 78. VTCXO Block Diagram

PAVREF

PAVREF is an 8-bit DAC whose output can be used as reference power supply for the RF power amplifier. Figure 79 shows a block diagram. PAVREF is powered up by TXNONFST=High and TXON=High. One output pin is selected by combining TBNDSEL2 pin and TBNDSEL1 pin from among three output pins, enabling the output voltage. The serial interface does not control the selection of the power up, and the output terminal. The output voltage is controlled by a register named DAC. The output voltage corresponds to the data of DACW register. The DACW register can be controlled through the serial interface, and the default is 80h. More detail is given in the *SERIAL INTERFACE Section*. Table 13 shows the control of PAVREF. PAVREF has a special LDO and has good characteristics for the power supply ripple rejection. And, a load current of 5 mA or less can be supplied by the output buffer. The output buffer is off, and all the output pins are pulled down to GND, in TXONFST=High and TXON=Low, although internal circuits (DAC, LDO) of PAVREF are turned on. The output buffer is off and all the output pins are also pulled down to GND in TBNDSEL2=High and TBMDSEL1=High although internal circuit (DAC, LDO) of PAVREF are turned on. When PAVREF is powered up by TXONFST pin, and TXON pin from power down, the output voltage is kept at the same voltage before power down by the DACW register. CRESET pin goes low or REG_EN pin goes low, the DACW register is reset and output voltage returns to the default voltage. Turn off PAVREF before changing the output terminal. Also turn off PAVREF in the condition of VBAT< 3.1 V.

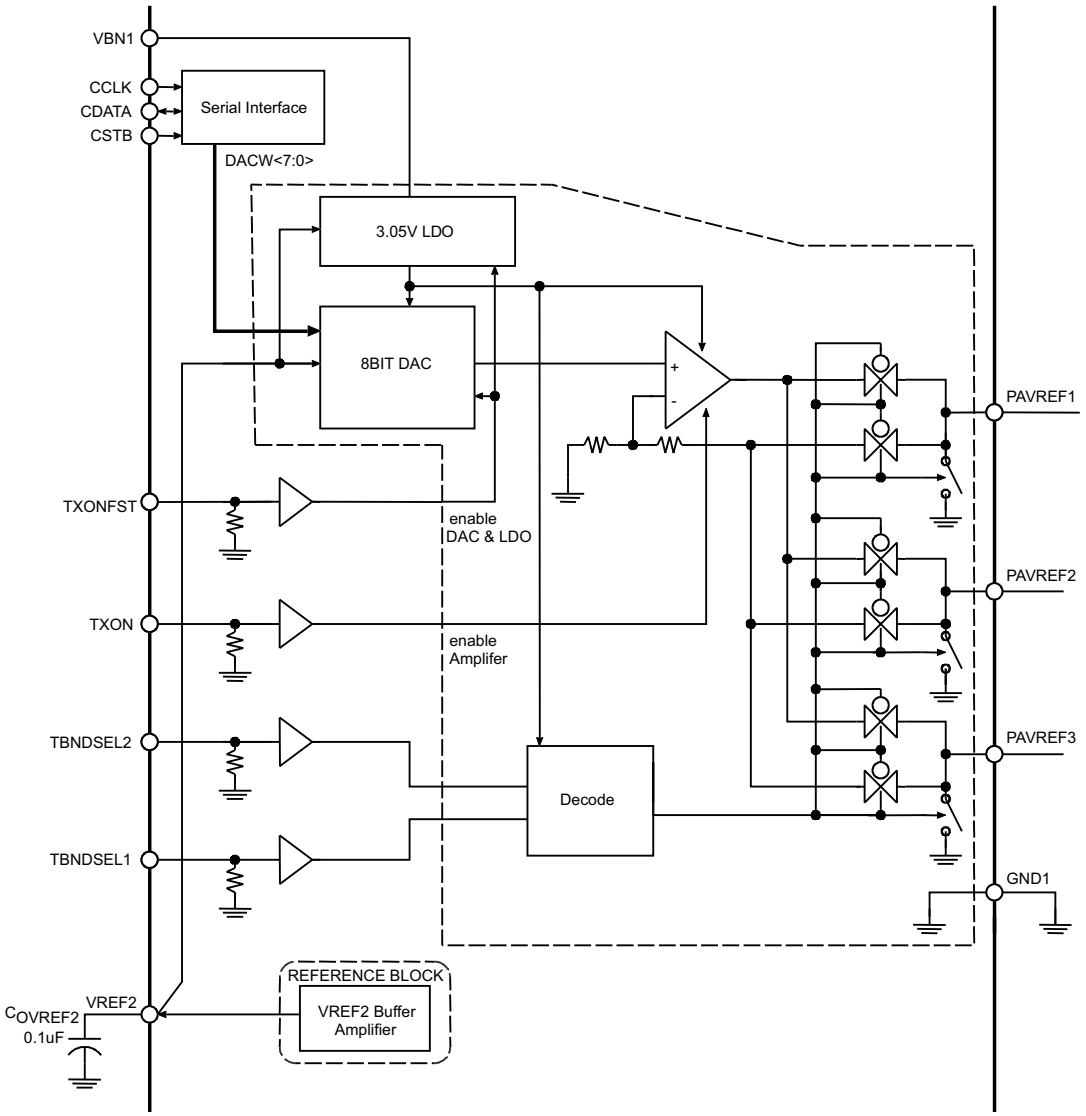


Figure 79. PAVREF Block Diagram

Table 13. PAVREF Control

REG _EN(1)	TXONFST	TXON	TBNDSEL1	TBNDSEL2	OUTPUT BUFFER	PAVREF1	PAVREF2	PAVREF3
1	0	Don't Care	Don't Care	Don't Care	**OFF**	**Hi-z**	**Hi-z**	**Hi-z**
1	1	0	0	0	**OFF**	**OFF**	**OFF**	**OFF**
1	1	0	1	0	**OFF**	**OFF**	**OFF**	**OFF**
1	1	0	0	1	**OFF**	**OFF**	**OFF**	**OFF**
1	1	0	1	1	**OFF**	**OFF**	**OFF**	**OFF**
1	1	1	0	0	**ON**	**ON**	**OFF**	**OFF**
1	1	1	1	0	**ON**	**OFF**	**ON**	**OFF**
1	1	1	0	1	**ON**	**OFF**	**OFF**	**ON**
1	1	1	1	1	**OFF**	**OFF**	**OFF**	**OFF**
0	Don't Care	Don't Care	Don't Care	Don't Care	**OFF**	**Hi-z**	**Hi-z**	**Hi-z**

(1) REG_EN sequence is described in *SEQUENCE CONTROL*.

AFCDAC

AFCDAC is a 12-bit DAC that can be used for the adjustment of VCTCXO oscillation frequency. Figure 80 shows a block diagram. AFCDAC controls the on/off switch based on SYSCLK_EN pin and r[PSCNTAFC]. Register command r[PSCNTAFC] can be controlled through the serial interface; default is High. The output voltage is controlled by registers named AFCMSB and AFCLSB. The output voltage corresponds to the data of r[AFCMSB] and r[AFCLSB]. The r[AFCMSB] and r[AFCLSB] registers can be controlled through the serial interface, and default is 800h. AFCDAC can be controlled by both CSPI and TSP interfaces. When the output voltage changes from CSPI interface, the first access register must be the r[AFCMSB], then the r[AFCLSB] next. If it is not in the correct order the output voltage can not change the value. When the output voltage changes from TSP interface, it can be one-time accessing. It does not need two-time accessing, like the CSPI interface. More detail is given in the *SERIAL INTERFACE Section*. Table 14 shows AFCDAC control. As for AFCDAC, it is a pull down in SYSCLK_EN=Low or r[PSCNTAFC]=Low to turn off to GND. When AFCDAC is powered up by SYSCLK_EN=Low to High, (r[PSCNTAFC]=High) or r[PSCNTAFC]=Low to High (SYSCLK_EN=High) from power down, the output voltage is kept at the same voltage before power down by the r[AFCMSB] and r[AFCLSB] registers. But the CRESET pin goes low, or REG_EN pin goes low, the r[AFCMSB] and r[AFCLSB] registers are reset, and the output voltage returns to the default voltage. Note that the electrical characteristics of AFCDAC are not assured within the range of 2.7V<VBAT<3.1V function. Moreover, the output voltage decreases when VBAT decreases according to the output voltage. Turn AFCDAC off when not in use.

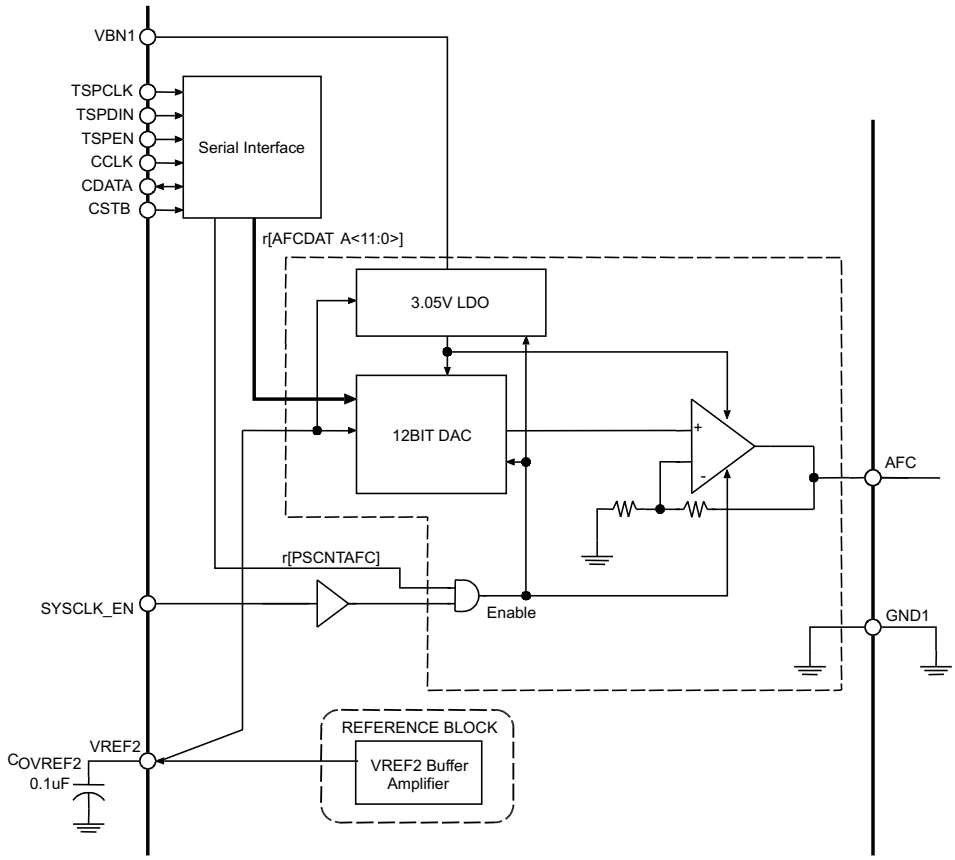


Figure 80. AFCDAC Block Diagram

Table 14. AFCDAC Control

REG_EN(1)	SYSCLK_EN	r[PSCNTAFC]	AFC
1	1	1	**ON**
1	1	0	**OFF**
1	0	1	**OFF**
1	0	0	**OFF**
0	Don't Care	Don't Care	**OFF**

(1) REG_EN sequence is described in *SEQUENCE CONTROL*.

CLOCK DISTRIBUTION

CLOCK DISTRIBUTION is a clock buffer where a clipped sine wave of 26 MHz, input from VCTCXO, is distributed to three output pins. Figure 81 shows a block diagram. Three output pins can be controlled by each signal shown in Table 15, Table 16 and Table 17. Because SYSCLK_EN pin is used as an enable signal of VCTCXO LDO and AFCDAC, VTCXO and SIN_SYSCLK1 of CLOCK DISTRIBUTION is turned on without fail in SYSCLK_EN=High. AFCDAC depends on r[PSCNTAFC]. The output of SIN_SYSCLK1 pin becomes the output amplitude of –3dB (typ) for the input amplitude. The output amplitude of IN_SYSCLK2 pin and SIN_SYSCLK3 pin are –1dB (typ). Note that the electrical characteristics of CLOCK DISTRIBUTION are not assured within the range of 2.7V<VBAT<3.1V function.

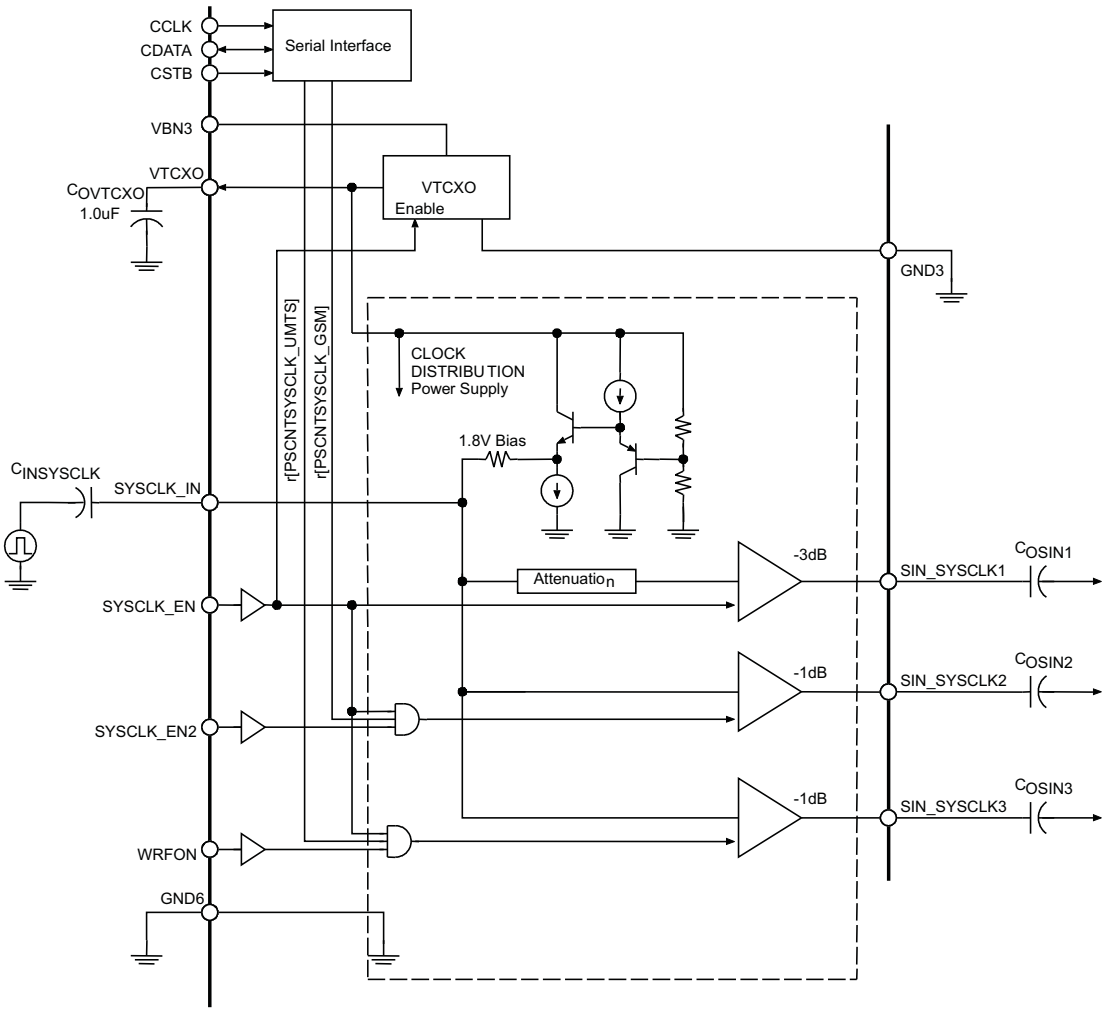


Figure 81. Clock Distribution Block Diagram

Table 15. SIN_SYSCLK1 Output Control

REG_EN(1)	SYSCLK_EN	SIN_SYSCLK1
1	1	**ON**
1	0	**OFF**
0	Don't Care	**OFF**

(1) REG_EN sequence is described in *SEQUENCE CONTROL*.

Table 16. SIN_SYSCLK2 Output Control

REG_EN(1)	SYSCLK_EN	r[PSCNTSYSCLK_GSM]	SYSCLK_EN2	SIN_SYSCLK2
1	1	1	1	**ON**
1	0	0	1	**OFF**
1	0	1	0	**OFF**
1	0	1	1	**OFF**
1	1	0	0	**OFF**(2)
1	1	0	1	**OFF**(2)
1	1	1	0	**OFF**(2)
1	0	0	0	**OFF**
0	Don't Care	Don't Care	Don't Care	**OFF**

(1) REG_EN sequence is described in *SEQUENCE CONTROL*.
(2) The output voltage level of OFF state has VTCXO (2.85 V (typ)) level. Otherwise, it is 0 V level.

Table 17. SIN_SYSCLK3 Output Control

REG_EN(1)	SYSCLK_EN	r[PSCNTSYSCLK_UMTS]	WRFON	SIN_SYSCLK3
1	1	1	1	**ON**
1	0	0	1	**OFF**
1	0	1	0	**OFF**
1	0	1	1	**OFF**
1	1	0	0	**OFF**(2)
1	1	0	1	**OFF**(2)
1	1	1	0	**OFF**(2)
1	0	0	0	**OFF**
0	Don't Care	Don't Care	Don't Care	**OFF**

(1) REG_EN sequence is described in *SEQUENCE CONTROL*.
(2) The output voltage level of OFF state has VTCXO [2.85 V (typ)] level. Otherwise is 0 V level.

VREF1, VREF2

The TPS65040 adopts the bandgap circuit and the highly accurate bias current source as an internal standard voltage. There are two kinds of bandgap circuits, Sub bandgap and Main bandgap. The Sub bandgap circuit, of the low-power consumption mode, always powers up when REG_EN=High. The Main bandgap circuit powers up when the normal mode of the LDO, and other blocks are powered up. The highly accurate bias current source also powers up when Main bandgap powers up; and, the bias current is supplied to each block. Bandgap output is distributed using two buffer amplifiers, and are output to the VREF1 pin and the VREF2 pin respectively. VREF2 pin outputs the Sub-bandgap while Sub bandgap is powered up, and Main bandgap is powered down. When Main bandgap powers up, Main bandgap is output from the VREF2 pin. VREF1 pin only outputs Main bandgap. When Main bandgap is powered down or r[PSCNTDC/DC] is set to low, VREF1 pin goes to 0V. The block diagram circuit is shown in Figure 82.

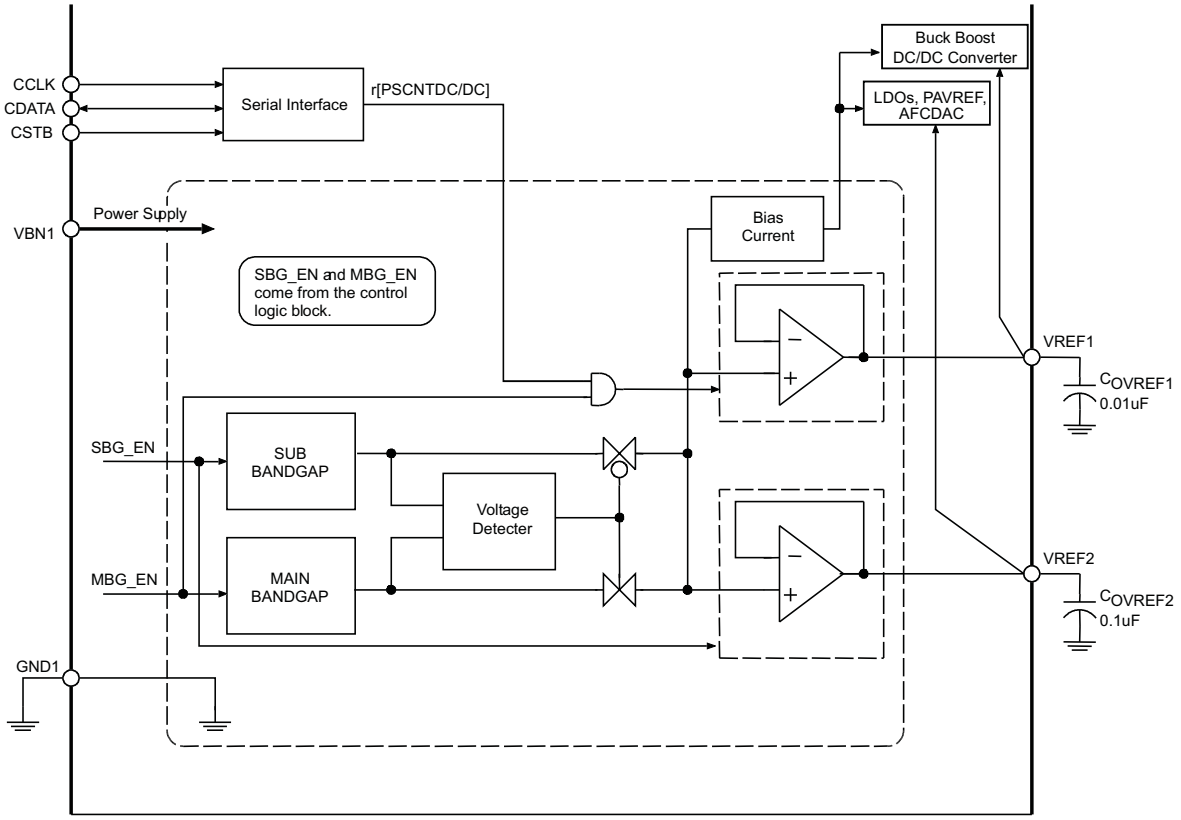


Figure 82. Reference Block Diagram

See the following tables for bandgap information:

- Table 18– Sub Bandgap Power-Up Condition
- Table 19– Main bandgap Power-Up Condition (REG_EN=VIO1V8=Hi)
- Table 20– Main Bandgap Power-Down Condition (REG_EN=VIO1V8=Hi)
- Table 21– External Pin Control
- Table 22– VREF1/VREF2 BG Buffer Power-Up Condition

Table 18. Sub Bandgap Power-Up Condition

PIN	CONDITION	MBG(1)	SBG(2)
REG_EN	Low	OFF	OFF
	High	Table 19 or Table 20	ON

(1) MBG: Main Bandgap
(2) SBG: Sub Bandgap

Table 19. Main Bandgap Power-Up Condition

BLOCK	CONDITION	MBG	SBG
NOTE: When one of these blocks turns on, Main bandgap turns on.			
DC/DC converter	Power Up	ON	ON
V11_V28TX	Power Up	ON	
V12_V28RX	Power Up	ON	
V13_V28A	Normal Mode	ON	
V15_V18A	Normal Mode	ON	
VGGE1_V28	Normal Mode	ON	
VGGE2_V28	Normal Mode	ON	
VGGE3_V28	Normal Mode	ON	
PAVREF	Power Up	ON	
VTCXO	Power Up	ON	
AFCDAC			
CLOCK DISTRIBUTION			

Table 20. Main Bandgap at Power-Down Condition

BLOCK	CONDITION	MBG	SBG
NOTE: When all blocks are in the condition listed, Main bandgap turns off.			
DC/DC converter	Power Down	OFF	ON
V11_V28TX	Power Down		
V12_V28RX	Low Power Mode or Power Down		
V13_V28A	Low Power Mode or Power Down		
V15_V18A	Low Power Mode or Power Down		
VGGE1_V28	Low Power Mode or Power Down		
VGGE2_V28	Low Power Mode or Power Down		
VGGE3_V28	Low Power Mode or Power Down		
PAVREF	Power Down		
VTCXO	Power Down		
AFCDAC			
CLOCK DISTRIBUTION			

Table 21. Main Bandgap by External Pin Control

PIN	CONDITION	POWER UP BLOCK	MBG	SBG
NOTE: When one of these pins goes High, Main bandgap turns on. But the POWER UP BLOCK depends on the register control.				
SYSCLK_EN	High	VTCXO, AFCDAC, CLOCK DISTRIBUTION	ON	ON
WRFON	High	V11_V28TX=ON (r[PSCNT11]=High), V12_V28RX = V13_V28A = V15_V18A =Normal mode	ON	
SYSCLK_EN2	High	VGGE1_V28=VGGE2_V28=VGGE1_V28=Normal mode (r[GGEmodecnt]=Low)	ON	
TXONFST	High	DC/DC converter, PAVREF	ON	

Table 22. VREF1/VREF2 BG Buffer Power-Up Condition

CONDITION	VREF1 BG BUFFER	VREF2 BG BUFFER
REG_EN=Hi, (SBG=ON)	See below	ON
MBG=ON and r[PSCNTDC/DC]=1	ON	ON
MBG=ON and r[PSCNTDC/DC]=0	OFF	ON
In Table 20 Condition	OFF	ON

THERMAL PROTECTION

Thermal Shutdown

When an abnormally high junction temperature (160°C typical, or more) is detected, TPS65040 shuts off the following three blocks, if they are turned on:

- DC/DC converter
- PAVREF
- V11_V28TX

The other blocks do not shut off under abnormally high temperatures. If the junction temperature falls, thermal shutdown is released (150°C (typical)) these three blocks turn on immediately, and the DC/DC converter is powered up through the softstart. The TPS65040 provides the read function for the thermal shutdown flag and uses the serial interface as a means to inform the host of the thermal shutdown condition. When thermal shutdown occurs, this function writes 1 in the register map (address: E6h and data: D7). This data can detect a thermal-shutdown condition by reading CSPI. This flag in the register can be cleared by VBAT = 0V, REG_EN pin going Low, or by a software reset (address: E8h, doing write access with option data). See the TSD operation in Figure 83.

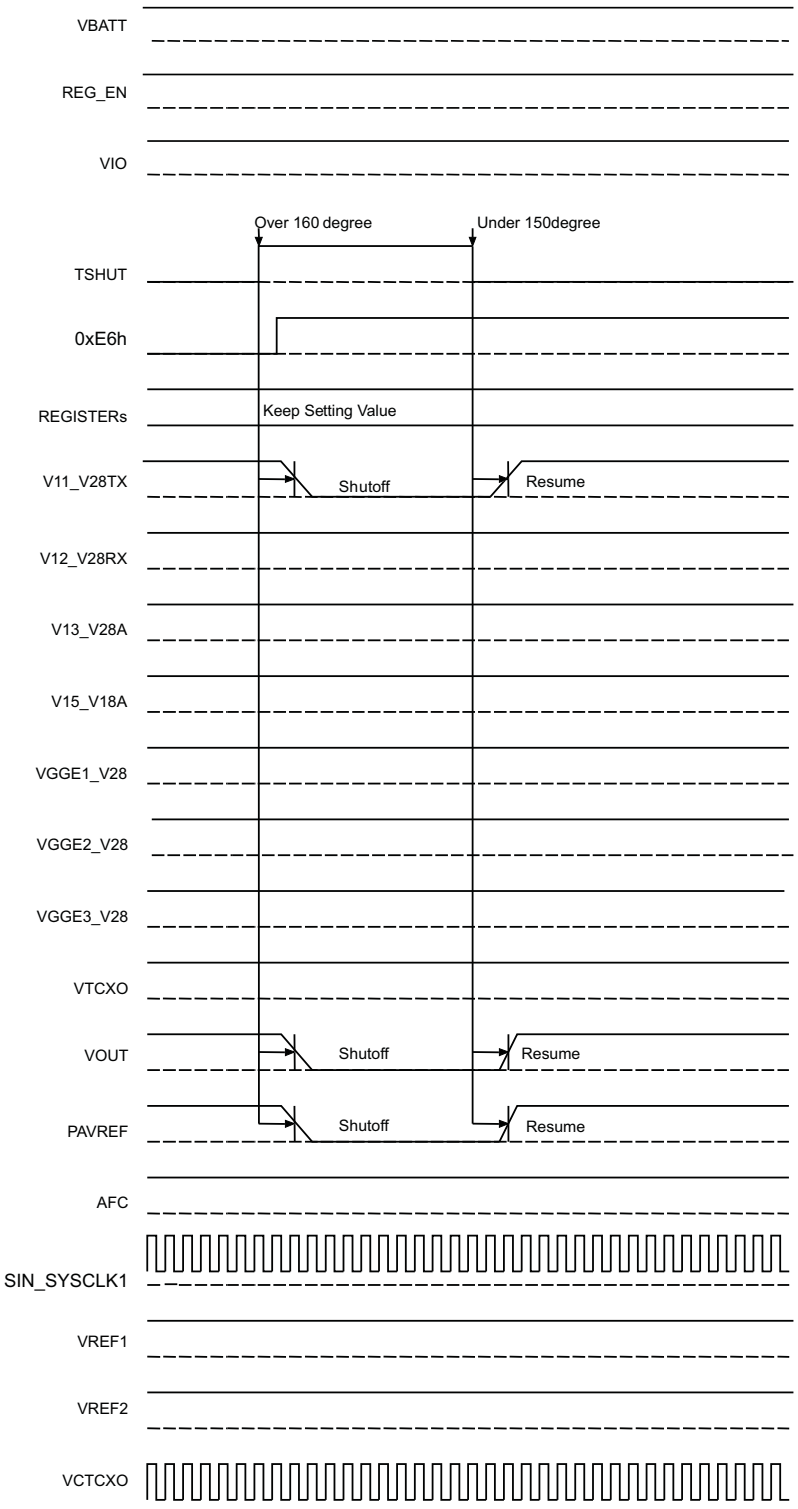


Figure 83. Thermal Shutdown Operation

HOT-DIE DETECTION

TPS65040 provides hot-die detection as a function of junction temperature. It is expressed as 3-BIT data representing rising junction temperatures of 110°C, 120°C, 130°C, 140°C, and 150°C. The 3-BIT data can be read via the serial interface. This function does not cause block shutoff (as in a thermal shutdown condition), but furnishes junction temperature data. Table 23 shows the 3-BIT threshold temperatures.

Table 23. Threshold Temperature

E6h:TEMP[2:0]	TEMPERATURE
000	Reserved
001	Reserved
010	Under 110°C
011	110°C ± 15°C
100	120°C ± 15°C
101	130°C ± 15°C
110	140°C ± 15°C
111	150°C ± 15°C
TSD Shutdown	160°C ± 15°C

SEQUENCE CONTROL

Power Up Sequence

The TPS65040 is designed to permit the power-up sequence shown in Figure 84. The sequences have the following relationship:

1. REG_EN=Low: TPS65040 power down
2. REG_EN=High: VGGE1_V28, VGGE2_V28, and VGGE3_V28 are powered up in Normal Mode.
3. VIO1V8=High: V12_V28RX, V13_V28A, V15_V18 are powered up in Normal Mode.
4. SYSCLK_EN=High: VTCXO, AFCDAC, CLOCK DISTRIBUTION (SIIN_SYSCLK1) are powered up. When VTCXO is powered up, the VCTCXO is supplied from VTCXO, and oscillation starts.
5. CRESET=High: V12_V28RX, V13_V28A, and V15_V18A change into low-power mode. The serial interface accepts data from the host CPU.
6. The oscillation of VCTCXO is steady.
7. Operation Starts (See *Power-Up Mode* below).

Asynchronous Input of CRESET

The TPS65040 accepts an asynchronous input of CRESET. If it is SYSCLK_EN=High as shown in Figure 85, it is possible to make the clock output from TPS65040 work without stopping. However, the block which is powered up or powered down by the register should note it so that all registers become the default values.

Power Supply Input Order and Level for VBN1, VBN2, VBN3, VBN4, VBN5, DDINA and VBDDP

The TPS65040 has seven power supply input pins. The order of input does not matter. Power up all power pins simultaneously. The power supply level for VBN1, VBN2, VBN3, VBN4, VBN5, DDINA and VBDDP should be the same level, as much as possible.

Power-Up Mode

This mode is only valid in the power-up sequence, which is shown by Figure 84. After a valid power-up sequence, the TPS65040 supplies the clock, and accepts serial interface communication from the host CPU. The TSP65040 then changes the mode to 2G mode, 3G mode, low-power mode, or no communication mode. Power-up mode is not a steady (i.e., continuous) mode.

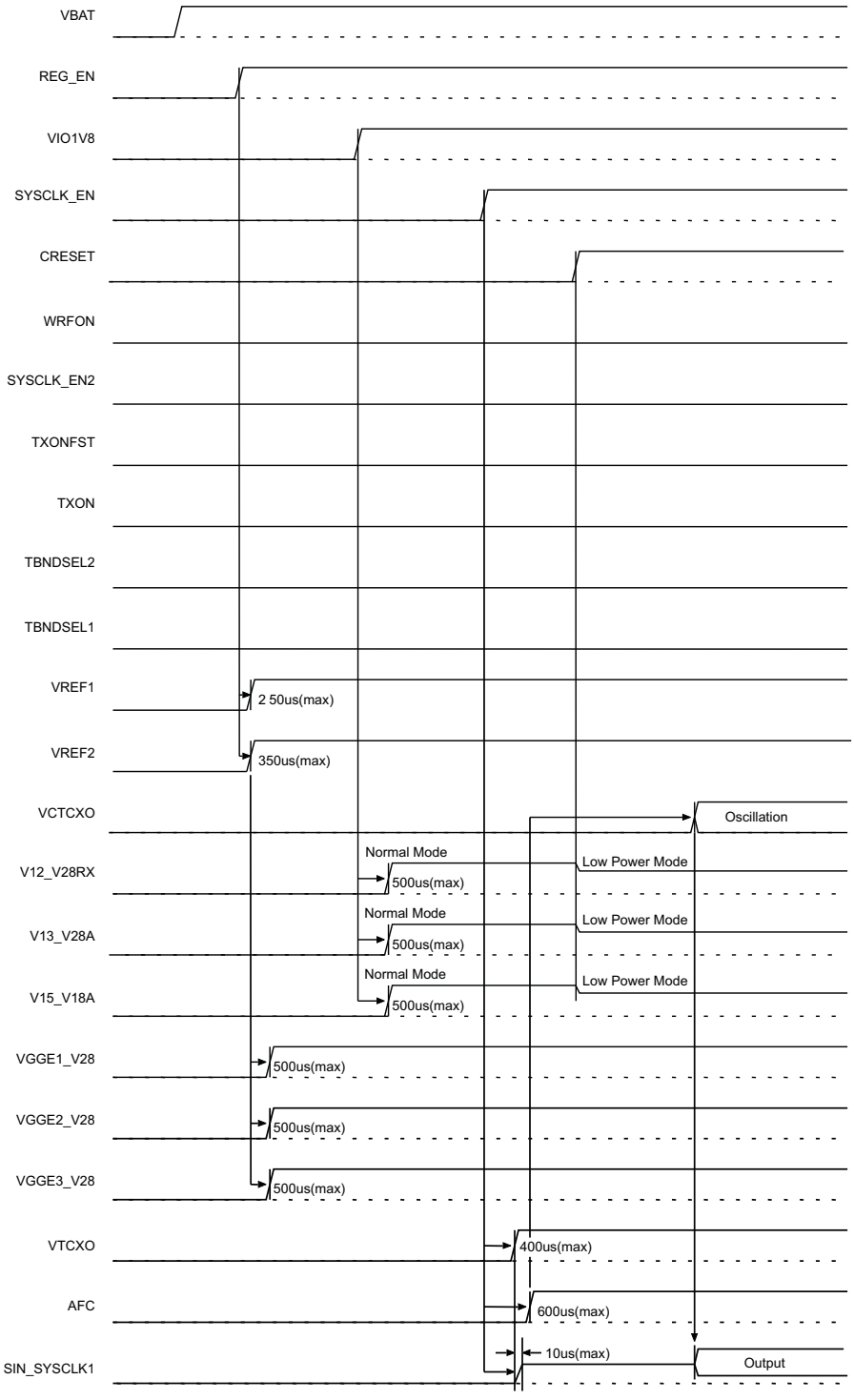


Figure 84. Power-Up Sequence

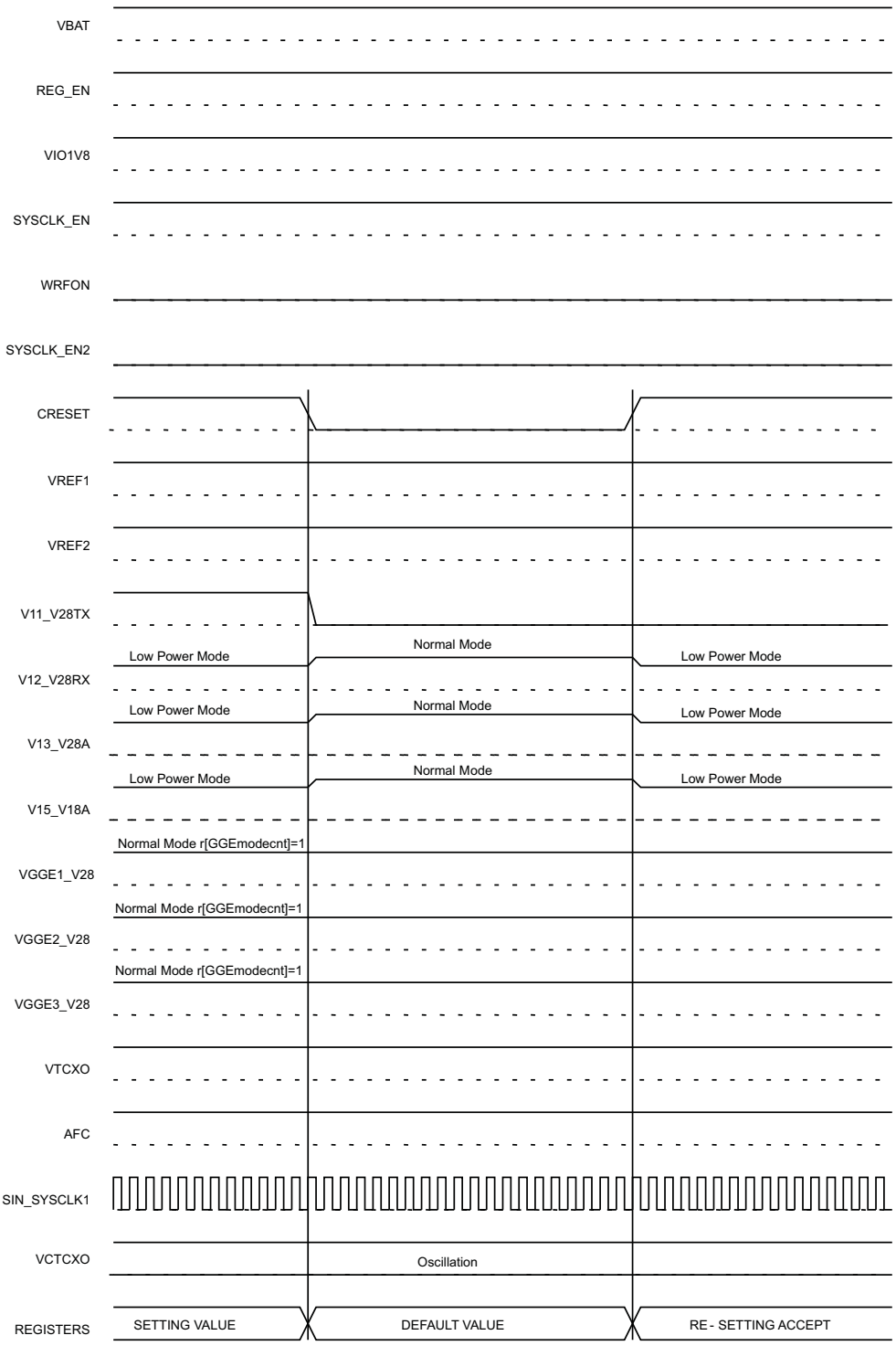


Figure 85. CRESET Asynchronous Input

SERIAL INTERFACE

The TPS65040 adopts two three-line type serial interfaces for communicating with the host. One is CSPI which provides data WRITE/READ function, another is TSP which provides data WRITE function. The register map of CSPI is shown in Table 25 and the register map of TSP is shown in Table 26. These register maps return to the

default value when the CRESET pin becomes Low. It gives priority to TSP for the addresses of Table 24, although CSPI and TSP are also possible for writing two interfaces simultaneously. It is not possible to write from CSPI while TSP is writing to CSPI. This operation is detected by the TSPEN signal. When TSPEN=Low, Table 24 priority operation goes active. The other addresses can be accessed from CSPI during TSPEN=Low. However, note that writing from CSPI becomes effective when there is writing from CSPI to the same address, after writing TSP ends. Internal logic is able to operate between 2.7V and 3.1V. But the DC/DC converter, PAVREF and V11_V28TX should be OFF. Also, V12_V28RX, V13_V28A, V15_V18A, VGGE1_V28, VGGE2_V28 and VGGE3_V28 should be OFF, or Low-power Mode.

Table 24. TSP Priority Address of Write Operation

CSPI		TSP	
ADDRESS	**REG. NAME**	**ADDRESS**	**REG. NAME**
F0h	AFCMSBW	0h	AFCDATA
F1h	AFCLSBW		
ECh	2GLDOW	1h	2GLDOCTL
F2h	AFCDACCTLW	2h	AFCDACCTL

CSPI

CSPI is an interface that consists of three lines (CDATA pin, CCLK pin, and CSTB pin). It changes into the output mode only when reading data, although CDATA is usually an input mode. Data length becomes 16-BIT (8-BIT data, 8-BIT address). The WRITE format is shown in Figure 86 and the READ format is shown in Figure 87. The timing of READ/WRITE for CSPI operation is shown in Figure 88.

CSPI Write Operation

The 8-BIT advance data becomes the WRITE operation, and the following 8-BIT group becomes an address by data. WRITE data is taken by the rising edge of CCLK, and reflected by the falling edge of CSTB.

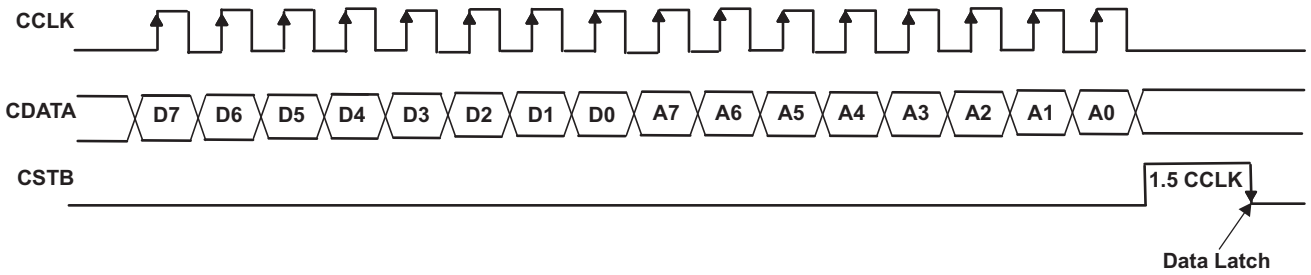


Figure 86. CSPI Write Format

Notification is given when the data of AFCDAC is re-written by using CSPI. AFCDAC has a 12-bit data length. Since the data length of CSPI is 8-bit, it can not re-write the 12-bIt data by the one-time-access. Therefore, the data of AFCDAC is written by two-times-access from CSPI. F0h: r[AFCMSBW] is written first, and the next is F1h: r[AFCLSBW]. This process is described as:

1. Write data in F0h : r [AFCMSBW]. Write '0' in the first 4 bits. This data is insignificant.
2. Write data in F1h : r [AFCLSBW].

Note 1. If step 2 is done before step 1, the correct data will not be reflected.

Note 2. If step 2 is done, but step 1 and step 2 are done sequentially, the correct data will be properly reflected.

CSPI Read Operation

In a READ operation, the 8-Bit advance data becomes the address, and the next 8-Bit group becomes the READ operation. The CSTB must be input after the address of 8-Bit advance data. CDATA pin condition remains in input mode until the falling edge of CSTB is input. Do not input CCLK and CDATA when CSTB is high. CDATA pin changes from the input mode to the output mode at the falling edge of CSTB. At the falling edge of CSTB, the data from CDATA pin is output, starting from MSB data. The next data will be read one by one at the falling edge of CCLK. CDATA pin returns from the output mode to the input mode after CCLK inputs 8 clocks.

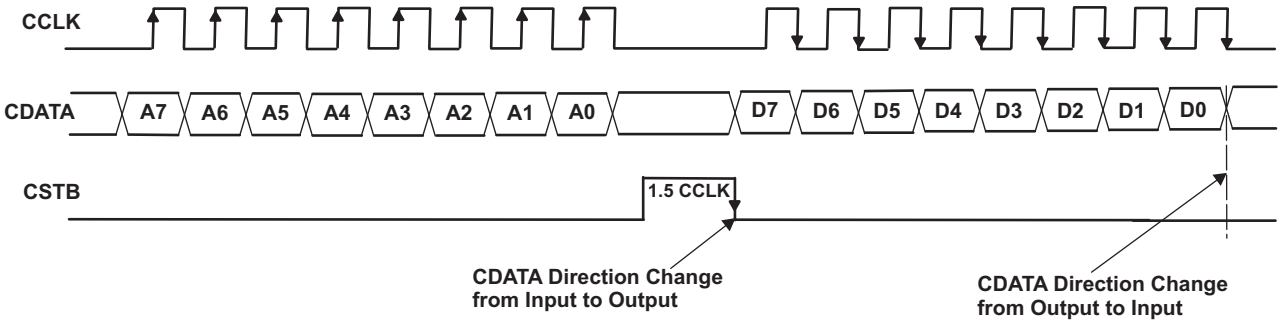


Figure 87. CSPI Read Format

Table 25 shows a register written, *RESERVED* in register map of CSPI. There are both registers for READ/WRITE. Even if data is written in the register for WRITE, the TPS65040 is not affected at all, and the TPS65040 continues the same operation before data is written. DATA doesn't change into the state of the output by the falling edge of CSTB, even if data is read from the READ register. The data is not output from TPS65040, and the CDATA pin maintains the input.

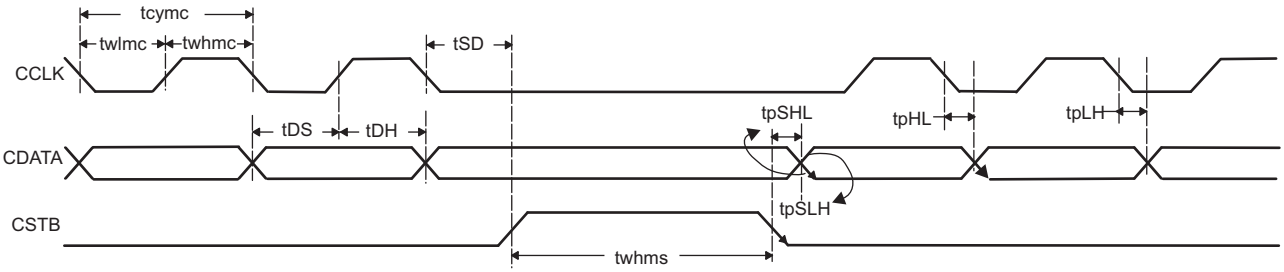


Figure 88. CSPI Timing

TSP

TSP is the interface that consists of three lines (TSPDIN pin, TSPCLK pin, and TSPEN pin as input). Data length is 16-BIT (12-BIT data, and 4-BIT address). Figure 89 shows WRITE format, while Figure 90 shows the WRITE timing of TSP. In a WRITE operation the first 4 BITs are the address bits, followed by 12 BITs of data. When TSPEN is low the address and data are taken by the rising edge of TSPCLK, and reflected by the rising edge of TSPEN. The register that TSP can control becomes AFCDATA, 2GLDOCTRL, and AFCDACCTL.

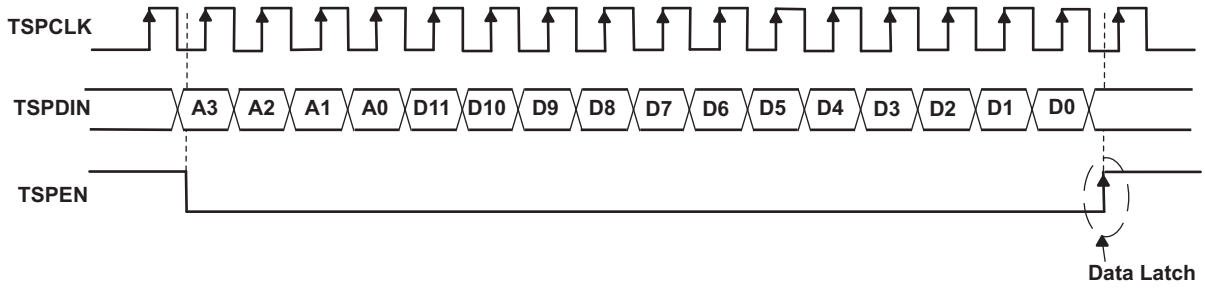


Figure 89. TSP Write Format

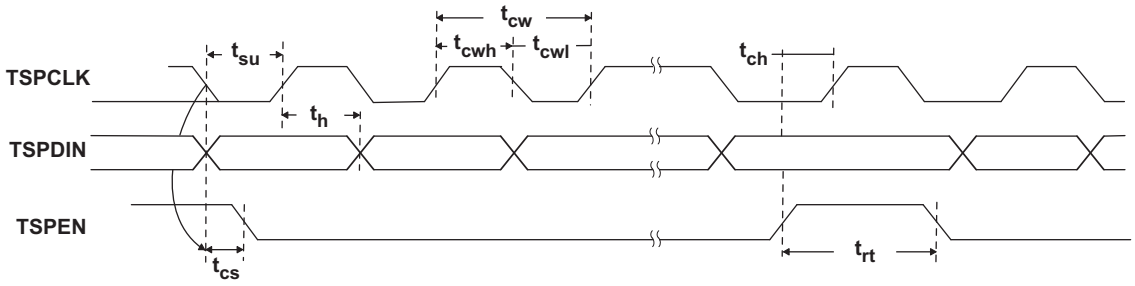


Figure 90. TSP Timing

REGISTER MAP

Table 25. CSPI Register Map

Address	R/W	Name	D7	D6	D5	D4	D3	D2	D1	F0
E0	W	PSCNT1W	PSCNT15	PSCNTR3V	non	non	non	non	non	PSCNT11
		Default	1	0	0	0	0	0	0	0
E1	W	Reserved	non	non	non	non	non	non	non	non
		Default	0	0	0	0	0	0	0	0
E2	W	Reserved	non	non	non	non	non	non	non	non
		Default	0	0	0	0	0	0	0	0
E3	W	Reserved	non	non	non	non	non	non	non	non
		Default	0	0	0	0	0	0	0	0
E4	R	AFCMSBR	non	non	non	non	D11	D10	D9	D8
		Default	0	0	0	0	1	0	0	0
E5	R	AFCLSBR	D7	D6	D5	D4	D3	D2	D1	D0
		Default	0	0	0	0	0	0	0	0
E6	R	ALM	TSD_FLAG	non	non	non	non	Temp Bit2	Temp Bit1	Temp Bit0
		Default	0	0	0	0	0	0	1	0
E7(1)	R	Reserved	non	non	non	non	non	non	non	non
		Default	0	0	0	0	0	0	0	0
E8	W	TSD_RESET	non	non	non	non	non	non	non	non
		Default	0	0	0	0	0	0	0	0
E9	W	Reserved	non	non	non	non	non	non	non	non
		Default	0	0	0	0	0	0	0	0
EA(2)	W	TEST	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0
		Default	0	0	0	0	0	0	0	0

(1) E7h explains the read register, but it can not read the 00h data after the CSTB low edge. It becomes High-Z condition during data read period.
(2) EAh is the test mode register for production test. Do not access this register.

Table 25. CSPI Register Map (continued)

Address	R/W	Name	D7	D6	D5	D4	D3	D2	D1	F0
EB	W	3GLDOW	PSCNTT3V	PSCNTDC/DC	PSCNT12	PSCNT13	non	PSCNTSYSCLK_UMTS	non	PSCNTDC/DC_EXT
		Default	0	1	1	1	0	1	1	0
EC	W	2GLDOW	GGE3ps mode	GGE2ps mode	GGE1ps mode	GGEmodecnt	PSCNTGGE3	PSCNT GGE2	PSCNT GGE1	PSCNT SYSCLK_GSM
		Default	1	1	1	1	1	1	1	1
ED	W	DACW	D7	D6	D5	D4	D3	D2	D1	D0
		Default	1	0	0	0	0	0	0	0
EE	W	Reserved	non	non	non	non	non	non	non	non
		Default	0	0	0	0	0	0	0	0
EF	R	VER	VCOD3	VCOD2	VCOD1	VCOD0	VER3	VER2	VER1	VER0
		Default	0	0	0	0	0	0	1	0
F0	W	AFCMSBW	non	non	non	non	D11	D10	D9	D8
		Default	0	0	0	0	1	0	0	0
F1	W	AFCLSBW	D7	D6	D5	D4	D3	D2	D1	D0
		Default	0	0	0	0	0	0	0	0
F2	W	AFCDACCTLW	non	non	non	non	non	non	non	PSCNTAFC
		Default	0	0	0	0	0	0	0	1
F3	R	PSCNT1R	PSCNT15	PSCNTR3V	non	non	non	non	non	PSCNT11
		Default	1	0	0	0	0	0	0	0
F4	R	3GLDOCTLR	PSCNTT3V	PSCNT DC/DC	PSCNT12	PSCNT13	non	PSCNTSYSCLK_UMTS	non	PSCNTDC/DC_EXT
		Default	0	1	1	1	0	1	1	0
F5	R	2GLDOCTLR	GGE3ps mode	GGE2ps mode	GGE1ps mode	GGEmode cnt	PSCNT GGE3	PSCNT GGE2	PSCNT GGE1	PSCNT SYSCLK_GSM
		Default	1	1	1	1	1	1	1	1
F6	R	DACR	D7	D6	D5	D4	D3	D2	D1	D0
		Default	1	0	0	0	0	0	0	0
F7	R	AFCDACCTLR	non	non	non	non	non	non	non	PSCNTAFC
		Default	0	0	0	0	0	0	0	1

Table 26. TSP Register Map

Address	R/W	Name	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	W	AFCDATA (1)	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		Default	1	0	0	0	0	0	0	0	0	0	0	0
1	W	2GLDOCTL	non	non	non	non	GGE3 psmode	GGE2 ps mode	GGE1 ps mode	GGE mode cnt	PSC NTG GE3	PSC NTG GE2	PSC NTG GE1	PSCNTS YSCLK _GSM
		Default	0	0	0	0	1	1	1	1	1	1	1	1
2	W	AFCDACCTL	non	non	non	non	non	non	non	non	non	non	non	PSC NTA FC
		Default	0	0	0	0	0	0	0	0	0	0	0	1

(1) AFCDATA is the same as AFCMSBW and AFCLSBW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS65040ZQE	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	71	360	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
TPS65040ZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	71	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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