WINSOURCE ELECTRONICS

THE DATASHEET OF

TPS715A01DRBRG4

TPS715A 80-mA, 24-V, 3.2-µA Quiescent Current, Low-Dropout Linear Regulator

1 Features

- Input voltage range:
  - 2.5 V to 24 V
- Available output voltage options:
  - Fixed: 1.8 V to 5 V
  - Adjustable: 1.205 V to 15 V
- Output current: Up to 80 mA
- Very low I_Q: 3.2 µA at 80-mA load current
- Overcurrent protection
- Package:
  - 3-mm × 3-mm VSON (DRB)
  - 2-mm × 2-mm WSON (DRV)
- Operating junction temperature: –40°C to +125°C
- For MSP430-specific output voltages see the TPS715

2 Applications

- Home and building automation
- Retail automation and payment
- Grid infrastructure
- Medical applications
- Lighting applications

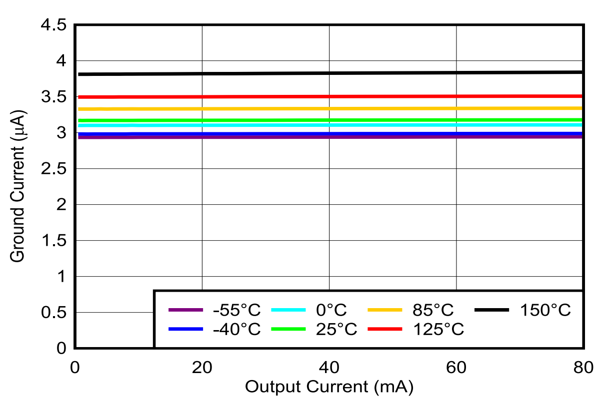


Figure 3-1. Quiescent Current vs Load Current for TPS715A (New Chip)

3 Description

The TPS715A low-dropout (LDO) linear voltage regulator is a low quiescent current device that offers the benefits of a wide input voltage range and low-power operation in miniaturized packaging. Thus, the TPS715A is designed for battery-powered applications and as a power-management attachment to low-power microcontrollers.

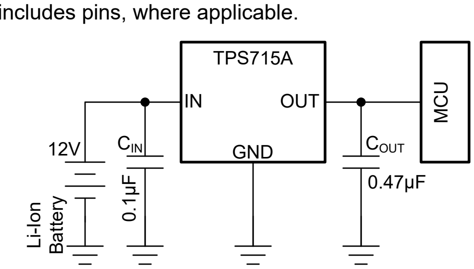
The TPS715A is available in both fixed and adjustable versions. For more flexibility or higher output voltages, the adjustable version uses external feedback resistors to set the output voltage from 1.205 V to 15 V. The TPS715A LDOs support a low dropout of 650 mV (typ) at 80 mA of load current. The low quiescent current (3.2 µA typically) is stable over the entire range of output load current (0 mA to 80 mA). The TPS715A (new chip) also features an internal soft-start to lower the inrush current. The built-in overcurrent limit helps protect the regulator in the event of a load short or fault.

The TPS715A is available in a 3-mm × 3-mm package for use in high power dissipation applications and a small 2-mm × 2-mm package for hand-held and ultra-portable applications. The 3-mm × 3-mm package is also available as a non-magnetic package for medical imaging applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS715A	DRB (VSON, 8)	3 mm × 3 mm
	DRV (WSON, 6)	2 mm × 2 mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

Table of Contents

4 Pin Configuration and Functions

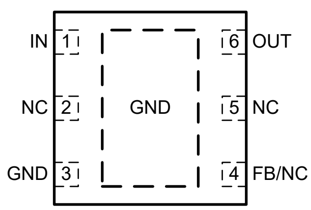


Figure 4-1. DRV Package, 6-Pin WSON (Top View)

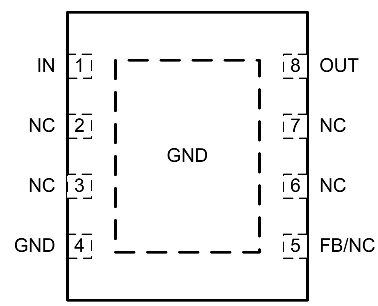


Figure 4-2. DRB Package, 8-Pin VSON (Top View)

Table 4-1. Pin Functions

NAME	VSON		WSON		I/O	DESCRIPTION
	FIXED	ADJ.	FIXED	ADJ.		
FB	—	5	—	4	I	In the adjustable configuration, this pin sets the output voltage with the help of the external feedback divider.
GND	4, Pad	4, Pad	3, Pad	3, Pad	—	Ground pin.
IN	1	1	1	1	I	Input supply pin. Use a capacitor with a value of 0.1 μF or larger from this pin to ground. See the *Input and Output Capacitor Requirements* section for more information.
NC	2, 3, 5, 6, 7	2, 3, 6, 7	2, 4, 5	2, 5	—	No connect pin. This pin is not connected internally. Connect this pin to ground for best thermal performance, or leave floating.
OUT	8	8	6	6	O	Output of the regulator. For the new chip, a capacitor with a value of 1 μF or larger is required from this pin to ground.(1) See the *Input and Output Capacitor Requirements* section for more information.

(1) The nominal output capacitance must be greater than 0.47 μF. Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 0.47 μF. The legacy chip is stable for any capacitor value ≥ 0.47 μF.

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
Voltage	V_{IN} (for legacy chip only)	–0.3	24	V
	V_{IN} (for new chip only)	–0.3	30	
	V_{OUT} (for fixed output new chip only)	–0.3	2 × $V_{OUT(typ)}$ or V_{IN} + 0.3 or 5.5 (whichever is lower)	
Voltage	V_{OUT} (for legacy chip only)	–0.3	16.5	V
Voltage	V_{OUT} (for adjustable output new chip only)	–0.3	V_{IN} + 0.3	V
	V_{FB} (for adjustable output new chip only)		2.4	
	V_{FB} (for adjustable output legacy chip only)	–0.3	4.5	
Current	Peak output current	Internally limited		
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.5		24	V
V_{OUT}	Output voltage	1.205		15	V
I_{OUT}	Output current	0		80	mA
C_{IN}	Input capacitor[(2)]	0	0.047		µF
C_{OUT}	Output capacitor (for legacy chip only)	0.47	1		
	Output capacitor (for new chip only) [(3)]	1			
T_J	Operating junction temperature	-40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.047 µF is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(3) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 0.47 µF minimum for the stability.

5.4 Thermal Information

THERMAL METRIC (1)		TPS715A (2)				UNIT
		DRV (WSON) 6 Pins		DRB (VSON) 8 Pins		
		Legacy chip	New chip	Legacy chip	New chip	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.5	69.5	69	55.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	110.5	108.0	76.8	82.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	35.4	44.6	29.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.2	5.9	8.1	6.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.3	35.4	44.8	29.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.3	7.2	27.5	8.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application note.

(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the Impact of board layout on LDO thermal performance application note.

5.5 Electrical Characteristics

over operating junction temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage [(1)]		I_O = 10 mA	2.5		24	V
			I_O = 80mA	3		24	
V_{OUT}	Output voltage range (TPS715A01) [legacy chip]			1.2		15	V
	Output voltage range (TPS715A01) [new chip]			1.205		15	
V_{OUT}	Output voltage accuracy [(1)]	TPS715A01 (legacy chip)	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, 1.2 V ≤ V_{OUT} ≤ 15 V, 0 ≤ I_{OUT} ≤ 80 mA	–4		4	%
		TPS715A01 (new chip)	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, 1.205 V ≤ V_{OUT} ≤ 15 V, 0 ≤ I_{OUT} ≤ 80 mA	–4		4	
		TPS715A33 (legacy chip)	4.3 V ≤ V_{IN} ≤ 24 V, 0 ≤ I_{OUT} ≤ 80 mA	3.135	3.3	3.465	V
		TPS715A33 (new chip)	4.3 V ≤ V_{IN} ≤ 24 V, 0 ≤ I_{OUT} ≤ 80 mA	3.168	3.3	3.432	
I_{GND}	Ground pin current (legacy chip) [(3)]		0 ≤ I_{OUT} ≤ 80mA, T_J = –40°C to 85°C		3.2	4.1	µA
			0 mA ≤ I_{OUT} ≤ 80mA		3.2	4.3	
			0 mA ≤ I_{OUT} ≤ 80mA, V_{IN} = 24 V			4.5	
	Ground pin current (new chip) [(3)]		0 ≤ I_{OUT} ≤ 80mA, T_J = –40°C to 85°C		3.2	4.2	
			0 mA ≤ I_{OUT} ≤ 80mA		3.2	4.8	
			0 mA ≤ I_{OUT} ≤ 80mA, V_{IN} = 24 V			5.8	
$\Delta V_{OUT\ (\Delta IOUT)}$	Load regulation		I_{OUT} = 100 µA to 80 mA		35		mV
$\Delta V_{OUT\ (\Delta VIN)}$	Output voltage line regulation (legacy chip) [(1)]		$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 24 V		20	60	mV
	Output voltage line regulation (new chip) [(1)]		$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 24 V		20	22	
V_n	Output noise voltage (legacy chip) [(4)]		BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		575		µVrms
	Output noise voltage (new chip)[(4)]		BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		425		
I_{CL}	Output current limit (legacy chip)		V_{OUT} = 0 V	160		1100	mA
	Output current limit (new chip)		V_{OUT} = 0 V, V_{IN} ≥ 3.5 V	160		500	
	Output current limit (new chip)		V_{OUT} = 0 V, V_{IN} < 3.5 V	90		500	
PSRR	Power-supply ripple rejection (legacy chip)		f = 100 kHz, C_{OUT} = 10 µF		60		dB
	Power-supply ripple rejection (new chip)				60		
V_{DO}	Dropout voltage (legacy chip)		V_{IN} = $V_{OUT(nom)}$ – 0.1 V, I_{OUT} = 80 mA		670	1120	mV
	Dropout voltage (new chip)				650	900	

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or the value shown for *Input voltage* in this table, whichever is greater.
(2) This device employs a leakage null control circuit. This circuit is active only if output current is less than pass transistor leakage current. The circuit is typically active when output load is less than 5 µA, V_{IN} is greater than 18 V, and die temperature is greater than 100°C.
(3) See the *Device Nomenclature*section for details about new and legacy chip descriptions.

5.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

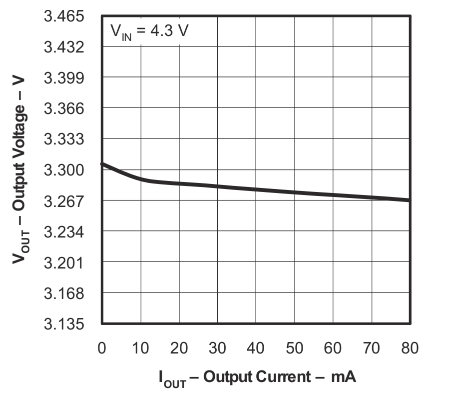


Figure 5-1. TPS715A33 Output Voltage vs Output Current (Legacy Chip)

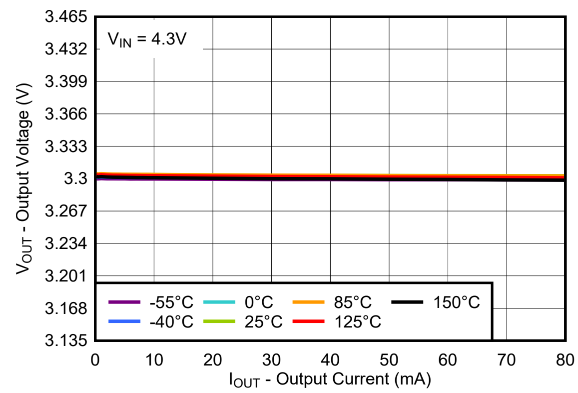


Figure 5-2. TPS715A33 Output Voltage vs Output Current (New Chip)

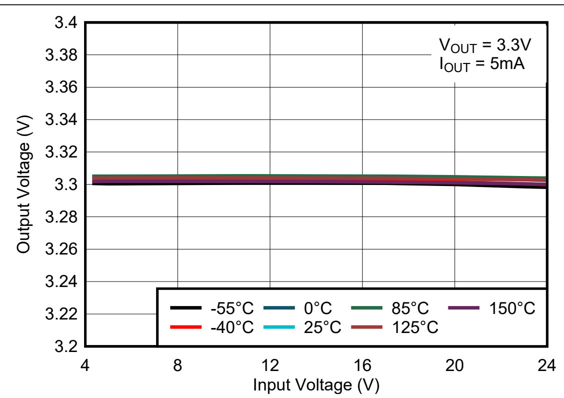


Figure 5-3. TPS715A33 Output Voltage vs Input Voltage (New Chip)

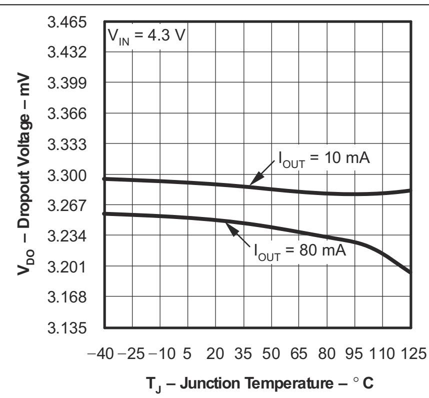


Figure 5-4. Output Voltage vs Junction Temperature (Legacy Chip)

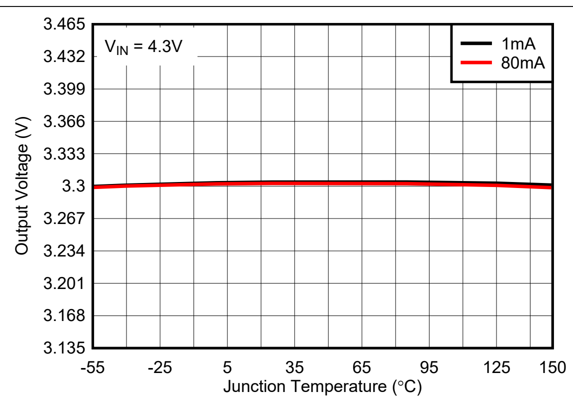


Figure 5-5. Output Voltage vs Junction Temperature (New Chip)

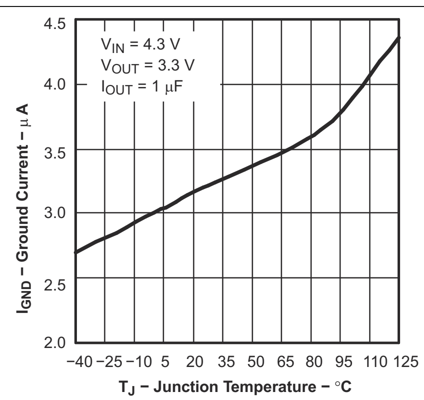


Figure 5-6. Ground Current vs Junction Temperature (Legacy Chip)

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

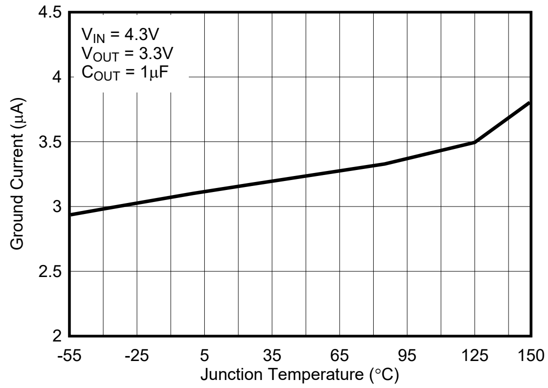


Figure 5-7. Ground Current vs Junction Temperature (New Chip)

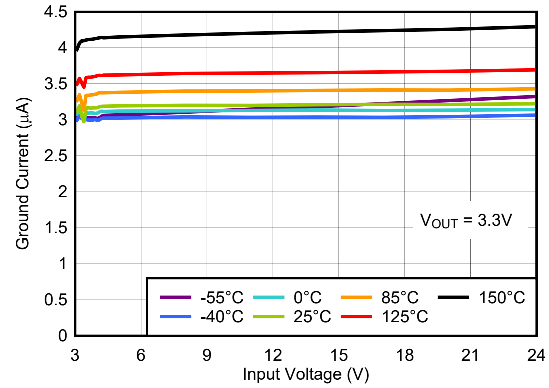


Figure 5-8. Ground Pin Current vs Input Voltage (New Chip)

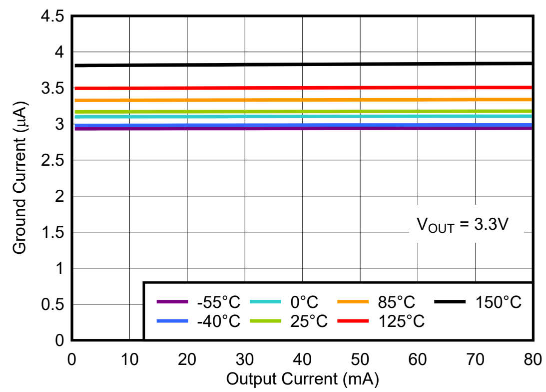


Figure 5-9. Ground Pin Current vs Load Current (New Chip)

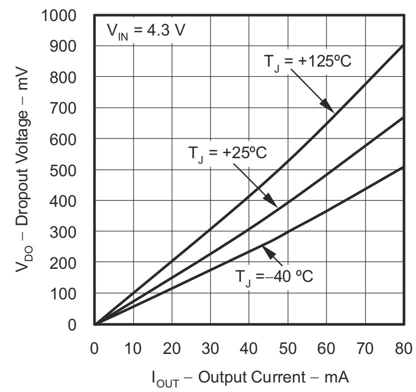


Figure 5-10. TPS715A33 Dropout Voltage vs Output Current (Legacy Chip)

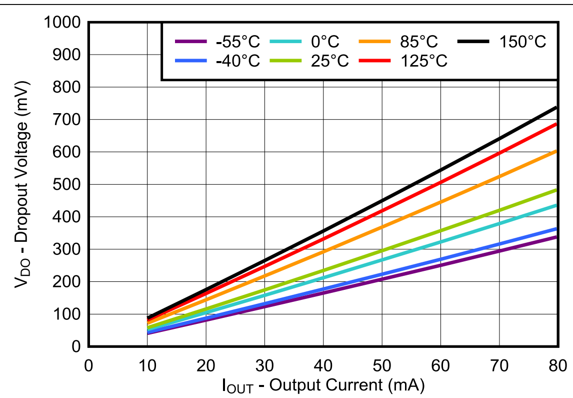


Figure 5-11. TPS715A33 Dropout Voltage vs Output Current (New Chip)

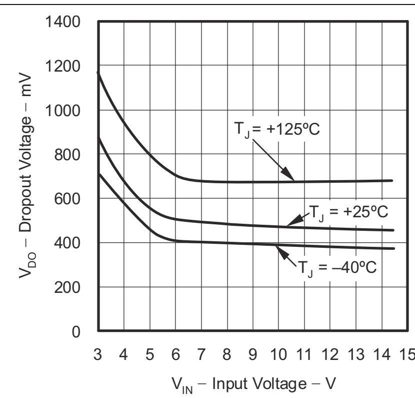


Figure 5-12. TPS715A01 Dropout Voltage vs Input Voltage (Legacy Chip)

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

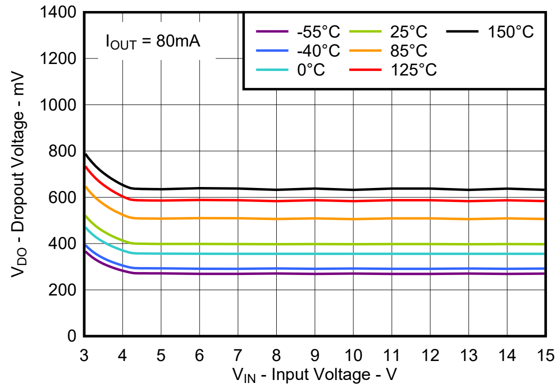


Figure 5-13. TPS715A01 Dropout Voltage vs Input Voltage (New Chip)

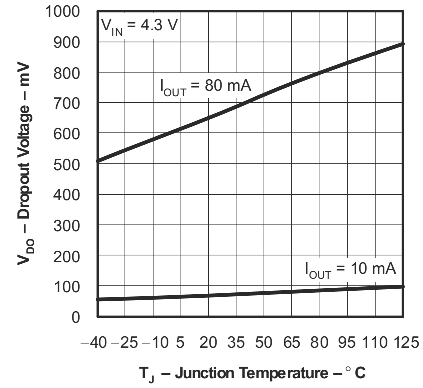


Figure 5-14. TPS715A33 Dropout Voltage vs Junction Temperature (Legacy Chip)

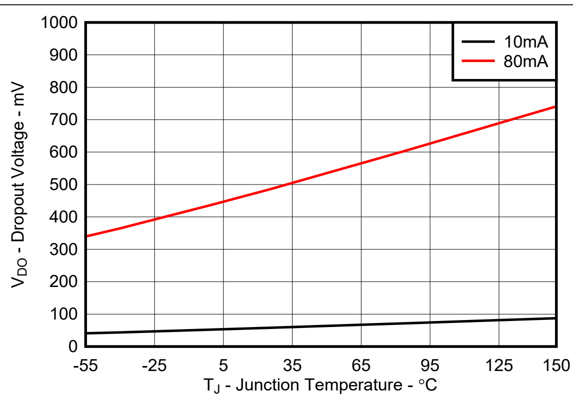


Figure 5-15. TPS715A33 Dropout Voltage vs Junction Temperature (New Chip)

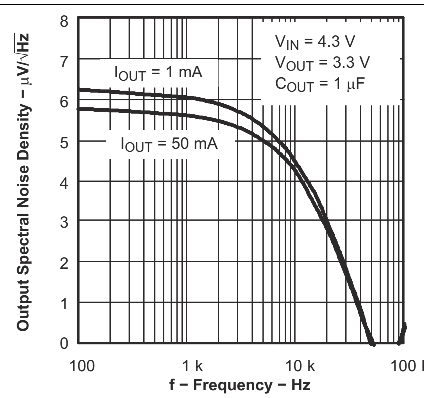


Figure 5-16. Output Spectral Noise Density vs Frequency (Legacy Chip)

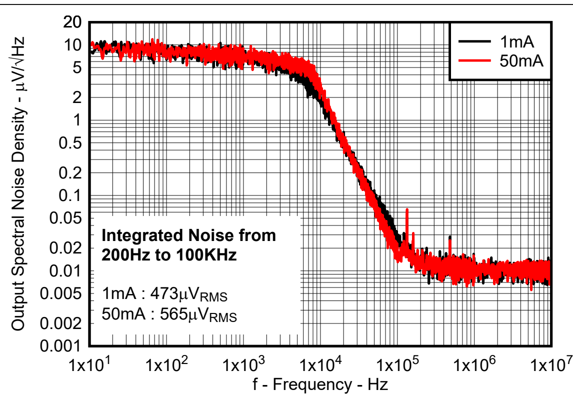


Figure 5-17. Output Spectral Noise Density vs Frequency (New Chip)

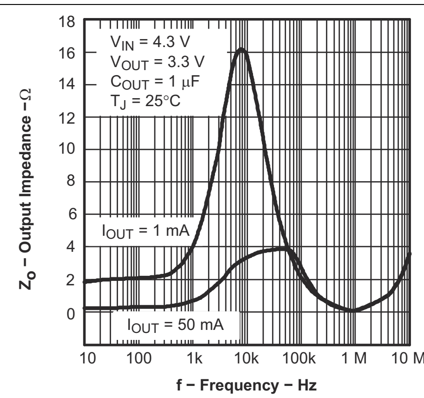


Figure 5-18. Output Impedance vs Frequency (Legacy Chip)

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

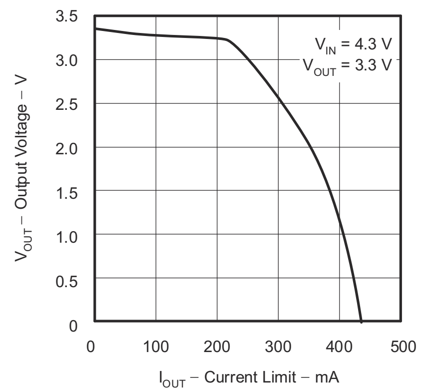


Figure 5-19. Output Voltage vs Current Limit (Legacy Chip)

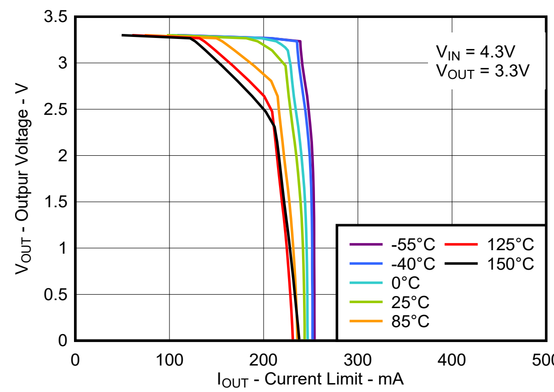


Figure 5-20. Output Voltage vs Current Limit (New Chip)

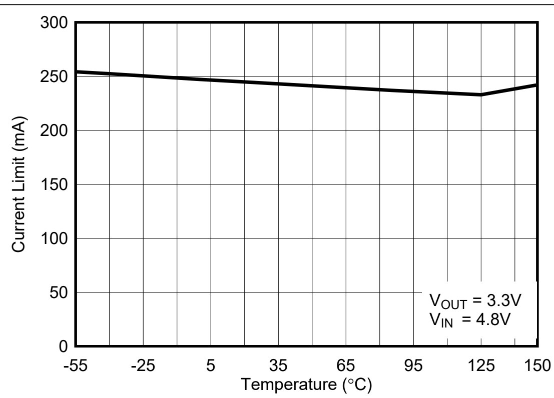


Figure 5-21. Current Limit vs Junction Temperature (New Chip)

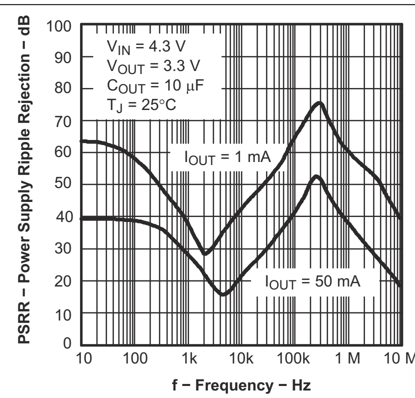


Figure 5-22. Power-Supply Ripple Rejection vs Frequency (Legacy Chip)

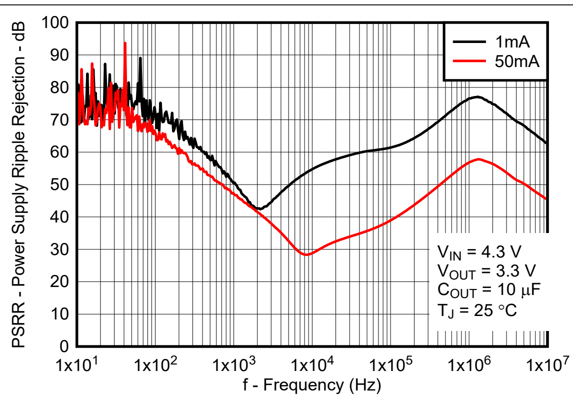


Figure 5-23. Power-Supply Ripple Rejection vs Frequency (New Chip)

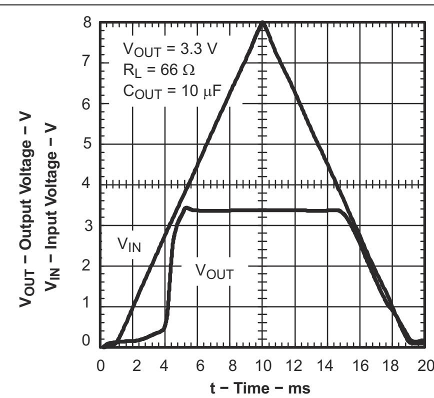


Figure 5-24. Power-Up and Power-Down (Legacy Chip)

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

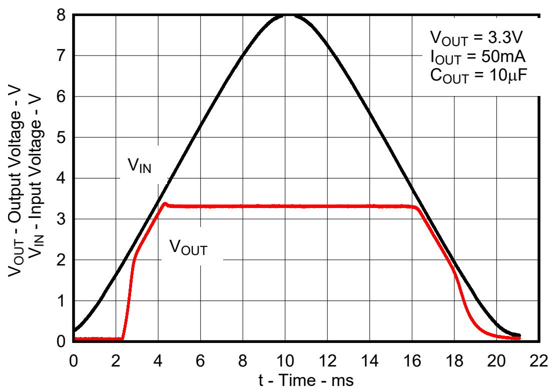


Figure 5-25. Power-Up, Power-Down (New Chip)

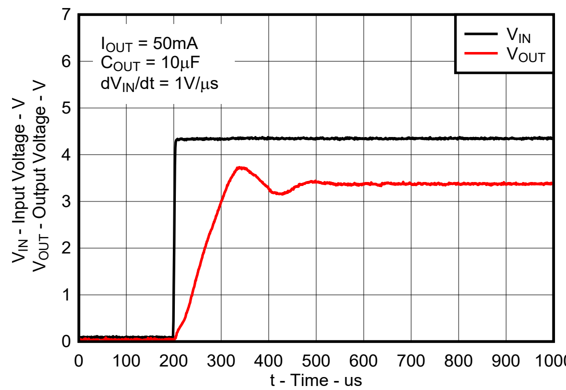


Figure 5-26. Fast Power-Up (Legacy Chip)

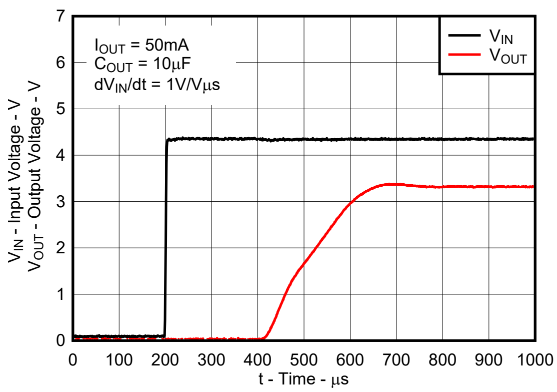


Figure 5-27. Fast Power-Up (New Chip)

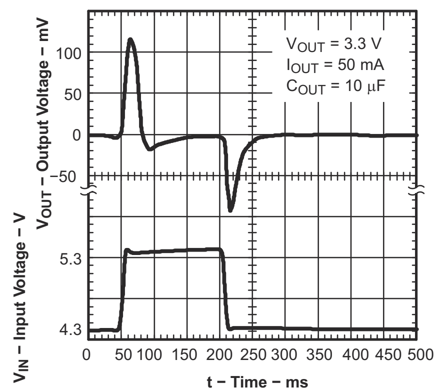


Figure 5-28. Line Transient Response (Legacy Chip)

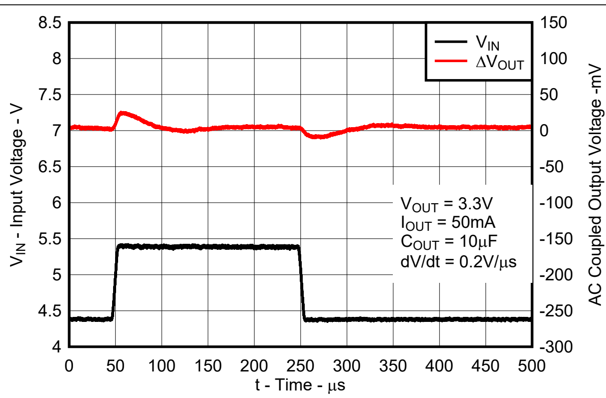


Figure 5-29. Line Transient Response (New Chip)

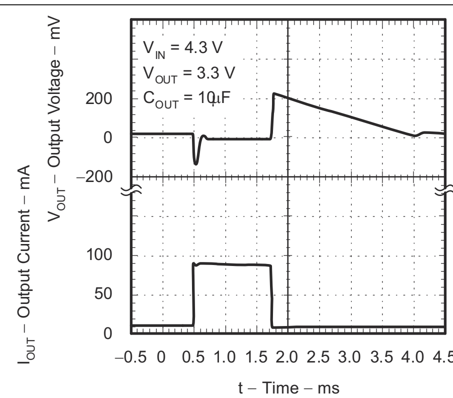


Figure 5-30. Load Transient Response (Legacy Chip)

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

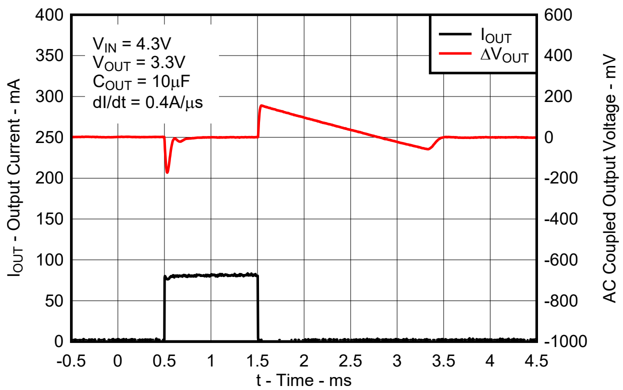


Figure 5-31. Load Transient Response (New Chip)

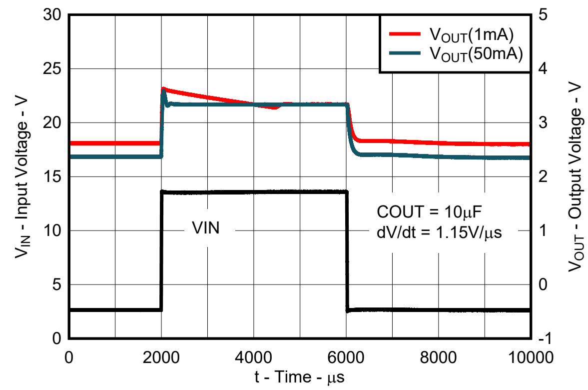


Figure 5-32. Line Transient Response (New Chip)

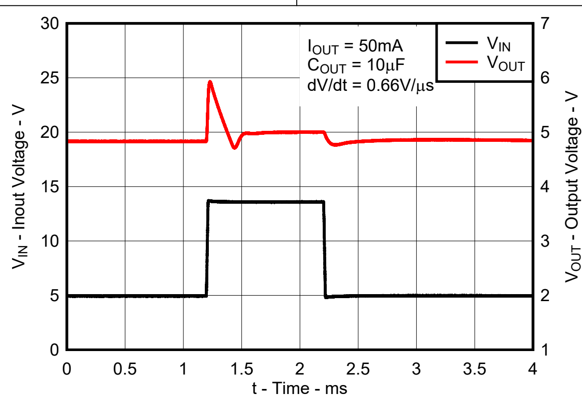


Figure 5-33. Dropout Exit Transient Response (New Chip)

6 Detailed Description

6.1 Overview

The TPS715A low-dropout regulator (LDO) consumes only 3.2 µA (typ) of quiescent current across the entire output current range, while offering a wide input voltage range and low-dropout voltage in small packaging. The device, which operates over an input range of 2.5 V to 24 V, is stable with any output capacitance greater than or equal to 0.47 µF. The low quiescent current across the complete load current range makes the TPS715A optimal for powering battery-operated applications. The TPS715A has internal soft-start to control inrush current into the output capacitor. This LDO also has overcurrent protection during a load-short or fault condition on the output.

6.2 Functional Block Diagrams

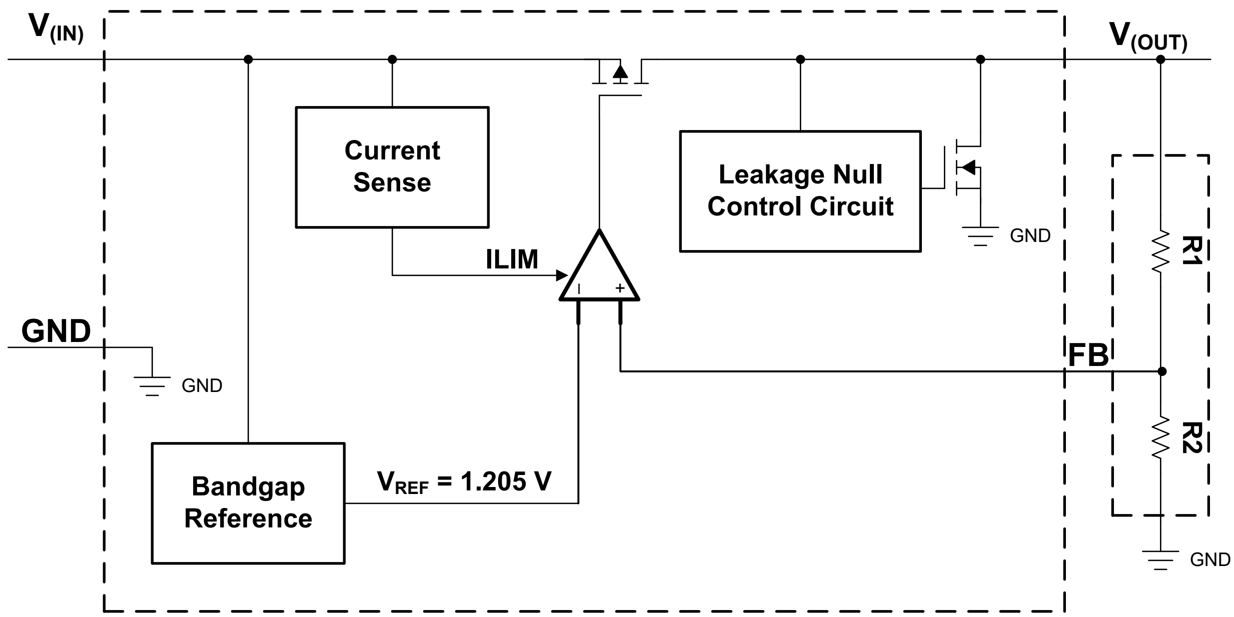


Figure 6-1. Functional Block Diagram: Adjustable Version

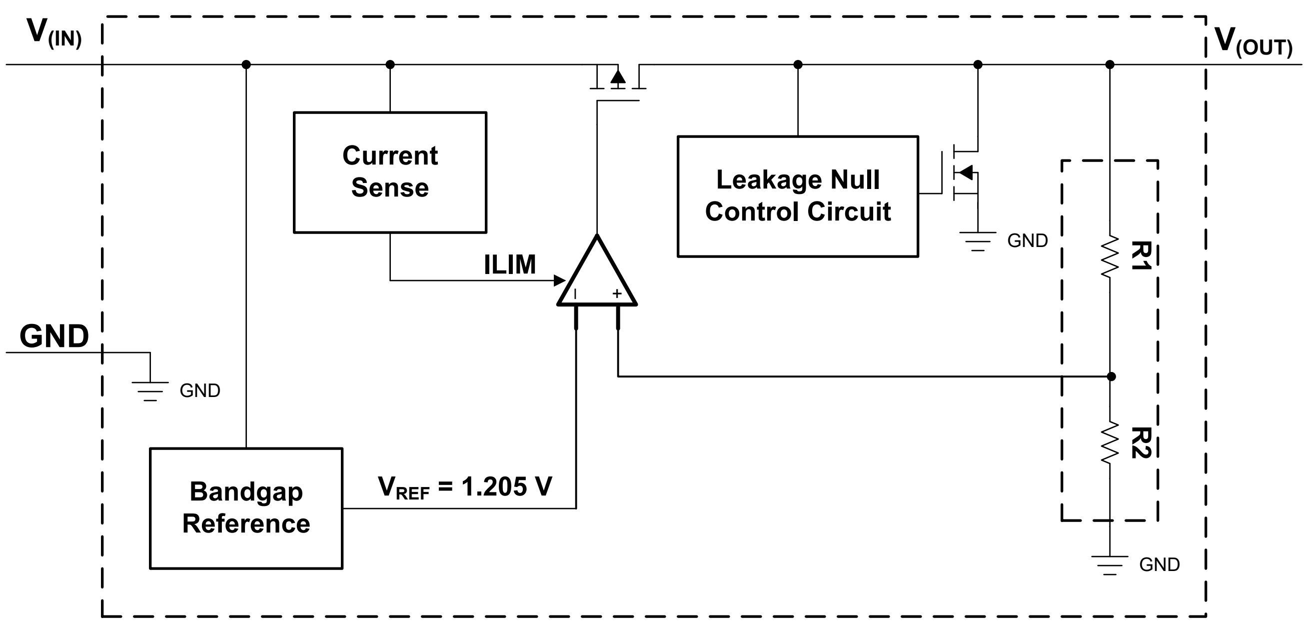


Figure 6-2. Functional Block Diagram: Fixed Version

6.3 Feature Description

6.3.1 Wide Supply Range

This device has an operational input supply range of 2.5 V to 24 V, allowing for a wide range of applications. This wide supply range is optimal for applications that have either large transients or high dc voltage supplies.

6.3.2 Low Supply Current

This device only requires 3.2 µA (typical) of quiescent current across the complete load current range (0 mA to 80 mA) and has a maximum current consumption of 4.8 µA (for the new device only) at –40°C to +125°C.

6.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. For more information on current limits, see the *Know Your Limits* application note. The LDO is not designed to operate in a steady-state current limit.

Figure 6-3 shows a diagram of the current limit.

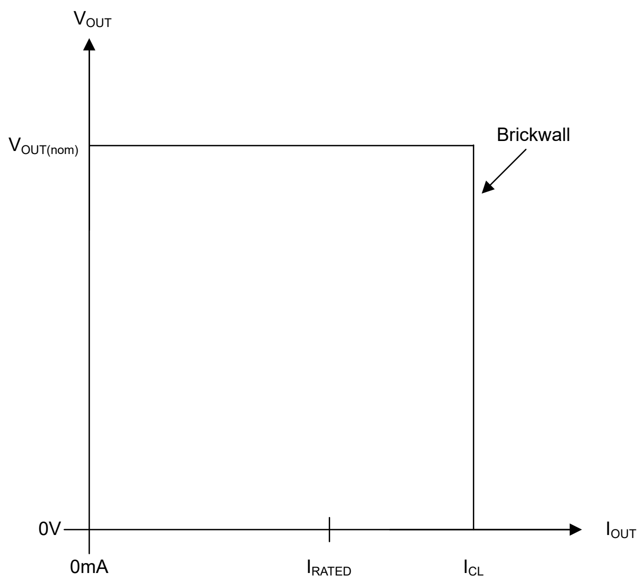


Figure 6-3. Current Limit

6.3.4 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use Equation 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.4 Device Functional Modes

Table 6-1 provides a quick comparison between the normal and dropout modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS715A LDO regulator is designed for battery-powered applications and is a good supply for low-power microcontrollers (such as the MSP430) because of the device low I_Q performance across load current range. The ultra-low-supply current of the TPS715A maximizes efficiency at light loads, and the high input voltage range and flexibility of output voltage selection in the adjustable configuration and fixed output levels makes the device an optimal supply for building automation and power tools.

7.2 Typical Applications

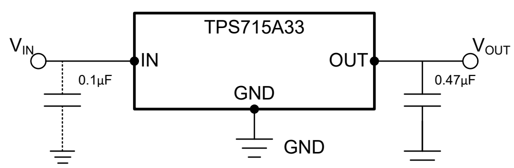
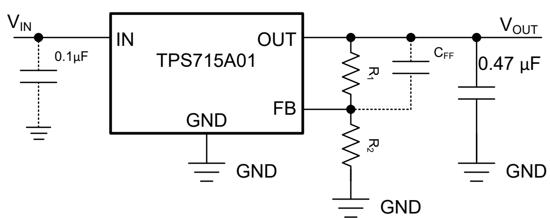


Figure 7-1. Typical Application Circuit (Fixed-Voltage Version)



Output Voltage	R1	R2
1.8V	0.499 MΩ	1MΩ
2.8V	1.33 MΩ	1MΩ
5.0V	3.16 MΩ	1MΩ

Figure 7-2. TPS715A01 Adjustable LDO Regulator Programming

7.2.1 Design Requirements

Minimum output capacitor (C_{OUT}) value for stability is needed as suggested in the *Recommended Operating Conditions* table.

Table 7-1 summarizes the design requirements for this application.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage	4.3 V
Output voltage	3.3 V
Output current	50 mA

7.2.2 Detailed Design Procedure

7.2.2.1 Setting V_{OUT} for the TPS715A01 Adjustable LDO

The TPS715A contains an adjustable version, the TPS715A01, which sets the output voltage using an external resistor divider as shown in Figure 7-2. The output voltage operating range is 1.205 V to 15 V, and is calculated using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

where:

- V_{REF} = 1.205 V (typical)

Choosing resistors R1 and R2 allows approximately 1.5 µA of current through the resistor divider. Lower value resistors can be used for improved noise performance, but consume more power. Avoid higher resistor values because leakage current into or out of FB across R1 / R2 creates an offset voltage that is proportional to V_{OUT} divided by V_{REF}. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using Equation 3:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (3)$$

Figure 7-2 depicts this configuration.

7.2.2.2 External Capacitor Requirements

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

Although not required, use a 0.1-µF or larger input bypass capacitor, connected between IN and GND and located close to the device, to improve transient response and noise rejection of the power supply as a whole. A higher-value input capacitor can be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

7.2.2.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5 Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of a large output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.2.2.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the PMOS pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

Figure 7-3 shows one approach for protecting the device.

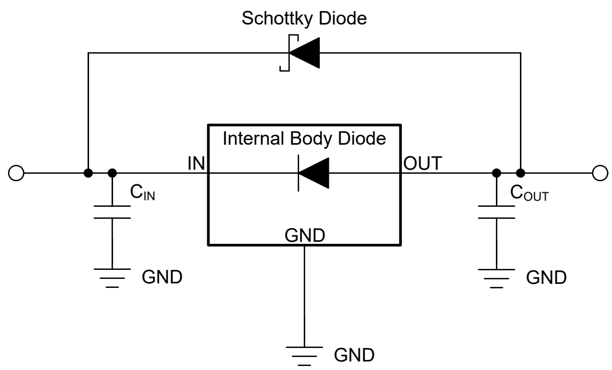


Figure 7-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.2.2.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

$C_{FF} \geq 10$ pF is required for stability if the feedback divider current is less than 5 μA. Equation 6 calculates the feedback divider current.

$$I_{FB\_Divider} = V_{OUT} / (R_1 + R_2) \quad (6)$$

To avoid start-up time increases from C_{FF}, limit the product $C_{FF} \times R_1 < 50$ μs.

For an output voltage of 1.205 V with the FB pin tied to the OUT pin, no C_{FF} is used.

7.2.2.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (7)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{θJA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{θJA} \times P_D) \quad (8)$$

Thermal resistance ($R_{θJA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.2.2.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter ($ψ_{JT}$) and junction-to-board characterization parameter ($ψ_{JB}$). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter ($ψ_{JT}$) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter ($ψ_{JB}$) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + ψ_{JT} \times P_D \quad (9)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + ψ_{JB} \times P_D \quad (10)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.2.3 Application Curves

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 μF, and C_{OUT} = 1 μF (unless otherwise noted)

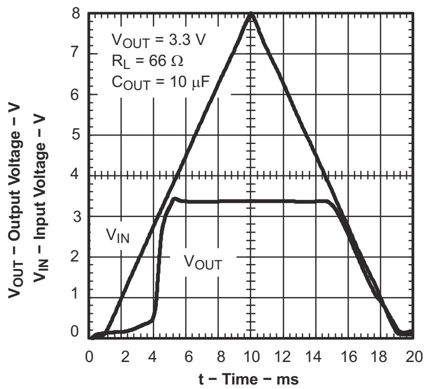


Figure 7-4. Power-Up and Power-Down (Legacy Chip)

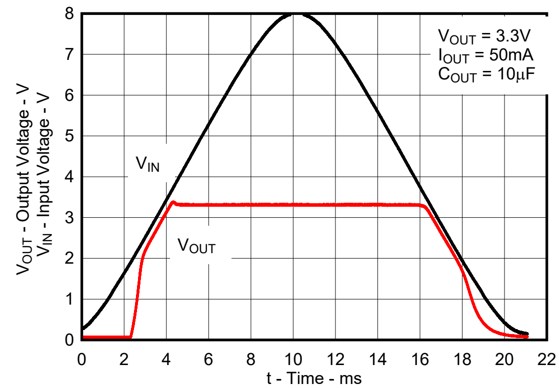


Figure 7-5. Power-Up, Power-Down (New Chip)

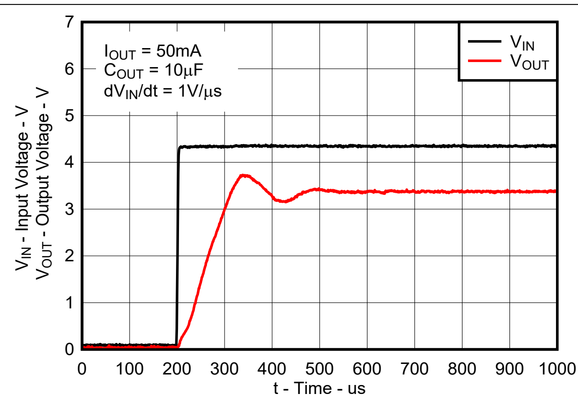


Figure 7-6. Fast Power-Up (Legacy Chip)

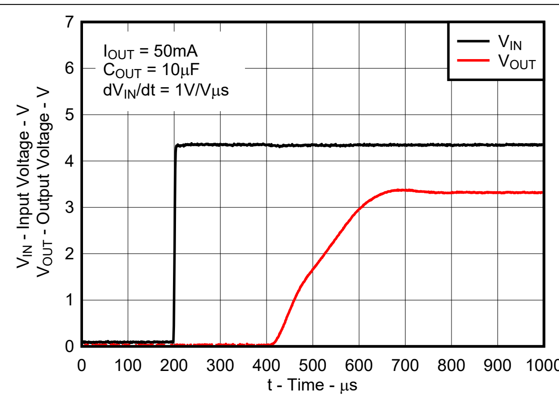


Figure 7-7. Fast Power-Up (New Chip)

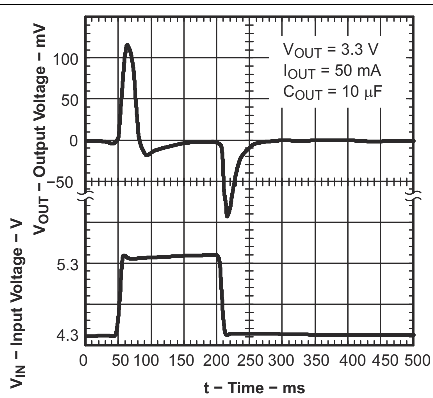


Figure 7-8. Line Transient Response (Legacy Chip)

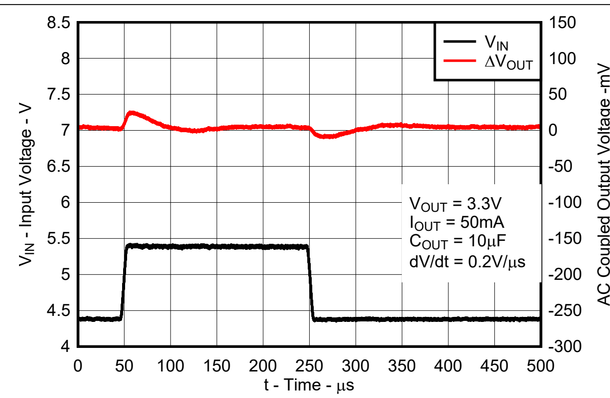


Figure 7-9. Line Transient Response (New Chip)

7.2.3 Application Curves (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)

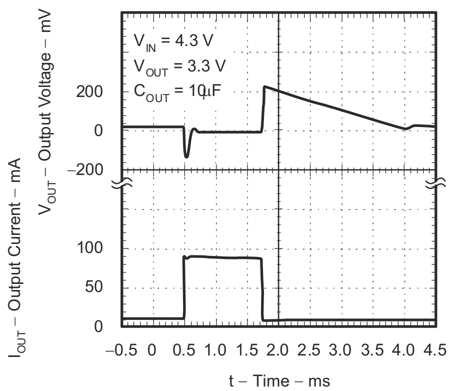


Figure 7-10. Load Transient Response (Legacy Chip)

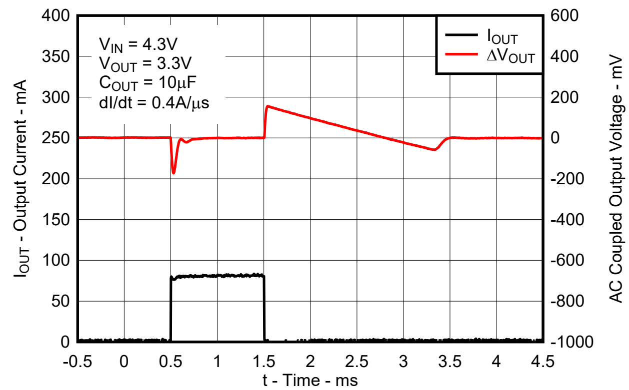


Figure 7-11. Load Transient Response (New Chip)

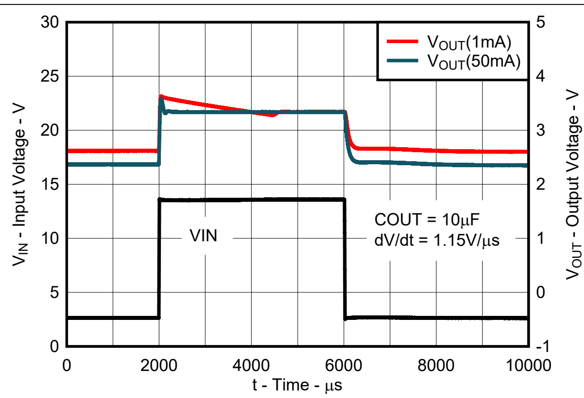


Figure 7-12. Line Transient Response (New Chip)

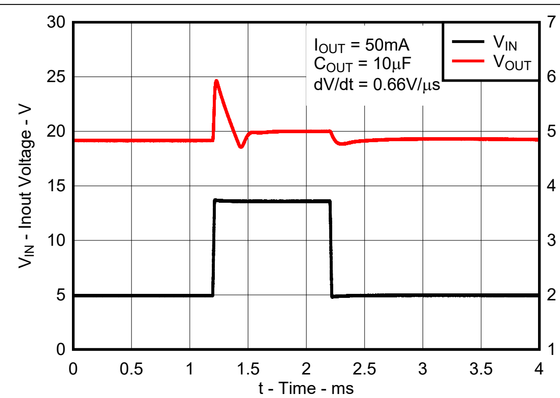


Figure 7-13. Dropout Exit Transient Response (New Chip)

7.3 Best Design Practices

Place at least one 0.47-µF capacitor as close as possible to the OUT and GND pins of the regulator.

Do not connect the output capacitor to the regulator using a long, thin trace.

Connect an input capacitor of 0.047 µF as close as possible to the IN and GND pins of the regulator for best performance.

Do not exceed the absolute maximum ratings.

7.4 Power Supply Recommendations

The TPS715A is designed to operate with an input voltage supply range from 2.5 V to 24 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.5 Layout

7.5.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the printed circuit board (PCB) and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. Avoid using vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or the resistor divider because doing so negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is recommended to be embedded either in the PCB or located on the bottom side of the PCB opposite the components. This reference plane provides accuracy of the output voltage and shields the LDO from noise.

7.5.1.1 Power Dissipation

To provide reliable operation, worst-case junction temperature must not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To make sure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 11.

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (11)$$

where:

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table)
- T_A is the ambient temperature

The regulator power dissipation is calculated using Equation 12.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (12)$$

For a higher power package version of the TPS715A, see the TPS715A.

7.5.2 Layout Example

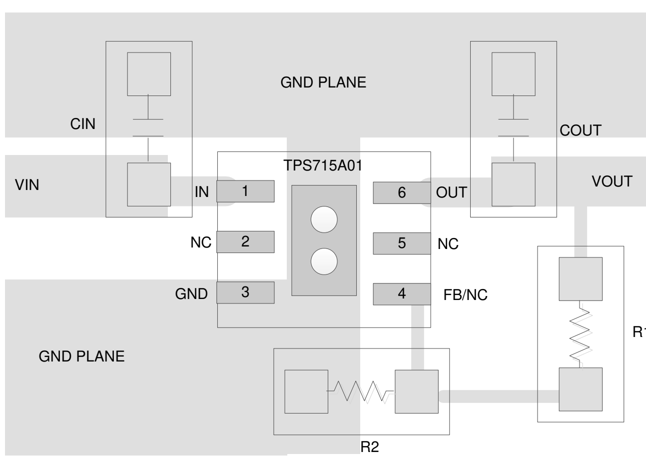


Figure 7-14. Example Layout for the TPS715A01DRV

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS715A. The TPS715AXXEVM-065 evaluation module (and related user's guide) can be requested at the TI web site through the product folders or purchased directly from the TI eStore.

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS715A is available through the product folders under *Tools & Software*.

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS715A**xxyyyz** Legacy chip	**xx** is the nominal output voltage (for example, 33 = 3.3V, 01 = adjustable) **yyy** is the package designator **z** is the package quantity
TPS715A**xxyyyz M3** New chip	**xx** is the nominal output voltage (for example, 33 = 3.3V, 01 = adjustable) **yyy** is the package designator **z** is the package quantity **M3** is a suffix designator for new chip redesigns on the latest TI process technology.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS715AxxEVM* user guide
- Texas Instruments, *LDO Noise Demystified* application note
- Texas Instruments, *LDO PSRR Measurement Simplified* application note
- Texas Instruments, *A Topical Index of TI LDO Application Notes* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (March 2016) to Revision I (November 2023) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Changed entire document to align with current family format... 1
- Changed SON to WSON (for DRV) or VSON (for DRB) throughout document.. 1

Changes from Revision G (May 2015) to Revision H (March 2016) — **Page**

- Changed third *Applications* bullet 1
- Added package designators to *Device Information* table for clarity 1
- Changed pin numbers in *Pin Functions* table to align with pin out configurations.. 2
- Added last three items to *Related Documentation* 22

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS715A01DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANO	Samples
TPS715A01DRBRG4	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANO	Samples
TPS715A01DRBRM3	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ANO	Samples
TPS715A01DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SBE	Samples
TPS715A01DRVRM3	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBE	Samples
TPS715A30DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SAV	Samples
TPS715A30DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SAV	Samples
TPS715A33DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANN	Samples
TPS715A33DRBRM3	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ANN	Samples
TPS715A33DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANN	Samples
TPS715A33DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ANN	Samples
TPS715A33DRVRM3	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ANN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

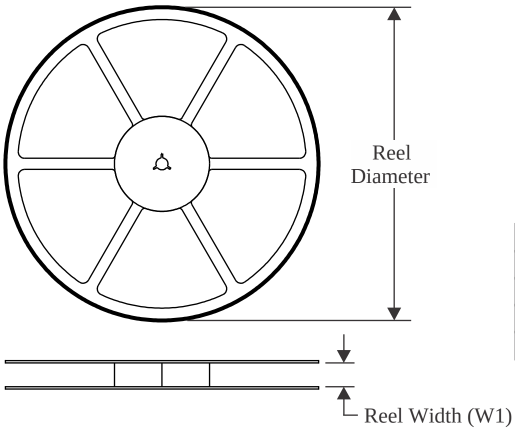
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

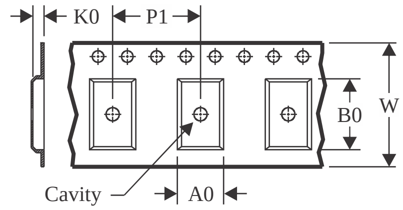
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

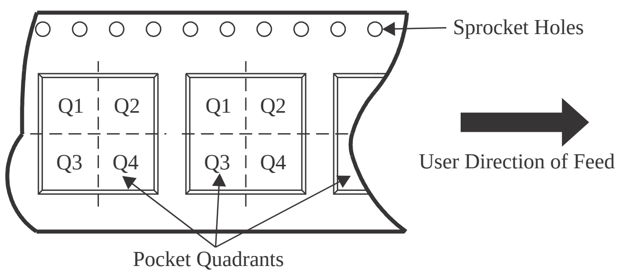


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

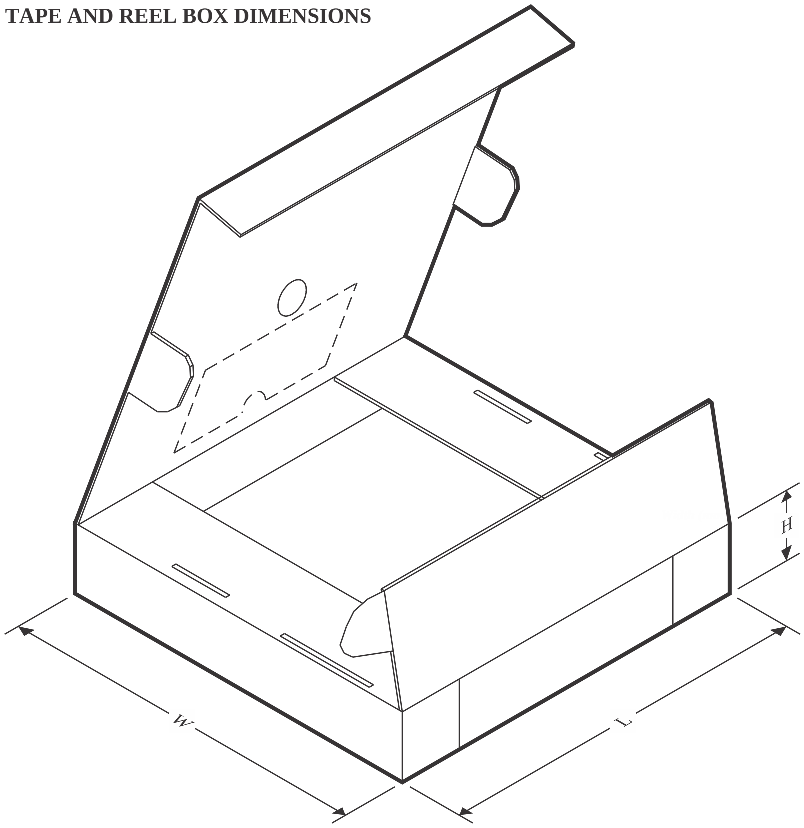
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

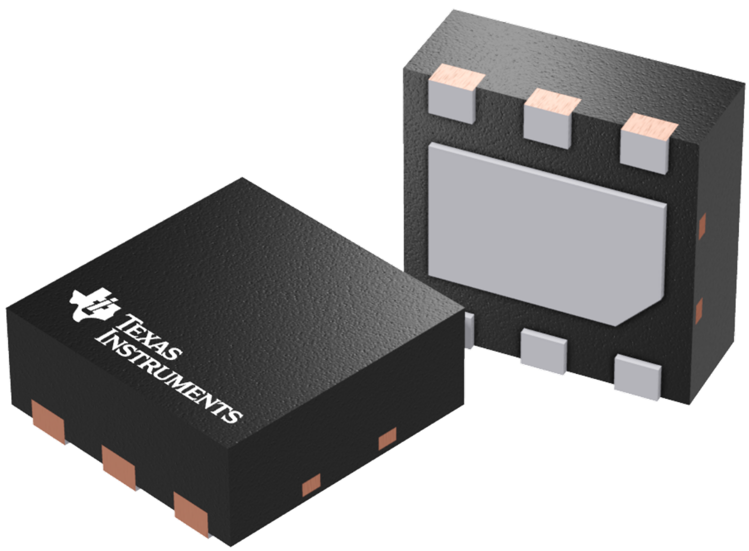
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS715A01DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS715A01DRBRM3	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS715A01DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS715A01DRVRM3	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS715A30DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS715A30DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS715A33DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS715A33DRBRM3	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS715A33DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS715A33DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS715A33DRVRM3	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

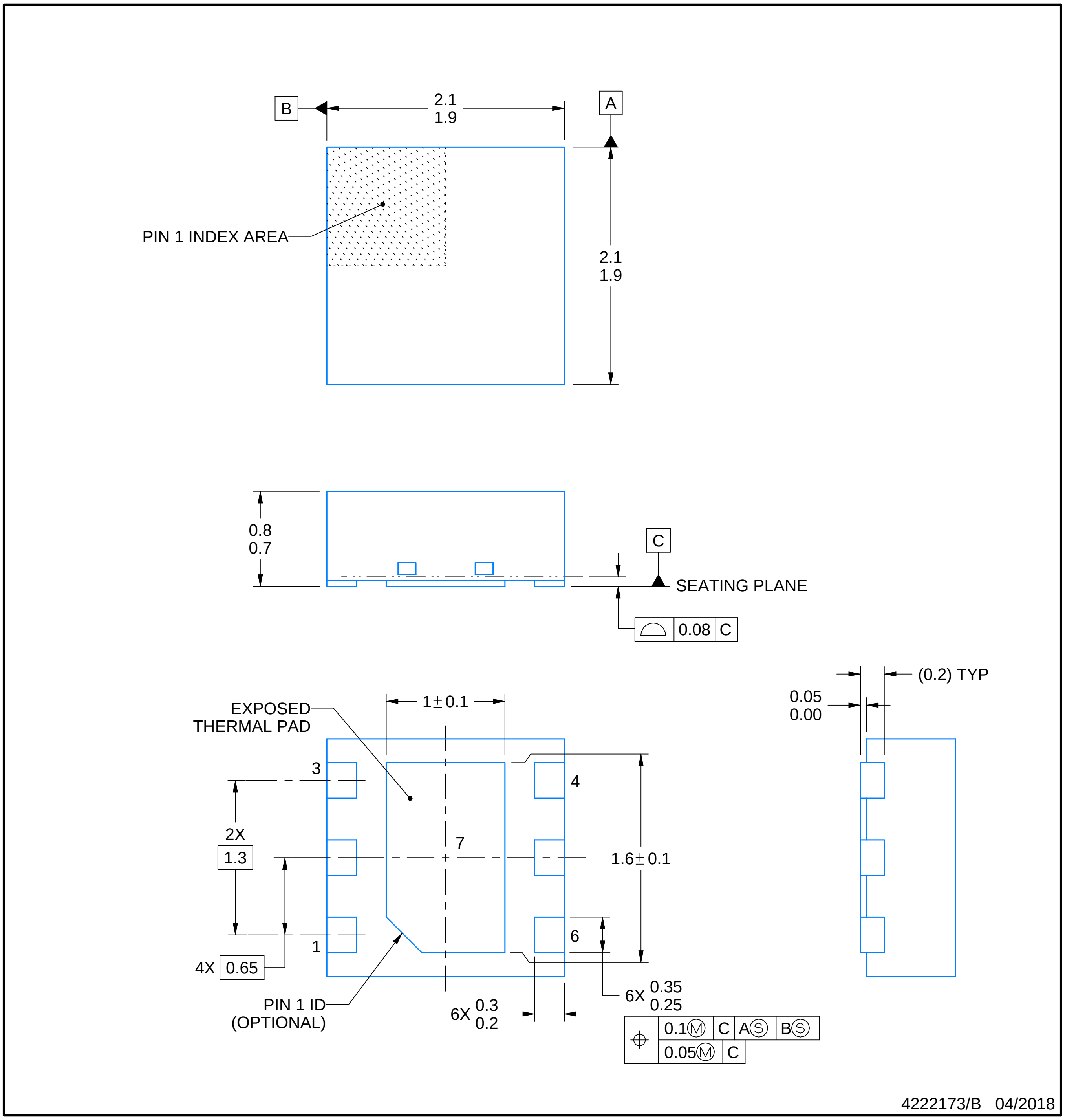


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS715A01DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS715A01DRBRM3	SON	DRB	8	3000	367.0	367.0	35.0
TPS715A01DRVR	WSON	DRV	6	3000	213.0	191.0	35.0
TPS715A01DRVRM3	WSON	DRV	6	3000	210.0	185.0	35.0
TPS715A30DRVR	WSON	DRV	6	3000	195.0	200.0	45.0
TPS715A30DRVT	WSON	DRV	6	250	213.0	191.0	35.0
TPS715A33DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS715A33DRBRM3	SON	DRB	8	3000	367.0	367.0	35.0
TPS715A33DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS715A33DRVR	WSON	DRV	6	3000	213.0	191.0	35.0
TPS715A33DRVRM3	WSON	DRV	6	3000	210.0	185.0	35.0

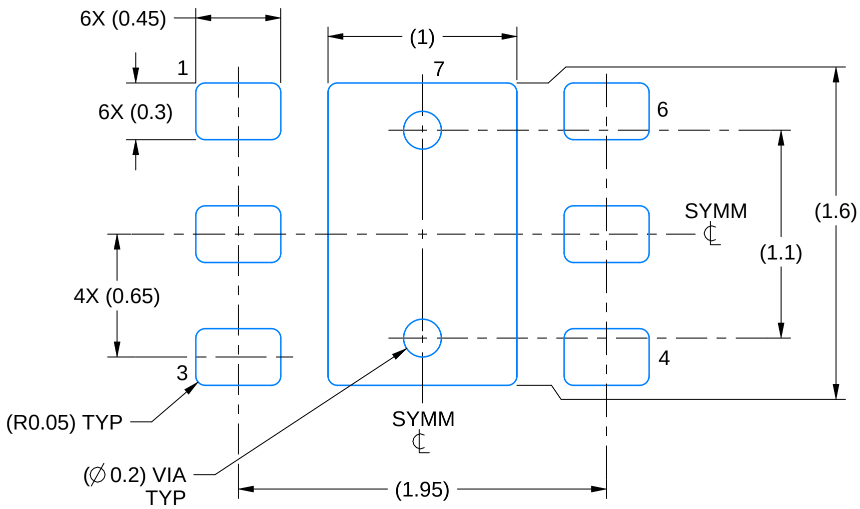


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

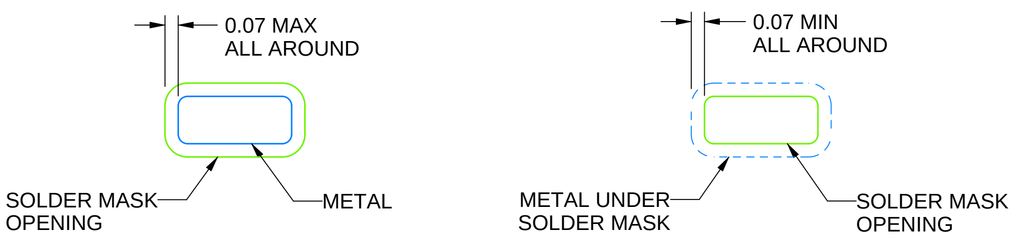


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



NON SOLDER MASK
DEFINED
(PREFERRED)

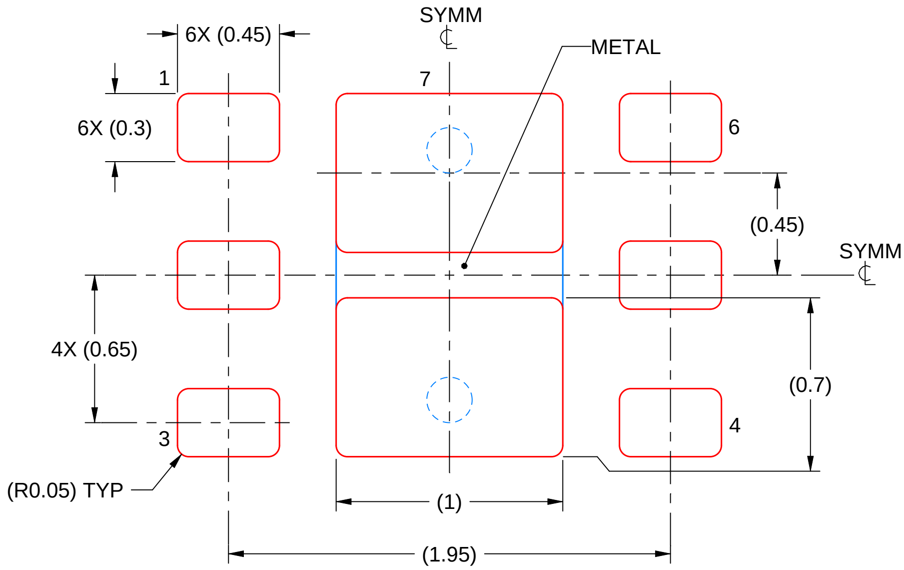
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



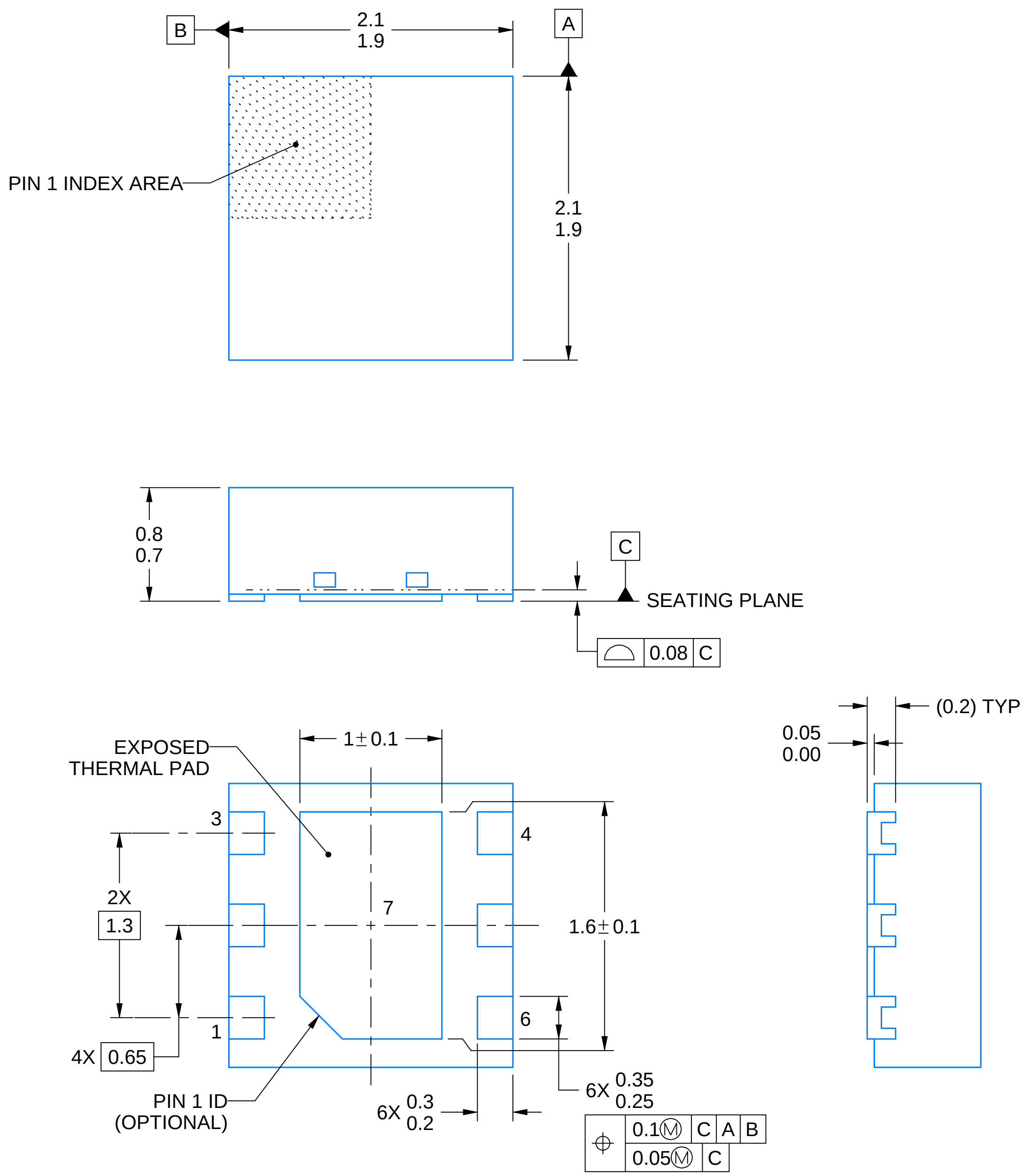
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

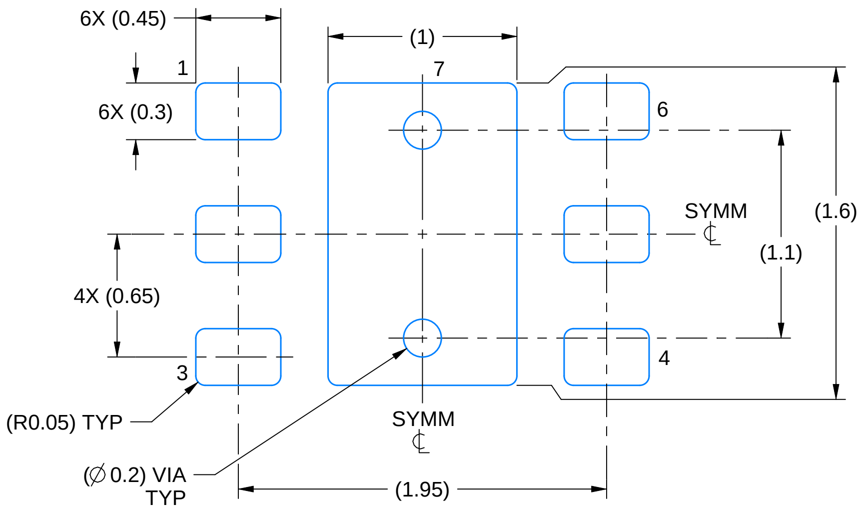
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



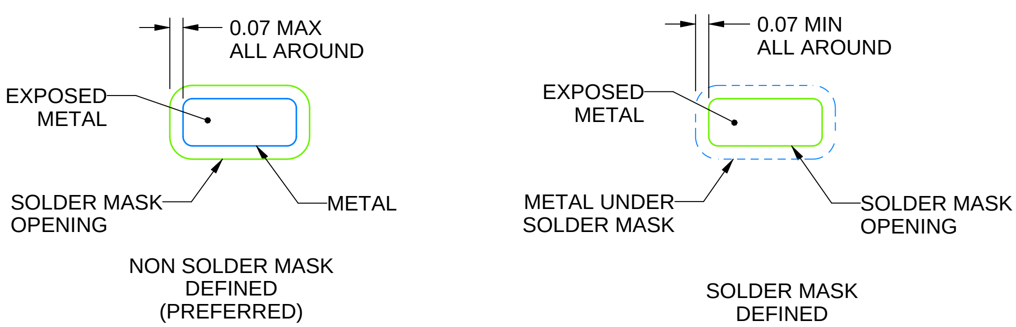
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

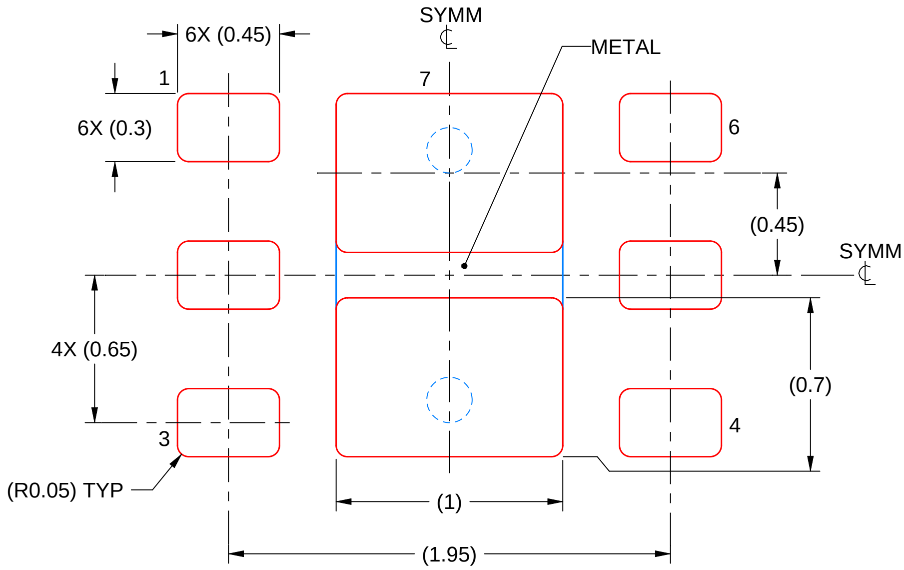


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

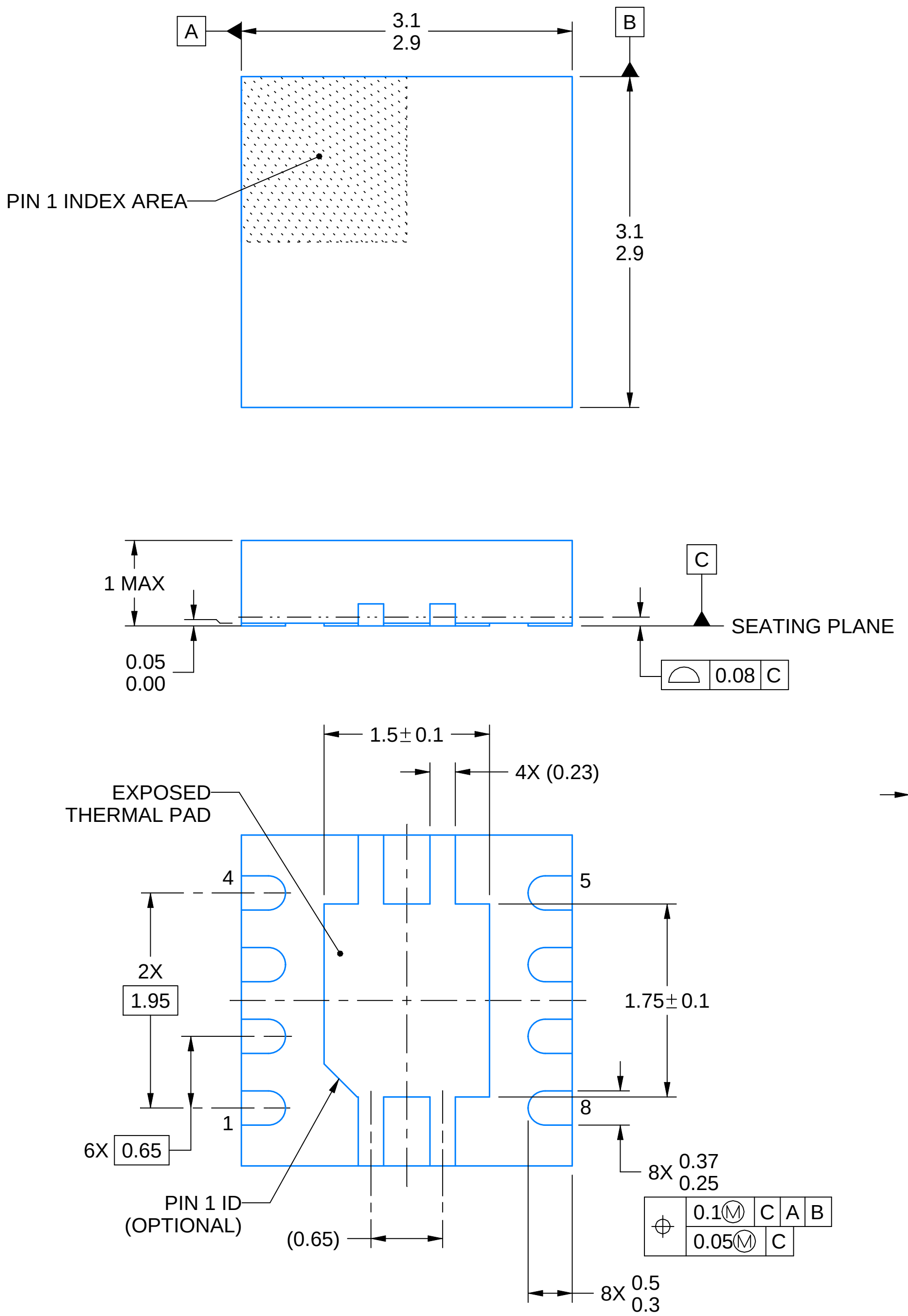
EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

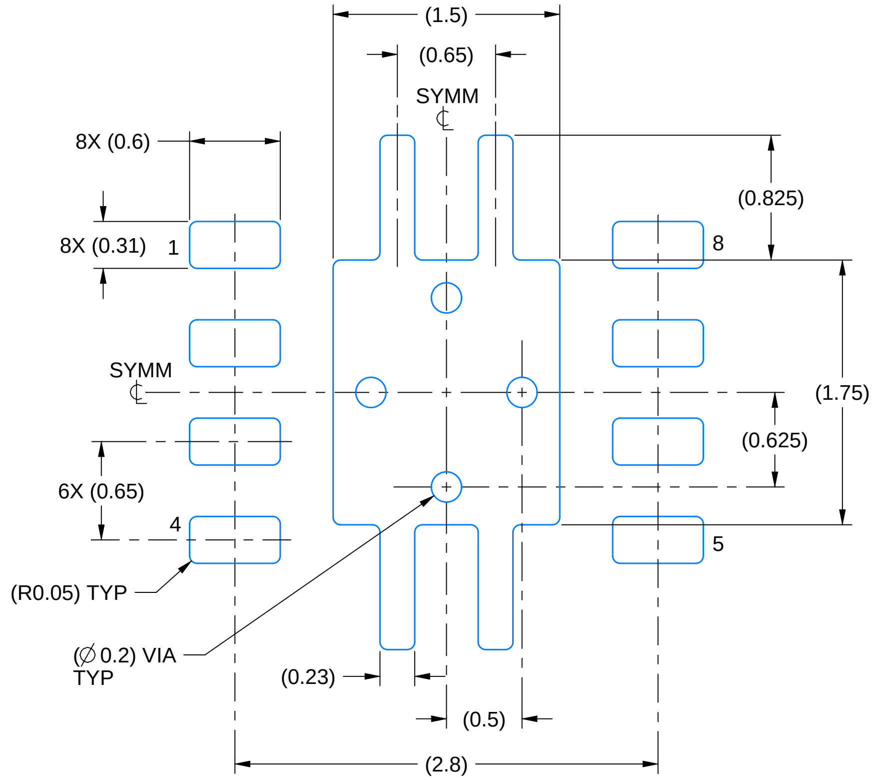


DIM A	
OPT 1	OPT 2
(0.1)	(0.2)

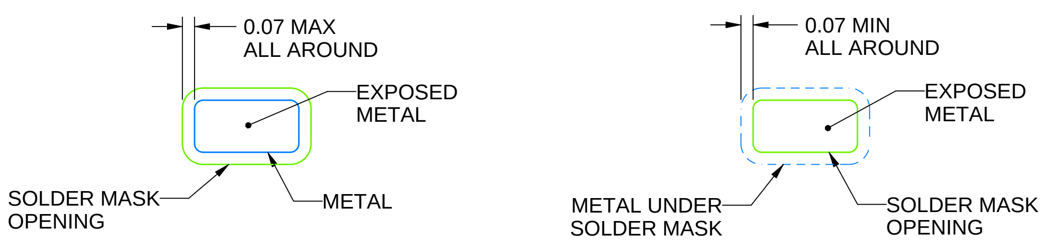
4218875/A 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

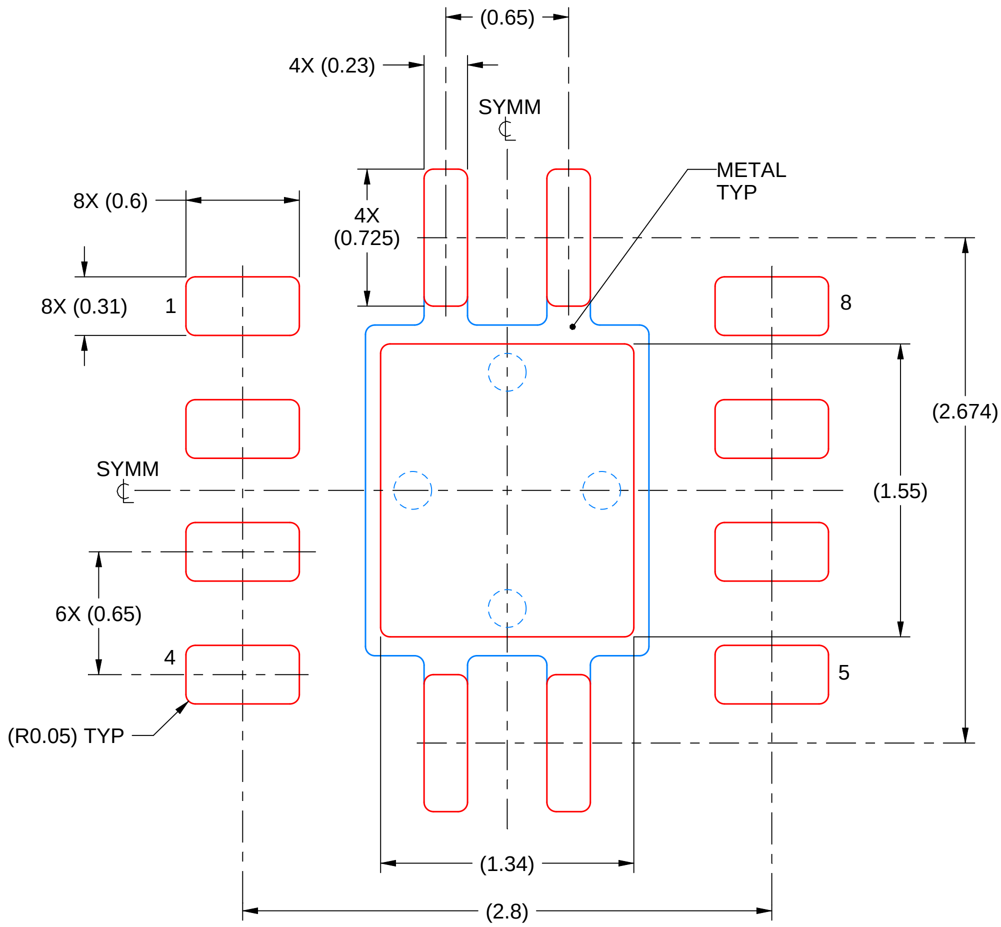
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265