



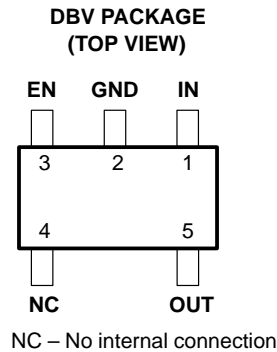
**THE DATASHEET OF
TPS76050DBVR**



TPS76030, TPS76032, TPS76033, TPS76038, TPS76050 LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

SLVS144D – JULY 1998 – REVISED MAY 2001

- 50-mA Low-Dropout Regulator
- Fixed Output Voltage Options: 5 V, 3.8 V, 3.3 V, 3.2 V, and 3 V
- Dropout Typically 120 mV at 50 mA
- Thermal Protection
- Less Than 1- μ A Quiescent Current in Shutdown
- -40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 Package
- ESD Protection Verified to 1.5 kV Human Body Model (HBM) per MIL-STD-883C



description

The TPS760xx is a 50 mA, low dropout (LDO) voltage regulator designed specifically for battery-powered applications. A proprietary BiCMOS fabrication process allows the TPS760xx to provide outstanding performance in all specifications critical to battery-powered operation.

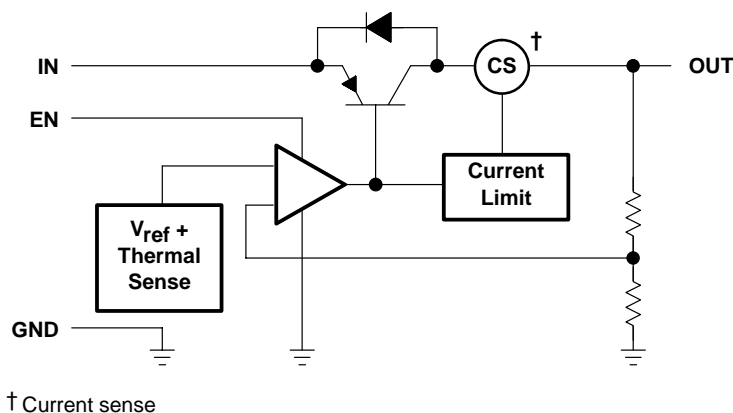
The TPS760xx is available in a space-saving SOT-23 package and operates over a junction temperature range of -40°C to 125°C .

AVAILABLE OPTIONS

| T_J | VOLTAGE | PACKAGE | PART NUMBER | SYMBOL |
|--|---------|---------|--------------|--------|
| -40°C to 125°C | 3 V | SOT-23 | TPS76030DBVR | PAGI |
| | 3.2 V | | TPS76032DBVR | PAOI |
| | 3.3 V | | TPS76033DBVR | PAHI |
| | 3.8 V | | TPS76038DBVR | PAJI |
| | 5 V | | TPS76050DBVR | PANI |

NOTE: The DBV package is available taped and reeled only.

functional block diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated

TPS76030, TPS76032, TPS76033, TPS76038, TPS76050

LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

SLVS144D – JULY 1998 – REVISED MAY 2001

Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------|-----|-----|--------------------------|
| EN | 3 | I | Enable input |
| GND | 2 | | Ground |
| IN | 1 | I | Input voltage |
| NC | 4 | | No connection |
| OUT | 5 | O | Regulated output voltage |

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|------------------------------|
| Input voltage range, V_I ‡ | –0.3 V to 16 V |
| Voltage range at EN | –0.3 V to $V_I + 0.3$ V |
| Peak output current | internally limited |
| Continuous total dissipation | See Dissipation Rating Table |
| Operating junction temperature range, T_J | –40°C to 150°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |
| ESD rating, HBM | 1.5 kV |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to device GND pin.

DISSIPATION RATING TABLE

| BOARD | PACKAGE | $R_{\theta JC}$ | $R_{\theta JA}$ | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A \leq 25^\circ\text{C}$ POWER RATING | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|---------|-----------------|-----------------|--|--|---------------------------------------|---------------------------------------|
| Low K§ | DBV | 65.8 °C/W | 259 °C/W | 3.9 mW/°C | 386 mW | 212 mW | 154 mW |
| High K¶ | DBV | 65.8 °C/W | 180 °C/W | 5.6 mW/°C | 555 mW | 305 mW | 222 mW |

§ The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.

¶ The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---------------------------------------|----------|-----|-----|------|
| Input voltage, V_I | TPS76030 | 3.2 | 16 | V |
| | TPS76032 | 3.4 | 16 | |
| | TPS76033 | 3.5 | 16 | |
| | TPS76038 | 4 | 16 | |
| | TPS76050 | 5.2 | 16 | |
| Continuous output current, I_O | 0 | | 50 | mA |
| Operating junction temperature, T_J | –40 | | 125 | °C |



TPS76030, TPS76032, TPS76033, TPS76038, TPS76050 LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

SLVS144D – JULY 1998 – REVISED MAY 2001

**electrical characteristics over recommended operating free-air temperature range,
 $V_I = V_{O(nom)} + 1\text{ V}$, $I_O = 1\text{ mA}$, $EN = V_I$, $C_O = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-------------------------|-----------------------------------|---|---|------|------|------------------|------|
| V_O | Output voltage | TPS76030 | $T_J = 25^\circ\text{C}$ | 2.96 | 3 | 3.04 | V |
| | | | $T_J = 25^\circ\text{C}$, $1\text{ mA} < I_O < 50\text{ mA}$ | 2.92 | | 3.04 | |
| | | | $1\text{ mA} < I_O < 50\text{ mA}$ | 2.91 | | 3.07 | |
| | | TPS76032 | $T_J = 25^\circ\text{C}$ | 3.16 | 3.2 | 3.24 | V |
| | | | $T_J = 25^\circ\text{C}$, $1\text{ mA} < I_O < 50\text{ mA}$ | 3.13 | | 3.24 | |
| | | | $1\text{ mA} < I_O < 50\text{ mA}$ | 3.1 | | 3.3 | |
| | | TPS76033 | $T_J = 25^\circ\text{C}$ | 3.26 | 3.3 | 3.34 | V |
| | | | $T_J = 25^\circ\text{C}$, $1\text{ mA} < I_O < 50\text{ mA}$ | 3.23 | | 3.34 | |
| | | | $1\text{ mA} < I_O < 50\text{ mA}$ | 3.2 | | 3.4 | |
| | TPS76038 | $T_J = 25^\circ\text{C}$ | 3.76 | 3.8 | 3.84 | V | |
| | | $T_J = 25^\circ\text{C}$, $1\text{ mA} < I_O < 50\text{ mA}$ | 3.73 | | 3.84 | | |
| | | $1\text{ mA} < I_O < 50\text{ mA}$ | 3.7 | | 3.9 | | |
| | TPS76050 | $T_J = 25^\circ\text{C}$ | 4.95 | 5 | 5.05 | V | |
| | | $T_J = 25^\circ\text{C}$, $1\text{ mA} < I_O < 50\text{ mA}$ | 4.91 | | 5.05 | | |
| | | $1\text{ mA} < I_O < 50\text{ mA}$ | 4.89 | | 5.1 | | |
| $I_{I(\text{standby})}$ | Standby current | $EN = 0\text{ V}$ | | | 1 | μA | |
| | Quiescent current (GND current) | $I_O = 0\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 90 | 115 | μA | |
| | | | $I_O = 0\text{ mA}$ | | | | 130 |
| | | $I_O = 1\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 100 | 130 | | |
| | | | $I_O = 1\text{ mA}$ | | | | 170 |
| | | $I_O = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 190 | 215 | | |
| | | | $I_O = 10\text{ mA}$ | | | | 260 |
| | | $I_O = 50\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 850 | 1100 | | |
| | | | $I_O = 50\text{ mA}$ | | | | 1200 |
| Input regulation | TPS76030 | $4\text{ V} < V_I < 16$, $I_O = 1\text{ mA}$ | | 3 | 10 | mV | |
| | TPS76032 | $4.2\text{ V} < V_I < 16$, $I_O = 1\text{ mA}$ | | 3 | 10 | | |
| | TPS76033 | $4.3\text{ V} < V_I < 16$, $I_O = 1\text{ mA}$ | | 3 | 10 | | |
| | TPS76038 | $4.8\text{ V} < V_I < 16$, $I_O = 1\text{ mA}$ | | 3 | 10 | | |
| | TPS76050 | $6\text{ V} < V_I < 16$, $I_O = 1\text{ mA}$ | | 3 | 10 | | |
| V_n | Output noise voltage | $BW = 300\text{ Hz to } 50\text{ kHz}$, $C_O = 10\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$ | | 190 | | μVrms | |
| | Ripple rejection | $f = 1\text{ kHz}$, $C_O = 10\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$ | | 63 | | dB | |
| Dropout voltage | | $I_O = 0\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 1 | 3 | mV | |
| | | | $I_O = 0\text{ mA}$ | | | | 5 |
| | | $I_O = 1\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 7 | 10 | | |
| | | | $I_O = 1\text{ mA}$ | | | | 15 |
| | | $I_O = 10\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 40 | 60 | | |
| | | | $I_O = 10\text{ mA}$ | | | | 90 |
| | | $I_O = 50\text{ mA}$, $T_J = 25^\circ\text{C}$ | | 120 | 150 | | |
| $I_O = 50\text{ mA}$ | | | | 180 | | | |
| | Peak output current/current limit | | 100 | 125 | 135 | mA | |
| | High level enable input | | 2 | | | V | |
| | Low level enable input | | | | 0.8 | V | |
| I_I | Input current (EN) | $EN = 0\text{ V}$ | -1 | 0 | 1 | μA | |
| | | $EN = V_I$ | | 2.5 | 5 | μA | |



TPS76030, TPS76032, TPS76033, TPS76038, TPS76050 LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

SLVS144D – JULY 1998 – REVISED MAY 2001

Table of Graphs

| | | | FIGURE |
|-----------------|-------------------------|-------------------------|---------|
| V _O | Output voltage | vs Output current | 1, 2, 3 |
| | | vs Free-air temperature | 4, 5, 6 |
| | Ground current | vs Free-air temperature | 7, 8, 9 |
| | Output noise | vs Frequency | 10 |
| Z _O | Output impedance | vs Frequency | 11 |
| V _{DO} | Dropout voltage | vs Free-air temperature | 12 |
| | Line transient response | | 13, 15 |
| | Load transient response | | 14, 16 |



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

TPS76030
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT

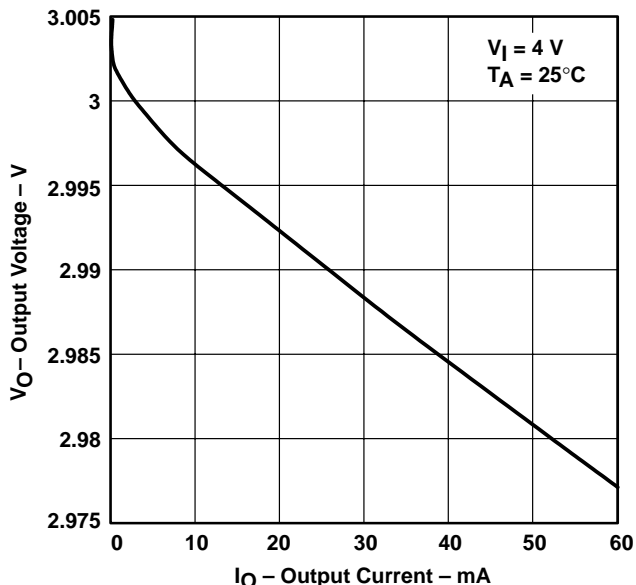


Figure 1

TPS76033
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT

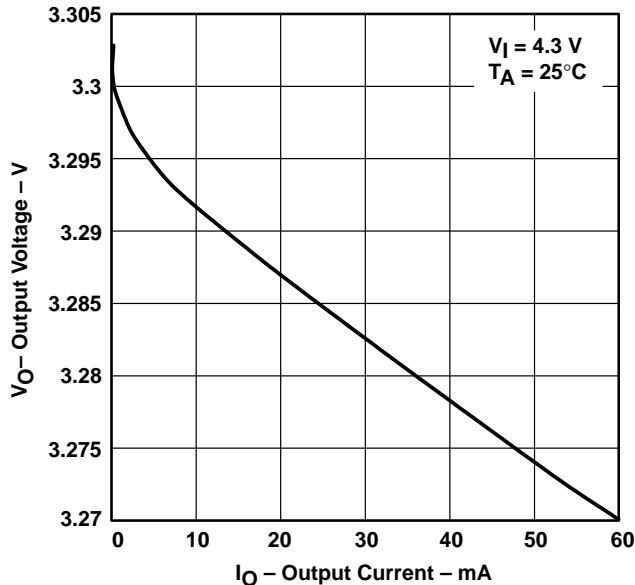


Figure 2

TPS76050
 OUTPUT VOLTAGE
 vs
 OUTPUT CURRENT

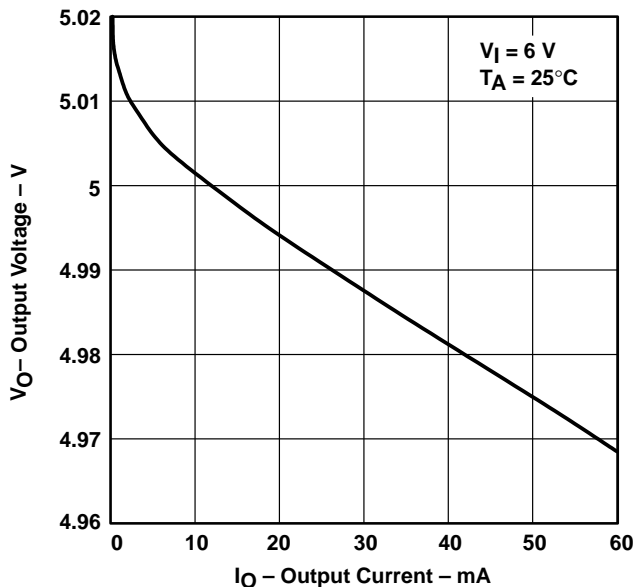


Figure 3

TPS76030
 OUTPUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

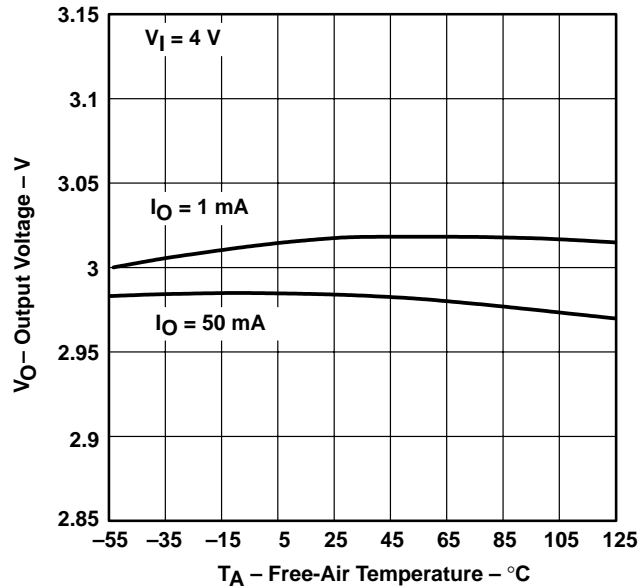


Figure 4

TPS76030, TPS76032, TPS76033, TPS76038, TPS76050 LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

SLVS144D – JULY 1998 – REVISED MAY 2001

TYPICAL CHARACTERISTICS

TPS76033
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

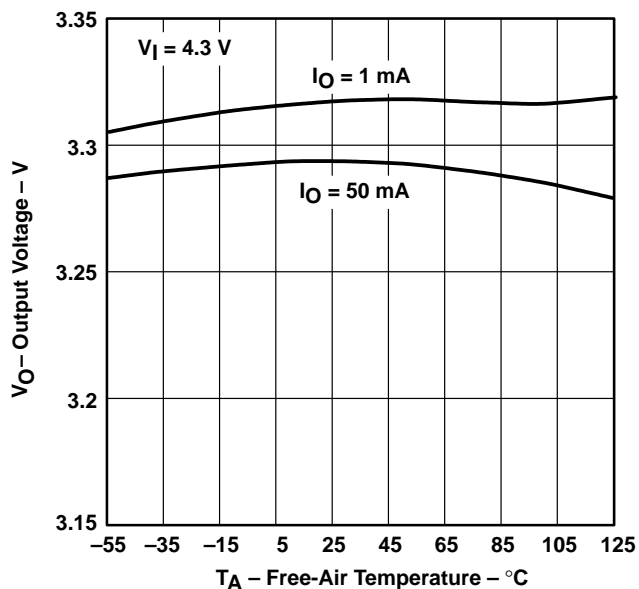


Figure 5

TPS76050
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

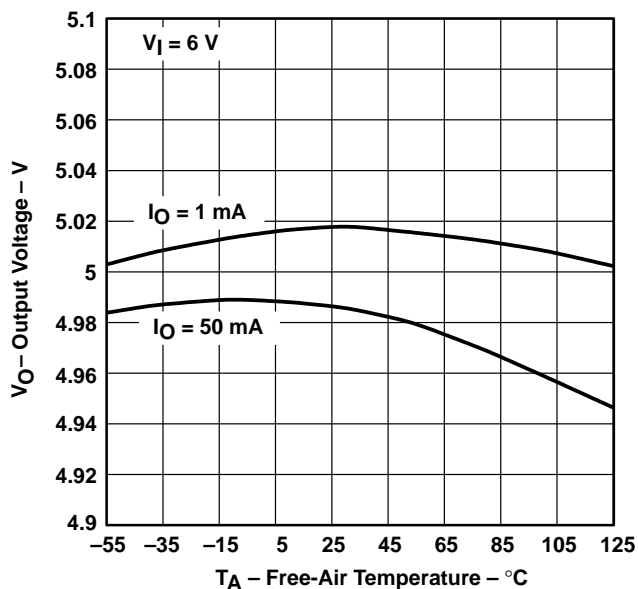


Figure 6

TPS76030
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

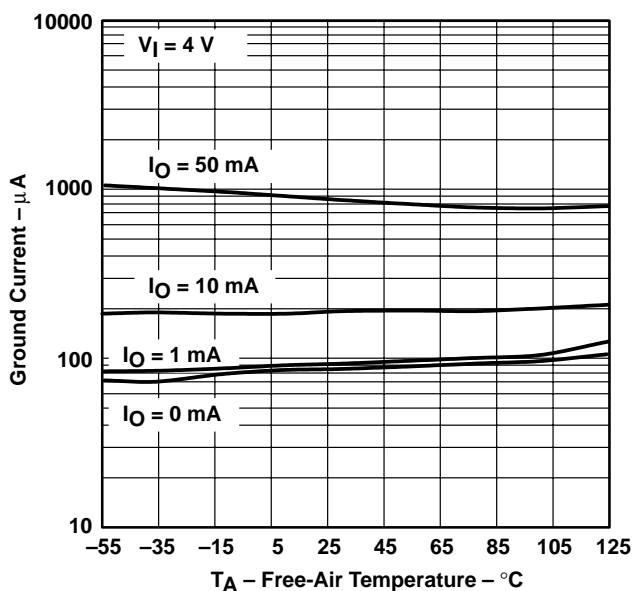


Figure 7

TPS76033
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

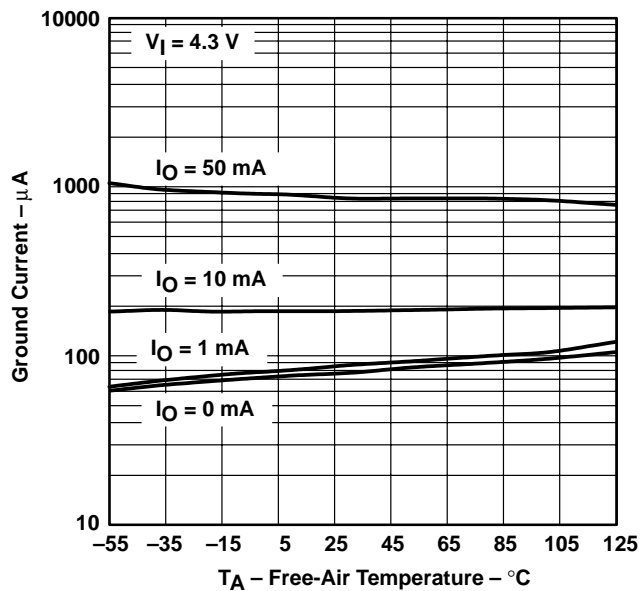
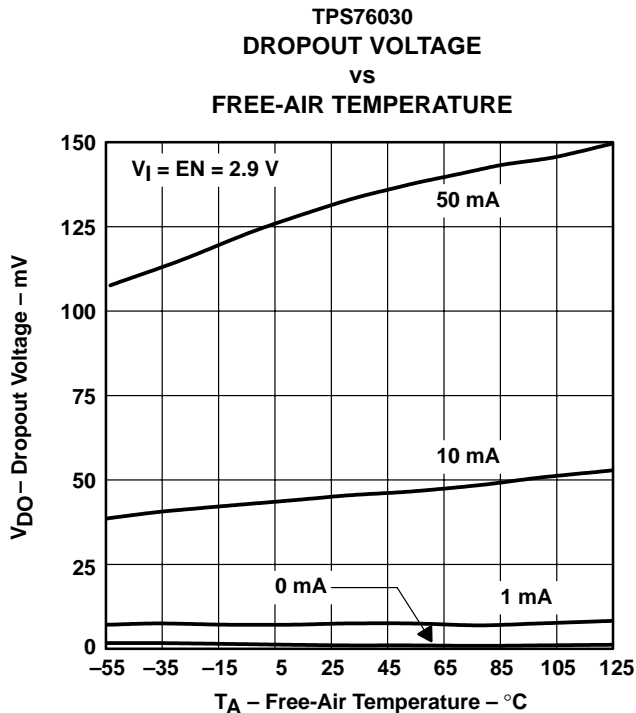
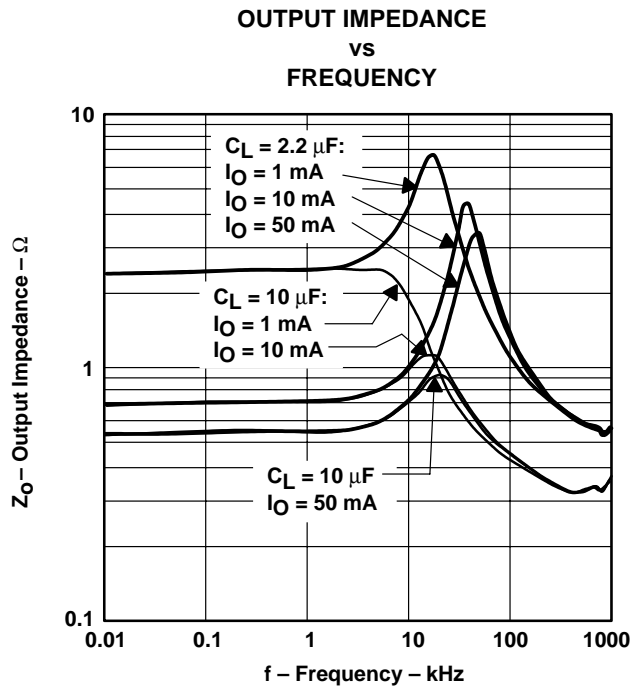
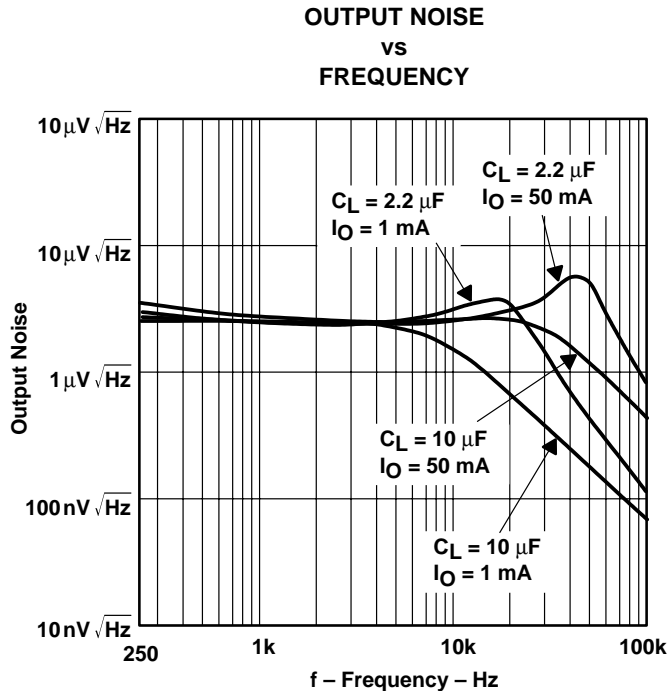
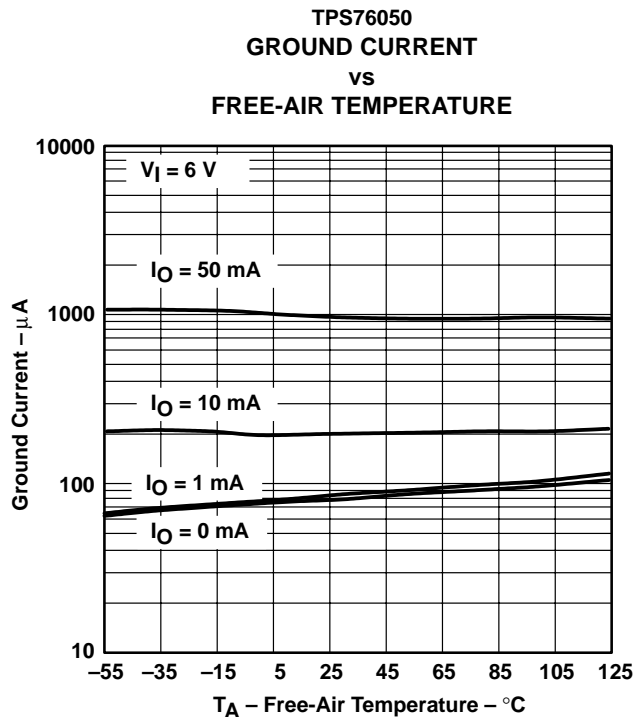


Figure 8



TYPICAL CHARACTERISTICS



TPS76030, TPS76032, TPS76033, TPS76038, TPS76050

LOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

SLVS144D – JULY 1998 – REVISED MAY 2001

TYPICAL CHARACTERISTICS

TPS76033
LINE TRANSIENT RESPONSE

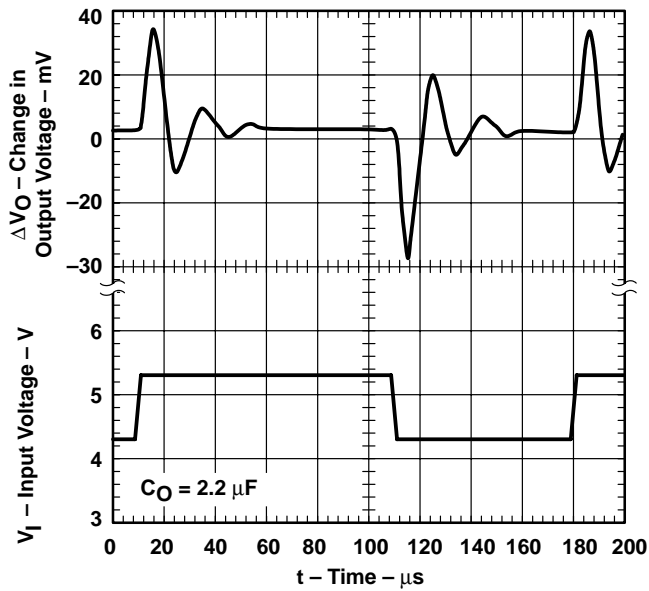


Figure 13

TPS76033
LOAD TRANSIENT RESPONSE

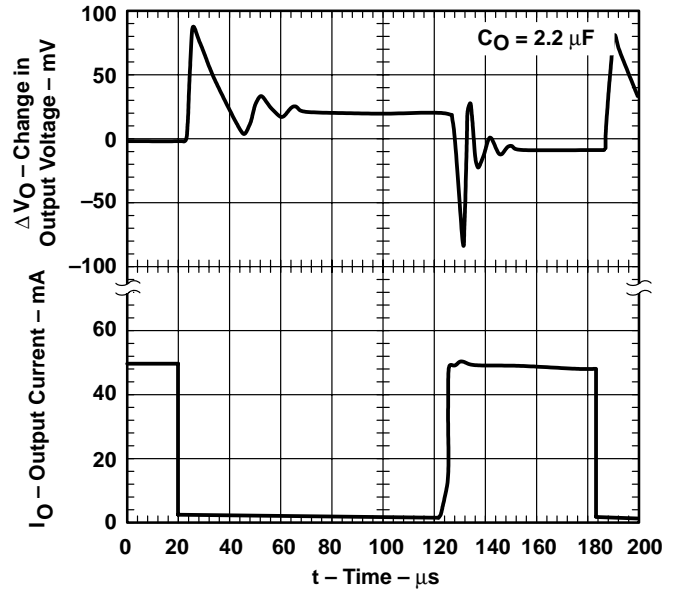


Figure 14

TPS76050
LINE TRANSIENT RESPONSE

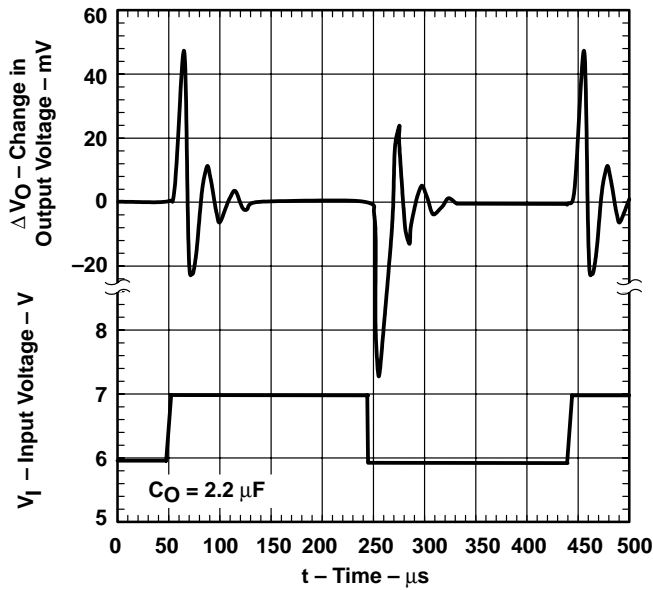


Figure 15

TPS76050
LOAD TRANSIENT RESPONSE

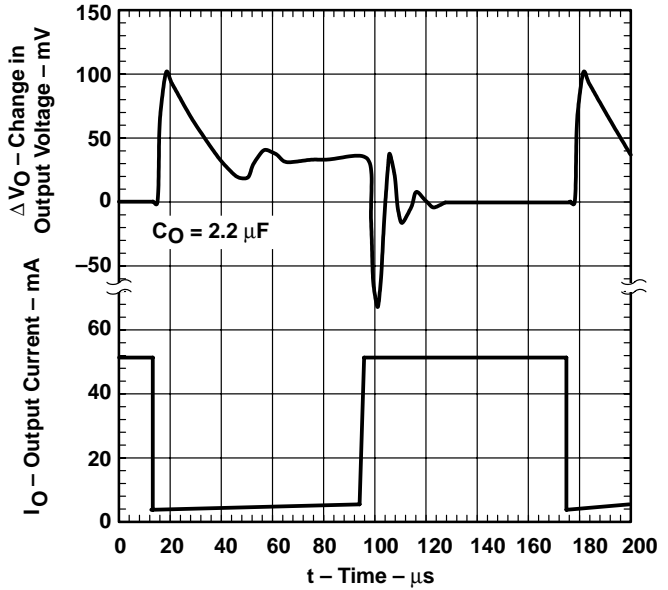


Figure 16

APPLICATION INFORMATION

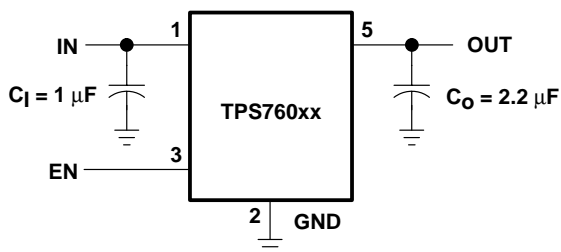


Figure 17. TPS760xx Typical Application

over current protection

The over current protection circuit forces the TPS760xx into a constant current output mode when the load is excessive or the output is shorted to ground. Normal operation resumes when the fault condition is removed. An overload or short circuit may also activate the over temperature protection if the fault condition persists.

over temperature protection

The thermal protection system shuts the TPS760xx down when the junction temperature exceeds 160°C. The device recovers and operates normally when the temperature drops below 155°C.

input capacitor

A 0.047 μF or larger ceramic decoupling capacitor with short leads connected between IN and GND is recommended. The decoupling capacitor may be omitted if there is a 1 μF or larger electrolytic capacitor connected between IN and GND and located reasonably close to the TPS760xx. However, the small ceramic device is desirable even when the larger capacitor is present, if there is a lot of high frequency noise present in the system.

output capacitor

Like all low dropout regulators, the TPS760xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 2.2 μF and the ESR (equivalent series resistance) must be between 0.1 Ω and 20 Ω . Capacitor values of 2.5- μF or larger are acceptable, provided the ESR is less than 20 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 2.2- μF surface-mount solid-tantalum capacitors, including devices from Sprague, Kemet, and Nichicon, meet the ESR requirements stated above. Multilayer ceramic capacitors should have minimum values of 2.5 μF over the full operating temperature range of the equipment.

enable (EN)

A logic zero on the enable input shuts the TPS760xx off and reduces the supply current to less than 1 μA . Pulling the enable input high causes normal operation to resume. If the enable feature is not used, EN should be connected to IN to keep the regulator on all of the time. The EN input must not be left floating.

reverse current path

The power transistor used in the TPS760xx has an inherent diode connected between IN and OUT as shown in the functional block diagram. This diode conducts current from the OUT terminal to the IN terminal whenever IN is lower than OUT by a diode drop. This condition does not damage the TPS760xx, provided the current is limited to 100 mA.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS76030DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PAGI | Samples |
| TPS76030DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PAGI | Samples |
| TPS76032DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PAOI | Samples |
| TPS76033DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PAHI | Samples |
| TPS76033DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PAHI | Samples |
| TPS76038DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PAJI | Samples |
| TPS76038DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PAJI | Samples |
| TPS76050DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PANI | Samples |
| TPS76050DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PANI | Samples |
| TPS76050DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PANI | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS76030DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76030DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76032DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76033DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76033DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76038DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76038DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS76050DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS76050DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS76030DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS76030DBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TPS76032DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS76033DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76033DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS76038DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS76038DBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TPS76050DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS76050DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View TPS76050DBVR on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management