

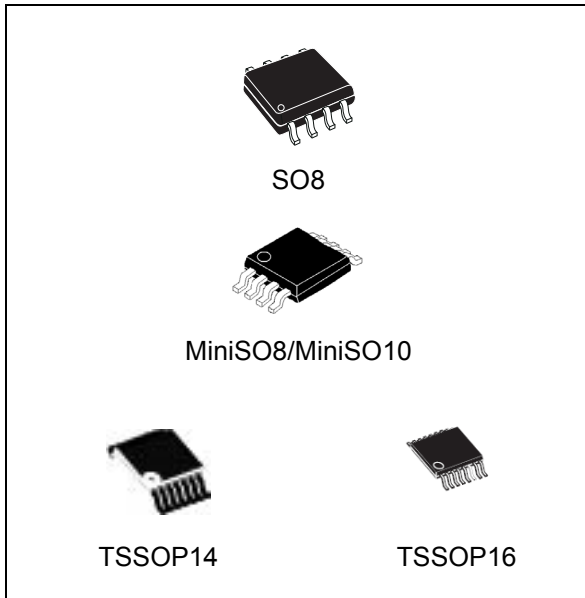


# THE DATASHEET OF TSV624IPT



## Rail-to-rail input/output, 29 $\mu$ A, 420 kHz CMOS operational amplifiers

Datasheet - production data



### Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

### Description

The TSV622, TSV622A, TSV623, TSV623A, TSV624, TSV624A, TSV625, and TSV625A dual and quad operational amplifiers offer low voltage, low power operation, and rail-to-rail input and output.

The TSV62x/TSV62xA series feature an excellent speed/power consumption ratio, offering a 420 kHz gain bandwidth product while consuming only 29  $\mu$ A at 5 V supply voltage.

These op-amps are unity gain stable for capacitive loads up to 100 pF. They also feature an ultra-low input bias current and low input offset voltage. TSV623 (dual) and TSV625 (quad) have two shutdown pins to reduce power consumption.

These features make the TSV62x/TSV62xA family ideal for sensor interfaces, battery-supplied and portable applications, and active filtering.

### Features

- Rail-to-rail input and output
- Low power consumption: 29  $\mu$ A typ, 36  $\mu$ A max
- Low supply voltage: 1.5 – 5.5 V
- Gain bandwidth product: 420 kHz typ
- Unity gain stable on 100 pF capacitor
- Low power shutdown mode: 5 nA typ
- Good accuracy: 800  $\mu$ V max (A version)
- Low input bias current: 1 pA typ
- EMI hardened operational amplifiers

### Related products

- See the TSV61x series for more power savings (120 kHz for 9  $\mu$ A)
- See the TSV63x series for higher gain bandwidth (880 kHz for 60  $\mu$ A)

**Table 1. Device summary**

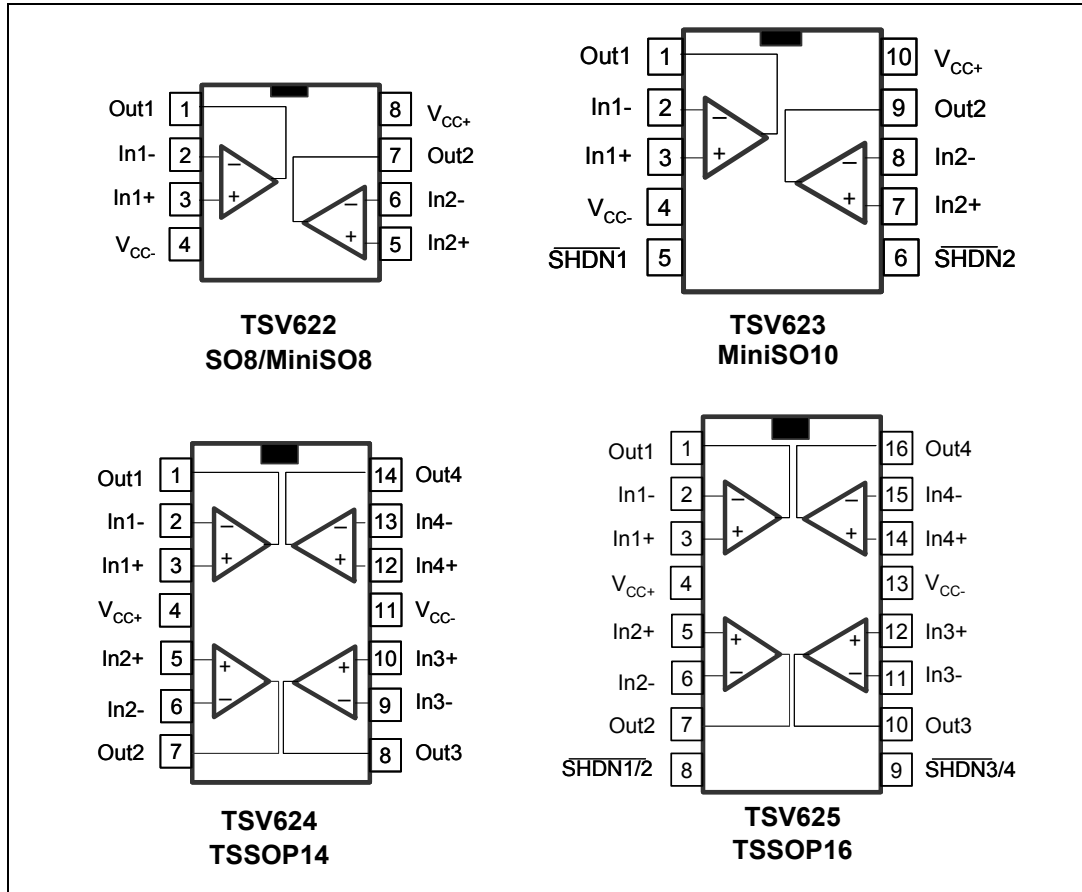
Reference	Dual version		Quad version	
	Without standby	With standby	Without standby	With standby
TSV62x	TSV622	TSV623	TSV624	TSV625
TSV62xA	TSV622A	TSV623A	TSV624A	TSV625A

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# 1 Package pin connections

Figure 1. Pin connections for each package (top view)



## 2 Absolute maximum ratings and operating conditions

**Table 2. Absolute maximum ratings (AMR)**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	6	V
$V_{id}$	Differential input voltage <sup>(2)</sup>	$\pm V_{CC}$	
$V_{in}$	Input voltage <sup>(3)</sup>	$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	
$I_{in}$	Input current <sup>(4)</sup>	10	mA
$\overline{SHDN}$	Shutdown voltage <sup>(3)</sup>	$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	V
$T_{stg}$	Storage temperature	-65 to 150	°C
$R_{thja}$	Thermal resistance junction to ambient <sup>(5) (6)</sup>		°C/W
	MiniSO8	190	
	SO8	125	
	MiniSO10	113	
	TSSOP14	100	
	TSSOP16	95	
$T_j$	Maximum junction temperature	150	°C
ESD	HBM: human body model <sup>(7)</sup>	4	kV
	MM: machine model <sup>(8)</sup>	200	V
	CDM: charged device model <sup>(9)</sup>	1.5	kV
	Latch-up immunity	200	mA

1. All voltage values, except differential voltages are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3.  $V_{CC-} - V_{in}$  must not exceed 6 V,  $V_{in}$  must not exceed 6V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6.  $R_{th}$  are typical values.
7. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

**Table 3. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	1.5 to 5.5	V
$V_{icm}$	Common mode input voltage range	$(V_{CC-}) - 0.1$ to $(V_{CC+}) + 0.1$	
$T_{oper}$	Operating free air temperature range	-40 to 125	°C

### 3 Electrical characteristics

Table 4. Electrical characteristics at  $V_{CC+} = 1.8\text{ V}$  with  $V_{CC-} = 0\text{ V}$ ,  $V_{icm} = V_{CC}/2$ ,  $T_{amb} = 25\text{ }^{\circ}\text{C}$ , and  $R_L$  connected to  $V_{CC}/2$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Offset voltage	TSV62x TSV62xA TSV623AIST - MiniSO10			4 0.8 1	mV
		TSV62x - $T_{min} < T_{op} < T_{max}$ TSV62xA - $T_{min} < T_{op} < T_{max}$ TSV623AIST - $T_{min} < T_{op} < T_{max}$			6 2 2.2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		$\mu\text{V}/^{\circ}\text{C}$
$I_{io}$	Input offset current ( $V_{out} = V_{CC}/2$ )			1	10 <sup>(1)</sup>	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
$I_{ib}$	Input bias current ( $V_{out} = V_{CC}/2$ )			1	10 <sup>(1)</sup>	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio $20 \log(\Delta V_{ic}/\Delta V_{io})$	0 V to 1.8 V, $V_{out} = 0.9\text{ V}$	53	74		dB
		$T_{min} < T_{op} < T_{max}$	51			
$A_{vd}$	Large signal voltage gain	$R_L = 10\text{ k}\Omega$ , $V_{out} = 0.5\text{ V to }1.3\text{ V}$	78	95		dB
		$T_{min} < T_{op} < T_{max}$	73			
$V_{OH}$	High level output voltage ( $V_{OH} = V_{CC} - V_{out}$ )	$R_L = 10\text{ k}\Omega$ $T_{min} < T_{op} < T_{max}$		5	35 50	mV
$V_{OL}$	Low level output voltage	$R_L = 10\text{ k}\Omega$ $T_{min} < T_{op} < T_{max}$		4	35 50	
$I_{out}$	Isink	$V_{out} = 1.8\text{ V}$	6	12		mA
		$T_{min} < T_{op} < T_{max}$	4			
	Isource	$V_{out} = 0\text{ V}$	6	10		
		$T_{min} < T_{op} < T_{max}$	4			
$I_{CC}$	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$		25	31	$\mu\text{A}$
		$T_{min} < T_{op} < T_{max}$			33	
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $f = 100\text{ kHz}$	275	340		kHz
$F_u$	Unity gain frequency			280		
$\phi_m$	Phase margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ ,		41		Degrees
$G_m$	Gain margin			8		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $A_v = 1$	0.1	0.155		$\text{V}/\mu\text{s}$

1. Guaranteed by design.

**Table 5. Shutdown characteristics  $V_{CC} = 1.8\text{ V}$  (TSV623, TSV625)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$I_{CC}$	Supply current in shutdown mode (all operators)	$\overline{\text{SHDN}} = V_{CC-}$		2.5	50	nA
		$T_{\min} < T_{op} < 85\text{ }^{\circ}\text{C}$			200	
		$T_{\min} < T_{op} < 125\text{ }^{\circ}\text{C}$				1.5
$t_{on}$	Amplifier turn-on time	$R_L = 5\text{ k}$ , $V_{out} = (V_{CC-}) \text{ to } (V_{CC-}) + 0.2\text{ V}$		200		ns
$t_{off}$	Amplifier turn-off time	$R_L = 2\text{ k}$ , $V_{out} = (V_{CC+}) - 0.5\text{ V}$ to $(V_{CC+}) - 0.7\text{ V}$		20		
$V_{IH}$	$\overline{\text{SHDN}}$ logic high		1.35			V
$V_{IL}$	$\overline{\text{SHDN}}$ logic low				0.6	
$I_{IH}$	$\overline{\text{SHDN}}$ current high	$\overline{\text{SHDN}} = V_{CC+}$		10		pA
$I_{IL}$	$\overline{\text{SHDN}}$ current low	$\overline{\text{SHDN}} = V_{CC-}$		10		
$I_{OLeak}$	Output leakage in shutdown mode	$\overline{\text{SHDN}} = V_{CC-}$		50		nA
		$T_{\min} < T_{op} < 125\text{ }^{\circ}\text{C}$		1		

**Table 6. Electrical characteristics at  $V_{CC+} = 3.3\text{ V}$  with  $V_{CC-} = 0\text{ V}$ ,  $V_{icm} = V_{CC}/2$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$ , and  $R_L$  connected to  $V_{CC}/2$  (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Offset voltage	TSV62x TSV62xA TSV623AIST - MiniSO10			4 0.8 1	mV
		TSV62x - $T_{min} < T_{op} < T_{max}$ TSV62xA - $T_{min} < T_{op} < T_{max}$ TSV623AIST - $T_{min} < T_{op} < T_{max}$			6 2 2.2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		$\mu\text{V}/^\circ\text{C}$
$I_{io}$	Input offset current			1	10 <sup>(1)</sup>	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
$I_{ib}$	Input bias current			1	10 <sup>(1)</sup>	
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0 V to 3.3 V, $V_{out} = 1.65\text{ V}$	57	79		dB
		$T_{min} < T_{op} < T_{max}$	53			
$A_{vd}$	Large signal voltage gain	$R_L = 10\text{ k}\Omega$ , $V_{out} = 0.5\text{ V to } 2.8\text{ V}$	81	98		
		$T_{min} < T_{op} < T_{max}$	76			
$V_{OH}$	High level output voltage ( $V_{OH} = V_{CC} - V_{out}$ )	$R_L = 10\text{ k}\Omega$ $T_{min} < T_{op} < T_{max}$		5	35 50	mV
$V_{OL}$	Low level output voltage	$R_L = 10\text{ k}\Omega$ $T_{min} < T_{op} < T_{max}$		4	35 50	
$I_{out}$	Isink	$V_o = 5\text{ V}$	23	45		mA
		$T_{min} < T_{op} < T_{max}$	20			
	Isource	$V_o = 0\text{ V}$	23	38		
		$T_{min} < T_{op} < T_{max}$	20			
$I_{CC}$	Supply current (per operator)	No load, $V_{out} = 2.5\text{ V}$		26	33	$\mu\text{A}$
		$T_{min} < T_{op} < T_{max}$			35	
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $f = 100\text{ kHz}$	310	380		kHz
$F_u$	Unity gain frequency			310		
$\phi_m$	Phase margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		41		Degrees
$G_m$	Gain margin			8		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $A_V = 1$	0.11	0.175		$\text{V}/\mu\text{s}$

1. Guaranteed by design.

**Table 7. Electrical characteristics at  $V_{CC+} = 5\text{ V}$  with  $V_{CC-} = 0\text{ V}$ ,  $V_{icm} = V_{CC}/2$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$ , and  $R_L$  connected to  $V_{CC}/2$  (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Offset voltage	TSV62x TSV62xA TSV623AIST - MiniSO10			4 0.8 1	mV
		TSV62x - $T_{min} < T_{op} < T_{max}$ TSV62xA - $T_{min} < T_{op} < T_{max}$ TSV62xA - $T_{min} < T_{op} < T_{max}$			6 2 2.2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		$\mu\text{V}/^\circ\text{C}$
$I_{io}$	Input offset current			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
$I_{ib}$	Input bias current			1	$10^{(1)}$	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0\text{ V to }5\text{ V}$ , $V_{out} = 2.5\text{ V}$	60	80		dB
		$T_{min} < T_{op} < T_{max}$	55			
$A_{vd}$	Large signal voltage gain	$R_L = 10\text{ k}\Omega$ , $V_{out} = 0.5\text{ V to }4.5\text{ V}$	85	98		dB
		$T_{min} < T_{op} < T_{max}$	80			
SVR	Supply voltage rejection ratio $20 \log (\Delta V_{CC}/\Delta V_{io})$	$V_{CC} = 1.8\text{ to }5\text{ V}$	75	102		dB
		$T_{min} < T_{op} < T_{max}$	73			
EMIRR	EMI rejection ratio EMIRR = $-20 \log (V_{RFpeak}/\Delta V_{io})$	$V_{RF} = 100\text{ mV}_{rms}$ , $f = 400\text{ MHz}$		61		dB
		$V_{RF} = 100\text{ mV}_{rms}$ , $f = 900\text{ MHz}$		85		
		$V_{RF} = 100\text{ mV}_{rms}$ , $f = 1800\text{ MHz}$		92		
		$V_{RF} = 100\text{ mV}_{rms}$ , $f = 2400\text{ MHz}$		83		
$V_{OH}$	High level output voltage ( $V_{OH} = V_{CC} - V_{out}$ )	$R_L = 10\text{ k}\Omega$		7	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
$V_{OL}$	Low level output voltage	$R_L = 10\text{ k}\Omega$		6	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
$I_{out}$	$I_{sink}$	$V_o = 5\text{ V}$	40	69		mA
		$T_{min} < T_{op} < T_{max}$	35			
	$I_{source}$	$V_o = 0\text{ V}$	40	74		
		$T_{min} < T_{op} < T_{max}$	35			
$I_{CC}$	Supply current (per operator)	No load, $V_{out} = 2.5\text{ V}$		29	36	$\mu\text{A}$
		$T_{min} < T_{op} < T_{max}$			38	
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $f = 100\text{ kHz}$	350	420		kHz
$F_u$	Unity gain frequency	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		360		

**Table 7. Electrical characteristics at  $V_{CC+} = 5\text{ V}$  with  $V_{CC-} = 0\text{ V}$ ,  $V_{icm} = V_{CC}/2$ ,  $T_{amb} = 25\text{ °C}$ , and  $R_L$  connected to  $V_{CC}/2$  (unless otherwise specified) (continued)**

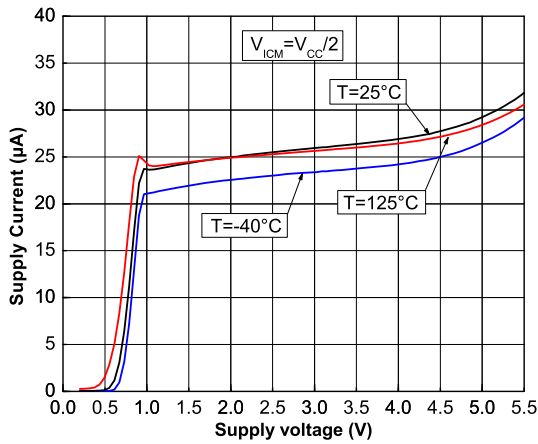
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$\phi_m$	Phase margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		40		Degrees
$G_m$	Gain margin			8		dB
SR	Slew rate	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $A_V = 1$	0.12	0.19		V/ $\mu$ s
$e_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$		77		$\frac{nV}{\sqrt{Hz}}$
THD+ $e_n$	Total harmonic distortion + noise	$A_V = 1$ , $f = 1\text{ kHz}$ , $R_L = 100\text{ k}\Omega$ , $V_{icm} = V_{CC}/2$ , $V_{out} = 2\text{ Vpp}$		0.002		%

1. Guaranteed by design.

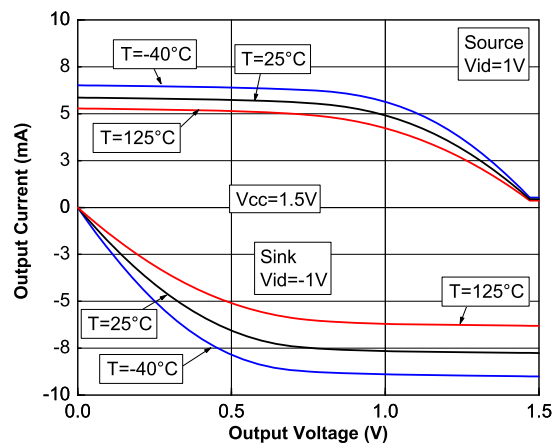
**Table 8. Shutdown characteristics at  $V_{CC} = 5\text{ V}$  (TSV623, TSV625)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$I_{CC}$	Supply current in shutdown mode (all operators)	$\overline{\text{SHDN}} = V_{IL}$		5	50	nA
		$T_{min} < T_{op} < 85\text{ °C}$			200	
		$T_{min} < T_{op} < 125\text{ °C}$				1.5
$t_{on}$	Amplifier turn-on time	$R_L = 5\text{ k}\Omega$ , $V_{out} = (V_{CC-})$ to $(V_{CC-}) + 0.2\text{ V}$		200		ns
$t_{off}$	Amplifier turn-off time	$R_L = 5\text{ k}\Omega$ , $V_{out} = (V_{CC+}) - 0.5\text{ V}$ to $(V_{CC+}) - 0.7\text{ V}$		20		
$V_{IH}$	$\overline{\text{SHDN}}$ logic high		2			V
$V_{IL}$	$\overline{\text{SHDN}}$ logic low				0.8	
$I_{IH}$	$\overline{\text{SHDN}}$ current high	$\overline{\text{SHDN}} = V_{CC+}$		10		pA
$I_{IL}$	$\overline{\text{SHDN}}$ current low	$\overline{\text{SHDN}} = V_{CC-}$		10		
$I_{OLeak}$	Output leakage in shutdown mode	$\overline{\text{SHDN}} = V_{CC-}$		50		
		$T_{min} < T_{op} < 125\text{ °C}$		1		nA

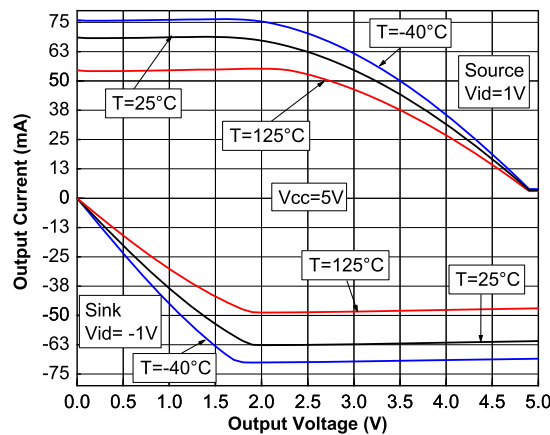
**Figure 2. Supply current vs. supply voltage at  $V_{icm} = V_{CC}/2$**



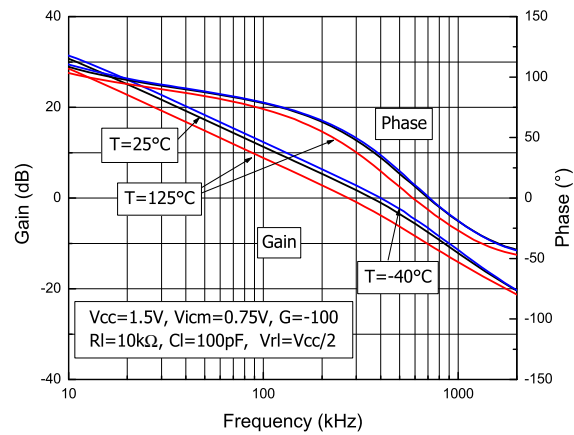
**Figure 3. Output current vs. output voltage at  $V_{CC} = 1.5 V$**



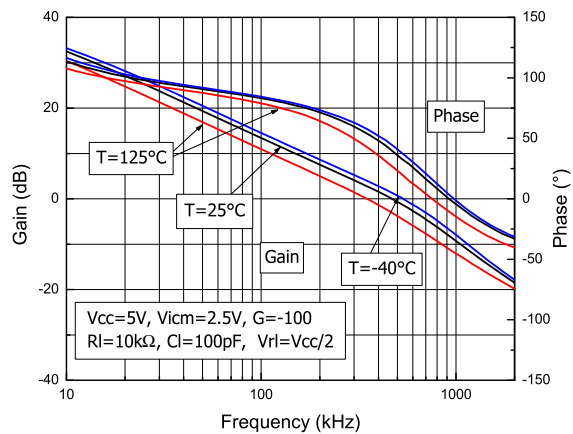
**Figure 4. Output current vs. output voltage at  $V_{CC} = 5 V$**



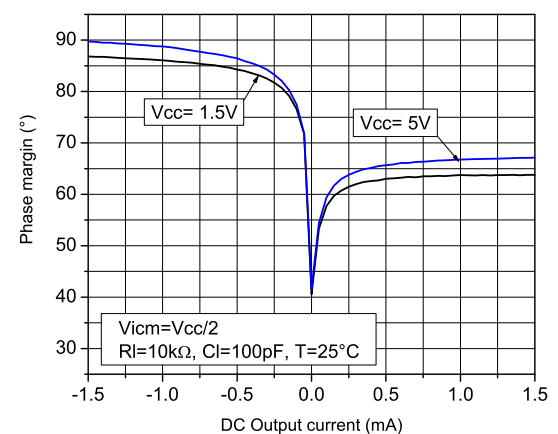
**Figure 5. Voltage gain and phase vs. frequency at  $V_{CC} = 1.5 V$**



**Figure 6. Voltage gain and phase vs. frequency at  $V_{CC} = 5 V$**



**Figure 7. Phase margin vs. output current at  $V_{CC} = 1.5 V$  and  $V_{CC} = 5 V$**



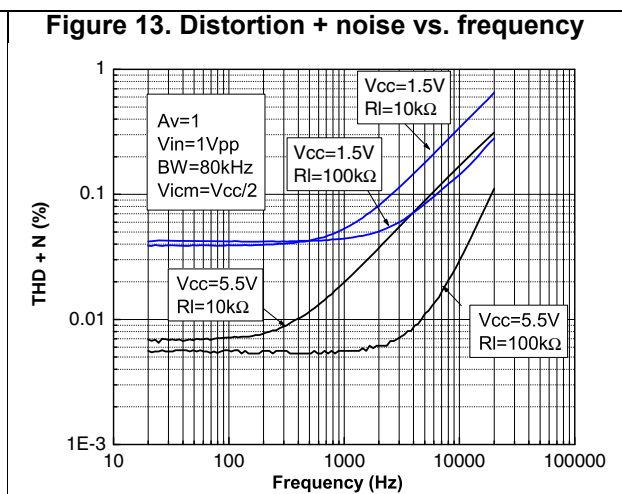
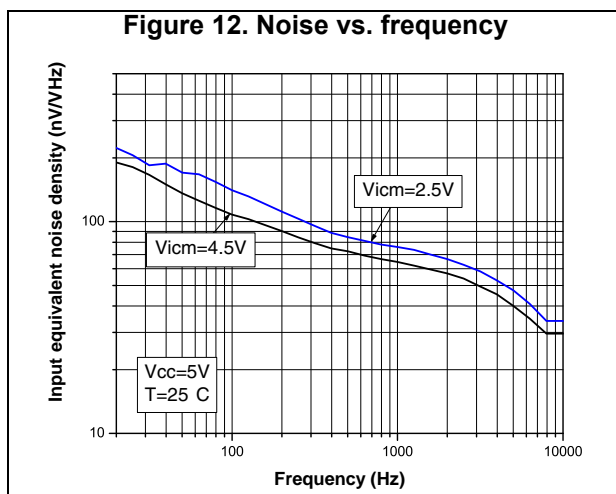
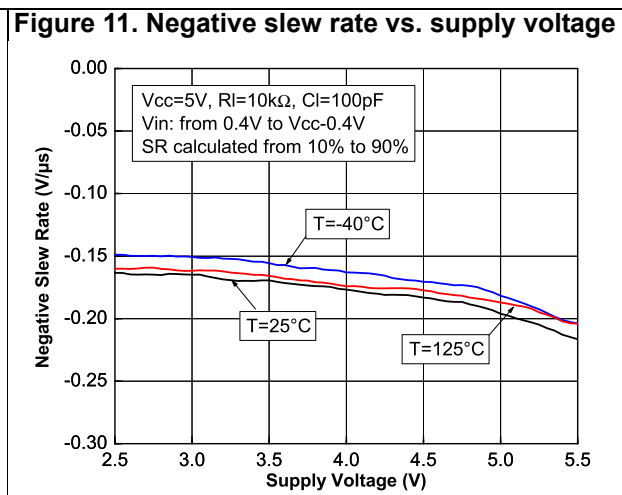
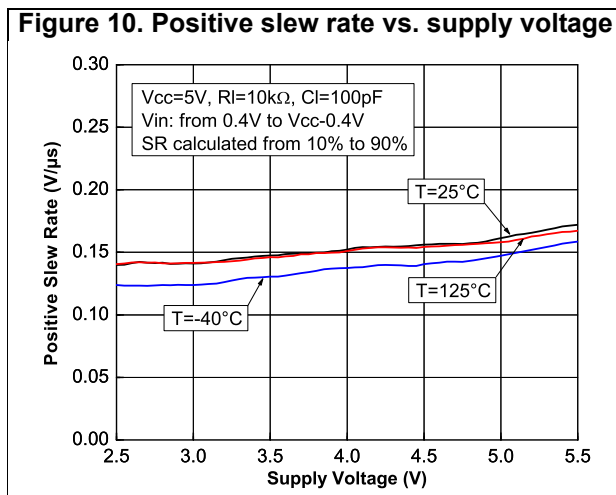
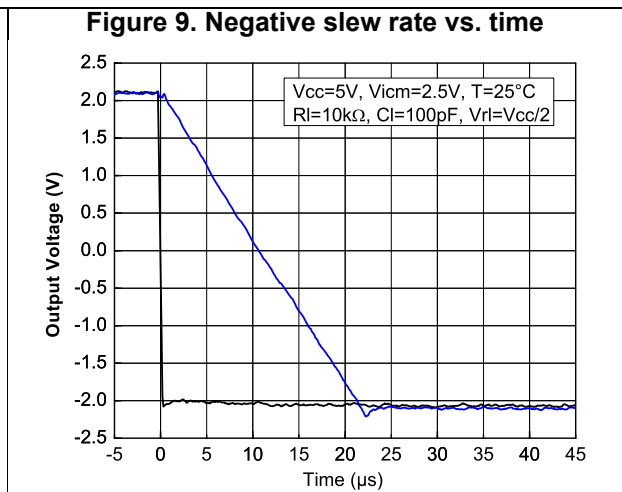
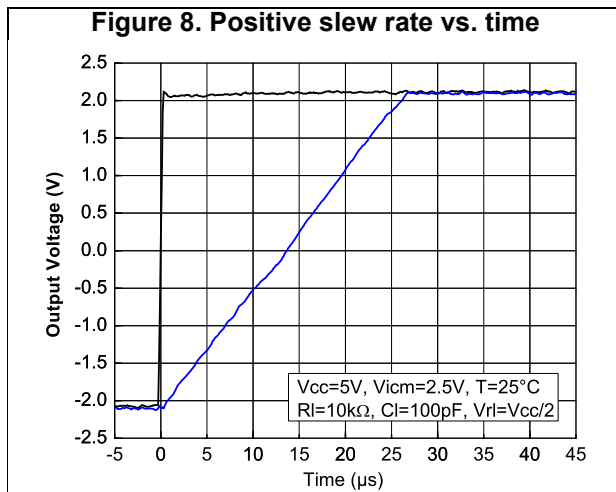


Figure 14. Distortion + noise vs. output voltage

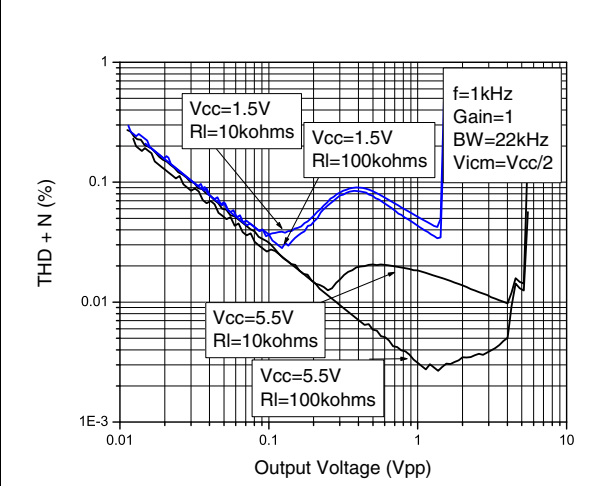
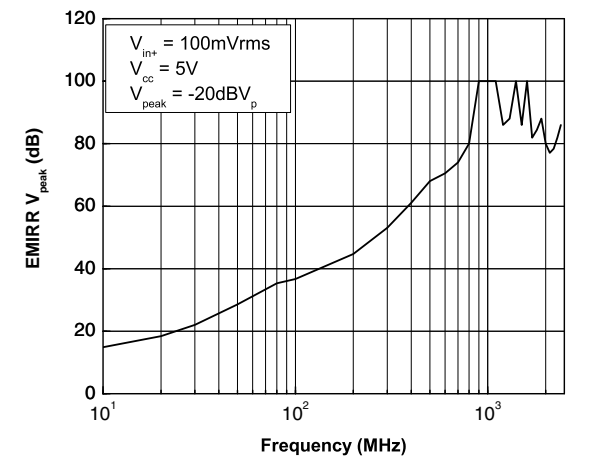


Figure 15. EMIRR vs. frequency at V<sub>CC</sub> = 5 V, T = 25 °C



## 4 Application information

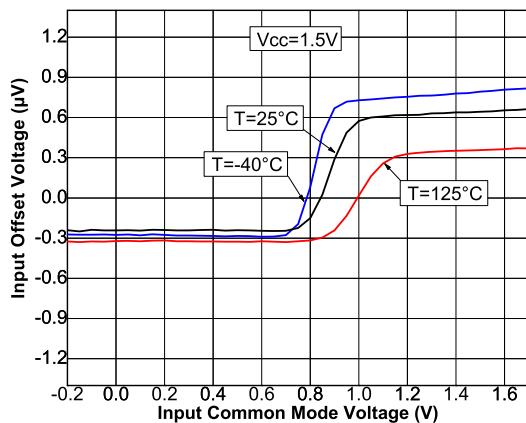
### 4.1 Operating voltages

The TSV62x/TSV62xA can operate from 1.5 to 5.5 V. Parameters are fully specified for 1.8-, 3.3-, and 5-V power supplies. However, the parameters are very stable in the full  $V_{CC}$  range and several characterization curves show the TSV62x/TSV62xA characteristics at 1.5 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 °C to 125 °C.

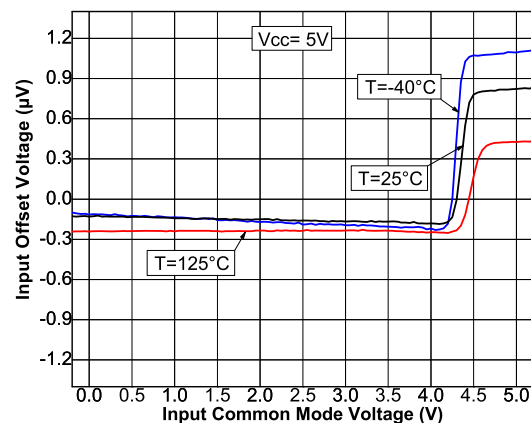
### 4.2 Rail-to-rail input

The TSV62x/TSV62xA is built with two complementary PMOS and NMOS input differential pairs. The device has a rail-to-rail input, and the input common mode range is extended from  $(V_{CC-}) - 0.1$  V to  $(V_{CC+}) + 0.1$  V. The transition between the two pairs appears at  $(V_{CC+}) - 0.7$  V. In the transition region, the performance of CMRR, PSRR,  $V_{io}$  (Figure 16 and Figure 17) and THD is slightly degraded.

**Figure 16. Input offset voltage vs input common mode at  $V_{CC} = 1.5$  V**



**Figure 17. Input offset voltage vs input common mode at  $V_{CC} = 5$  V**



The devices are guaranteed without phase reversal.

### 4.3 Rail-to-rail output

The operational amplifier's output level can go close to the rails: 35 mV maximum above and below the rail when connected to a 10 k $\Omega$  resistive load to  $V_{CC}/2$ .

### 4.4 Optimization of DC and AC parameters

These operational amplifiers use an innovative approach to reduce the spread of the main DC and AC parameters. An internal adjustment achieves a very narrow spread of current consumption (29  $\mu\text{A}$  typical, min/max at  $\pm 17\%$ ). Parameters linked to the current consumption value, such as GBP, SR and AVd benefit from this narrow dispersion. All parts present a similar speed and the same behavior in terms of stability. In addition, the minimum values of GBP and SR are guaranteed (GBP = 350 kHz min, SR = 0.12 V/ $\mu\text{s}$  min).

### 4.5 Shutdown function (TSV623, TSV625)

The operational amplifier is enabled when the  $\overline{\text{SHDN}}$  pin is pulled high. To disable the amplifier, the  $\overline{\text{SHDN}}$  must be pulled down to  $V_{\text{CC-}}$ . When in shutdown mode, the amplifier output is in a high impedance state. The  $\overline{\text{SHDN}}$  pin must never be left floating but tied to  $V_{\text{CC+}}$  or  $V_{\text{CC-}}$ . The turn-on and turn-off times are calculated for an output variation of  $\pm 200$  mV (Figure 18 and Figure 19 show the test configurations). Figure 20 and Figure 21 show output voltage behavior when the  $\overline{\text{SHDN}}$  pin is toggled.

Figure 18. Test configuration for turn-on time (Vout pulled down)

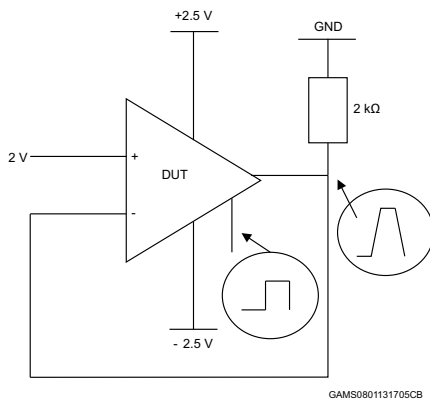


Figure 19. Test configuration for turn-off time (Vout pulled down)

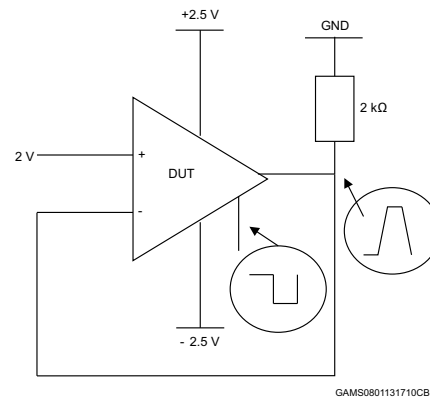


Figure 20. Turn-on time,  $V_{\text{CC}} = \pm 2.5$  V, Vout pulled down,  $T = 25$  °C

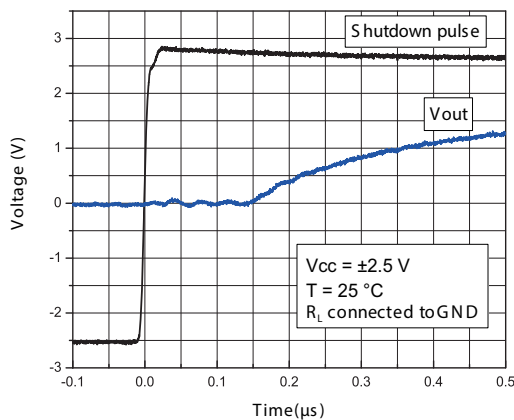
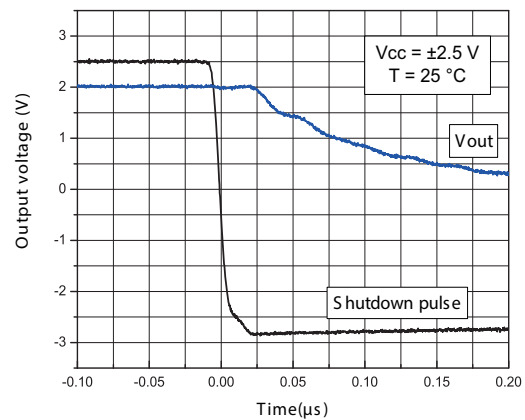


Figure 21. Turn-off time,  $V_{\text{CC}} = \pm 2.5$  V, Vout pulled down,  $T = 25$  °C

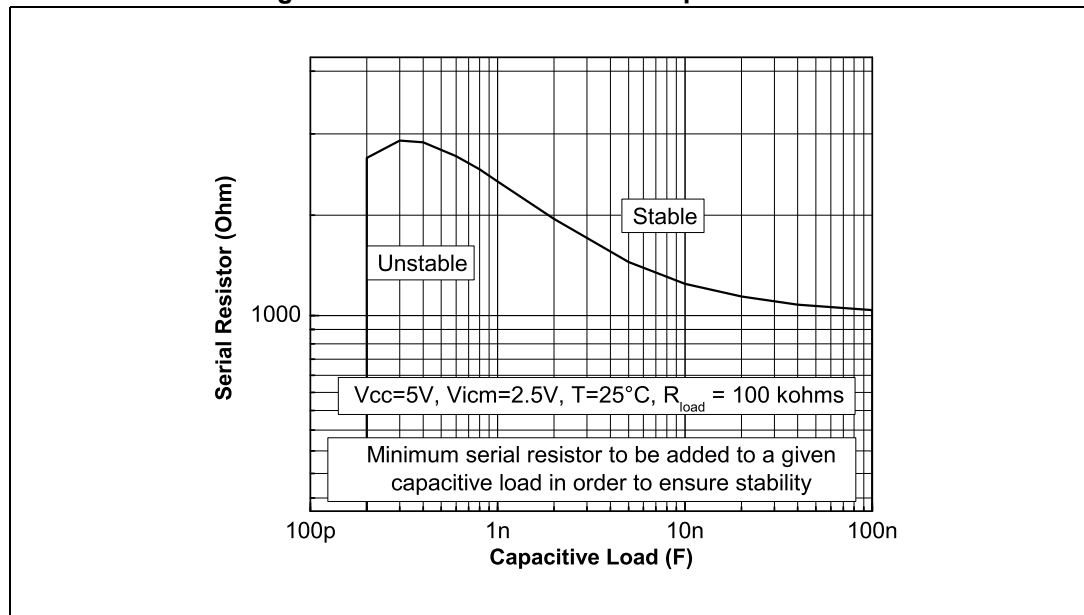


## 4.6 Driving resistive and capacitive loads

These products are micro-power, low-voltage operational amplifiers optimized to drive rather large resistive loads, above 5 k $\Omega$ . For lower resistive loads, the THD level may significantly increase.

In a *follower* configuration, these operational amplifiers can drive capacitive loads up to 100 pF with no oscillations. When driving larger capacitive loads, adding a small resistor in series at the output can improve the stability of the device (see [Figure 22](#) for recommended in-series resistor values). Once the value of the in-series resistor has been selected, the stability of the circuit should be tested on bench and simulated with the simulation model.

**Figure 22. In-series resistor vs. capacitive load**



## 4.7 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

## 4.8 Macromodel

Two accurate macromodels (with or without shutdown feature) of TSV62x/TSV62xA are available on STMicroelectronics' web site at [www.st.com](http://www.st.com). This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV62x/TSV62xA operational amplifiers. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It helps to validate a design approach and to select the right operational amplifier, *but it does not replace on-board measurements*.

## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 5.1 SO8 package information

Figure 23. SO8 package outline

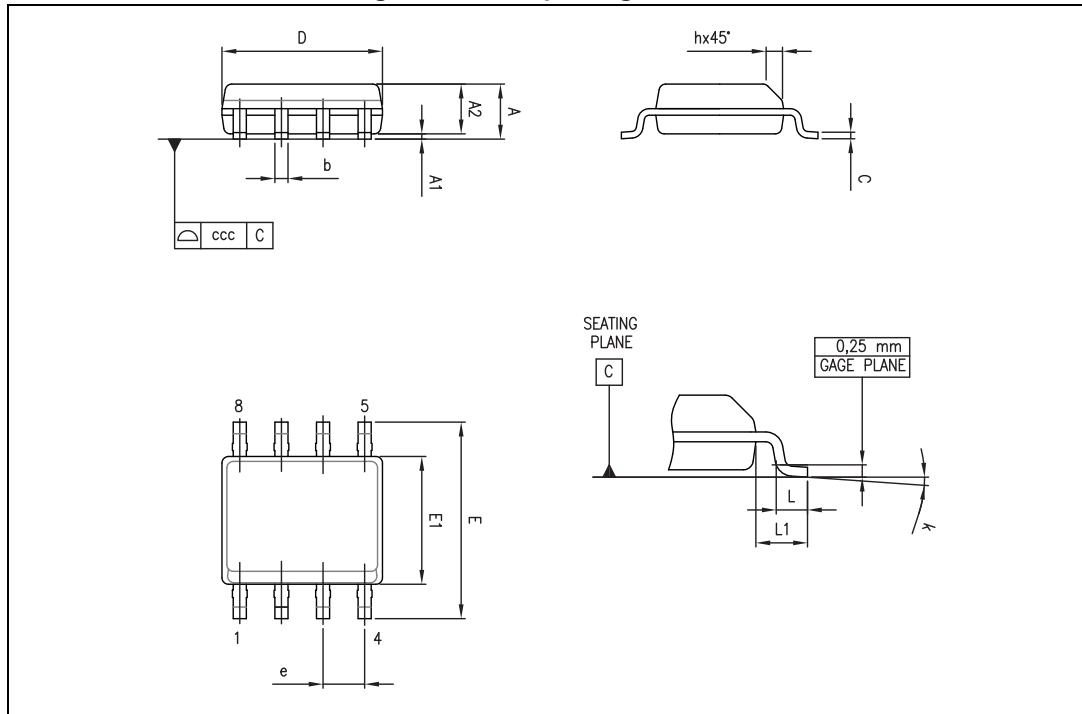


Table 9. SO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0		8°	1°		8°
ccc			0.10			0.004

## 5.2 MiniSO8 package information

Figure 24. MiniSO8 package outline

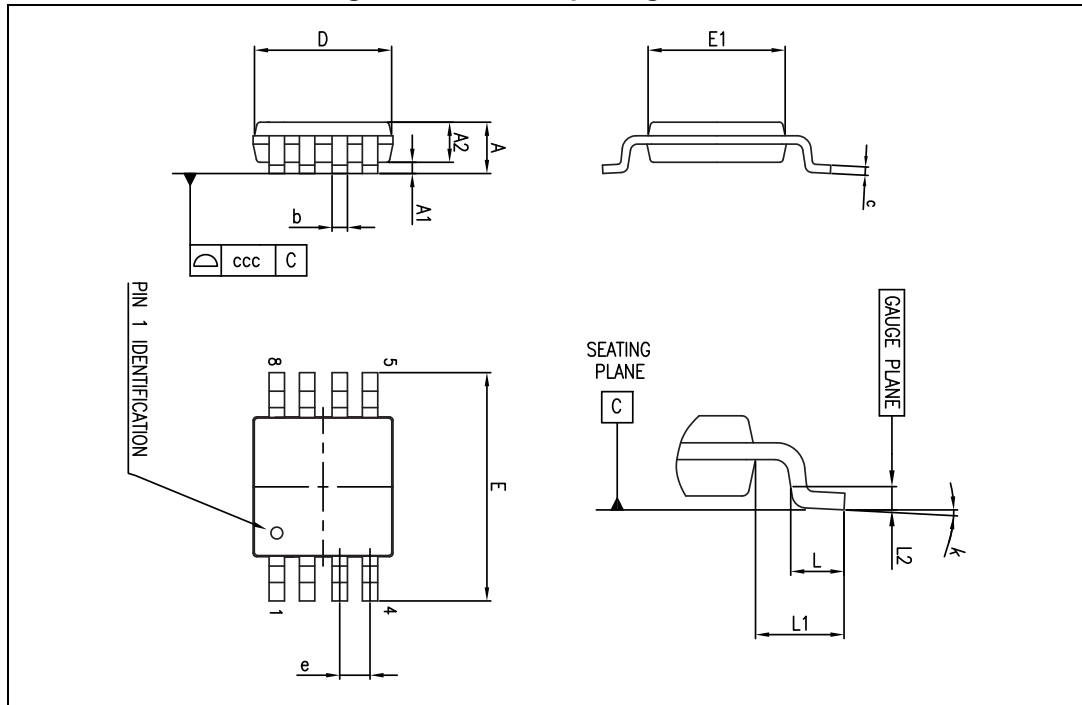


Table 10. MiniSO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

### 5.3 MiniSO10 package information

Figure 25. MiniSO10 package outline

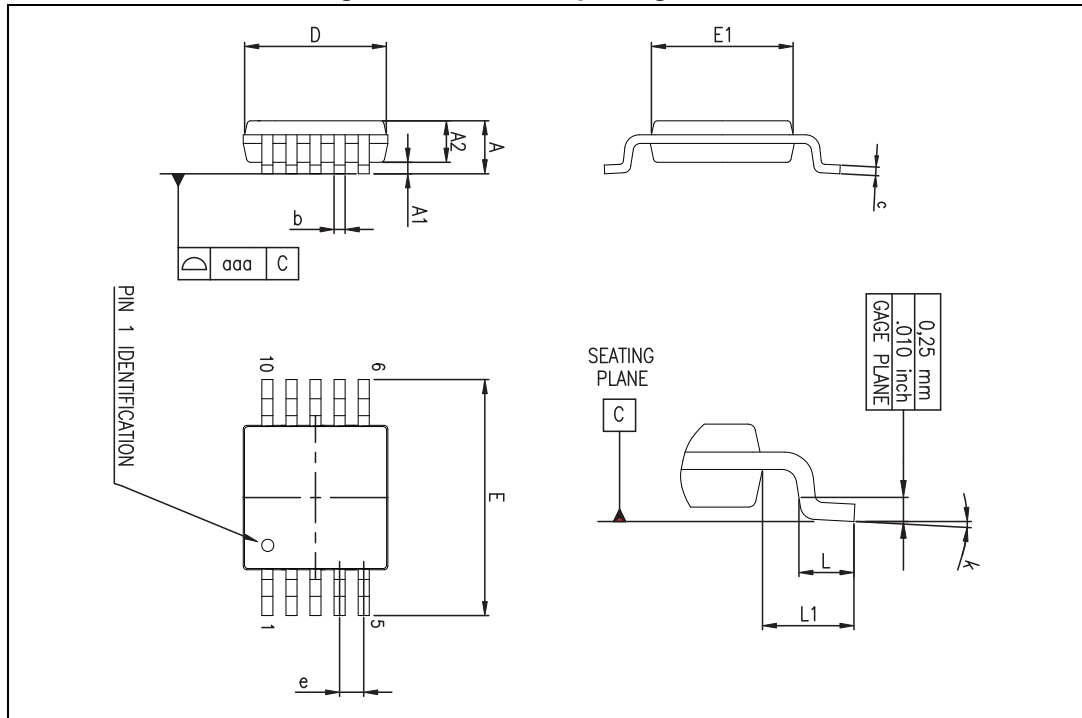


Table 11. MiniSO10 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.10			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.034	0.037
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.15	0.23	0.30	0.006	0.009	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.50			0.020	
L	0.40	0.55	0.70	0.016	0.022	0.028
L1		0.95			0.037	
k	0°	3°	6°	0°	3°	6°
aaa			0.10			0.004

### 5.4 TSSOP14 package information

Figure 26. TSSOP14 package outline

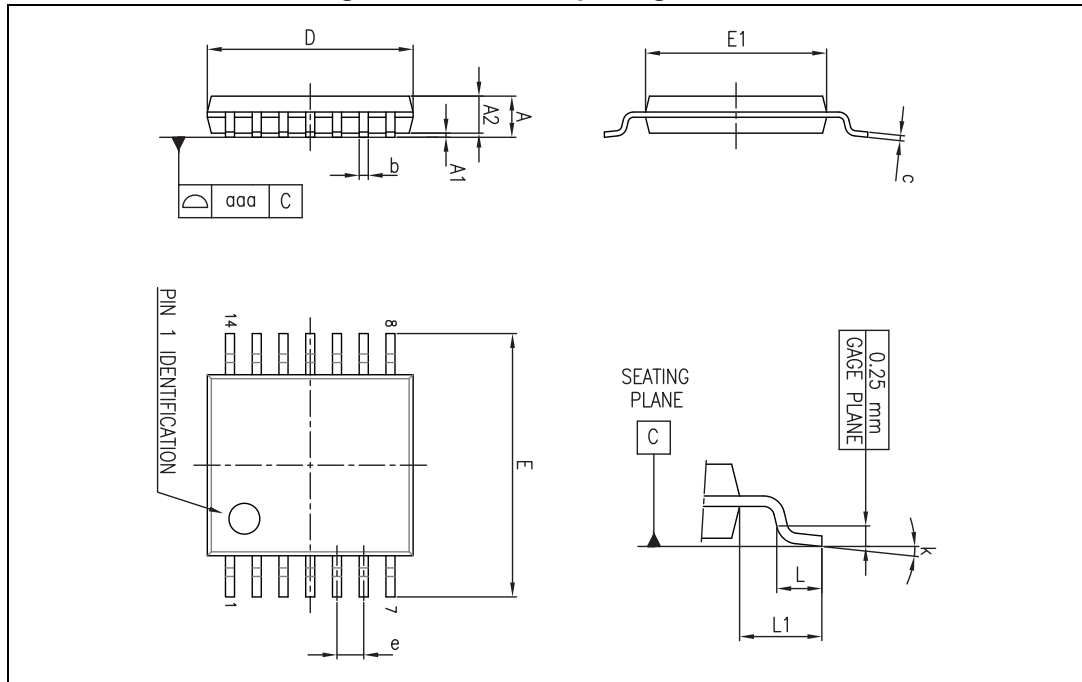


Table 12. TSSOP14 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

### 5.5 TSSOP16 package information

Figure 27. TSSOP16 package outline

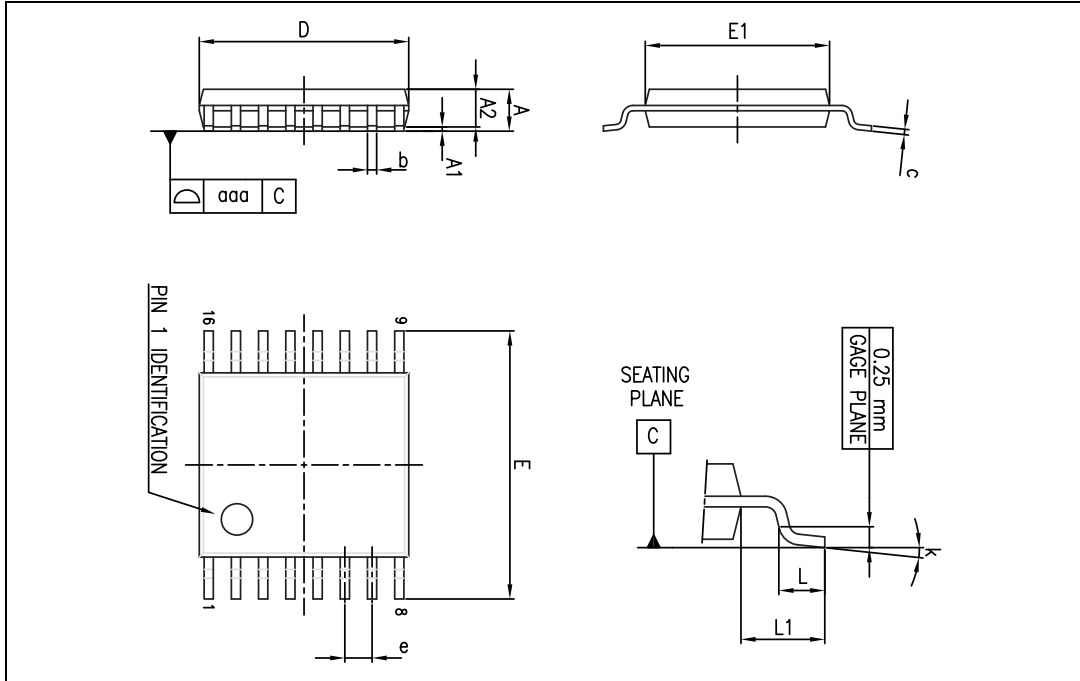


Table 13. TSSOP16 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
aaa			0.10			0.004

## 6 Ordering information

Table 14. Order codes

Order codes	Temperature range	Package	Packing	Marking
TSV622IDT	-40 °C to 125 °C	SO8	Tape and reel	TSV622
TSV622AIDT				TSV622A
TSV622IST		MiniSO8		K107
TSV622AIST				K143
TSV623IST		MiniSO10		K114
TSV623AIST				K144
TSV624IPT		TSSOP14		TSV624
TSV624AIPT				TSV624A
TSV625IPT		TSSOP16		TSV625
TSV625AIPT				TSV625A

## 7 Revision history

**Table 15. Document revision history**

Date	Revision	Changes
25-May-2009	1	Initial release.
15-Jun-2009	2	Corrected pin connection diagram in Figure 1.
24-Aug-2009	3	Added root part numbers (TSv62xA) and Table 1: Device summary on cover page. Added order code TSV622AILT in Table 15: Order codes.
22-Oct-2009	4	Corrected error in Table 15: Order codes: TSV625 offered in TSSOP16.
09-Jan-2013	5	Updated Features. Updated Figure 1. Table 4, Table 6, and Table 7: replaced $DV_{iO}$ with $\Delta V_{iO}/\Delta T$ . Section 4.5: Shutdown function (TSV623, TSV625): added explanation of Figure 20 and Figure 21; replaced Figure 18 and Figure 19; updated Figure 20 and Figure 21. Corrected error in Table 15: Order codes: the marking for the order code TSV622AILT is K143.
23-May-2017	6	Changed part number layout on cover page Removed package SOT23-5 <a href="#">Table 4</a> , <a href="#">Table 6</a> , and <a href="#">Table 7</a> : updated $V_{OH}$ parameter information and changed min. values to max. values. <a href="#">Table 14: Order codes</a> : removed obsolete order codes: TSV622ILT, TSV622AILT, TSV622ID, TSV622AID

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