THE DATASHEET OF

UC3843AN

UC1842A, UC1843A, UC1844A, UC1845A
UC2842A, UC2843A, UC2844A, UC2845A
UC3842A, UC3843A, UC3844A, UC3845A

SLUS224F – SEPTEMBER 1994 – REVISED OCTOBER 2017

UCx84xA Current-Mode PWM Controller

1 Features

- Optimized for Off-Line and DC-DC Converters
- Low Start-Up Current (< 0.5 mA)
- Trimmed Oscillator Discharge Current
- Automatic Feedforward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Undervoltage Lockout With Hysteresis
- Double Pulse Suppression
- High-Current Totem Pole Output
- Internally-Trimmed Bandgap Reference
- Up to 500-kHz Operation
- Create a Custom Design Using the UCx84xA With the WEBENCH® Power Designer

2 Applications

- Switch Mode Power Supplies (SMPS)
- DC-DC Converters
- Power Modules
- Industrial PSU
- Battery Operated PSU

3 Description

The UCx84xA family of control devices is a pin-for-pin compatible improved version of the UCx84x family. Providing the necessary features to control current-mode or switched-mode power supplies, this family of devices has many improved features: startup current is less than 0.5 mA, oscillator discharge is trimmed to 8.3 mA, and during UVLO, the output stage can sink at least 10 mA at less than 1.2 V for V_{CC} over 5 V.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UC1842A, UC1843A, UC1844A, UC1845A	CDIP (8)	6.67 mm × 9.60 mm
	LCCC (20)	8.89 mm × 8.89 mm
UC2843A	PLCC (20)	8.96 mm × 8.96 mm
UC2842A, UC2843A, UC2844A, UC2845A, UC3842A, UC3843A, UC3844A, UC3845A	PDIP (8)	6.35 mm × 9.81 mm
	SOIC (8)	3.91 mm × 4.90 mm
	SOIC (14)	3.91 mm × 8.65 mm
	SOIC (16)	7.50 mm × 10.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Device Comparison Table

DEVICE	UVLO ON	UVLO OFF	MAX DUTY CYCLE
UC1842A	16 V	10 V	<100%
UC1843A	8.4 V	7.6 V	<100%
UC1844A	16 V	10 V	<50%
UC1845A	8.4 V	7.6 V	<50%

Simplified Application Diagram

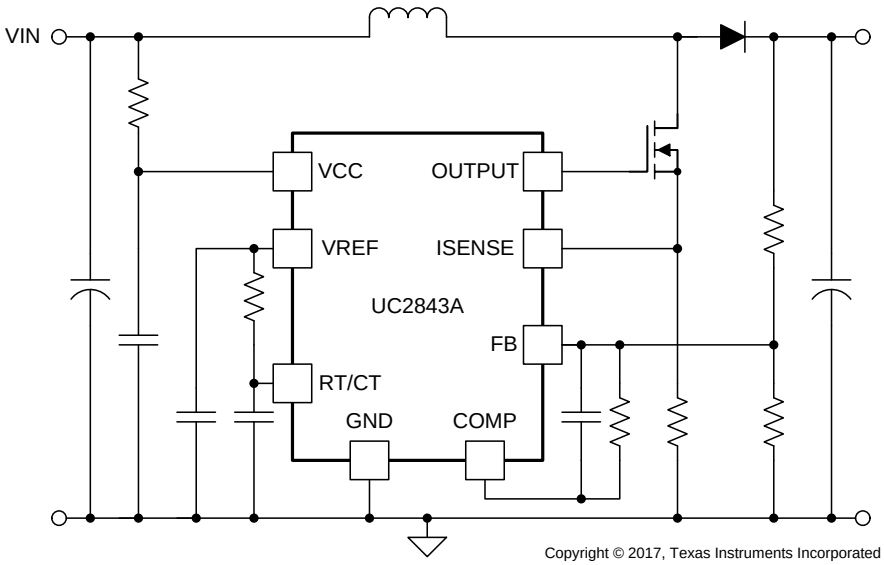


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2017) to Revision F **Page**

- Added WEBENCH links in three places, Features, Application and Implementation and Device and Documentation Support. 1
- Added copyright information to the Simplified Application Diagram 1
- Changed operating free-air temperature of the UC284xA changed from 125°C to 85°C. 6
- Changed operating free-air temperature of the UC384xA changed from -40°C to 0°C. 6
- Changed operating free-air temperature of the UC384xA changed from 85°C to 70°C. 6
- Changed the frequency (f) calculation to the correct equation..... 13
- Changed the C_{OUT} equation to the corrected equation. 17
- Changed the L_{PM} equation to the corrected equation. 18
- Added $G_{CO}(f)$ definition and equation. 19
- Changed the f_{RHPz} equation to the corrected equation. 19

Changes from Revision D (July 2011) to Revision E **Page**

- Added *Applications* section, *Device Information* table, *Pin Configuration and Functions* section, *Specifications* section, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Deleted *Ordering Information Table*; see POA at the end of the datasheet 1

Changes from Revision C (August 2010) to Revision D **Page**

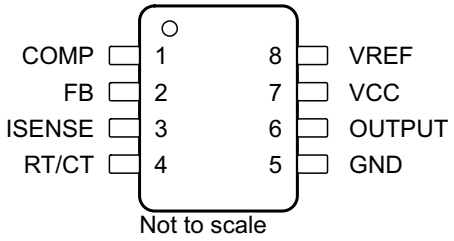
- Changed Absolute Maximum ratings table with maximum negative voltage and GND pin notes. 6

Changes from Revision B (September 2009) to Revision C **Page**

- Corrected I_{SINK} voltage..... 8

5 Pin Configuration and Functions

CDIP, PDIP, and SOIC Packages
8-Pin JG, P, and D
Top View



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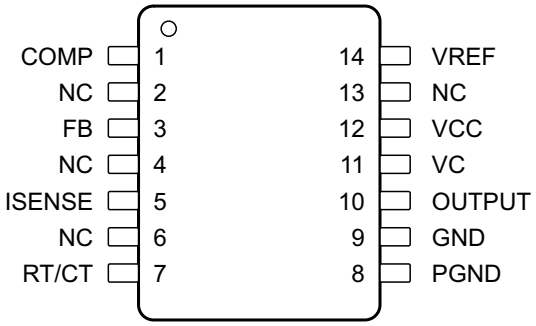
SOIC Package
14-Pin D
Top View



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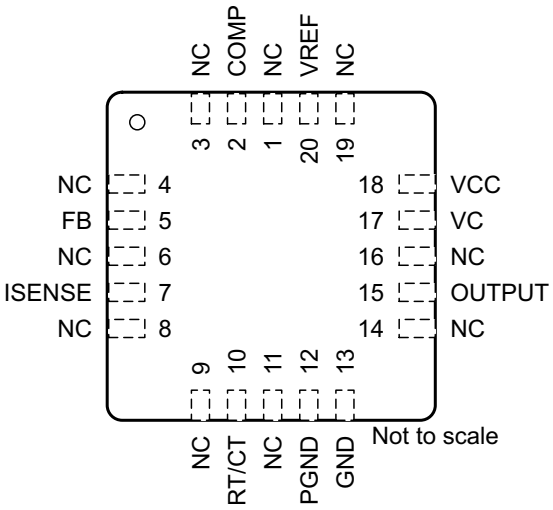
LCCC and PLCC Packages
20-Pin FK and FN
Top View



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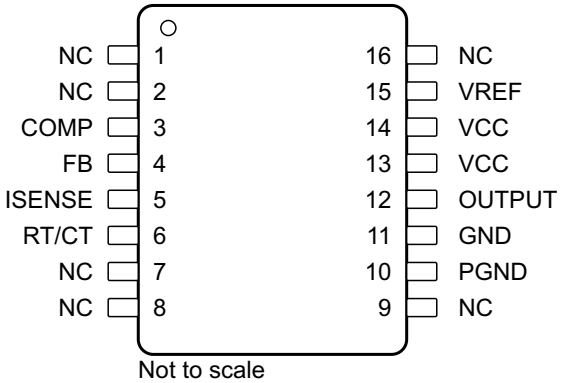
SOIC Package
16-Pin DW
Top View



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Pin Functions

PIN					I/O	DESCRIPTION
NAME	NO.					
	CDIP (8), PDIP (8), SOIC (8)	LCCC (20), PLCC (20)	SOIC (14)	SOIC (16)		
COMP	1	2	1	3	O	Outputs the low impedance 1-MHz internal error amplifier that is also the input to the peak current limit or PWM comparator, with an open-loop gain (AVOL) of 80 dB. This pin is capable of sinking a maximum of 6 mA and is not internally current limited.
FB	2	5	3	4	I	Input to the error amplifier that can be used to control the power converter voltage-feedback loop for stability.
GND	5	13	9	11	—	This is the controller signal ground.
ISENSE	3	7	5	5	I	Input to the peak current limit, PWM comparator of the UCx84xA controllers. When used in conjunction with a current sense resistor, the error amplifier output voltage controls the power systems cycle-by-cycle peak current limit. The maximum peak current sense signal is internally clamped to 1 V. See *Functional Block Diagram*.
OUTPUT	6	15	10	12	O	Output of 1-A totem pole gate driver. This pin can sink and source up to 1 A of gate driver current. A gate driver resistor must be used to limit the gate driver current.
PGND	—	12	8	10	—	Power ground and the gate driver return. For devices that have this pin, star grounding techniques can be used to redirect the gate driver current away from the signal ground pin (GND). This technique can reduce PWM controller instabilities caused by gate driver return current.
RT/CT	4	10	7	6	I	Input to the internal oscillator that is programmed with an external timing resistor (RT) and timing capacitor (CT). See *Oscillator* for information on properly selecting these timing components. TI recommends using capacitance values from 470 pF to 4.7 nF. TI also recommends that the timing resistor values chosen be from 5 kΩ to 100 kΩ.
VC	—	17	11	—	I	Bias input to the gate driver. For PWM controllers that do not have this pin, the gate driver is biased from the VCC pin. This pin must have a biasing capacitor that is at least 10 times greater than the gate capacitance of the main switching FET used in the design.
VCC	7	18	12	13, 14	I	Bias input to the gate driver. This pin must have a biasing capacitor that is at least 10 times greater than the gate capacitance of the main switching FET used in the design.
VREF	8	20	14	15	O	Reference voltage output of the PWM controller. This pin must supply no more than 10 mA under normal operation. This output is short-circuit protected at roughly 100 mA. This reference is also used for internal comparators and needs a high frequency bypass capacitor of 1 µF. The VCC capacitor also must be at least 10 times greater than the capacitor on the VREF pin.
NC	—	1, 3, 4, 6, 8, 9, 11, 14, 16, 19	2, 4, 6, 13	1, 2, 7, 8, 9, 16	—	No connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage (low impedance source)	VCC pin		30	V
Output current, I_{OUT}			±1	A
Output energy (capacitive load)			5	µJ
Analog inputs		–0.3	6.3	V
Maximum negative voltage	All pins	–0.3		V
Differential voltage between VC and VCC	VC pin	–0.3		V
Error amplifier output sink current, I_{COMP}			10	mA
Power dissipation at $T_A \leq 25°C$			1	W
Lead temperature (soldering, 10 s)			300	°C
Junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Bias supply voltage	VCC pin		11		V
V_{FB}, V_{RC}, V_{VFB}	Voltage on analog pins	FB, ISENSE, and RT/CT pins	–0.1		5	V
V_{OUT}	Gate driver output voltage		–0.1		V_{CC}	V
I_{VCC}	Supply bias current				25	mA
I_{VREF}	Output current	VREF pin			10	mA
f_{OSC}	Oscillator frequency				500	kHz
T_A	Operating free-air temperature	UC184xA	–55		125	°C
		UC284xA	–40		85	
		UC384xA	0		70	

6.4 Thermal Information

THERMAL METRIC[1]		UC184xA		UC2843A	UC284xA, UC384xA				UNIT
		JG (CDIP)	FK (LCCC)	FN (PLCC)	P (PDIP)	D (SOIC)	D (SOIC)	DW (SOIC)	
		8 PINS	20 PINS	20 PINS	8 PINS	8 PINS	14 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	—	—	56.7	53.4	104.3	77.9	73.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64	36.2	34.6	46.4	46.8	35.8	35	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.5	35.4	21.8	30.7	45.3	32.5	38.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	—	—	10.4	16.8	6	6.6	9.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	—	—	21.5	30.6	44.6	32.2	37.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.1	4.1	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C (UC184xA), T_A = –40°C to 125°C (UC284xAQ), T_A = –40°C to 85°C (UC284xA), T_A = 0°C to 70°C (UC384xA); $T_A = T_J$; V_{CC} = 15 V[1]; R_T = 10 kΩ; C_T = 3.3 nF.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE						
Output voltage	T_J = 25°C, I_O = 1 mA	UC184xA, UC284xA	4.95	5	5.05	V
		UC384xA	4.9	5	5.1	
Line regulation	12 ≤ V_{IN} ≤ 25 V			6	20	mV
Load regulation	1 ≤ I_O ≤ 20 mA			6	25	mV
Temperature stability	See [2][3]			0.2	0.4	mV/°C
Total output variation	Line, Load, Temperature	UC184xA, UC284xA	4.9		5.1	V
		UC384xA	4.82		5.18	
Output noise voltage	10 Hz ≤ f ≤ 10 kHz; T_J = 25°C[2]			50		µV
Long-term stability	T_A = 125°C, 1000 hrs[2]			5	25	mV
Output short circuit			–30	–100	–180	mA
OSCILLATOR						
Initial accuracy	T_J = 25°C[4]		47	52	57	kHz
Voltage stability	12 ≤ V_{CC} ≤ 25 V			0.2%	1%	
Temperature stability	$T_{MIN} \le T_A \le T_{MAX}$[2]			5%		
Amplitude	$V_{RT/CT}$ peak to peak[2]			1.7		V
Discharge current	T_J = 25°C, $V_{RT/CT}$ = 2 V[5]		7.8	8.3	8.8	mA
	$V_{RT/CT}$ = 2 V[5]	UC184xA, UC284xA	7.5		8.8	
		UC384xA	7.6		8.8	

(1) Adjust V_{CC} above the start threshold before setting at 15 V.
(2) Ensured by design, but not 100% production tested.
(3) Temperature stability, sometimes referred to as *average temperature coefficient*, is described by: Temperature stability = ($V_{REF(max)} - V_{REF(min)}$) / ($T_{J(max)} - T_{J(min)}$). $V_{REF(max)}$ and $V_{REF(min)}$ are the maximum and minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.
(5) This parameter is measured with R_T = 10 kΩ to V_{REF}. This contributes approximately 300 µA of current to the measurement. The total current flowing into the RT/CT pin is approximately 300 µA higher than the measured value.

Electrical Characteristics (continued)

Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C (UC184xA), T_A = –40°C to 125°C (UC284xAQ), T_A = –40°C to 85°C (UC284xA), T_A = 0°C to 70°C (UC384xA); $T_A = T_J$; V_{CC} = 15 V(1); R_T = 10 kΩ; C_T = 3.3 nF.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ERROR AMPLIFIER							
	Input voltage	V_{COMP} = 2.5 V	UC184xA, UC284xA	2.45	2.5	2.55	V
			UC384xA	2.42	2.5	2.58	
	Input bias current				–0.3	–1	µA
					–0.3	–2	
A_{VOL}	Open-loop gain	2 ≤ V_O ≤ 4 V		65	90		dB
	Unity gain bandwidth	T_J = 25°C(2)		0.7	1		MHz
CMRR	Common mode rejection ratio	12 ≤ V_{CC} ≤ 25 V		60	70		dB
	Output sink current	V_{FB} = 2.7 V, V_{COMP} = 1.1 V		2	6		mA
	Output source current	V_{FB} = 2.3 V, V_{COMP} = 5 V		–0.5	–0.8		mA
	V_{OUT} high	V_{FB} = 2.3 V, R_L = 15 kΩ to ground		5	6		V
	V_{OUT} low	V_{FB} = 2.7 V, R_L = 15 kΩ to VREF			0.7	1.1	V
CURRENT SENSE							
	Gain	See (6)(7)		2.85	3	3.15	V/V
	Maximum input signal	V_{COMP} = 5 V(6)		0.9	1	1.1	V
PSRR	Power supply rejection ratio	12 ≤ V_{CC} 25 V(6)			70		dB
	Input bias current				–2	–10	µA
	Delay to output	V_{ISENSE} = 0 to 2 V(2)			150	300	ns
OUTPUT							
	Output low level	I_{SINK} = 20 mA			0.1	0.4	V
		I_{SINK} = 200 mA			15	2.2	
	Output high level	I_{SOURCE} = 20 mA		13	13.5		V
		I_{SOURCE} = 200 mA		12	13.5		
	Rise time	T_J = 25°C, C_L = 1 nF(2)			50	150	ns
	Fall time	T_J = 25°C, C_L = 1 nF(2)			50	150	ns
	UVLO saturation	V_{CC} = 5 V, I_{SINK} = 10 mA			0.7	1.2	V
UNDERVOLTAGE LOCKOUT							
	Start threshold	UC1842A, UC1844A, UC2842A, and UC2844A		15	16	17	V
		UC3842A and UC3844A		14.5	16	17.5	
		UCx843A and UCx845A		7.8	8.4	9	
	Minimum operation voltage after turnon	UC1842A, UC1844A, UC2842A, and UC2844A		9	10	11	V
		UC3842A and UC3844A		8.5	10	11.5	
		UCx843A and UCx845A		7	7.6	8.2	
PWM							
	Maximum duty cycle	UCx842A, UCx843A		94%	96%	100%	
		UCx844A, UCx845A		47%	48%	50%	
	Minimum duty cycle					0%	
TOTAL STANDBY CURRENT							
	Start-up current				0.3	0.5	mA
	Operating supply current	V_{FB} = V_{ISENSE} = 0 V			11	17	mA
	V_{CC} Zener voltage	I_{CC} = 25 mA		30	34		V

(6) Parameter measured at trip point of latch with V_{FB} = 0.
(7) Gain defined as: A = ΔV_{COMP} / ΔV_{ISENSE}; 0 ≤ V_{ISENSE} ≤ 0.8 V.

6.6 Typical Characteristics

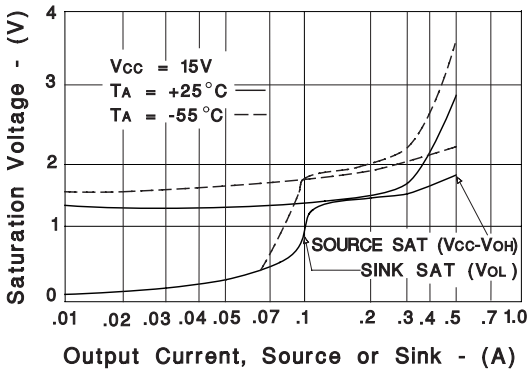


Figure 1. Output Saturation Characteristics

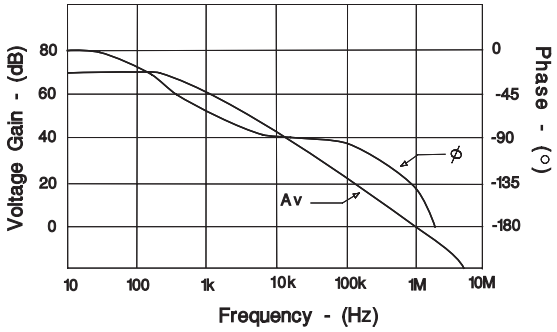


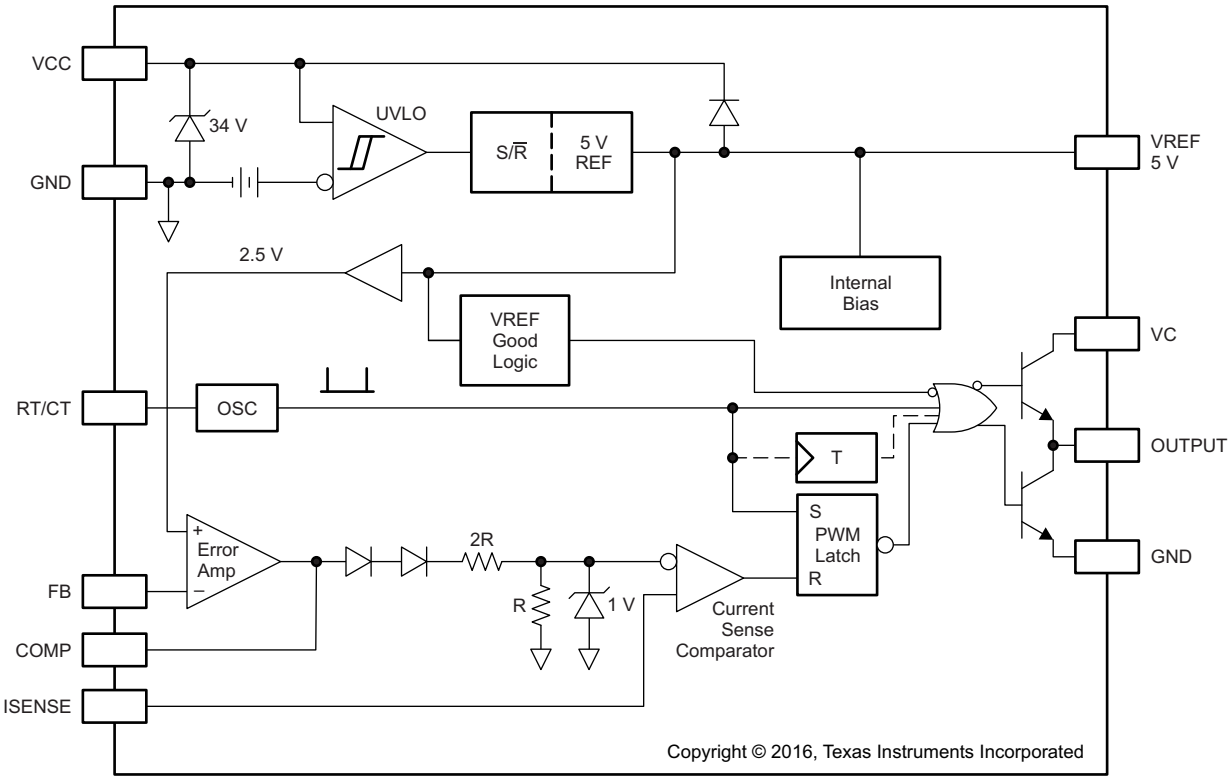
Figure 2. Error Amplifier Open-Loop Frequency Response

7 Detailed Description

7.1 Overview

The UCx84xA family of fixed-frequency pulse-width-modulator (PWM) controllers are designed to operate at switching frequencies of 500 kHz. These controllers are designed for peak current mode (PCM) and can be used in isolated and non-isolated power supply designs. These controllers can drive FETs directly from the output, which is capable of sourcing and sinking up to 1 A of gate driver current. These devices also have a built-in low-impedance amplifier that can be used in non-isolated designs to control the power supply output voltage and feedback loop.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pulse-by-Pulse Current Limiting

Pulse-by-pulse limiting is inherent in the current mode control scheme. An upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

7.3.2 Current Sense Circuit

Peak current (I_S) is determined by Equation 1:

$$I_{S(max)} \times \frac{1\,V}{R_S} \quad (1)$$

A small RC filter may be required to suppress switch transients.

Feature Description (continued)

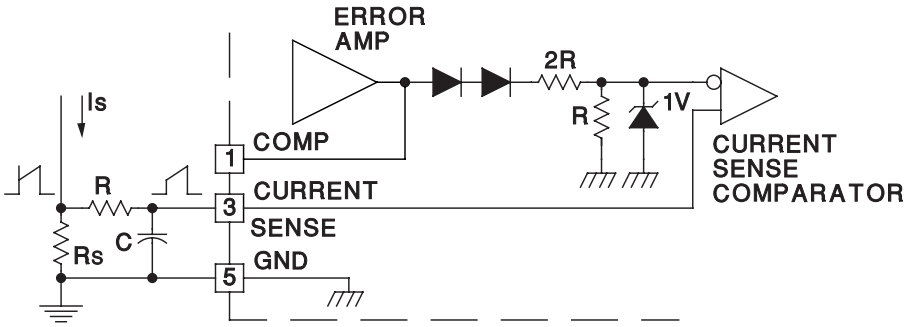


Figure 3. Current Sense Circuit Diagram

7.3.3 Error Amplifier Configuration

The error amplifier can source up to 0.8 mA, and sink up to 6 mA.

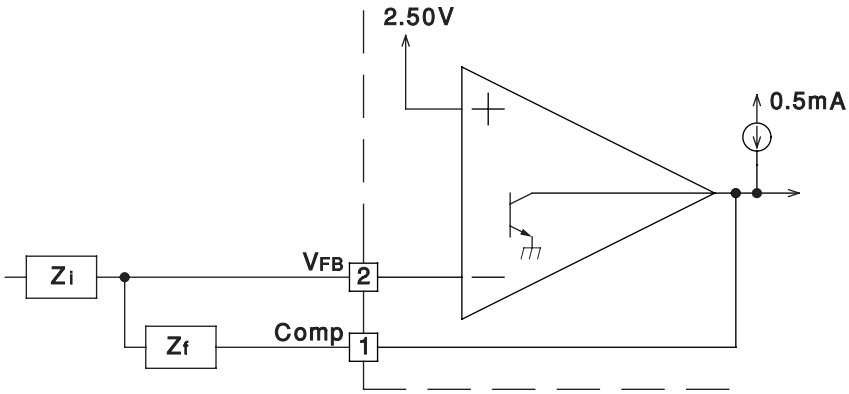


Figure 4. Error Amplifier Configuration Diagram

7.3.4 Undervoltage Lockout

The UCx84xA devices feature undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences. Undervoltage lockout thresholds for the UCx842A, UCx843A, UCx844A, and UCx845A devices are optimized for two groups of applications: off-line power supplies and DC-DC converters. With a wider VCC_{ON} to VCC_{OFF} range, the UCx842A and UCx844A devices are ideally suited to off-line AC input applications. The UCx843A and UCx845A controllers have a much narrower VCC_{ON} to VCC_{OFF} hysteresis and may be used in DC to DC applications where the input is considered regulated.

During UVLO the IC draws typically 0.3 mA of supply current. This VCC current is considerable less than the UCx84x family and results in lower power drawn from the line. The reduced start-up current is of particular concern in off-line supplies where the IC is *powered-up* from the high-voltage DC rail, then bootstrapped to an auxiliary winding on the main transformer. Power is then dissipated in the start-up resistor which is sized by the IC's start-up current. Lowering this by 50% in the UCx84xA version family, as compared to the UCx84x family, reduces the resistors power loss by the same percentage. Once crossing the turnon threshold the IC supply current increases typically to about 11 mA, During undervoltage lockout, the UCx84xA series of devices prevent the power MOSFET from parasitically turning on due to the *Miller* effect at power-up. This improved design to the lower totem-pole transistor's operation during undervoltage lockout allows the IC to sink higher currents, up to 10 mA, at saturation voltages as low as 0.7 V, compared to the UCx84x devices which would only sink up to 0.2 mA under the same conditions.

Feature Description (continued)

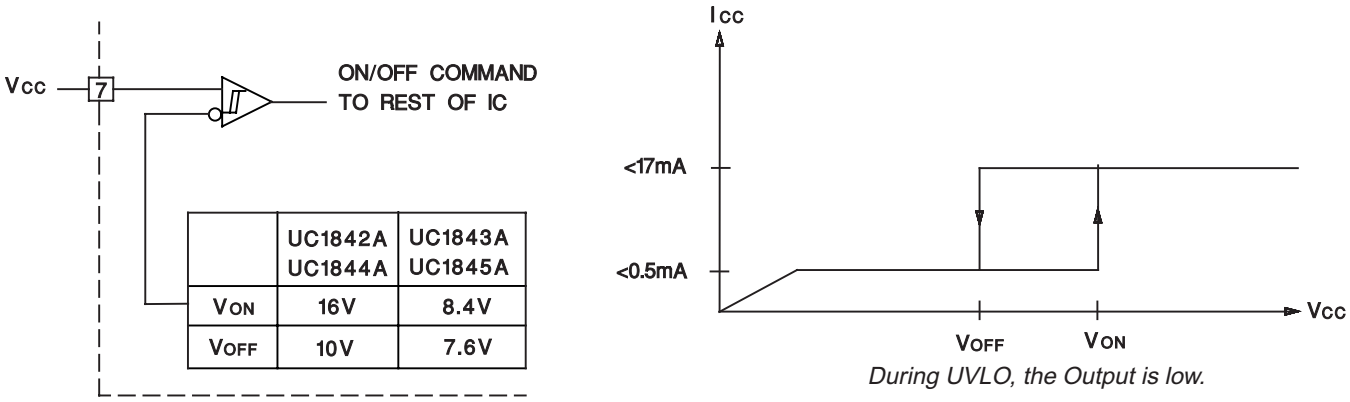


Figure 5. Undervoltage Lockout

7.3.5 Oscillator

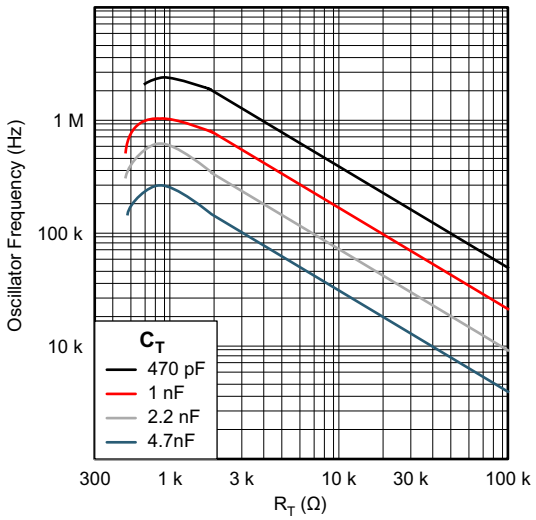


Figure 6. Oscillator Frequency vs Timing Resistance

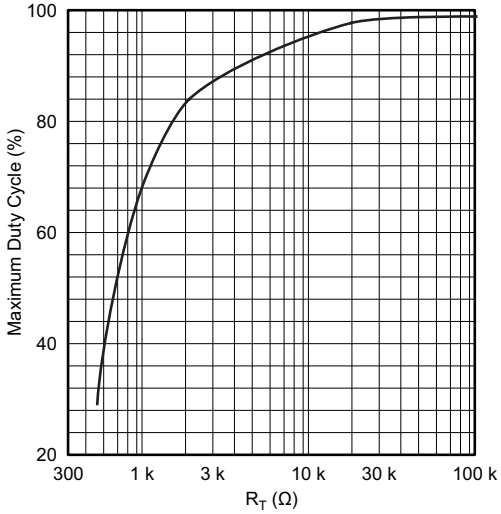


Figure 7. Maximum Duty Cycle vs Timing Resistance

Feature Description (continued)

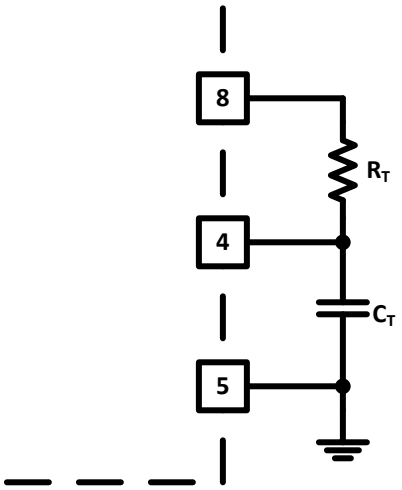


Figure 8. Oscillator Section

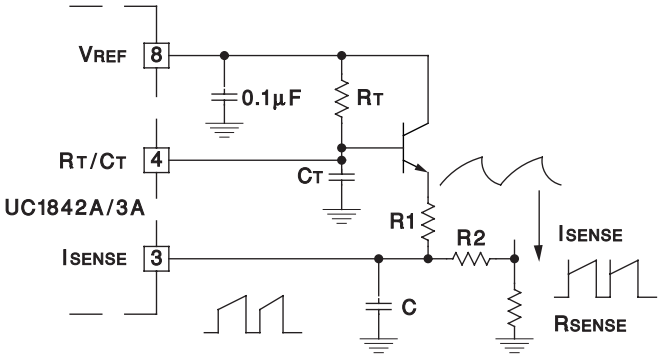


Figure 9. Slope Compensation

Precision operation at high frequencies with an accurate maximum duty cycle, see Figure 7, can now be obtained with the UCx84xA family of devices due to its trimmed oscillator discharge current. This nullifies the effects of production variations in the initial discharge current or dead time. Previous versions of the UCx84x devices had greater than a 2:1 oscillator discharge current range and resulted in less reliable maximum duty cycle programming.

A fraction of the oscillator ramp can be resistively summed with the current sense signal, to provide slope compensation for converters requiring duty cycles over 50%. Capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.

7.4 Device Functional Modes

7.4.1 Normal Operation

The IC can be used in peak current mode (PCM) control or voltage mode (VM) control. When the converter is operating in PCM, the voltage amplifier output will regulate the converter's peak current and duty cycle. When the IC is used in VM control, the voltage amplifier output will regulate the power converter's duty cycle. The regulation of the system's peak current and duty cycle can be achieved with the use of the integrated error amplifier and external feedback circuitry.

7.4.2 Undervoltage Lockout (UVLO) Start-Up

During system start-up, VCC voltage starts to rise from 0. Before the VCC voltage reaches its corresponding start threshold, the IC is operating in UVLO mode. After the UVLO turn start-up threshold is met the device will become active and the reference will come up to 5 V.

7.4.3 UVLO Turnoff Mode

If the bias voltage to VCC drops below the UVLO minimum operating voltage, PWM switching stops and the reference will become inactive, returning to 0 V. The device can be restarted by applying a voltage greater than the UVLO start threshold to the VCC pin.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCx84xA controllers are peak-current mode pulse-width modulators. These controllers have an onboard amplifier and can be used in isolated or nonisolated power supply designs. There is an onboard totem-pole gate driver capable of delivering 1 A of peak current. This is a high-speed PWM capable of operating at switching frequencies up to 500 kHz.

8.2 Typical Application

A typical application for the UC3842A in an off-line flyback converter is shown in Figure 10. The UC3842A uses an inner current control loop that contains a small current sense resistor which senses the primary inductor current ramp. This current sense resistor transforms the inductor current waveform to a voltage signal that is input directly into the primary side PWM comparator. This inner loop determines the response to input voltage changes. An outer voltage control loop involves comparing a portion of the output voltage to a reference voltage at the input of an error amplifier. When used in an off-line isolated application, the voltage feedback of the isolated output is accomplished using a secondary-side error amplifier and adjustable voltage reference, such as the TL431. The error signal crosses the primary to secondary isolation boundary using an opto-isolator whose collector is connected to the VREF pin and the emitter is connected to FB. The outer voltage control loop determines the response to load changes.

Typical Application (continued)

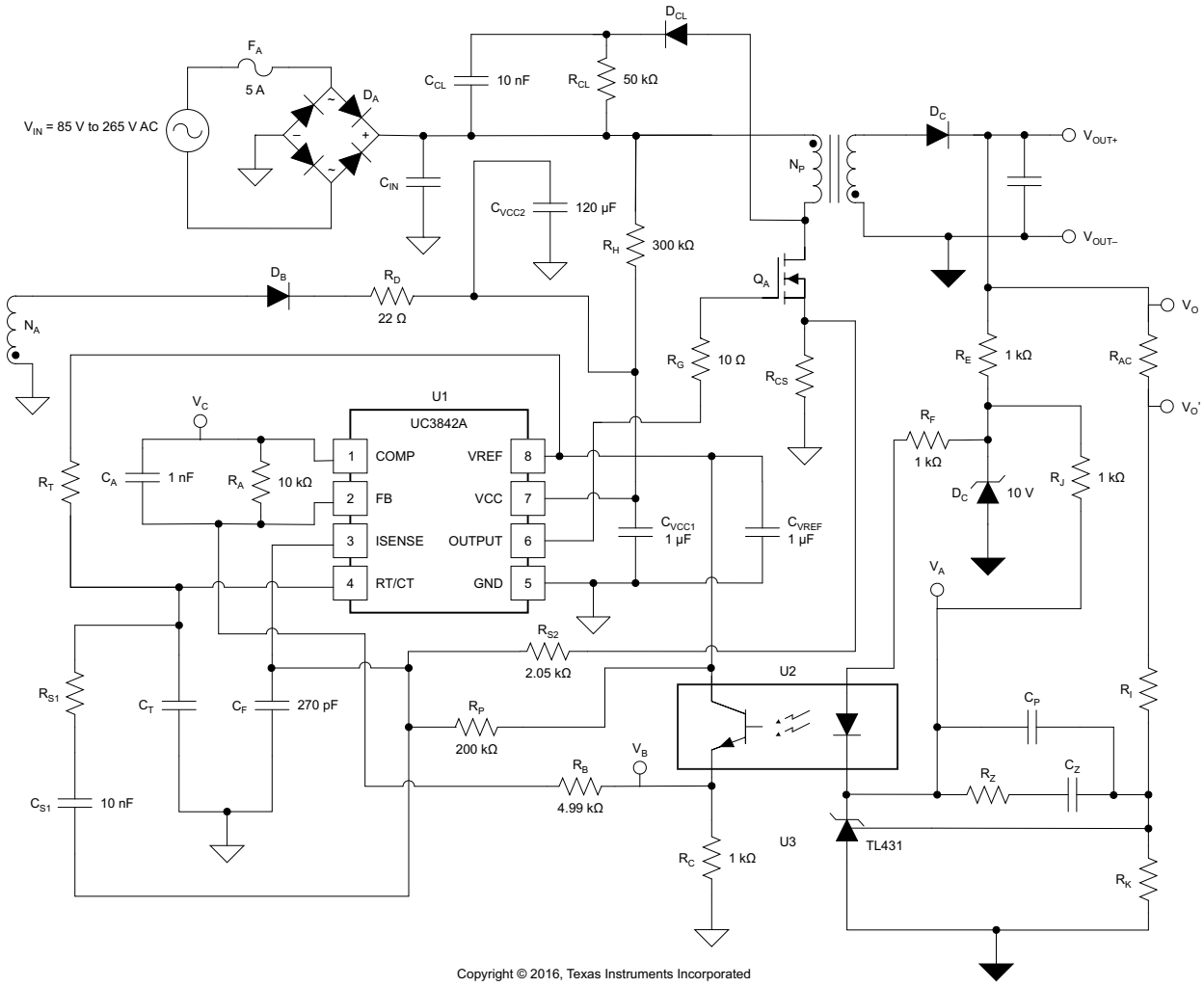


Figure 10. Typical Flyback Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
V_{IN}	Input voltage (RMS)	85		265	V
f_{LINE}	Line frequency	47		63	Hz
OUTPUT CHARACTERISTICS					
V_{OUT}	Output voltage	11.75	12	12.25	V
	Output ripple voltage		50		mV_{PP}
I_{OUT}	Output current		4	4.33	A
	Load step	11.75		12.25	V
SYSTEMS CHARACTERISTICS					
η	Maximum load efficiency	86%			

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCx84xA device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 UC2842A Design Procedure

This application design procedure shows how to setup and use the UC2842A peak current mode controller in an offline flyback converter, with universal input to a 12-V, 48-W regulated output.

Setting up and designing with the UC2842A peak current mode controller in a continuous mode flyback application requires knowing some things about the power stage. First, calculate the required input bulk capacitance (C_{IN}) based on output power level (P_{OUT}), efficiency (η), minimum input voltage ($V_{IN(min)}$), line frequency (f_{LINE}) and minimum bulk voltage. For this design example let $V_{BULK(min)}$ = 95 V.

$$V_{INripple} = \frac{2 \times \frac{P_{OUT}}{\eta} \times \left[0.25 + \frac{1}{\pi} \times \arcsin \times \left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right]}{\left(2 \times V_{IN(min)}^2 - V_{BULK(min)}^2 \right) \times f_{LINE}} \quad (2)$$

$$C_{IN} = \frac{2 \times \frac{P_{OUT}}{\eta} \times \left[0.25 + \frac{1}{\pi} \times \arcsin \times \left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right]}{\left(2 \times V_{IN(min)}^2 - V_{BULK(min)}^2 \right) \times f_{LINE}} \approx 180\ \mu F \quad (3)$$

The output capacitor (C_{OUT}) is sized so the output voltage does not droop more than 10% during a large-signal transient response. The voltage-loop crossover frequency (f_C) is estimated to be 2.5 kHz at this point in the design.

$$C_{OUT} \geq \frac{\frac{I_{OUT}}{f_C}}{V_{OUT} \times 10\%} \approx 1.33\text{mF} \tag{4}$$

The C_{OUT} selected for the design is a 2200-µF capacitor, with an equivalent series resistance (ESR) of 45 mΩ.

Next calculate the maximum primary to secondary turns ratio (N_{PS}) of the transformer, based on the minimum input voltage and output voltage.

$$N_{PS} \leq \frac{V_{IN(min)} \times \sqrt{2}}{V_{OUT}} = \frac{85\ \text{V} \times \sqrt{2}}{12\ \text{V}} \approx 10 \tag{5}$$

Next calculate the auxiliary to secondary turns ratio (N_{AS}) of the transformer, based on the output voltage and the bias voltage of the UC2842A.

$$N_{AS} \leq \frac{V_{VCC}}{V_{OUT}} = \frac{12\ V}{12\ V} = 1 \tag{6}$$

Once the transformer turns ratios have been determined, the minimum primary magnetizing inductance (L_{PM}) of the transformer can be calculated based on minimum bulk voltage, Duty Cycle (D), reflected output current and efficiency. The transformer used in this design has an L_{PM} of 1.7 mH, N_{PS} = 10, and a N_{AS} = 1, f_{sw} = 100 kHz

$$D = \frac{N_{PS} \times V_{OUT}}{V_{BULK(min)} + N_{PS} \times V_{OUT}} \approx 0.56 \tag{7}$$

$$L_{PM} \geq \frac{V_{BULK\,(min)} \times D}{\frac{70\% \times I_{OUT} \times f_{sw}}{\eta \times N_{PS}}} = 1.632\text{mH} \approx 1.7\text{mH} \tag{8}$$

After the transformer has been selected, the primary peak current (I_{LpPK}) of the transformer can be calculated based on the primary magnetizing inductance ripple (I_{LPM}) and the reflected output current across the transformer.

$$I_{LPM} = \frac{V_{BULK(min)} \times D}{f_{SW} \times L_M} \approx 0.31\ A \tag{9}$$

$$I_{LpPK} = \frac{I_{OUT}}{N_{PS} \times (1-D)} + \frac{I_{LM}}{2} \approx 1.1\ A \tag{10}$$

Once the primary peak current has been calculated the current sense resistor (R_{CS}) can be selected.

$$R_{CS} = \frac{1\ V}{I_{LpPK} \times 1.3} = 0.725\ \Omega \approx 0.75\ \Omega \tag{11}$$

Resistors R_{S1} and R_{S2} are used to set the slope compensation of the design. Capacitor C_{S1} is a DC blocking capacitor, and pull-up resistor R_P is used to provide some offset to the current sense signal for noise immunity. R_P and R_{S2} were preselected to add a DC offset of 50 mV to the current sense signal.

R_{S1} is selected to set the slope compensation to one-half of the ripple current down slope of the flyback inductor. This can be accomplished by calculating the secondary magnetizing inductance (L_{SM}) and using the following calculation for R_{S1}. The 1.7 V in the R_{S1} equation is the peak-to-peak ripple voltage amplitude of the oscillator.

$$R_{S1} = \frac{1.7\ V \times R_{S2} \times f_{SW} \times (2 \times L_{SM} \times N_{PS})}{V_{OUT} \times (1-D) \times R_{CS}} - R_{S2} = 27.72\ k\Omega \approx 27.4\ k\Omega$$

where

- $R_{S2} = 2.05\ k\Omega$

(12)

Resistors R_I and R_K are selected to the output reference and can be calculated by preselecting a value for R_K and knowing the TL431 reference voltage ($V_{TL431REF}$). After choosing 2.49 kΩ for R_K, R_I is calculated and a standard resistor value of 9.53 kΩ is chosen for this resistor.

$$R_I = \frac{R_K \times (V_{OUT} - V_{TL431REF})}{V_{TL431REF}} = \frac{2.49\ k\Omega \times (12\ V - 2.5\ V)}{2.5\ V} = 9.462\ k\Omega \approx 9.53\ k\Omega \tag{13}$$

This design using the UC2842A controller has an interesting control loop with many components. $G_{OPTO}(f)$ is the approximate transfer function across the opto isolator in the design. The pole frequency of the opto isolator is represented by f_P. The opto isolator used in this design has a current transfer ratio of 1 and pole frequency of roughly 5 kHz. See Figure 10 for component placement and node voltages. The voltage loop (f_C) must cross-over less than the opto isolator pole for simplified compensation.

$$s(f) = 2 \times \pi \times 1i \times f \tag{14}$$

$$f_P = 5\ kHz \tag{15}$$

$$G_{OPTO}(f) = \frac{\Delta V_B}{\Delta V_A} = \frac{R_C}{R_F} \times \frac{ctr}{\frac{s(f)}{2 \times \pi \times f_P} + 1} \quad (16)$$

$G_{BC}(f)$ is an estimate of the transfer function from the output of the opto isolator to the PWM's control voltage.

$$G_{BC}(f) = \frac{\Delta V_C}{\Delta V_B} = \frac{R_A}{R_B} \times \frac{1}{s(f) \times R_A \times C_A + 1} \quad (17)$$

The duty cycle varies with the bulk input voltage (V_{BULK}). V_{BULK} varies from 95 V to 375 V during normal operation. This causes the duty cycle to vary from 24% to 56%.

$$D = \frac{N_{PS} \times V_{OUT}}{V_{BULK} + N_{PS} \times V_{OUT}} = 0.24 \text{ to } 0.56 \quad (18)$$

$G_{CO}(f)$ is an estimate of the control (V_C) to output transfer function, where variable Q is the quality factor.

$$G_{CO}(f) = \frac{\Delta V_{OUT}}{\Delta V_C} = N_{PS} \times \frac{1-D}{1+D} \times \left[\frac{s(f) \times ESR \times C_{OUT} + 1}{s(f) \times R_{OUT} \times C_{OUT} + 1}\right] \times \left[1 - \frac{s(f) L_{SM} \times D}{R_{OUT} \times (1-D)^2}\right] \times \frac{\frac{1}{3}}{1 + \frac{s(f)}{2 \times \pi \times \frac{f_{SW}}{2} \times Q} + \left(\frac{s(f)}{2 \times \pi \times \frac{f_{SW}}{2}}\right)^2} \quad (19)$$

The quality factor (Q) is defined by the primary magnetizing inductance change in voltage (S_N) as a function of duty cycle; as well as, the added slope compensation (S_E).

$$S_N = \frac{V_{BULK} \times R_{CS}}{L_{PM}} \quad (20)$$

$$S_E = 1.7 \text{ V} \times \frac{R_{S2} \times f_{SW}}{R_{S1} + R_{S2}} \quad (21)$$

$$Q = \frac{1}{\pi \left[\left(1 + \frac{S_E}{S_N}\right) \times (1 - D) - 0.5\right]} \quad (22)$$

To ensure that the voltage loop is stable, the crossover frequency must be less than one half of the right-half-plane zero frequency (f_{RHPZ}) of the flyback converter. The right-half-plane zero frequency at the minimum bulk voltage would be roughly 9.8 kHz. For this design example the target crossover of the voltage loop is at 1 kHz. The actual f_C may be higher or lower than the target.

$$f_{RHPz} = \frac{(N_{PS})^2}{\frac{2 \times \pi \times Lpm}{R_{OUT}} \frac{D}{(1-D)^2}} \approx 9.8 kHz \quad (23)$$

$$f_C \leq \frac{f_{RHPz}}{2} \approx 5 \text{ kHZ} \quad (24)$$

The DC gain of $G_{CO}(f)$ moves with the bulk input voltage. Resistor R_Z is selected to crossover the voltage loop when input to the converter is at $V_{BULK(min)}$ and to crossover at 1/5th the maximum crossover frequency.

$$R_Z = \frac{R_I}{\left|G_{OPTO}(f_C/5) \times G_{BC}(f_C/5) \times G_O \times G_{CO}(f_C/5)\right|} = 23.95 \text{ k}\Omega, \text{ a } 23.7 \text{ k}\Omega \text{ was used} \quad (25)$$

Capacitor C_Z is selected to add 45° of phase margin at voltage loop crossover. For this design example a 6.8-nF capacitor was used.

$$C_Z = \frac{1}{2\pi \times \frac{f_C}{5} \times R_Z} \approx 6.7 \text{ nF} \quad (26)$$

Capacitor C_P is selected to attenuate the high frequency gain of the control loop.

$$C_P = \frac{C_Z}{10} = 680 \text{ pF} \quad (27)$$

$G_C(f)$ is the estimated transfer function of the TL431 compensation.

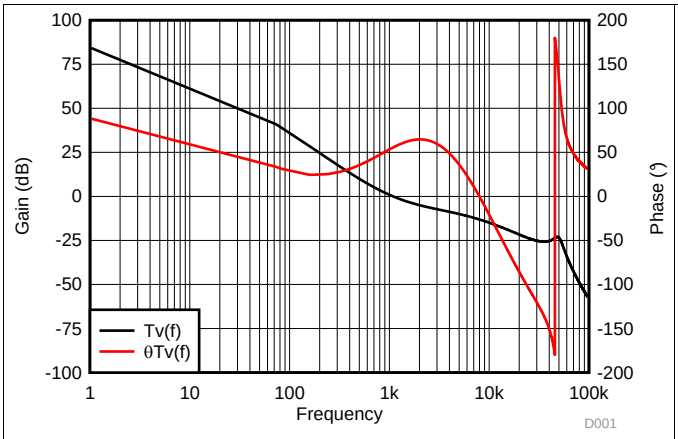
$$G_C(f) = \frac{\Delta V_C}{\Delta V_O'} = \frac{s(f) \times R_Z \times C_Z + 1}{s(f) \times R_I \times (C_Z + C_P) \times \left(\frac{s(f) \times R_Z \times C_Z \times C_P}{C_Z + C_P} + 1 \right)} \quad (28)$$

$T_V(f)$ is the estimated theoretical transfer function of the close-loop gain of the system. The feedback loop response may be different in the actual circuit and may have to be adjusted with a network analyzer to meet actual circuit performance and reliability. The feedback loop response must be evaluated over worse case variations in design parameters.

$$T_V(f) = G_C(f) \times G_{OPTO}(f) \times G_{BC}(f) \times G_O \times G_{CO}(f_C) \quad (29)$$

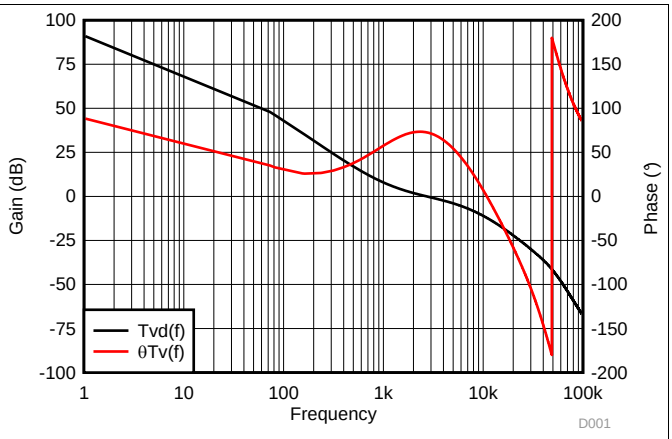
For this application example, this design technique generated a theoretical feedback loop ($T_V(f)$) crossover at 1 kHz with roughly 55° of phase margin at a minimum input bulk voltage of 95 V. The theoretical voltage loop at high-line crossed over at 2.7 kHz with a phase margin of 72°. See Figure 11 and Figure 12. $T_V(f)$ must be evaluated with a network analyzer and adjust the loop compensation as necessary based on the actual circuitry behavior. Also conduct transient testing to ensure that the device remains stable.

8.2.3 Application Curves



V_{BULK} = 95 V

Figure 11. Voltage Loop Gain



V_{BULK} = 375 V

Figure 12. Voltage Loop Gain

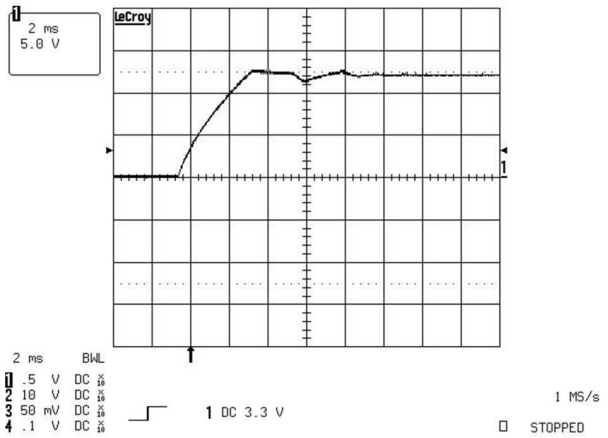


Figure 13. V_{OUT} Start-Up Full Load

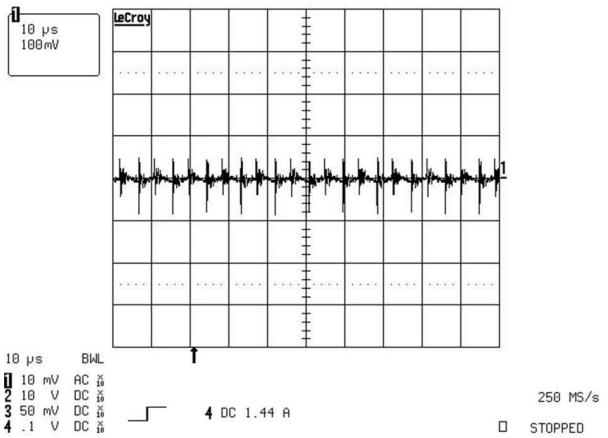


Figure 14. V_{OUT} Ripple Voltage

9 Power Supply Recommendations

TI recommends using the UCx84xA in isolated or non-isolated peak current mode control power supplies. The device can be used in buck, boost, flyback, and forwarded converter-based power supply topologies.

10 Layout

10.1 Layout Guidelines

- Star grounding techniques must be used.
- Current loops must be kept as short and narrow as possible.
- The IC ground and power ground must meet at the return for the input bulk capacitor. Ensure that high frequency and high current from the power stage does not go through the signal ground paths.
- A high-frequency bypass capacitor (C_{VCC1}) must be placed across VCC and GND pins as close as possible to the pins.
- Resistor R_{S2} and capacitor C_F form a low-pass filter for the current sense signal. C_F must be as close to CS and GND pins as possible.
- Capacitor C_{VREF} must be as close to VREF and GND pins as possible.
- Figure 15 shows the SMD components arranged for wave-solder on a single-layer board. If multiple layers are used, some components may be rearranged for easier interconnection and reduced current-loop areas. If the solder process allows, placing the SMD components in perpendicular orientations may improve interconnections and loop areas.

10.2 Layout Example

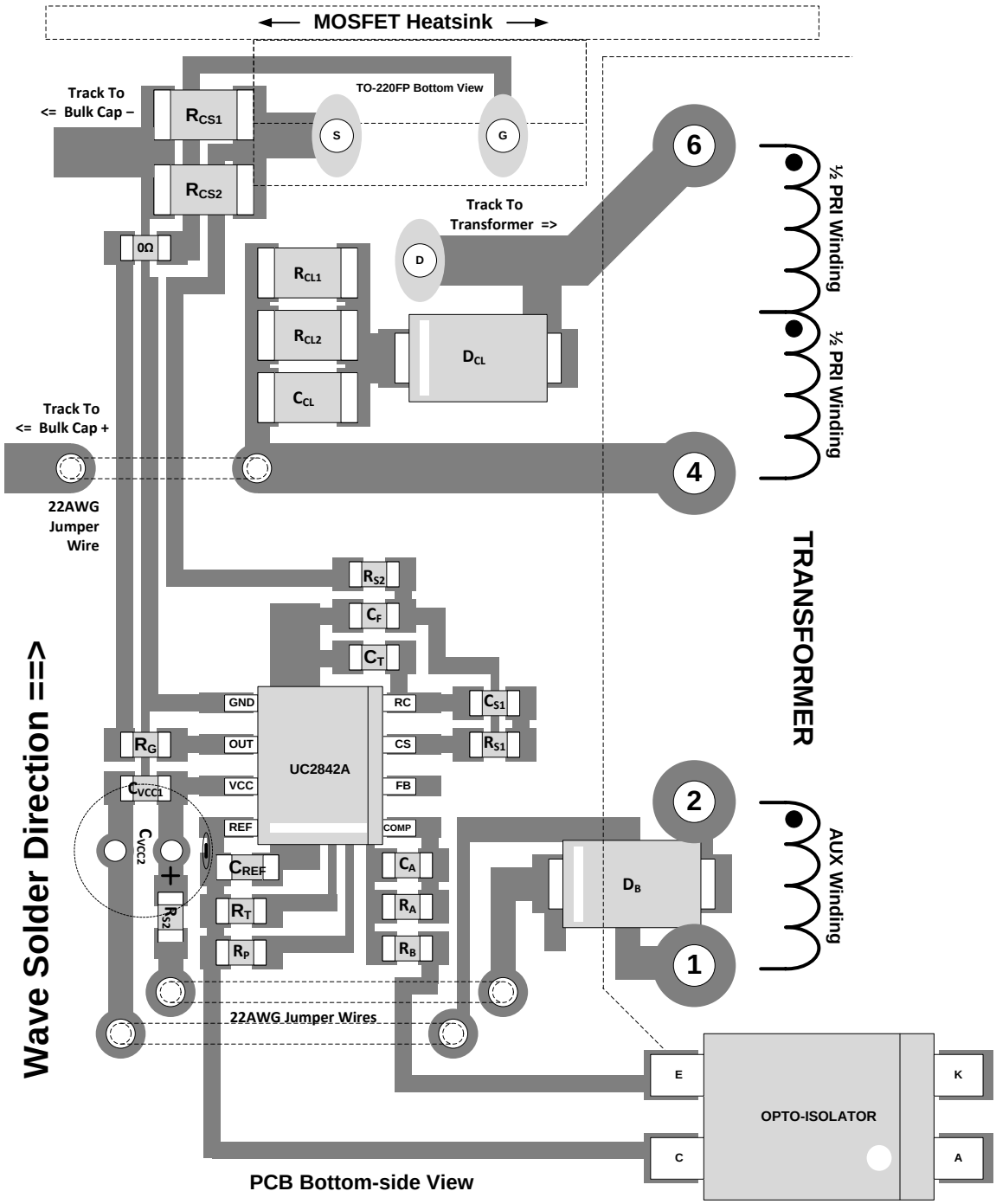


Figure 15. Layout Diagram

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

- TI Engineer-to-Engineer Support Forum, https://e2e.ti.com/

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCx84xA device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.1.2 Device Nomenclature

C_{IN}	Input bulk capacitance
C_{OUT}	Output capacitance
D	Duty cycle
ESR	Equivalent series resistance
$G_{BC}(f)$	An estimate of the transfer function from the output of the opto-isolator to the PWM control voltage.
G_O	The DC gain of the control to output transfer function.
$G_{OPTO}(f)$	The approximate transfer function across the opto-isolator in the design.
I_{LPM}	Transformer primary average current
I_{LpPK}	Peak transformer primary current
L_{PM}	Transformer primary magnetizing inductance
L_{SM}	Transformer secondary magnetizing inductance
N_{PS}	Primary to secondary transformer turns ratio
N_{AS}	Auxiliary to secondary transformer turns ratio
$T_V(f)$	is the feedback control loop transfer function.
$V_{INripple}$	Input ripple voltage

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Design Review: 150 Watt Current-Mode Flyback (SLUP078)

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UC1842A	Click here	Click here	Click here	Click here	Click here
UC1843A	Click here	Click here	Click here	Click here	Click here
UC1844A	Click here	Click here	Click here	Click here	Click here
UC1845A	Click here	Click here	Click here	Click here	Click here
UC2842A	Click here	Click here	Click here	Click here	Click here
UC2843A	Click here	Click here	Click here	Click here	Click here
UC2844A	Click here	Click here	Click here	Click here	Click here
UC2845A	Click here	Click here	Click here	Click here	Click here
UC3842A	Click here	Click here	Click here	Click here	Click here
UC3843A	Click here	Click here	Click here	Click here	Click here
UC3844A	Click here	Click here	Click here	Click here	Click here
UC3845A	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8670405PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670405PA UC1842A	Samples
5962-8670405XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670405XA UC1842AL/883B	Samples
5962-8670406PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670406PA UC1843A	Samples
5962-8670406XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670406XA UC1843AL/883B	Samples
5962-8670407PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670407PA UC1844A	Samples
5962-8670407XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670407XA UC1844AL/883B	Samples
5962-8670408PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670408PA UC1845A	Samples
5962-8670408XA	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670408XA UC1845AL/883B	Samples
UC1842AJ	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1842AJ	Samples
UC1842AJ883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670405PA UC1842A	Samples
UC1842AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670405XA UC1842AL/883B	Samples
UC1843AJ	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1843AJ	Samples
UC1843AJ883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670406PA UC1843A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC1843AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670406XA UC1843AL/883B	Samples
UC1844AJ	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1844AJ	Samples
UC1844AJ883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670407PA UC1844A	Samples
UC1844AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670407XA UC1844AL/883B	Samples
UC1845AJ	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	UC1845AJ	Samples
UC1845AJ883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	8670408PA UC1845A	Samples
UC1845AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-8670408XA UC1845AL/883B	Samples
UC2842AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842AD	Samples
UC2842AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842A UC2842 AD8	Samples
UC2842AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842A UC2842 AD8	Samples
UC2842AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842A UC2842 AD8	Samples
UC2842ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842AD	Samples
UC2842ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2842AD	Samples
UC2842ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2842ADW	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2842ADWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2842ADW	Samples
UC2842ADWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2842ADW	Samples
UC2842AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2842AN	Samples
UC2842ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2842AN	Samples
UC2843AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843AD	Samples
UC2843AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843A UC2843 AD8	Samples
UC2843AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843A UC2843 AD8	Samples
UC2843AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843A UC2843 AD8	Samples
UC2843AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843A UC2843 AD8	Samples
UC2843ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843AD	Samples
UC2843ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2843AD	Samples
UC2843AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2843AN	Samples
UC2843ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2843AN	Samples
UC2844AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844AD	Samples
UC2844AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844A UC2844 AD8	Samples
UC2844AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844A UC2844	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										AD8	
UC2844AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844A UC2844 AD8	Samples
UC2844AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844A UC2844 AD8	Samples
UC2844ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2844AD	Samples
UC2844AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2844AN	Samples
UC2844ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2844AN	Samples
UC2844AQD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2844AQ, UC2844AQ)	Samples
UC2844AQD8R	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2844AQ, UC2844AQ)	Samples
UC2844AQDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2844AQ, UC2844AQ)	Samples
UC2845AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845AD	Samples
UC2845AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845A UC2845 AD8	Samples
UC2845AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845A UC2845 AD8	Samples
UC2845AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845A UC2845 AD8	Samples
UC2845AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845A UC2845 AD8	Samples
UC2845ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UC2845AD	Samples
UC2845ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2845ADW	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2845AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2845AN	Samples
UC2845ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UC2845AN	Samples
UC3842AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842AD	Samples
UC3842AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842A UC3842 AD8	Samples
UC3842AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842A UC3842 AD8	Samples
UC3842AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842A UC3842 AD8	Samples
UC3842ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842AD	Samples
UC3842ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3842AD	Samples
UC3842ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3842ADW	Samples
UC3842AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3842AN	Samples
UC3842ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3842AN	Samples
UC3842J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-40 to 85	UC3842J	Samples
UC3843AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843AD	Samples
UC3843AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843A UC3843 AD8	Samples
UC3843AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843A UC3843 AD8	Samples
UC3843AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843A UC3843	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										AD8	
UC3843AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843A UC3843 AD8	Samples
UC3843ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843AD	Samples
UC3843ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3843AD	Samples
UC3843AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3843AN	Samples
UC3843ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3843AN	Samples
UC3844AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844AD	Samples
UC3844AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844A UC3844 AD8	Samples
UC3844AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844A UC3844 AD8	Samples
UC3844AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844A UC3844 AD8	Samples
UC3844ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844AD	Samples
UC3844ADTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3844AD	Samples
UC3844AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3844AN	Samples
UC3844ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3844AN	Samples
UC3845AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845AD	Samples
UC3845AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845A UC3845 AD8	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3845AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845A UC3845 AD8	Samples
UC3845AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845A UC3845 AD8	Samples
UC3845AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845A UC3845 AD8	Samples
UC3845ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845AD	Samples
UC3845ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845AD	Samples
UC3845ADTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UC3845AD	Samples
UC3845AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3845AN	Samples
UC3845ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UC3845AN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC1842A, UC1843A, UC1844A, UC1845A, UC2843A, UC3842A, UC3842M, UC3843A, UC3844A, UC3845A :

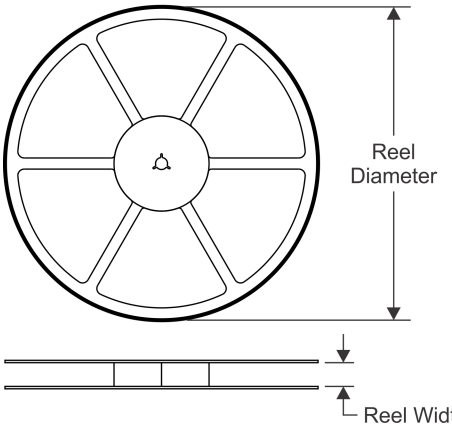
- Catalog: UC3842A, UC3843A, UC3844A, UC3845A, UC3842, UC3845AM
- Automotive: UC2843A-Q1
- Enhanced Product: UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP, UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP
- Military: UC1842A, UC1843A, UC1844A, UC1845A
- Space: UC1842A-SP, UC1843A-SP, UC1844A-SP, UC1845A-SP, UC1842A-SP, UC1843A-SP, UC1844A-SP, UC1845A-SP

NOTE: Qualified Version Definitions:

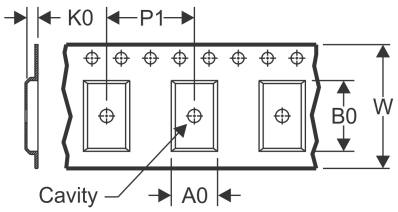
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

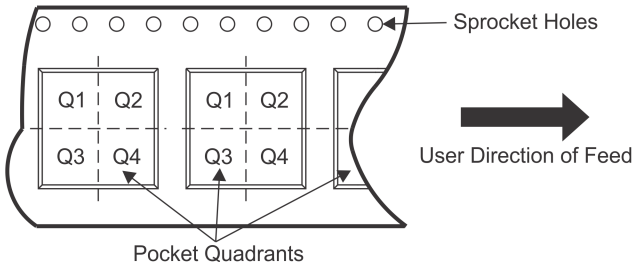


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

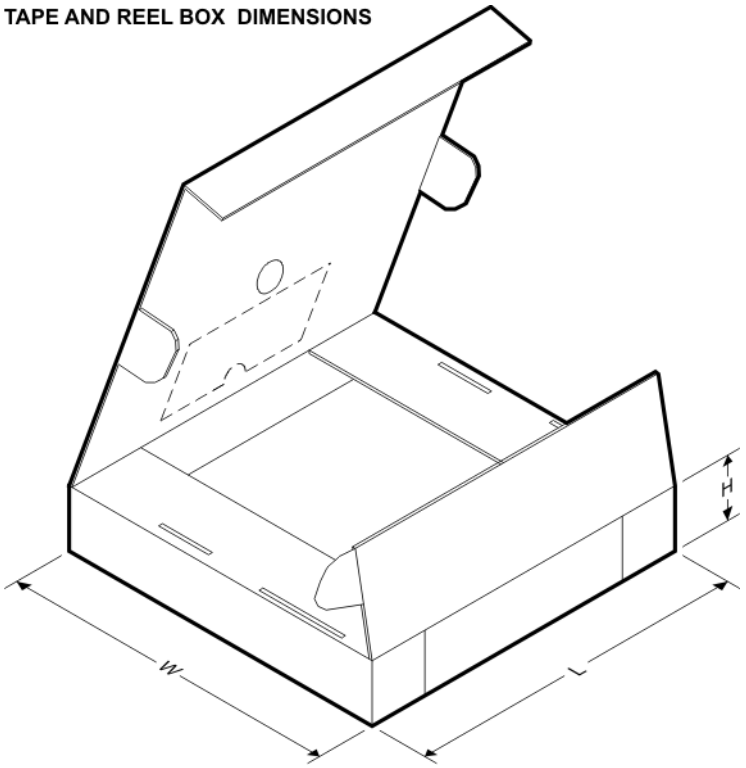


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2842AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2842ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2842ADWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC2843AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2843ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2844AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2844ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2844AQD8R	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2844AQDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2845AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2845ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3842AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3842ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3843AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3843ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3844AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3844ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3845AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3845ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



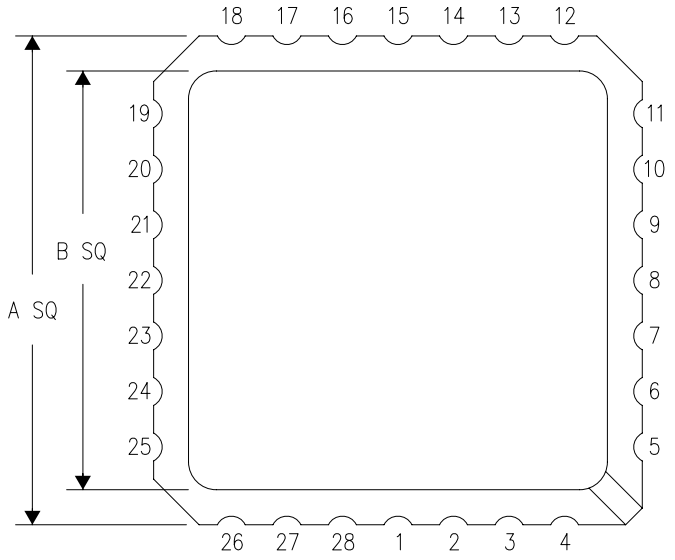
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2842AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2842ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2842ADWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UC2843AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2843ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2844AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2844ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2844AQD8R	SOIC	D	8	2500	367.0	367.0	35.0
UC2844AQDR	SOIC	D	14	2500	367.0	367.0	38.0
UC2845AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2845ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3842AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3842ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3843AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3843ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3844AD8TR	SOIC	D	8	2500	340.5	338.1	20.6

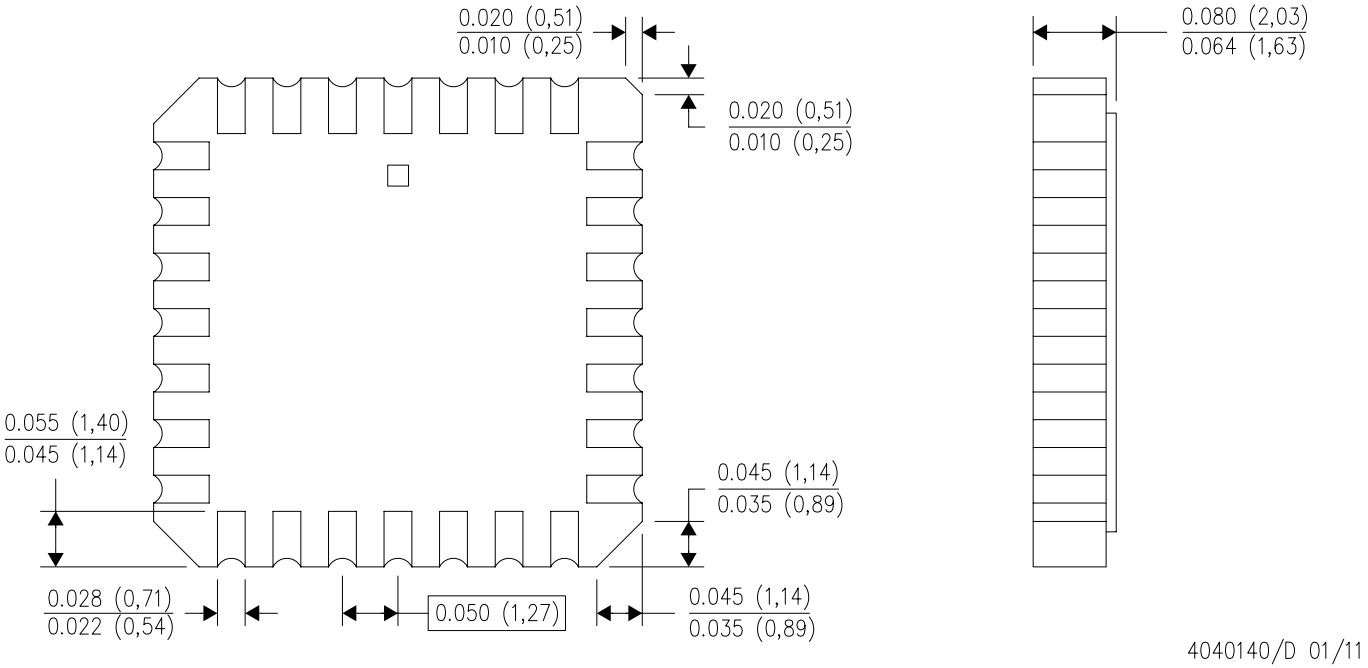
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3844ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3845AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3845ADTR	SOIC	D	14	2500	333.2	345.9	28.6

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

GENERIC PACKAGE VIEW

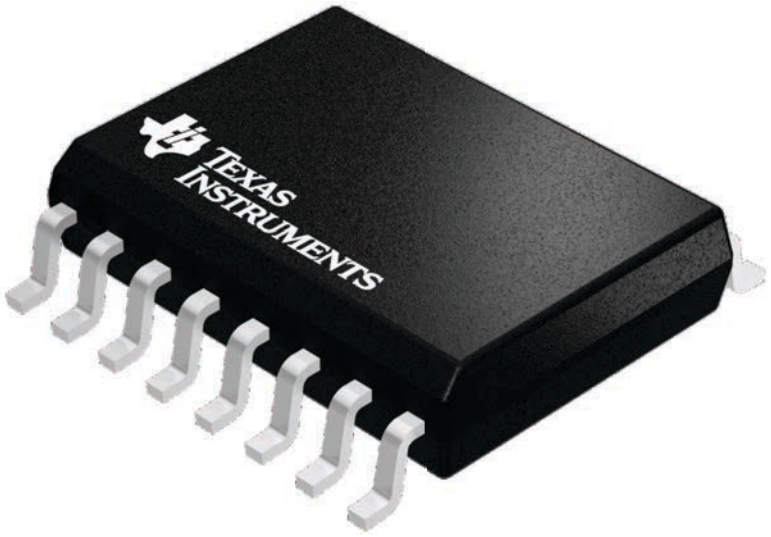
DW 16

SOIC - 2.65 mm max height

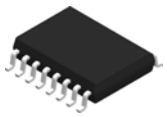
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

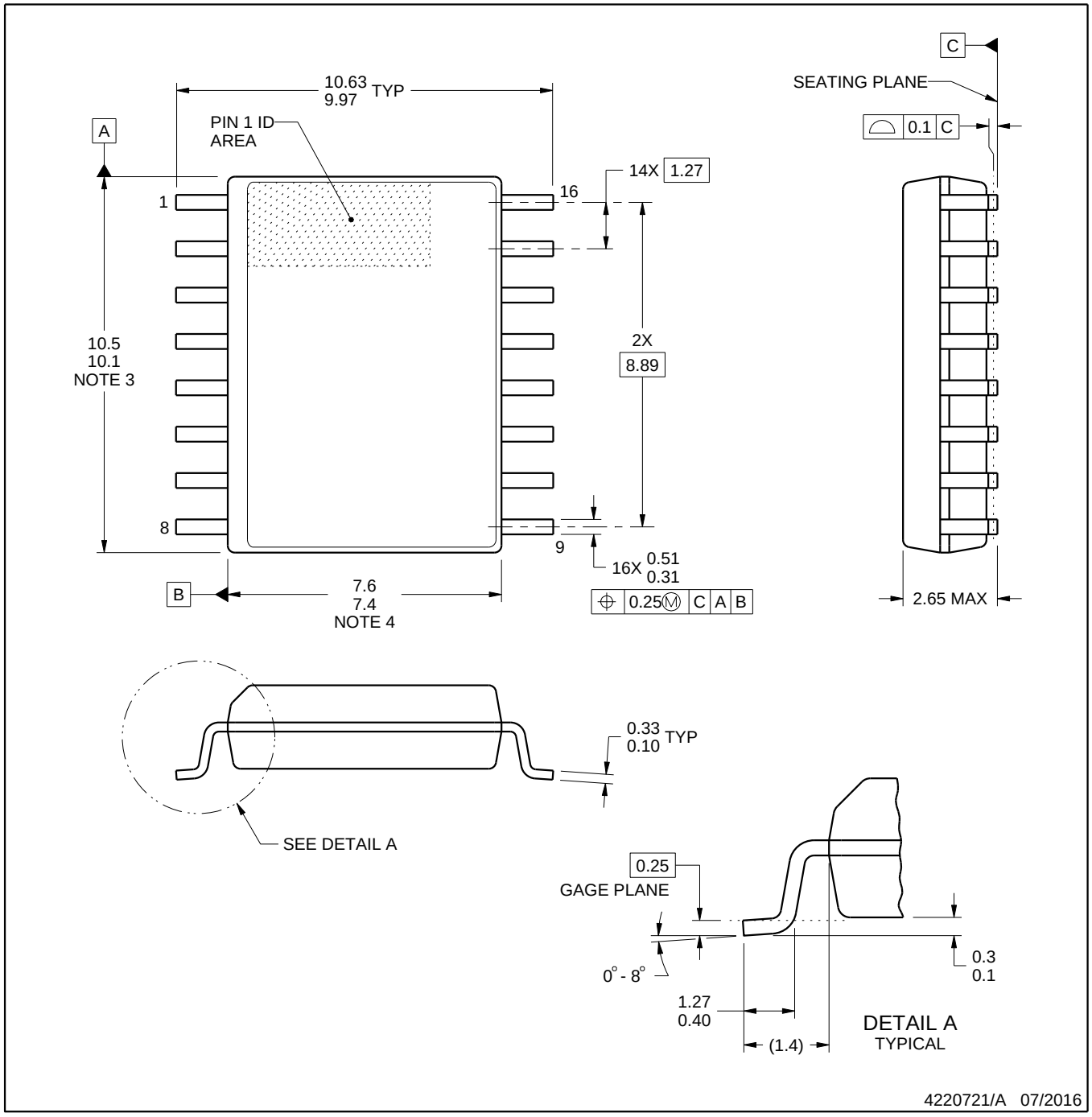


PACKAGE OUTLINE

DW0016A

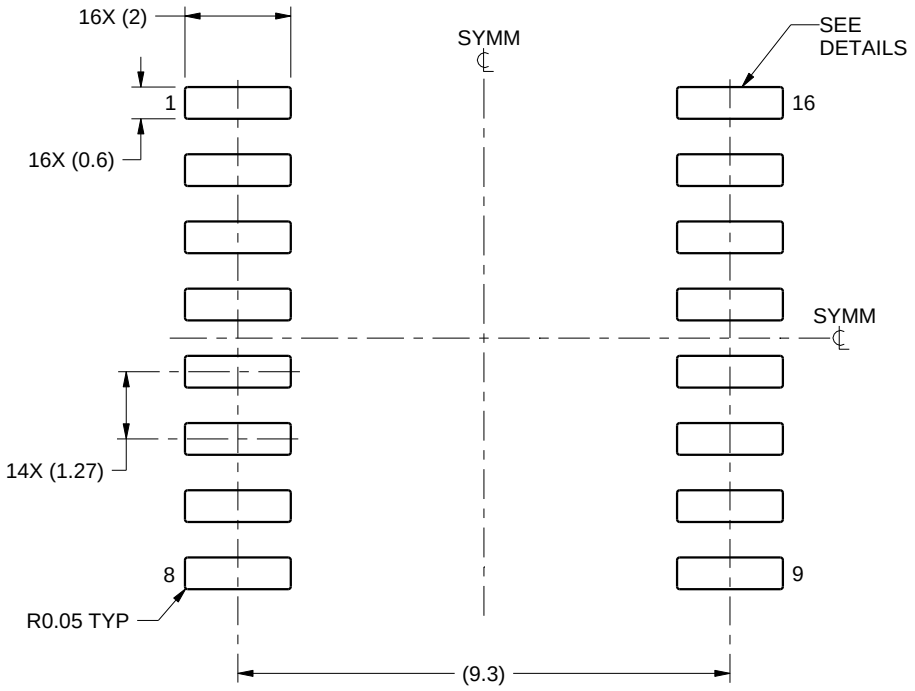
SOIC - 2.65 mm max height

SOIC

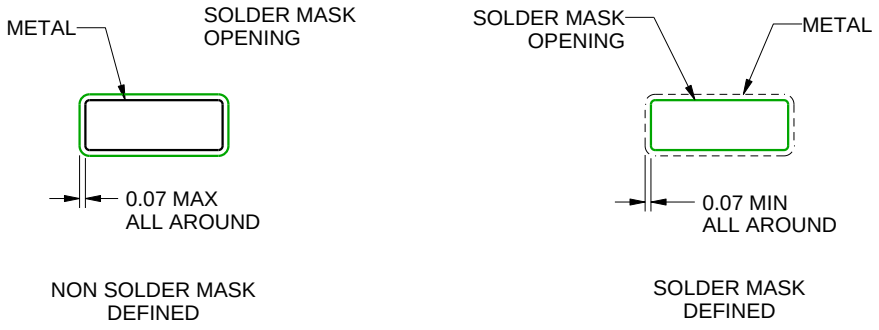


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

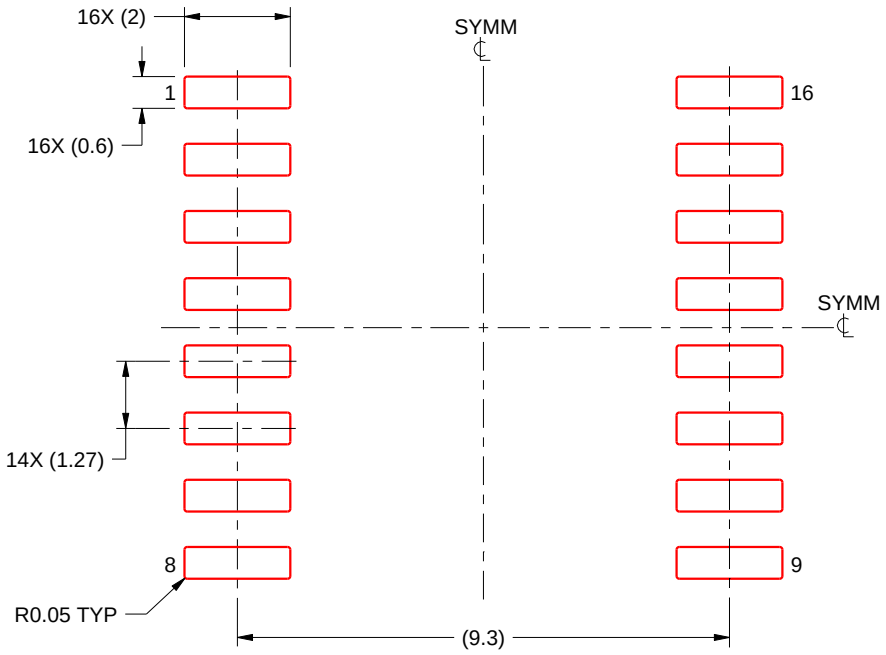


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



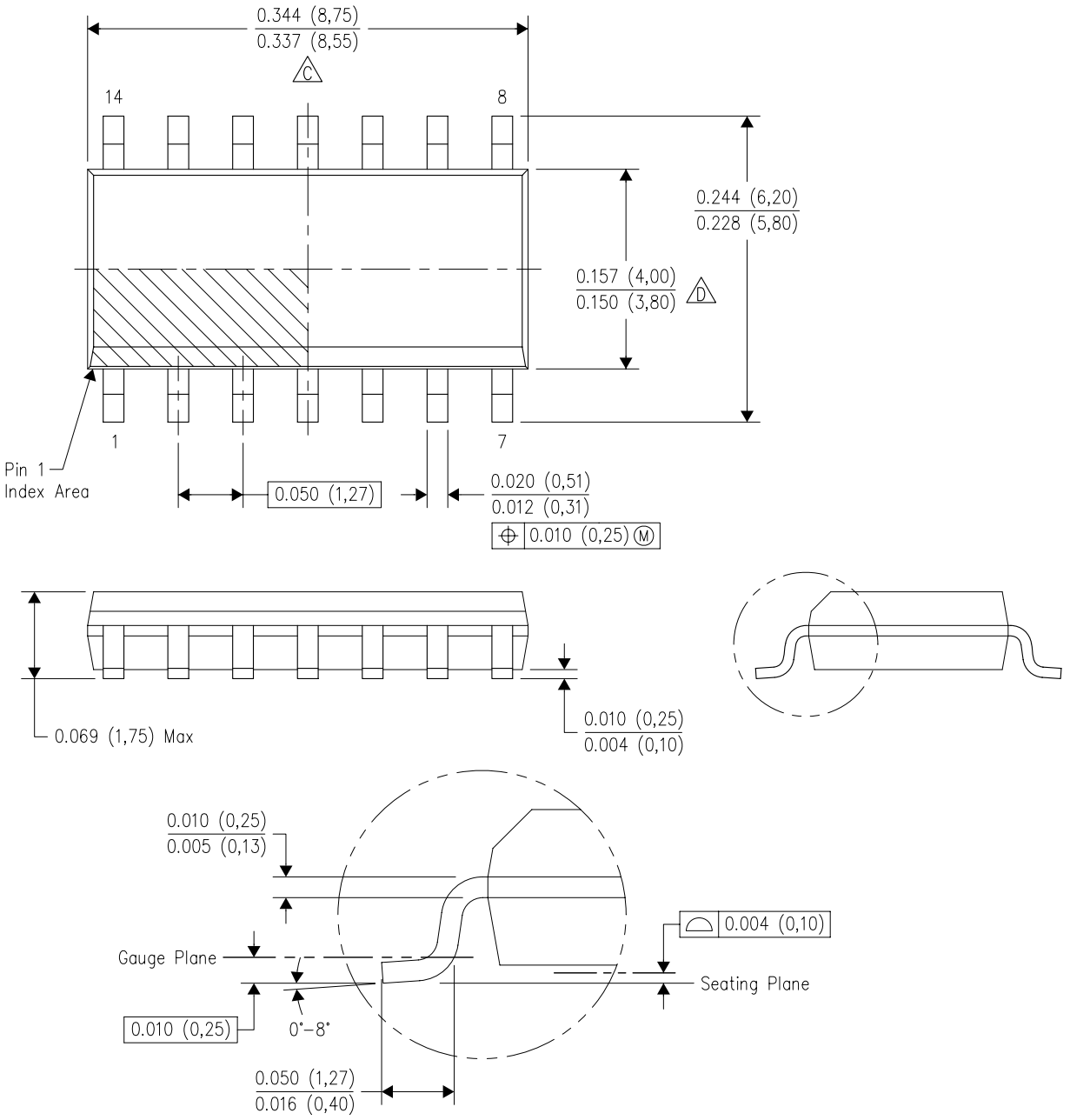
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

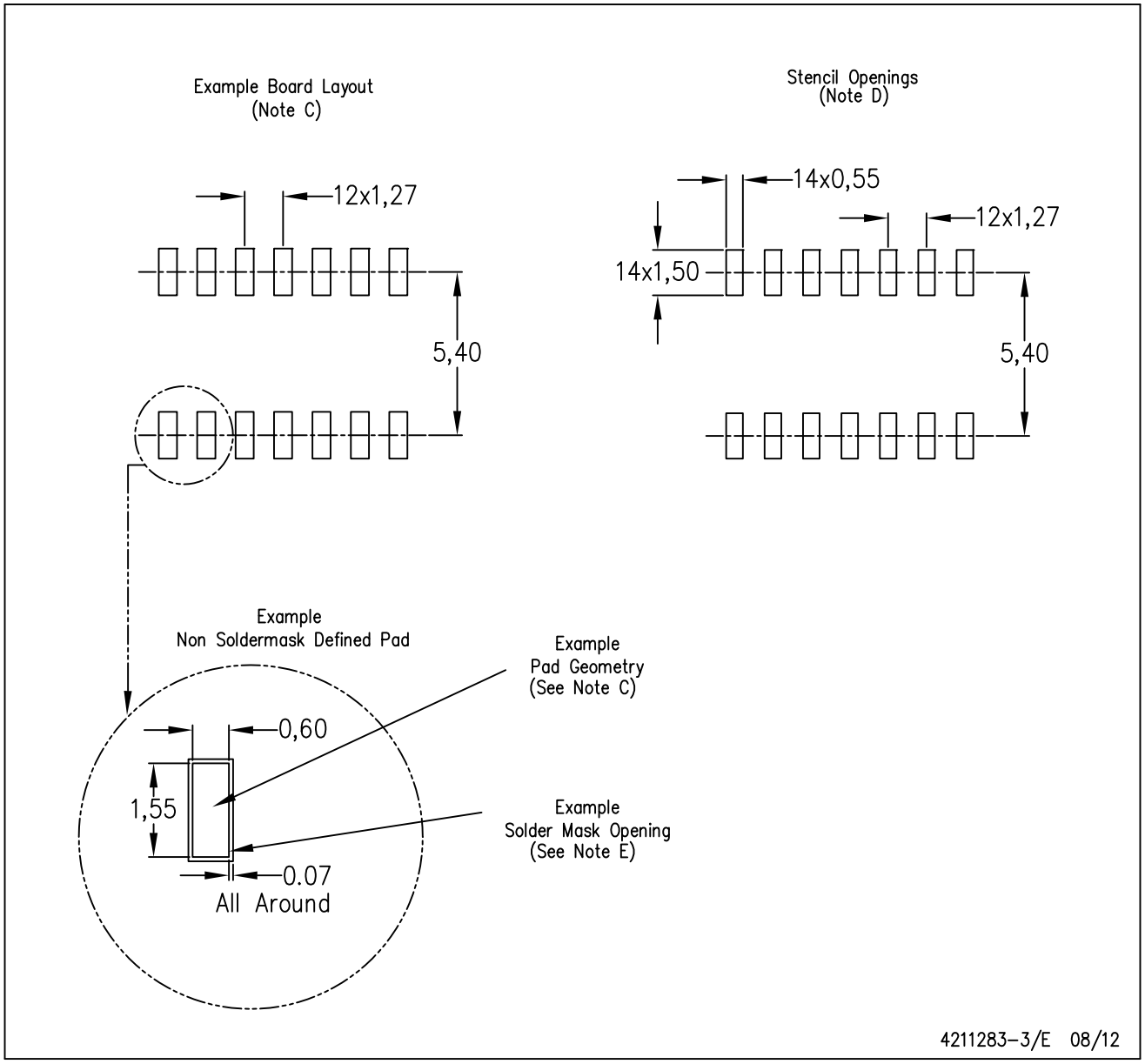
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



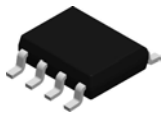
4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

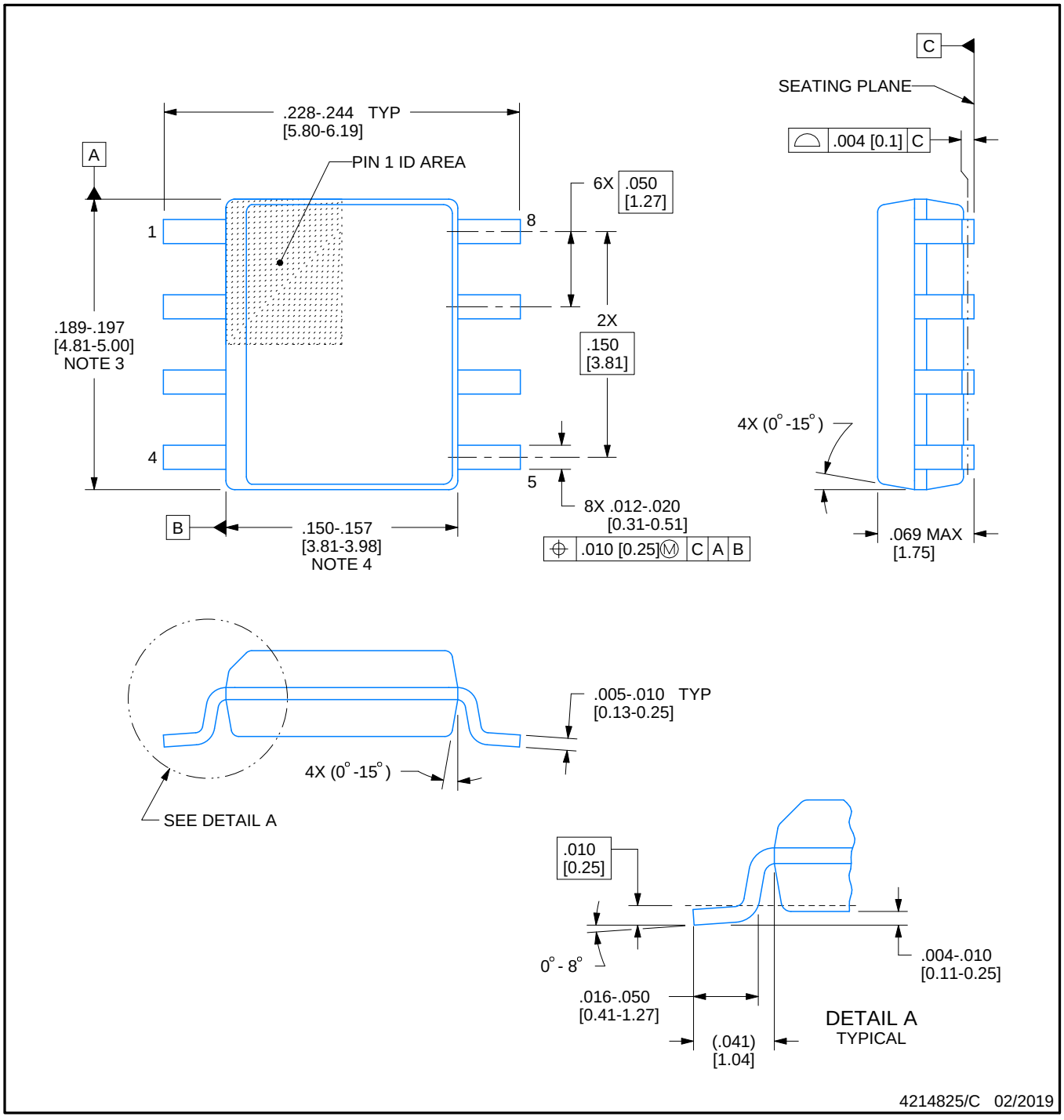


PACKAGE OUTLINE

D0008A

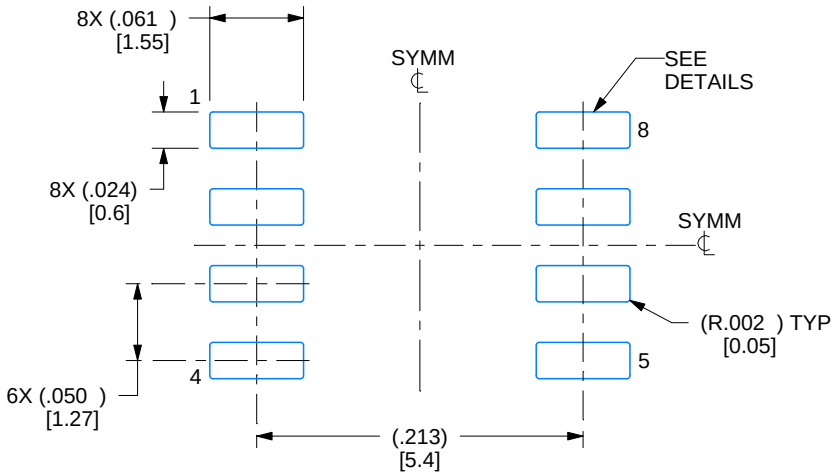
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

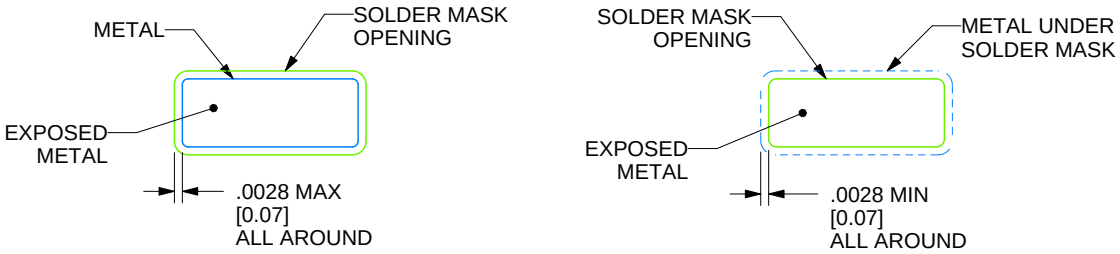


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

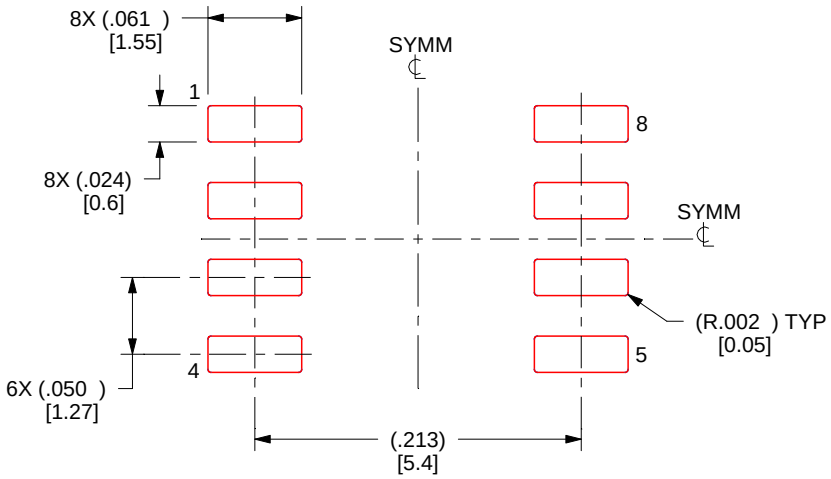
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

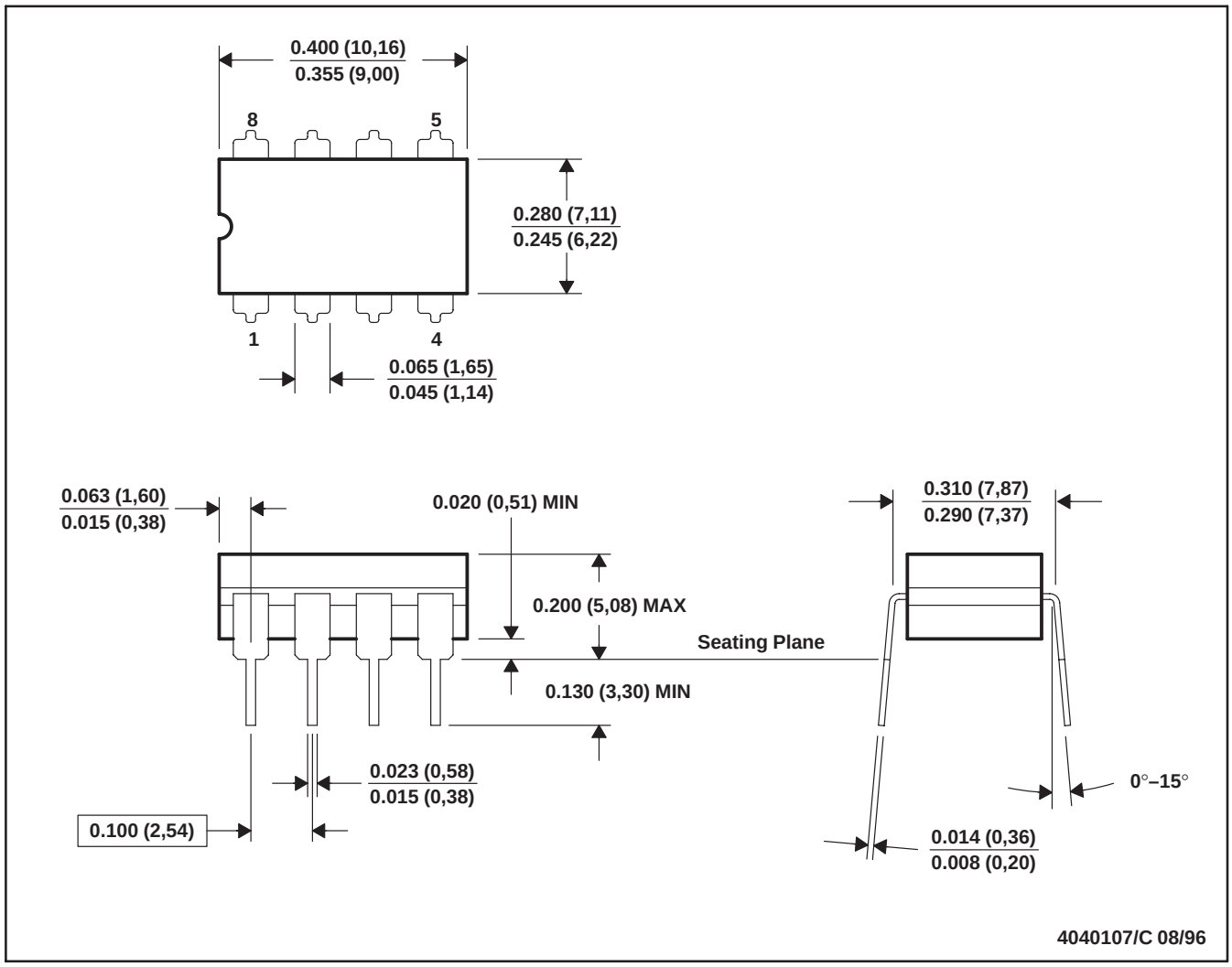
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

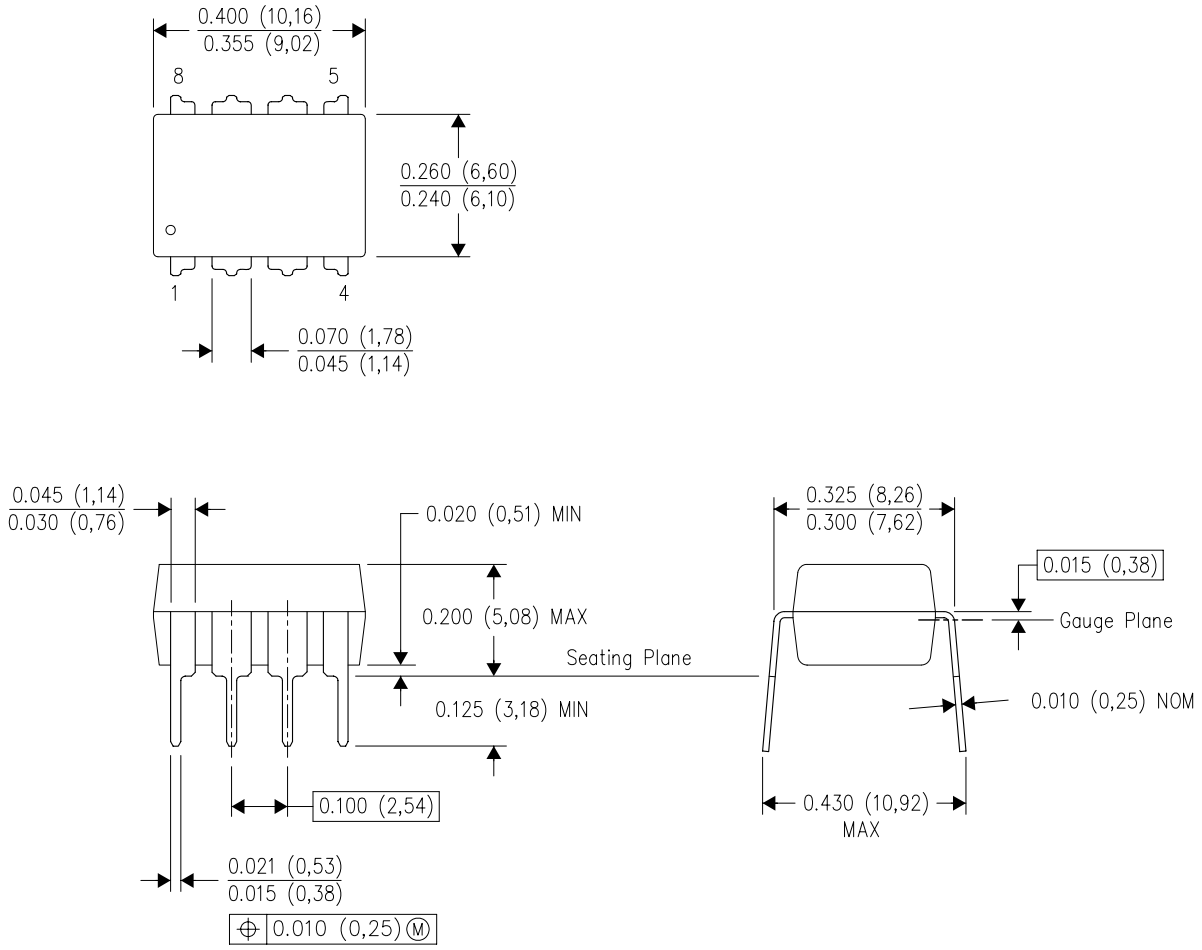
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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